CAT24AA01, CAT24AA02

EEPROM Serial 1/2-Kb I²C

Description

The CAT24AA01/24AA02 are EEPROM Serial 1/2−Kb I²C devices internally organized as 128x8/256x8 bits.

They feature a 16−byte page write buffer and support the Standard (100 kHz), Fast (400 kHz) and Fast−Plus (1 MHz) I²C protocols.

In contrast to the CAT24C01/24C02, the CAT24AA01/24AA02 have no external address pins, and are therefore suitable in applications that require a single CAT24AA01/02 on the I²C bus.

Features

- Supports Standard, Fast and Fast−Plus I²C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

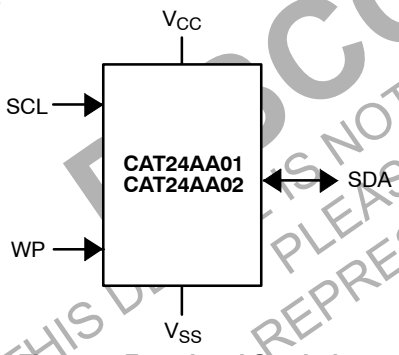


Figure 1. Functional Symbol

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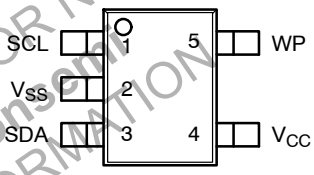
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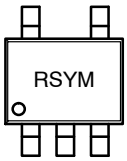
PIN CONFIGURATIONS

TSOT−23



(Top View)

MARKING DIAGRAM



RS = Device Code
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)

PIN FUNCTION

Pin Name	Function
SDA	Serial Data/Address
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. REABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode @ 25°C

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz		0.5	mA
I_{CCW}	Write Current	Write		1	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}		1	μA
I_L	I/O Pin Leakage	Pin at GND or V_{CC}		1	μA
V_{IL}	Input Low Voltage		−0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA		0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA		0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. PIN IMPEDANCE CHARACTERISTICS (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 2)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 2)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP} (Note 4)	WP Input Current	V_{IN} < V_{IH}	100	μA
		V_{IN} > V_{IH}	1	

4. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

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Table 5. A.C. CHARACTERISTICS (Note 5) (V_{CC} = 1.7 V to 5.5 V, T_A = −40°C to 85°C, unless otherwise specified.)

Symbol	Parameter	Standard V_{CC} = 1.7 V – 5.5 V		Fast V_{CC} = 1.7 V – 5.5 V		1 MHz V_{CC} = 2.5 V – 5.5 V		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.5		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.5		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		100		ns
t_R (Note 6)	SDA and SCL Rise Time		1000		300		300	ns
t_F (Note 6)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.4	μs
t_{DH}	Data Out Hold Time	100		50		50		ns
T_i (Note 6)	Noise Pulse Filtered at SCL and SDA Inputs		100		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 6, 7)	Power−up to Ready Mode		1		1		1	ms

5. Test conditions according to “A.C. Test Conditions” table.
6. Tested initially and after a design or process change that affects this parameter.
7. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

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Power−On Reset (POR)

Each CAT24AA01/02 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi−directional POR behavior protects the device against brown−out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the clock signal generated by the Master.

SDA: The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and delivered on the negative edge of SCL.

WP: When the Write Protect input pin is forced HIGH by an external source, all write operations are inhibited. When the pin is not driven by an external source, it is pulled LOW internally.

Functional Description

The CAT24AA01/02 supports the Inter−Integrated Circuit (I^2C) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic, and Slave devices which execute requests. The CAT24AA01/02 operates as a Slave device. Both Master and Slave can transmit or receive, but only the Master can assign those roles.

I^2C BUS PROTOCOL

The 2−wire I^2C bus consists of two lines, SCL and SDA, connected to the V_{CC} supply via pull−up resistors. The Master provides the clock to the SCL line, and the Master and Slaves drive the SDA line. A ‘0’ is transmitted by pulling a line LOW and a ‘1’ by releasing it HIGH. Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 2). A START is generated by a HIGH to LOW transition, while a STOP is generated by a LOW to HIGH transition. The START acts like a wake−up call. Absent a START, no Slave will respond to the Master. The STOP completes all commands.

Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8−bit Slave address (Figure 3). The four most significant bits of the Slave address are 1010 (Ah).

For the CAT24AA01/02 the next three bits must be 000.

The last bit, R/$\overline{W}$, instructs the Slave to either provide (1) or accept (0) data, i.e. it signals a Read (1) or a Write (0) request.

Acknowledge

During the 9th clock cycle following every byte sent onto the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 4). Bus timing is illustrated in Figure 5.

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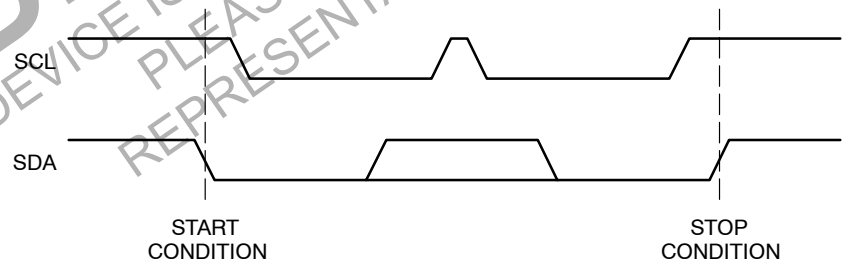


Figure 2. Start/Stop Timing

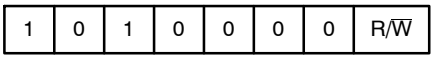


Figure 3. Slave Address Bits

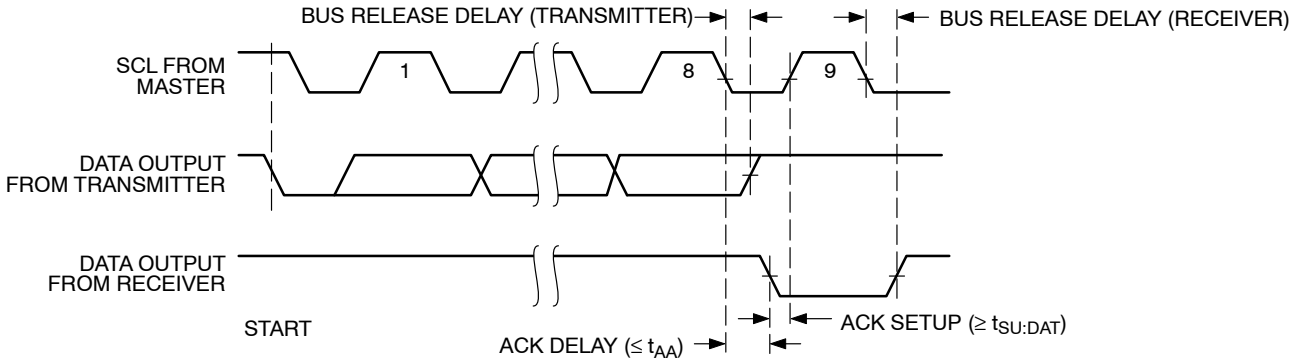


Figure 4. Acknowledge Timing

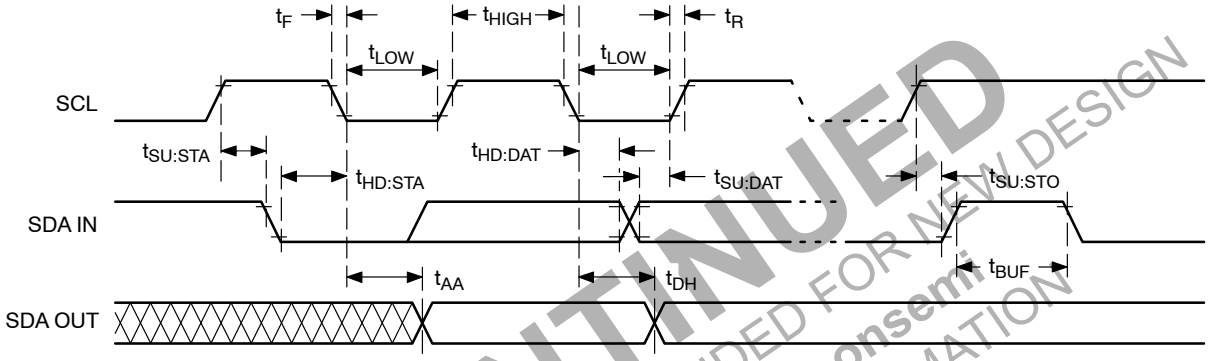


Figure 5. Bus Timing

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WRITE OPERATIONS

Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0'. The Master then sends an address byte and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 5). The STOP starts the internal Write cycle, and while this operation is in progress (t_{WR}), the SDA output is tri−stated and the Slave does not acknowledge the Master (Figure 6).

Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 7). Up to 16 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle (t_{WR}).

Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow−up with a new Read or Write request, rather than wait for the maximum specified Write time (t_{WR}) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the Write operation. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the 1st data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the Slave will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24AA01/02 is shipped erased, i.e., all bytes are FFh.

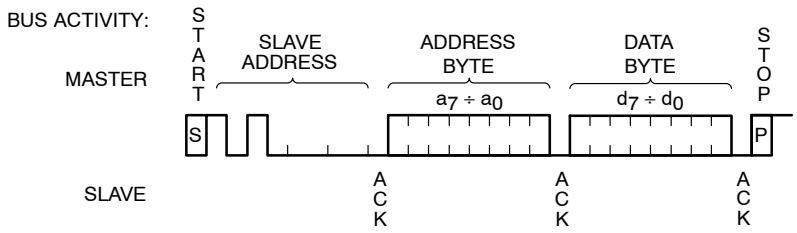


Figure 6. Byte Write Sequence

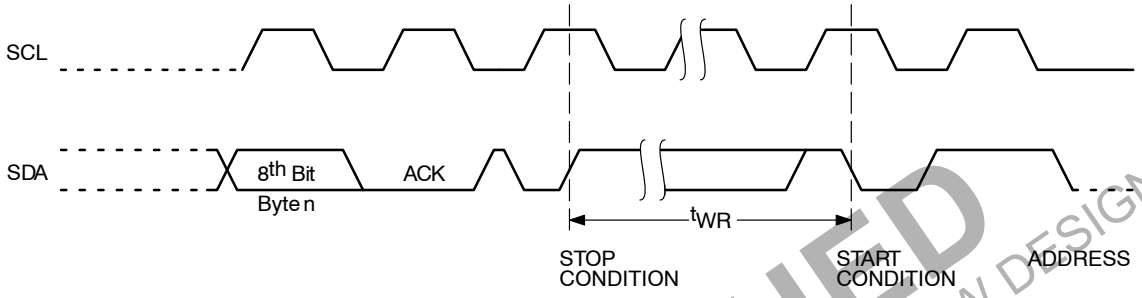


Figure 7. Write Cycle Timing

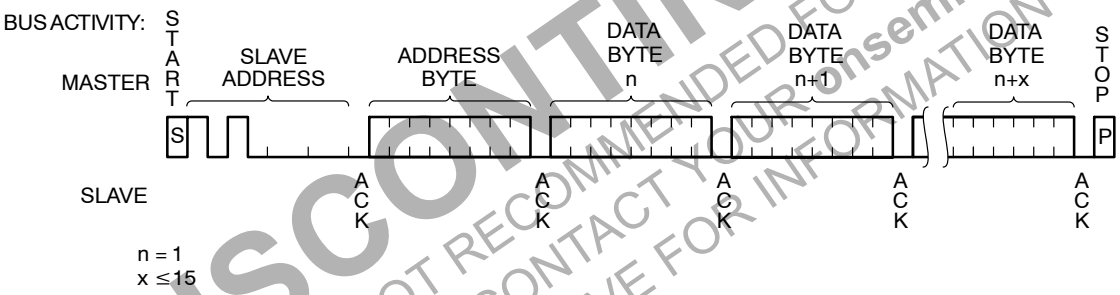


Figure 8. Page Write Sequence

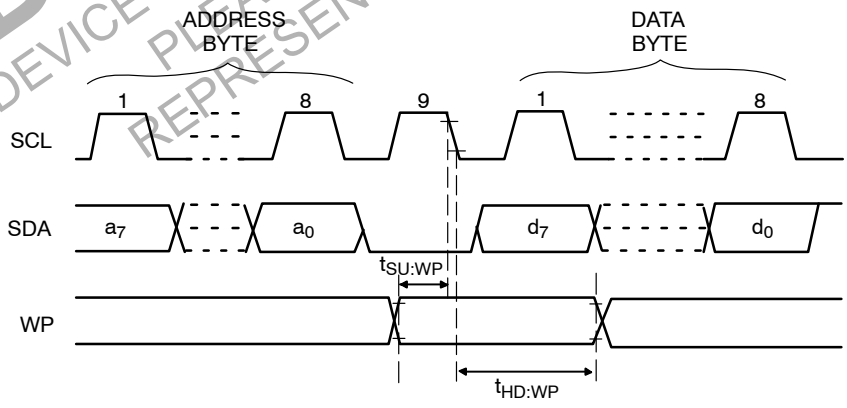


Figure 9. WP Timing

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READ OPERATIONS

Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to ‘1’. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 10). The Slave then returns to Standby mode.

Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the R/$\overline{W}$ bit set to ‘0’ and then sends an address byte to the Slave. Rather than completing the Byte Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the R/$\overline{W}$ bit set to ‘1’. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 11).

Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 12). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory. For the CAT24AA01, the internal address counter will not wrap around at the end of the 128 byte memory space.

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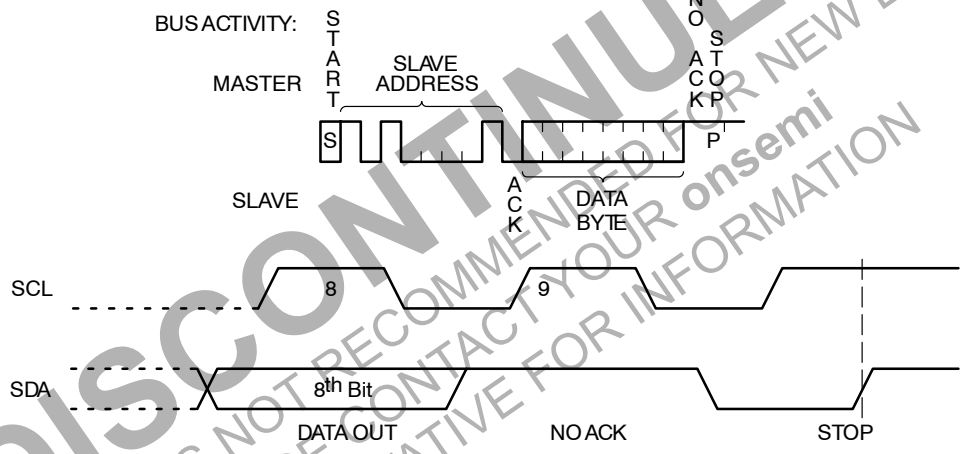


Figure 10. Immediate Read Sequence and Timing

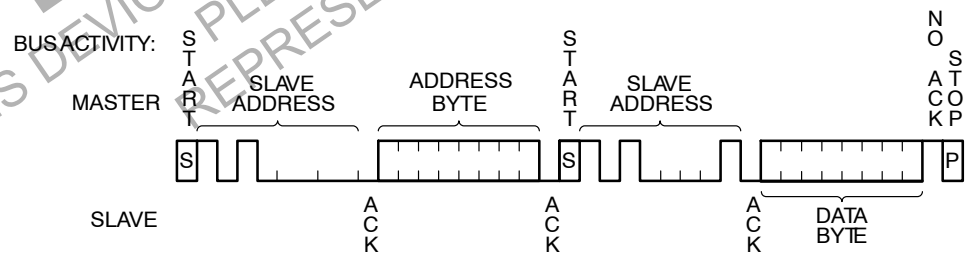


Figure 11. Selective Read Sequence

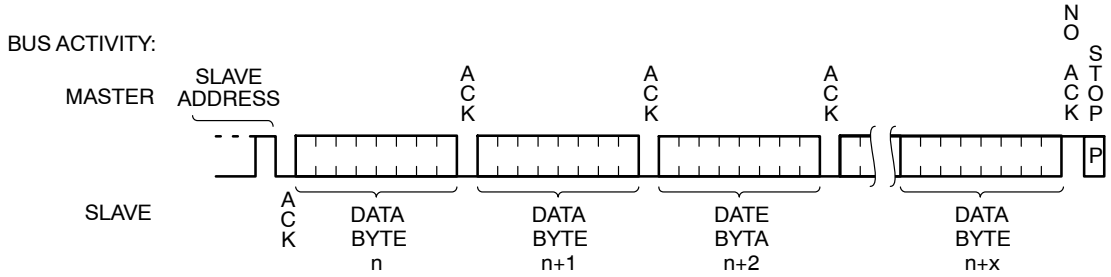


Figure 12. Sequential Read Sequence

Ordering Information

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24AA01TDI−GT3	RS	SOT−23−5	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24AA02TDI−GT3	RS	SOT−23−5	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

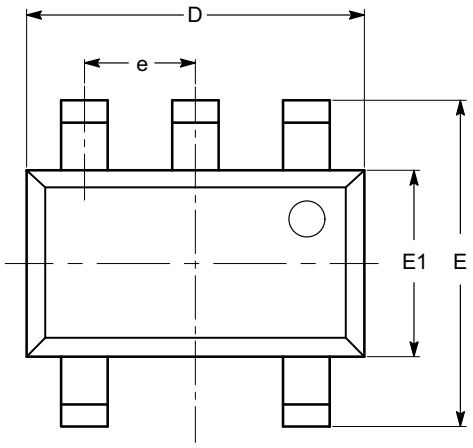
8. All packages are RoHS−compliant (Lead−free, Halogen−free).
9. The standard lead finish is NiPdAu.
10. For additional package and temperature options, please contact your nearest ON Semiconductor sales office.

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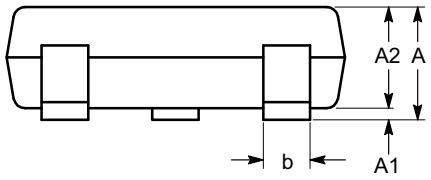
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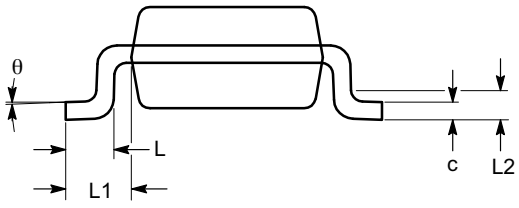


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 TYP	
L	0.30	0.40	0.50
L1		0.60 REF	
L2		0.25 BSC	
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-193.

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