

FEATURES:

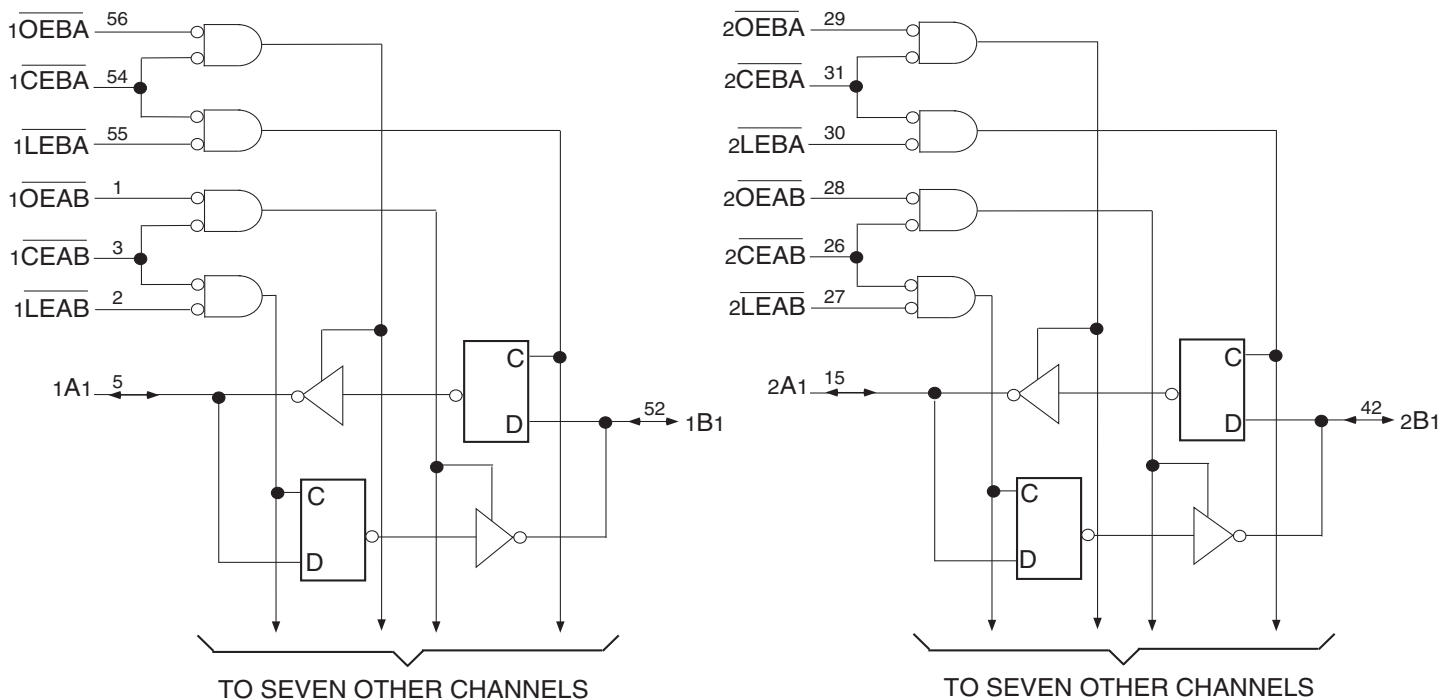
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical  $t_{sk(o)}$  (Output Skew) < 250ps
- Low input and output leakage  $\leq 1\mu A$  (max.)
- $V_{CC} = 5V \pm 10\%$
- High drive outputs (-32mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Power off disable outputs permit "live insertion"
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1.0V at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT16543T 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ( $\overline{xCEAB}$ ) must be low in order to enter data from the A port or to output data from the B port.  $\overline{xLEAB}$  controls the latch function. When  $\overline{xLEAB}$  is low, the latches are transparent. A subsequent low-to-high transition of  $\overline{xLEAB}$  signal puts the A latches in the storage mode.  $\overline{xOEAB}$  performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using  $\overline{xCEBA}$ ,  $\overline{xLEBA}$ , and  $\overline{xOEBA}$  inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

FUNCTIONAL BLOCK DIAGRAM



IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc.

## PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
TSSOP	PAG56	PAG
SSOP	PVG56	PVG

## PIN DESCRIPTION

Pin Names	Description
$\overline{xOEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{xOEB\overline{A}}$	B-to-A Output Enable Input (Active LOW)
$\overline{xCEAB}$	A-to-B Enable Input (Active LOW)
$\overline{xCEBA}$	B-to-A Enable Input (Active LOW)
$\overline{xLEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{xLEBA}$	B-to-A Latch Enable Input (Active LOW)
$\overline{xAx}$	A-to-B Data Inputs or B-to-A 3-State Outputs
$\overline{xBx}$	B-to-A Data Inputs or A-to-B 3-State Outputs

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	-0.5 to 7	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	-0.5 to $V_{CC}+0.5$	V
TSTG	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- All device terminals except FCT162XXX Output and I/O terminals.
- Outputs and I/O terminals for FCT162XXX.

## CAPACITANCE ( $T_A = +25^\circ\text{C}$ , $f = 1.0\text{MHz}$ )

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$V_{IN} = 0V$	3.5	6	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 0V$	3.5	8	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## FUNCTION TABLE<sup>(1, 2)</sup>

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{xCEAB}$	$\overline{xLEAB}$	$\overline{xOEB\overline{A}}$	$\overline{xAx}$ to $\overline{xBx}$	$\overline{xBx}$
H	X	X	Storing	Z
X	H	X	Storing	X
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs
L	L	H	Transparent	Z
L	H	H	Storing	Z

### NOTES:

- \* Before  $\overline{xLEAB}$  LOW-to-HIGH Transition  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{xCEBA}$ ,  $\overline{xLEBA}$  and  $\overline{xOEBA}$ .

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current (Input pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_i = V_{CC}$	—	—	$\pm 1$	$\mu\text{A}$
	Input HIGH Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{IL}$	Input LOW Current (Input pins) <sup>(5)</sup>		$V_i = \text{GND}$	—	—	$\pm 1$	
	Input LOW Current (I/O pins) <sup>(5)</sup>			—	—	$\pm 1$	
$I_{OZH}$	High Impedance Output Current (3-State Output pins) <sup>(5)</sup>	$V_{CC} = \text{Max.}$	$V_o = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_o = 0.5\text{V}$	—	—	$\pm 1$	
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_o = \text{GND}^{(3)}$		-80	-140	-250	mA
$V_H$	Input Hysteresis	—		—	100	—	mV
$I_{CCL}$	Quiescent Power Supply Current	$V_{CC} = \text{Max}$		—	5	500	$\mu\text{A}$
$I_{CCH}$		$V_{IN} = \text{GND or } V_{CC}$					
$I_{CCZ}$							

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$I_o$	Output Drive Current	$V_{CC} = \text{Max.}, V_o = 2.5\text{V}^{(3)}$		-50	—	-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -3\text{mA}$	2.5	3.5	—	V
			$I_{OH} = -15\text{mA}$	2.4	3.5	—	V
			$I_{OH} = -32\text{mA}^{(4)}$	2	3	—	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.2	0.55	V
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN} = \text{ or } V_o \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

### NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^{\circ}\text{C}$  ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. This test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^{\circ}\text{C}$ .

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	60	100	$\mu\text{A}/\text{MHz}$
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.6	1.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	0.9	2.3	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{xLEAB}$ , $\overline{xCEAB}$ and $\overline{xOEAB} = \text{GND}$ $\overline{xCEBA} = V_{CC}$ Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	4.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.4	16.5 <sup>(5)</sup>	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input (} V_{IN} = 3.4V)$   
 $D_H = \text{Duty Cycle for TTL Inputs High}$   
 $N_T = \text{Number of TTL Inputs at } D_H$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(2)</sup>	74FCT16543AT		74FCT16543CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	6.5	1.5	5.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay xLEBA to xAx, xLEAB to xBx		1.5	8	1.5	5.6	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Enable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	9	1.5	7.8	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Disable Time xOEBA or xOEAB to xAx or xBx xCEBA or xCEAB to xAx or xBx		1.5	7.5	1.5	6.5	ns
t <sub>SU</sub>	Set-up Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2	—	2	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW xAx or xBx to xLEAB or xLEBA		2	—	2	—	ns
t <sub>w</sub>	xLEAB or xLEBA Pulse Width LOW		4	—	4	—	ns
t <sub>SK(o)</sub>	Output Skew <sup>(3)</sup>		—	0.5	—	0.5	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

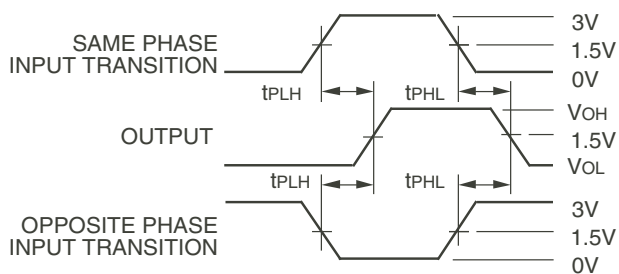
## TEST CIRCUITS AND WAVEFORMS



*Test Circuits for All Outputs*



*Set-up, Hold, and Release Times*



*Propagation Delay*

## SWITCH POSITION

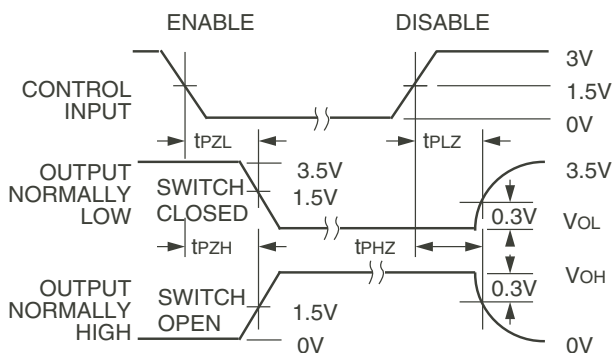
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

### DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Zout of the Pulse Generator.



*Pulse Width*

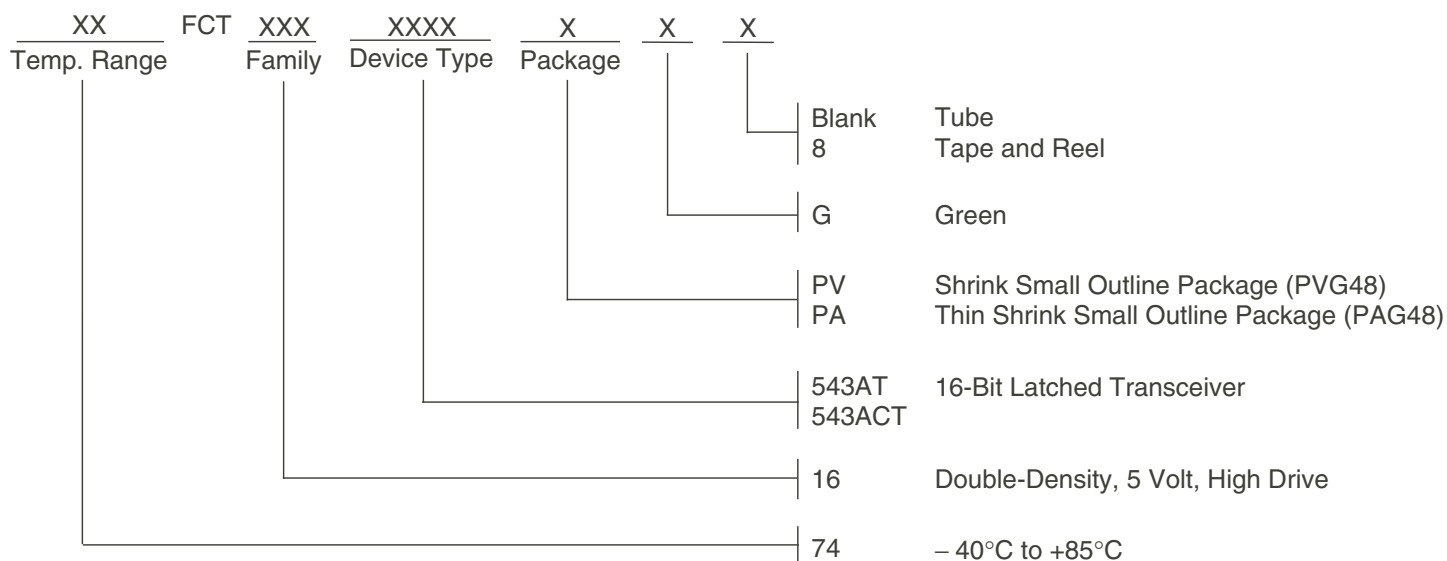


*Enable and Disable Times*

### NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $t_r \leq 2.5\text{ns}$ ;  $t_r \leq 2.5\text{ns}$ .

## ORDERING INFORMATION



## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT16543ATPAG	PAG56	TSSOP	I
	74FCT16543ATPAG8	PAG56	TSSOP	I
	74FCT16543ATPVG	PVG56	SSOP	I
	74FCT16543ATPVG8	PVG56	SSOP	I
C	74FCT16543CTPAG	PAG56	TSSOP	I
	74FCT16543CTPAG8	PAG56	TSSOP	I
	74FCT16543CTPVG	PVG56	SSOP	I
	74FCT16543CTPVG8	PVG56	SSOP	I

## Datasheet Document History

09/28/2009	Pg. 7	Updated the ordering information by removing the "IDT" notation and non RoHS part.
07/31/2017	Pg. 1, 2, 5, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram by deleting 543ET, TSSOP package and adding Tube, Tape and Reel. Added orderable part information table.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).