NextGen Components,Inc.

PART CODE: **1206N680J102CC**

SPECIFICATION SHEET

SPECIFICATION SHEET NO.	Q0618- 1206N680J102CC
DATE	June 18， 2023
REVISION	A2
DESCRIPITION	Multilayer Ceramic Chip Capacitors, Medium Voltage 1206 (3216 Metric) Series, L3.20mm*W1.60mm,Thickness: 1.05mm Max. Dielectric NP0, Capacitance 68pF, Tolerance ±5%, Rated Voltage 1KV, Operating Temp. Range -55°C ~+125°C Package in Tape/Reel, 3,000pcs/Reel RoHS/RoHS III compliant
CUSTOMER	
CUSTOMER PART NUMBER	
CROSS REF. PART NUMBER	
ORIGINAL PART NUMBER	Aillen 1206N680J102CC
PART CODE	1206N680J102CC

VENDOR APPROVE
Issued/Checked/Approved NextGen Components, Inc. Mandy Xu　NextGen Components, Inc. Ruby Zhang　NextGen Components, Inc. Jack Zhang
DATE: June 18， 2023

CUSTOMER APPROVE
DATE:

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NextGen Components,Inc.

PART CODE: **1206N680J102CC**

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

MAIN FEATURE

MLCC consists of a conducting material and electrodes. To manufacture a chip-type SMT and achieve miniaturization, high density and high efficiency, ceramic condensers are used. MLCC is made by NP0, X7R, and Y5V dielectric material and which provides medium Voltage product with high electrical precision, stability and reliability.

MAIN FEATURE

• RoHS III Compliant • Wide Operating Temperature Range -55~+125℃ • High capacitance and High Voltage in given case size • A wide selection of sizes is available (0805 to 1812) • Capacitor with lead-free termination (pure Tin)

APPLICATION

• DC to DC converter.• High voltage coupling/DC blocking • Back-lighting inverters • LAN/WLAN interface • Modem • Power supplies

RFQ
Request For Quotation

PART CODE GUIDE

Code	Name	Key Specification Option
1206	Size	0805 (2012): L2.00*W1.25mm; **1206 (3216) :L3.20*W1.60mm;** 1210 (3225): L3.20*W2.50mm; 1808 (4520) :L4.50*W2.00mm; 1812 (4532): L4.50*W3.20mm
N	Dielectric	**N: NP0 (C0G);** B: X7R; Y: Y5V
680	Capacitance	Two significant digits followed by number of Zero, The 3rd digit signifies the multiplying factor, and letter R is decimal point. 0R5: 0.5pF; 1R0:1.0pF; **680: 68pF;** 821: 820pF
J	Tolerance	B=±0.1pF; C=±0.25pF; D=±0.5pF; F=±1%; G=±2%; **J=±5%;** K=±10%; M=±20%; Z=-20/+80%
102	Rated Voltage	Two significant digits followed by No. of zeros. “R” is in place of decimal point. **102=1000 VDC;** 202=2000 VDC; 302=3000 VDC
C	Thickness	A: 0.60±0.10mm; B: 0.85 ±0.15mm; **C: 0.95±0.10mm;** D: 1.25±0.20mm G: 1.60±0.20mm; K: 2.00±0.20mm; M: 2.50±0.30mm; N: 0.50+0.05mm; P: 1.60+0.30/-0.10mm; U: 2.80±0.30mm;
C	Package	A: 1Kpcs/Reel; B: 2Kpcs/Reel; **C: 3Kpcs/Reel;** D: 4Kpcs/Reel; I: 10Kpcs/Reel; K: 0.5 Kpcs/Reel; F: others
	Internal Control	Internal Code: Letter + Number; Blank: N/A;

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

DIMENSION (Unit: mm)

Image for reference



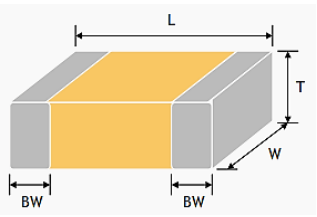


Table 1

Size Code	L	W	T	BW
0805 (2012)	2.00±0.15	1.25±0.1	1.35	0.50
1206 (3216)	3.20±0.20	1.60±0.20	1.80	0.30
1210 (3225)	3.20±0.40	2.50±0.30	2.80	0.30
1808 (4520)	4.50±0.40	2.00±0.20	2.20	0.26
1812 (4532)	4.50±0.40	3.20±0.30	2.80	0.26

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

GENERAL ELECTRONICAL CHARACTERISTICS

Table 2

Dielectric	NP0		X7R	
Size	0805, 1206, 1210, 1808, 1812		0805, 1206, 1210, 1812, 1808	
Rated voltage (WVDC)	1KV, 2KV, 3KV		1KV, 2KV, 3KV	
Capacitance range*	1KV	1.5pF ~ 2.2nF	1KV	100pF ~ 100nF
	2KV	1.5pF ~ 1.2nF	2KV	150pF ~ 12nF
	3KV	2.2pF ~ 470pF	3KV	150pF ~ 3.9nF
Capacitance tolerance	Cap≤5pF: B (±0.1pF), C (±0.25pF) 5pF<Cap<10pF: C (±0.25pF), D (±0.5pF) Cap≥10pF: F (±1%), G (±2%), J (±5%), K (±10%)		J (±5%), K (±10%), M (±20%)	
Tan δ*	Cap<30pF: Q≥400+20C Cap≥30pF: Q≥1000		≤2.5%	
Insulation resistance at 500Vdc for 60 seconds	≥100GΩ or R·C≥1000 whichever is smaller		≥10GΩ or R·C≥500Ω-F whichever is smaller	
Operating temperature	-55 to +125° C			
Temperature coefficient	±30ppm / ℃		±15%	
Termination	Ag (or Cu)/Ni/Sn (lead-free termination)			

Note:

1) * Measured at the condition of 30~70% related humidity.
2) NP0: Apply 1.0±0.2Vrms, 1.0MHz±10% for Cap≦1000pF and 1.0±0.2Vrms, 1.0kHz±10% for Cap>1000pF, 25°C at ambient temperature.
3) X7R: Apply 1.0±0.2Vrms, 1.0kHz±10%, at 25°C ambient temperature.

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-A

Size	1206		1210		1808			1812			0805
VDC (V)	1000	2000	1000	2000	1000	2000	3000	1000	2000	3000	1000
1.5pF (1R5)	B	B									D
1.8pF (1R8)	B	B									D
2.0pF (2R0)	B	B			D	D	D				D
2.2pF (2R2)	B	B			D	D	D				D
2.7pF (2R7)	B	B			D	D	D				D
3.3pF (3R3)	B	B			D	D	D				D
3.9pF (3R9)	B	B			D	D	D				D
4.7pF (4R7)	B	B			D	D	D				D
5.6pF (5R6)	B	B			D	D	D				D
6.8pF (6R8)	B	B			D	D	D				D
8.2pF (8R2)	B	B			D	D	D				D
10pF (100)	B	B	C	C	D	D	D	D	D	D	D
12pF (120)	B	B	C	C	D	D	D	D	D	D	D
15pF (150)	B	B	C	C	D	D	D	D	D	D	D
18pF (180)	B	B	C	C	D	D	D	D	D	D	D
22pF (220)	B	B	C	C	D	D	D	D	D	D	D
27pF (270)	B	B	C	C	D	D	D	D	D	D	D
33pF (330)	B	C	C	C	D	D	D	D	D	D	D
39pF (390)	B	C	C	C	D	D	D	D	D	D	D
47pF (470)	C	C	C	C	D	D	D	D	D	D	D
56pF (560)	C	D	C	D	D	D	D	D	D	D	D
68pF (680)	C	D	C	D	D	D	D	D	D	D	D
82pF (820)	D	D	C	D	D	D	D	D	D	D	D
100pF (101)	D	D	D	D	D	K	K	D	D	D	D
120pF (121)	D	G	D	D	D	K	K	D	D	D	D
150pF (151)	D	G	D	G	D	K	K	D	D	D	D
180pF (181)	G	G	D	G	D	K	K	D	K	K	D
220pF (221)	G	G	G	G	D	K	K	D	K	K	D
270pF (271)	G	P	G	K	K	K	K	D	K	K	D
330pF (331)	G	P	G	K	K	K	K	D	K	K	D

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 3-B

Size	1206		1210		1808			1812			0805
VDC (V)	1000	2000	1000	2000	1000	2000	3000	1000	2000	3000	1000
390pF (391)	G	P	G	M	K	K		D	K	K	D
470pF (471)	G		G	M	K	K		K	K	K	
560pF (561)	G		G		K	K		K	K		
680pF (681)	G		G		K	K		K	K		
820pF (821)	G		G		K			K	K		
1,000pF (102)	G		G		K			K	K		
1,200pF (122)			G					K			
1,500pF (152)			K					K			
1,800pF (182)			M					K			
2,200pF (222)			M					K			
2,700pF (272)			M					K			
3,300pF (332)			M					K			
3,900pF (392)			M					M			

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

Table 4-A

Size	1206		1210		1808			1812			0805
VDC (V)	1000	2000	1000	2000	1000	2000	3000	1000	2000	3000	1000
100pF (101)	D	D	D	D							B
120pF (121)	D	D	D	D							B
150pF (151)	D	D	D	D	D	D	D				B
180pF (181)	D	D	D	D	D	D	D				B
220pF (221)	D	D	D	D	D	D	D				B
270pF (271)	D	D	D	D	D	D	D	D	D	K	B
330pF (331)	D	D	D	D	D	D	K	D	D	K	B
390pF (391)	D	D	D	D	D	D	K	D	D	K	B
470pF (471)	D	D	D	D	D	D	K	D	D	K	B /D
560pF (561)	D	D	D	D	D	D	K	D	D	K	B
680pF (681)	D	D	D	D	D	D	K	D	D	K	B
820pF (821)	D	D	D	D	D	D	K	D	D	K	B
1,000pF (102)	D	B/C /D/G	D	D	D	K	K	D	D	K	B
1,200pF (122)	D	G	D	M	D	K	K	D	D	K	B
1,500pF (152)	D	G	D	M	D	K	K	D	D	K	D
1,800pF (182)	D	G	D	M	D	K	K	D	D	M	D
2,200pF (222)	D	C/G	D	M	D	K		D	D	M	D
2,700pF (272)	D	G	D	M	D	K		D	D	M	D
3,300pF (332)	D	G	D	M	D	K		D	K	M	D
3,900pF (392)	D		G	M	D	K		D	K		D
4,700pF (472)	D		G	M	D	K		D	K		D
5,600pF (562)	D		G	M	K	K		D	M		D
6,800pF (682)	D		G	M	K	K		D	M		D
8,200pF (822)	D		G	M	K			D	M		D
0.010µF (103)	D		G		K			D	M		
0.012µF (123)	G		G		K			K			

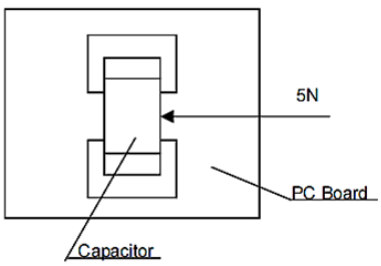
MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 0805, 1206,1210, 1808, 1812 SIZES

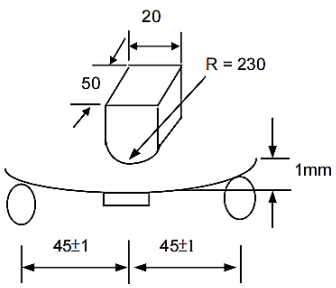
Table 4-B

Size	1206		1210		1808			1812			0805
VDC (V)	1000	2000	1000	2000	1000	2000	3000	1000	2000	3000	1000
0.015µF (153)	G		G		K			K			
0.018µF (183)			G		K			M			
0.022µF (223)			G		K			M			
0.033µF (333)			G		K			M			
0.039µF (393)			K		K			M			
0.047µF (473)			M		K			M			
0.056µF (563)			M		K			M			
0.068µF (683)			M					M			
0.10µF (104)								M			

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>Visual and Mechanical</td><td>-</td><td>* No remarkable defect.
* Dimensions to conform to individual spec. sheet.</td></tr>
<tr><td>Capacitance</td><td rowspan="2">Class I: C0G (NP0)
≦1000pF, 1.0±0.2Vrms, 1MHz±10%
＞1000pF, 1.0±0.2Vrms,1KHz±10%
Class II: (X7R)
1.0±0.2Vrms, 1KHz±10%</td><td>* Shall not exceed the limits given in the detailed spec.</td></tr>
<tr><td>Q/D.F (Dissipation Factor)</td><td>NP0: Cap≧30pF, Q≧1000;
Cap<30pF,Q≧400+20C
X7R: ≦2.5%</td></tr>
<tr><td>Dielectric Strength</td><td>* To apply voltage: 1.2 times of UR
* Duration: 1 to 5 sec.</td><td>* No evidence of damage or flash over during test.</td></tr>
<tr><td>Insulation Resistance</td><td>*To apply voltage at 500VDC for 60 sec.</td><td>Class I (NP0) : ≥100GΩ or RxC≥1000Ω-F whichever is smaller. Class II (X7R) : ≥10GΩ or RxC≥500Ω-F whichever is smaller.</td></tr>
<tr><td>Temperature Coefficient</td><td>With no electrical load @Oprtating Temp. Range
<table><tr><th>T.C</th><th>Temp. (°C)</th></tr><tr><td>NP0(C0G)</td><td>-55~125 at 25</td></tr><tr><td>X7R</td><td>-55~125 at 25</td></tr></table></td><td><table><tr><th>T.C</th><th>Capacitance Change</th></tr><tr><td>NP0 (C0G)</td><td>Within ±30ppm/℃</td></tr><tr><td>X7R</td><td>Within ±15%</td></tr></table></td></tr>
<tr><td>Adhesive Strength of Termination</td><td>*Capacitors mounted on a substrate. A force of 5N applied perpendicular to the place of substrate and parallel the line joining the center of terminations for 10±1 sec.

</td><td>* No remarkable damage or removal of the terminations.</td></tr>
</table>

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements
Humidity (Damp Heat) Steady State	*Test temp.: 40±2° C *Humidity: 90~95% RH *Test time: 500+24/-0hrs. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	*No remarkable damage. *Cap change: NP0 within ±5% or ±2pF whichever is larger X7R within ±15% *Q/D.F Value: NP0: Cap≥30pF :Q≥350 10pF≤Cap<30pF :Q≥275+2.5C Cap<10pF :Q ≥200+10C X7R: ≤7.0% * I.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.
Resistance to Flexure of Substrate	* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1mm per second until the deflection becomes 1mm. 	* No remarkable damage. * Cap change: NP0 : within ±10% X7R : within ±12.5% (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test.)
High Temperature Load (Endurance)	*Test temp.: NP0, X7R: 125±3° C *To apply voltage: 120% of rated voltage. *Test time: 1000+24/-0 hrs. * Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).	*No remarkable damage. *Cap change: NP0 within ±3% or ±3pF whichever is larger X7R within ±20% *Q/D.F Value: NP0: Cap≥30pF :Q≥350 10pF≤Cap<30pF :Q≥275+2.5C Cap<10pF :Q ≥200+10C X7R: ≤7.0% * I.R.: ≥10V, ≥1GΩ or RxC≥50Ω-F whichever is smaller.

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>Resistance to Soldering Heat</td><td>* Solder temperature: 260±5° C
* Dipping time: 10±1 sec
* Preheating: 120 to 150° C for 1 minute before immerse the capacitor in a eutectic solder.
*Before initial measurement (Class II only): Perform 150+0/-10° C for 1 hr and then set for 48±4 hrs at room temp.
* Measurement to be made after keeping at room temp. for 24±2hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
* Cap change:
NP0: within ±2.5% or 0.25pF whichever is larger
X7R: within ±7.5%;
* 25% max. leaching on each edge.</td></tr>
<tr><td>Temperature Cycle</td><td>*Conduct the five cycles according to the temperatures and time.
<table><tr><th>Step</th><th>Temp. (°C)</th><th>Time(min)</th></tr><tr><td>1</td><td>Min. operating temp.+0/-3</td><td>30±3</td></tr><tr><td>2</td><td>Room temp.</td><td>2~3</td></tr><tr><td>3</td><td>Max. operating temp.+3/-0</td><td>30±3</td></tr><tr><td>4</td><td>Room temp.</td><td>2~3</td></tr></table>* Before initial measurement (Class II only): Perform 150+0/-10° C for 1 hr and then set for 48±4 hrs at room temp.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
* Cap change：
NP0: within ±2.5% or 0.25pF whichever is larger
X7R: within ±15%
* Q/D.F.:
NP0: ≤2.0 × Initial requirement
X7R: ≤1.5 × Initial requirement
* I.R.≥ 0.25 × initial requirement</td></tr>
<tr><td>Solderability</td><td>* Solder temperature: 235±5° C
* Dipping time: 5±0.5 sec.</td><td>75% min. coverage of all metalized area</td></tr>
</table>

RECOMMENDED PROFILE CONDITIONS

PREHEAT:

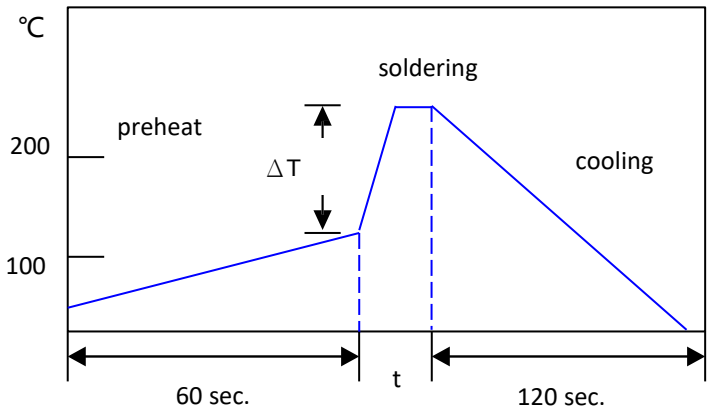
In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 4℃ per second and the final preheat temperature should be within 100℃ of the soldering temperature for small chips such as 1206, within 50℃ of the soldering temperature for bigger chips such as 1210 and 1808, 1812, etc

SOLDERING

(1) Use middy activated rosin RA and RMA fluxes do not use activated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

(2) Hand soldering with temperature-controlled iron not exceeding 30 watts and diameter of tip less than 1.2 mm is recommended, tip of iron should not contact the ceramic body directly, and the temperature of iron should be set to not more than 260℃.

RECOMMENDED SOLDERING PROFILES



Soldering	Solder Temp.(T)	Soldering Time (t)
Reflow	235 – 260 ℃	< 15 sec.
Wave	230 – 260 ℃	< 5 sec.

Chip Size	ΔT
1206	100 ℃
1210, 1808, 1812,	50 ℃

(3) For bigger chips such as 1210 1808 and 1812, etc. wave soldering and hand soldering are no recommended.

(4) Refer IPC/JEDEC J-STD-020D Method recommended soldering profiles :

Reflow not sooner than 15 minutes and not longer than 4 hrs after removal from the temperature/humidity chamber, subject the sample to 3 cycle of the appropriate reflow conditions as defined as blow Table description.

(5) Lead-free : Soldering temperature = 235 to 260℃, depending on product.

(6) Maximum temperature = Minimum temperature (235℃)+ΔT+ Tolerance for oven process and measurement (5 ~ 7℃)

(7) Time at peak temperature = 10sec, Dwell above 217℃ = 90sec, Ramping rate = 3℃/sec(heating) and 6 ℃/sec (heating).

COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint. A cooling rate not exceeding 4℃ per second should be used when forced cooling is necessary.

CLEANING

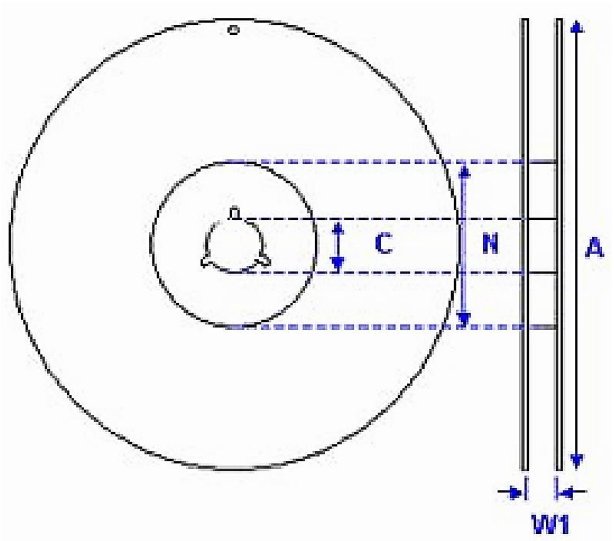
All flux residues must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contamination that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is depends upon many factors such as component mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

PACKAGING STYLE AND QUANTITY

Size	Thickness (Symbol)		Paper Tape		Plastic Tape	
			7" Reel	13" Reel	7" Reel	13" Reel
0805 (2012)	0.50±0.10	N	4,000	15,000		
	0.60±0.10	A	4,000	15,000		
	0.85±0.15	B	4,000	15,000		
	0.85±0.10	T	4,000	15,000		
	1.25±0.15	C			3,000	10,000
1206 (3216)	0.85±0.15	B	4,000	15,000		
	0.85±0.10	T	4,000	15,000		
	0.95±0.10	I			3,000	10,000
	1.15±0.15	J			3,000	10,000
	1.25±0.15	C			3,000	10,000
	1.60±0.15	D			2,000	10,000
	1.60+0.30/-0.10	P			2,000	9,000
1210 (3225)	0.85±0.10	T			3,000	10,000
	0.95±0.10	I			3,000	10,000
	1.25±0.15	C			3,000	10,000
	1.60±0.15	D			2,000	
	2.00±0.20	K			1,000	6,000
	2.50±0.30	M			1,000	6,000
1808 (4520)	1.25±0.15	C			2,000	10,000
	1.10±0.15	F			2,000	10,000
	1.60±0.15	D			2,000	8,000
	2.00±0.20	K			1,000	6,000
1812 (4532)	1.25±0.15	C			1,000	5,000
	1.60±0.15	D			1,000	
	2.00±0.20	K			1,000	
	2.50±0.30	M			500	3,000
	2.80±0.30	U			500	

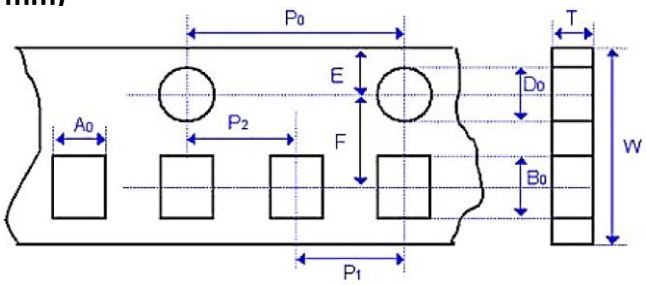
REEL DIMENSION (Unit: mm)



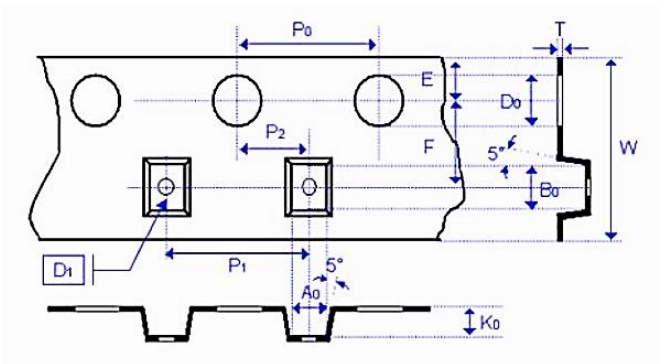
Size Code	0805, 1206, 1210, 1812			1808, 1812
Reel Size	7”	10”	13”	7”
C	13.0+0.5/-0.2	13.0+0.5/-0.2	13.0+0.5/-0.2	13.0+0.5/-0.2
W 1	8.4+1.5/-0	8.4+1.5/-0	8.4+1.5/-0	12.4+2.0/-0
A	178.0±0.10	250.0±1.0	330.0±1.0	178.0±0.10
N	60.5±1.0	100.0±1.0	100±1.0	60.5±1.0

TAPE DIMENSION (Unit: mm)

Paper Tape



Plastic Tape



Size	0805	
Thickness	B	D
A0	1.5±0.20	<1.80
B0	2.3±0.20	<2.70
T	≦1.20	0.23±0.10
K0		
W	8.0±0.30	8.0±0.30
P0	4.0±0.10	4.0±0.10
10xP0	40±0.20	40±0.20
P1	4.0±0.10	4.0±0.10
P2	2.0±0.05	2.0±0.05
D0	1.5+0.1/-0	1.5+0.1/-0
D1		1.0±0.10
E	1.75±0.10	1.75±0.10
F	3.5±0.05	3.5±0.05

MULTILAYER CERAMIC CHIP CAPACITORS 1206 SERIES

TAPE DIMENSION (Unit: mm)

Size	1206			1210	
Thickness	B	C,D	G, P	C, D, P, K	M
A0	2.00±0.10	<2.00	<2.00	<3.05	<3.10
B0	3.50±0.10	<3.60	<3.70	<3.80	<4.00
T	0.95±0.05	0.23±0.05	0.23±0.05	0.23±0.05	0.23±0.05
K0	-	<2.50	<2.50	<2.50	<3.50
W	8.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10	8.00±0.10
P0	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.100	4.00±0.10
10xP0	40.0±0.20	40.00±0.20	40.00±0.20	40.00±0.20	40.0±0.20
P1	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10	4.00±0.10
P2	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05	2.00±0.05
D0	1.50±0.05	1.50±0.10/-0	1.50±0.10/-0	1.50±0.10/-0	1.50±0.10/-0
D1	-	1.00±0.10	1.00±0.10	1.00±0.10	1.00±0.10
E	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10	1.75±0.10
F	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05	3.50±0.05

Size	1808, 1812	
Thickness	D, G, P	K
A0	<2.50	<2.50
B0	<5.30	<5.30
T	0.25±0.05	0.25±0.05
K0	<2.50	<2.50
W	12.0±0.20	12.0±0.20
P0	4.00±0.10	4.00±0.10
10xP0	40.0±0.20	40.0±0.20
P1	4.00±0.10	4.00±0.10
P2	2.00±0.05	2.00±0.05
D0	1.50±0.10/-0	1.50+0.10/-0
D1	1.50±0.10	1.50±0.10
E	1.75±0.10	1.75±0.10
F	5.50±0.05	5.50±0.05

STORAGE AND HANDLING CONDITIONS

(1) To store products at 5 to 40℃ ambient temperature and 20 to 70%. related humidity conditions.

(2) No harmful gases containing sulfuric acid, ammonia, hydrogen sulfide or chlorine. Packaging should not be opened until the capacitors are required for use. If opened, the pack should be re-sealed as soon as is practicable. Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesion performance. The capacitors should be used within one year and checked the solderability before use.

(3) Don't open the tape until the parts are to be used, use the chips within 3 months after the tape is opened.

(4) For product of high dielectric constant (Class2 & 3, characteristics B/W & Y), the Electro static capacity changes with the passage of time due to the inherent characteristics of ceramic dielectric materials. The changed capacity reverts to nominal at the temperature it reaches during the soldering process.

(5) HANDLING : Chip capacitors are dense, hard, brittle, and abrasive materials. They are liable to suffer mechanical damage, in the form of cracks or chips. Chip Capacitors should be handled with care to avoid contamination or damage. To use vacuum or plastic tweezers to pick up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

CAUTIONS

(1) The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solder ability. Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)

(2) In corrosive atmosphere, solder ability might be degraded, and silver migration might occur to cause low reliability.

(3) Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sun light, the solder ability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

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