MP2145

5.5V, 6A, 1.2MHz, High-Efficiency, 40μA I_Q Constant On-Time Synchronous, Step-Down Switcher

The Future of Analog IC Technology®

DESCRIPTION

The MP2145 is a monolithic, step-down, switch-mode converter with internal power MOSFETs. It can achieve up to 6A continuous output current from a 2.8V-to-5.5V input voltage with excellent load and line regulation. The output voltage can be regulated to as low as 0.6V.

Constant-on-time control provides a fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP2145 is available in a small QFN2×3mm package and requires only a minimal number of readily-available, standard, external components.

The MP2145 is ideal for a wide range of applications, including storage (SSD, HDD), high-performance DSPs, FPGAs, and distributed power systems.

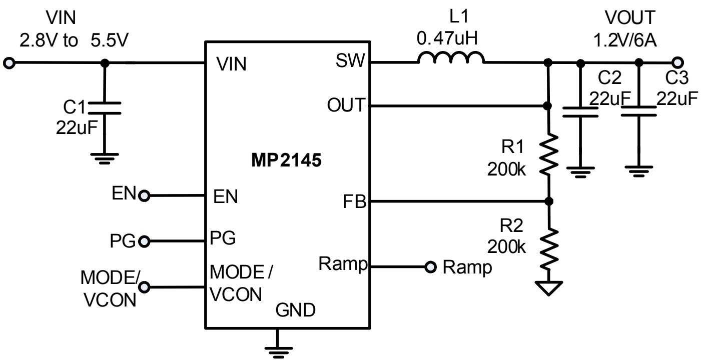
FEATURES

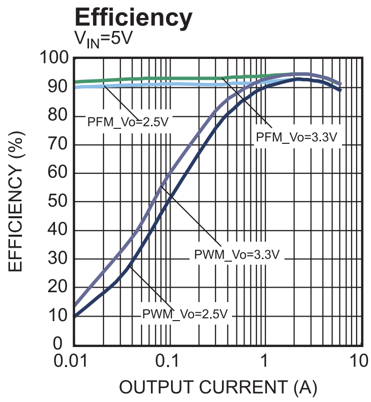
- Up to 6A Output Current
- Wide 2.8V-to-5.5V Operating Input Range
- 20mΩ and 12mΩ Internal Power MOSFETs
- 40μA Quiescent Current
- 1.2MHz Fixed Switching Frequency
- 100% Duty Cycle in Dropout
- 1% Feedback Accuracy
- External Mode Control
- External VCON Control
- Adjustable Output from 0.6V
- 1.5ms Internal SS Time with Pre-Bias Startup
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Thermal Shutdown
- Available in a 2mm×3mm QFN Package
- Output Discharge Function

APPLICATIONS

- Storage (SSD, HDD)
- Portable Instruments
- Battery-Powered Devices

TYPICAL APPLICATION



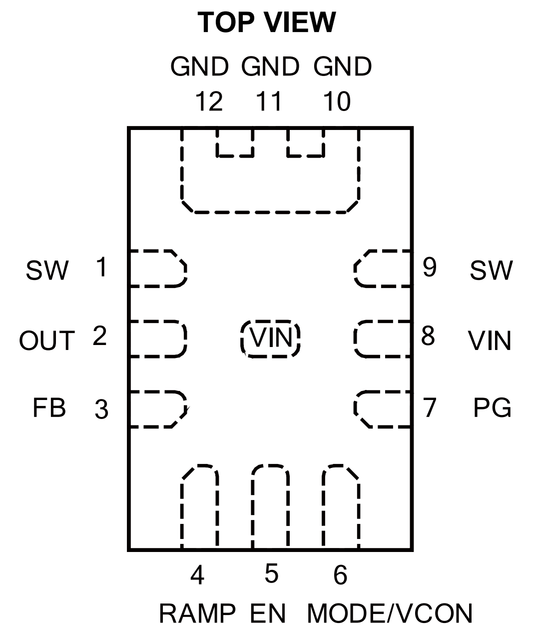


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2145GD	QFN-12 (2mmx3mm)	AFV

* For Tape & Reel, add suffix –Z (e.g. MP2145GD–Z);

PACKAGE REFERENCE



QFN-12 (2mm×3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 6V
V_{SW} ....
……..–0.3V (-3V for <10ns) to 6V (8V for <10ns)
All Other Pins .... –0.3V to +6 V
Junction Temperature .... 150°C
Lead Temperature .... 260°C
Continuous Power Dissipation (T_A = +25°C)(2)
.... 1.78W

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .... 2.8V to 5.5V
Output Voltage V_{OUT}........................ 0.6V to 5.5V
Operating Junction Temp. ....-40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-12 (2mmx3mm)..………………	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, T_A = 25°C, unless otherwise noted.

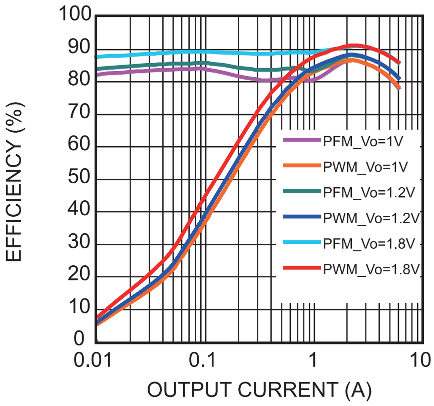
Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Quiescent)	I_Q	V_{IN}=3.6V, V_{EN}=2V, V_{FB} = 0.65V		40	60	μA
Shutdown Current		V_{EN} = 0V		0.1	1	μA
IN Under-Voltage Lockout Threshold			2.4	2.55	2.7	V
IN Under-Voltage Lockout Hysteresis				300		mV
Regulated FB Voltage	V_{FB}	2.8V<V_{IN}<5.5V	0.594	0.600	0.606	V
FB Input Current		V_{FB} = 0.65V		50		nA
EN High Threshold			1.6			V
EN Low Threshold					0.4	V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
Internal Soft-Start Time (5)	τ_{SS}			1.5		ms
High-Side Switch On-Resistance	R_{DSON_P}			20		mΩ
Low-Side Switch On-Resistance	R_{DSON_N}			12		mΩ
SW Leakage Current				0	1	μA
High-Side Switch Current Limit		Sourcing	7.5	8.1		A
Low-Side Switch Current Limit (6)		Sinking, PWM Mode		5		A
		Sinking, PFM Mode		0		
Oscillator Frequency			0.96	1.2	1.44	MHz
Minimum On Time	τ_{ON_MIN}			50		ns
Minimum Off Time	τ_{OFF_MIN}			60		ns
PG UV Threshold Rising	PGTH_Hi			0.9		VFB
PG UV Threshold Falling	PGTH_Lo			0.85		VFB
PG OV Threshold Rising	PGTH_Hi			1.15		VFB
PG OV Threshold Falling	PGTH_Lo			1.1		VFB
PG Delay	PG_{TD}			140		μs
PG Sink Current Capability		Sink 1mA			0.4	V
PG INTERNAL Pull Up Resistor				500		kΩ
Thermal Shutdown Threshold (6)				150		°C
Thermal Shutdown Hysteresis (6)				20		°C
MODE Forced PWM Threshold		V_{IN}=3.6V, V_{EN}=2V	1.2			V
MODE PFM Threshold		V_{IN}=3.6V, V_{EN}=2V			0.4	V

Notes:
5) Guaranteed by characterization
6) Guaranteed by design.

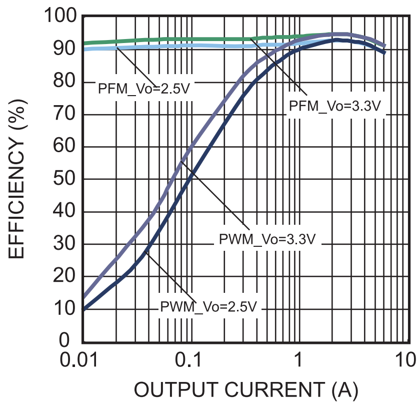
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

Efficiency

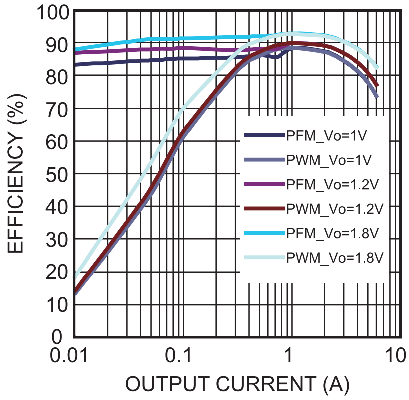


Efficiency

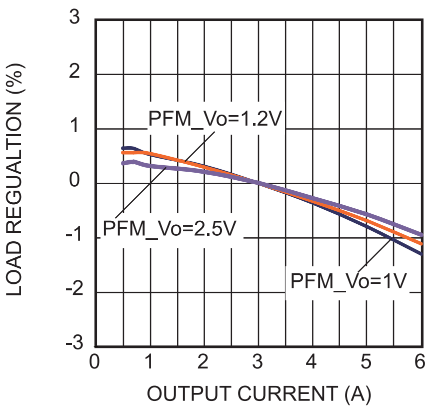


Efficiency

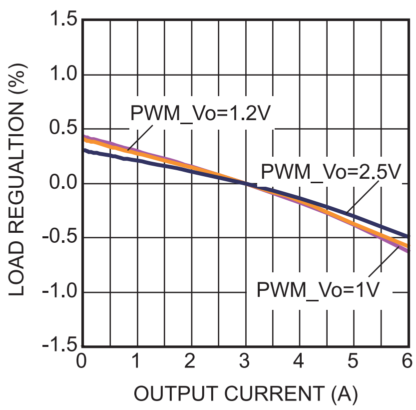
V_{IN}=3.3V



Load Regulation

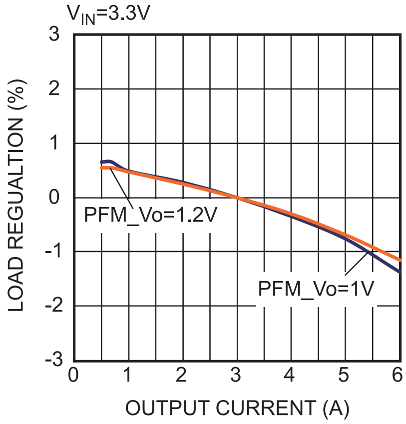


Load Regulation



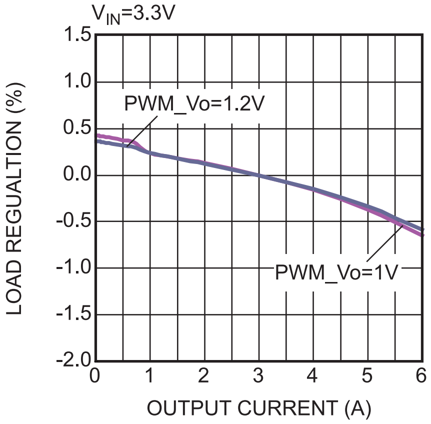
Load Regulation

V_{IN}=3.3V

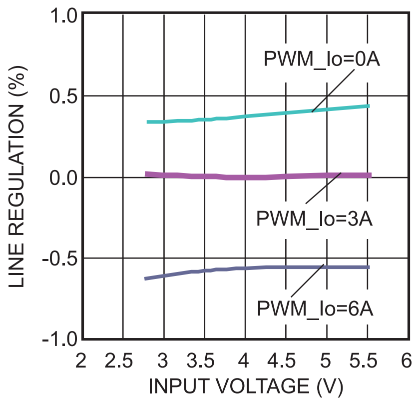


Load Regulation

V_{IN}=3.3V

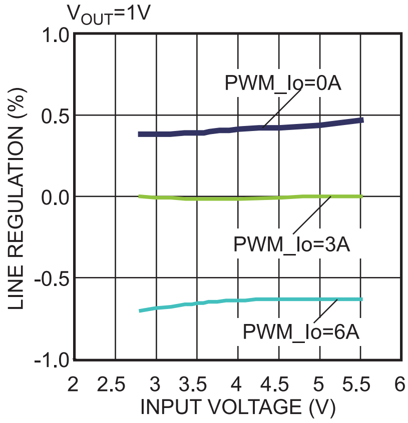


Line Regulation



Line Regulation

V_{OUT}=1V

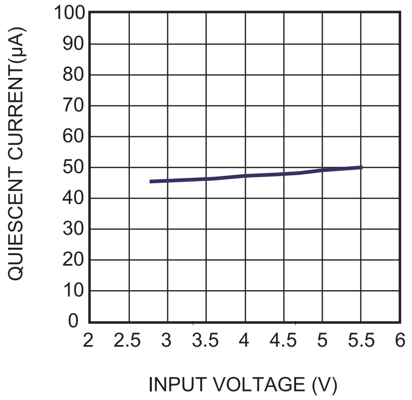


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

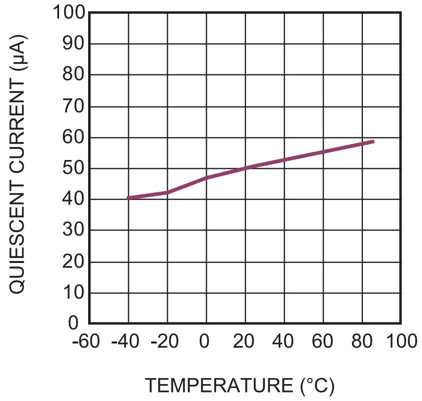
V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

Quiescent Current vs. Input Voltage

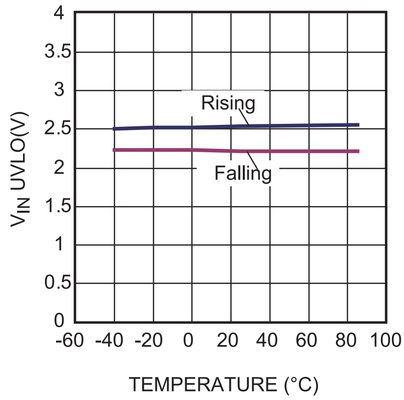
EN=2V, FB=0.65V,SW=GND



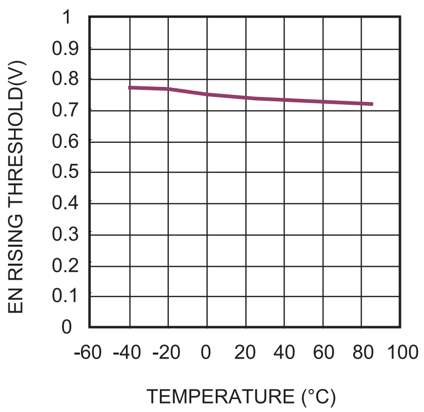
Quiescent Current vs. Temperature



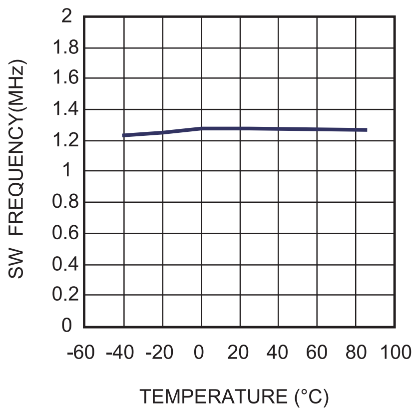
V_{IN} UVLO Rising Threshold vs. Temperature



EN Rising Threshold vs. Temperature

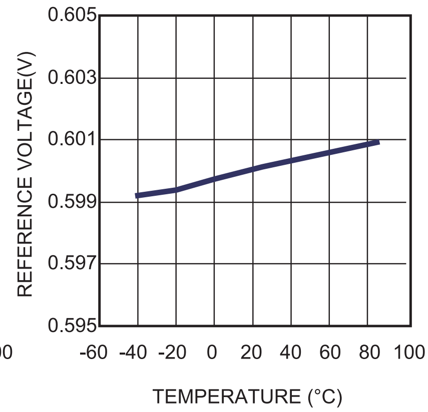


Switch Frequency vs. Temperature

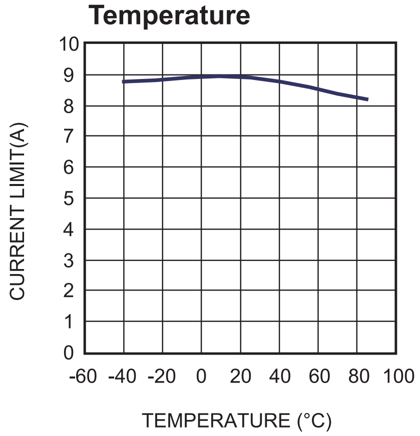


Reference Voltage vs. Temperature

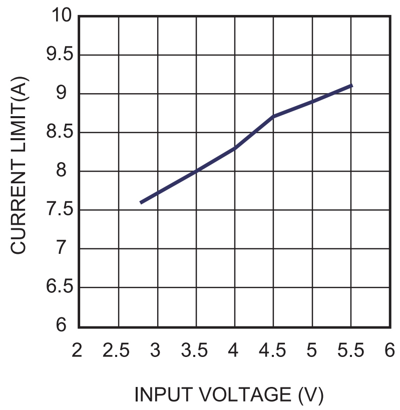
V_{IN}=3.6V



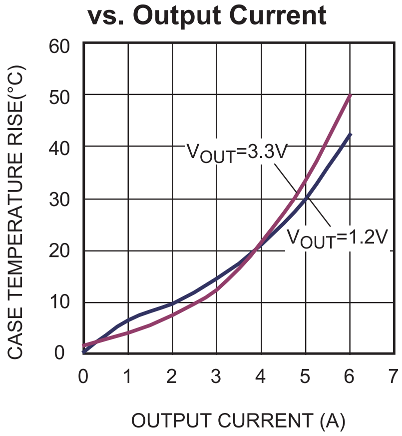
Current Limit vs. Temperature



Current Limit vs. V_{IN}

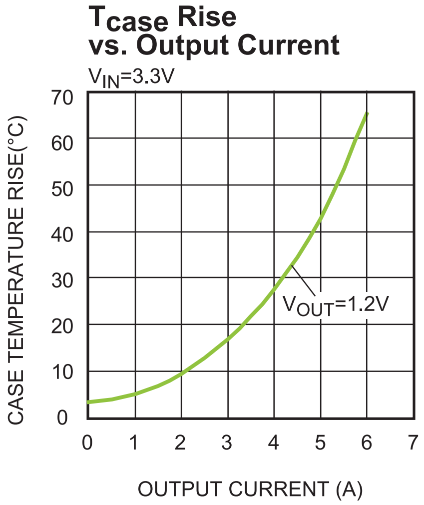


T_{case} Rise vs. Output Current



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

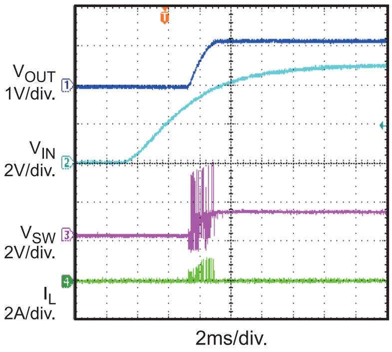


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

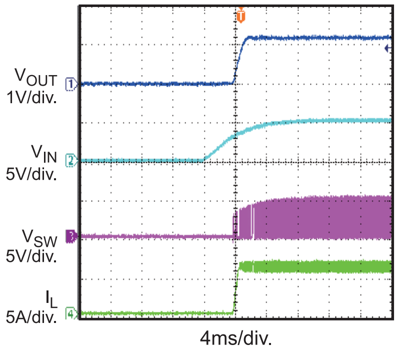
Power Up

I_{OUT}= 0A, PFM



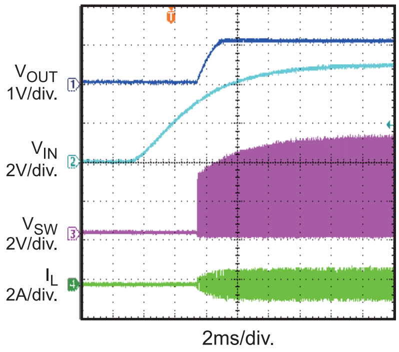
Power Up

I_{OUT}= 6A, PFM



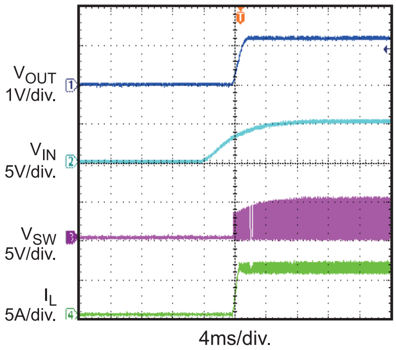
Power Up

I_{OUT}= 0A, PWM



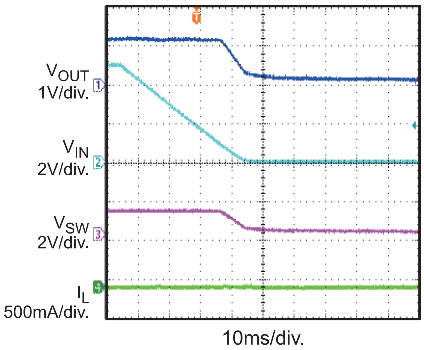
Power Up

I_{OUT}= 6A, PWM



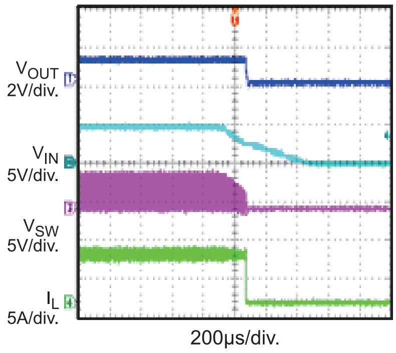
Power Off

I_{OUT}= 0A, PFM



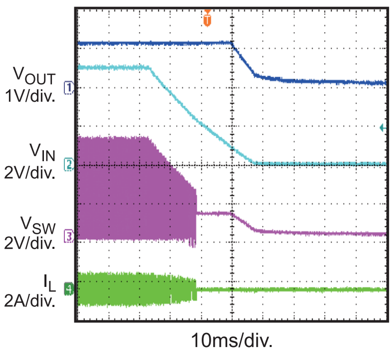
Power Off

I_{OUT}= 6A, PFM



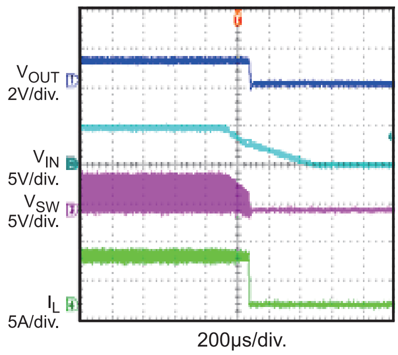
Power Off

I_{OUT}= 0A, PWM



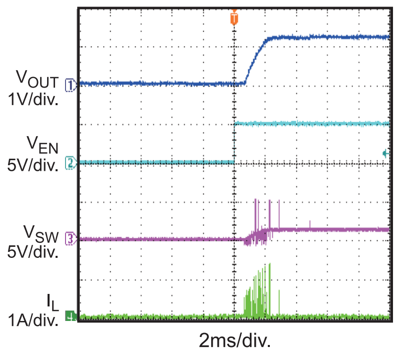
Power Off

I_{OUT}= 6A, PWM



Enable On

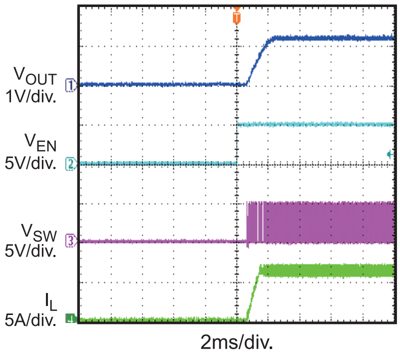
I_{OUT}= 0A, PFM



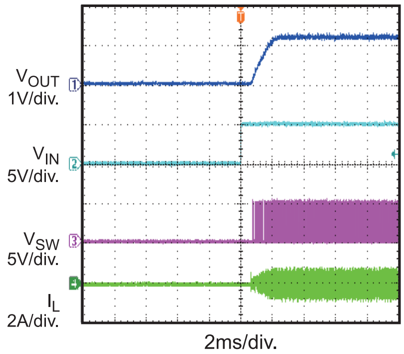
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

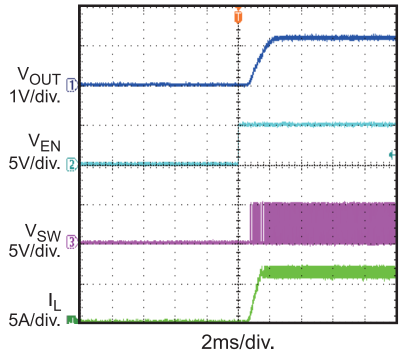
Enable On
I_{OUT}= 6A, PFM



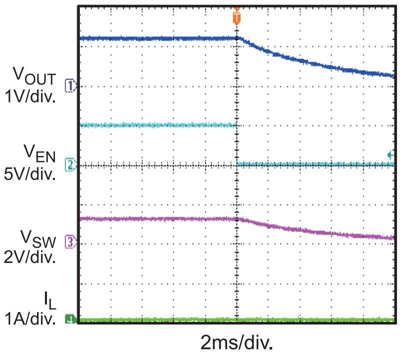
Enable On
I_{OUT}= 0A, PWM



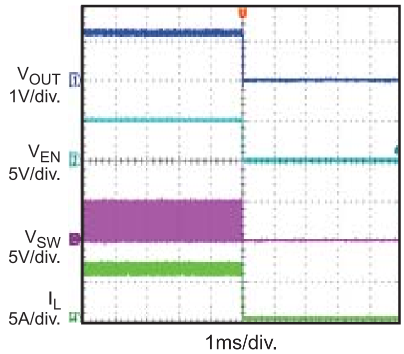
Enable On
I_{OUT}= 6A, PWM



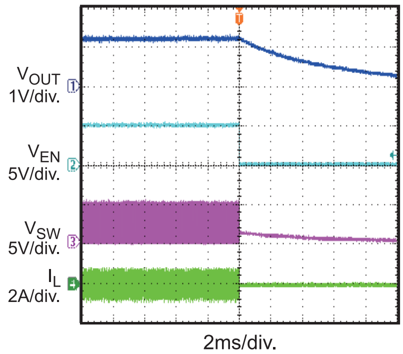
Enable Shutdown
I_{OUT}= 0A, PFM



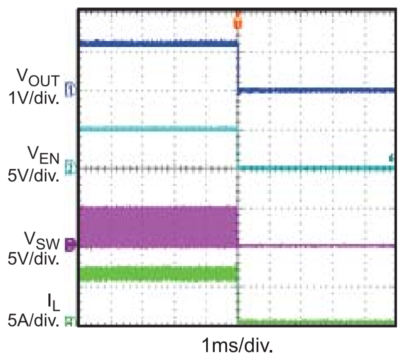
Enable Shutdown
I_{OUT}= 6A, PFM



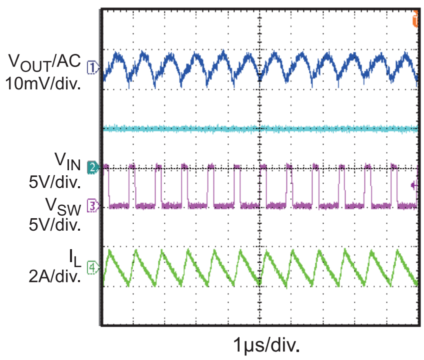
Enable Shutdown
I_{OUT}= 0A, PWM



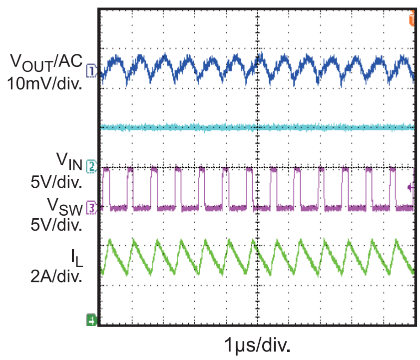
Enable Shutdown
I_{OUT}= 6A, PWM



Steady State
No Load, PWM



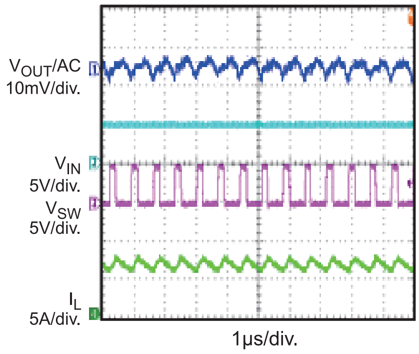
Steady State
Half Load 3A, PWM



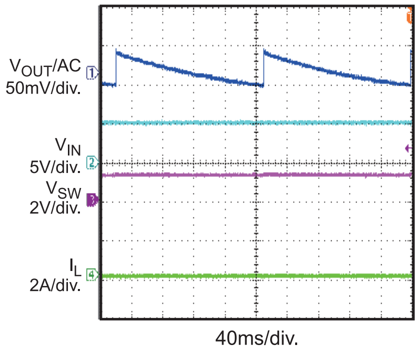
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT}=22µF×2, T_A = 25°C, unless otherwise noted.

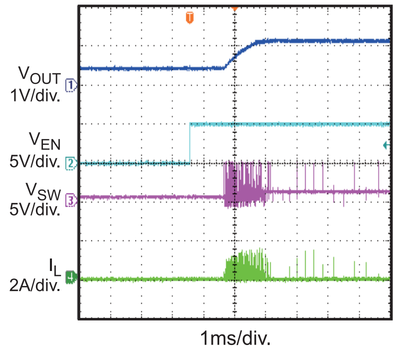
Steady State
Full Load 6A, PWM



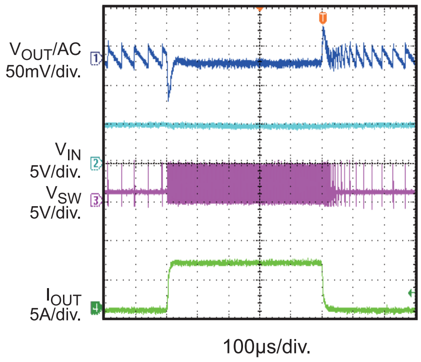
Steady State
No Load, PFM



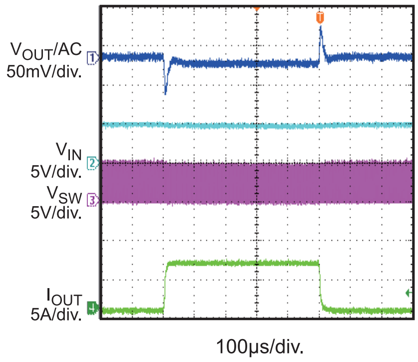
V_{OUT} Prebias Start Up
V_{PRE}=0.5V, I_{OUT}= 0A, PFM



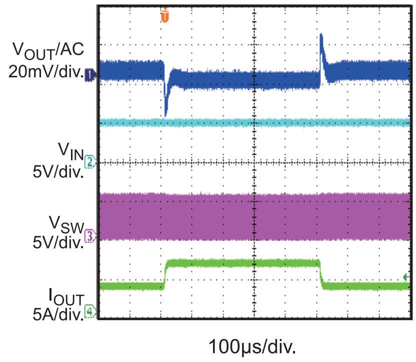
Load Transient Response
I_{OUT}=0A-6A, PFM



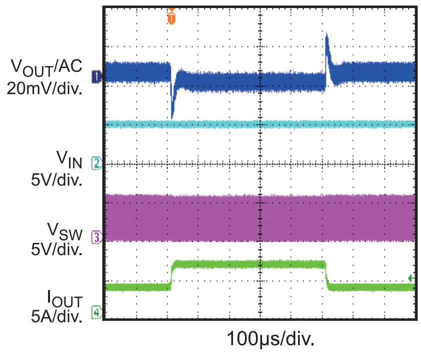
Load Transient Response
I_{OUT}=0A-6A, PWM



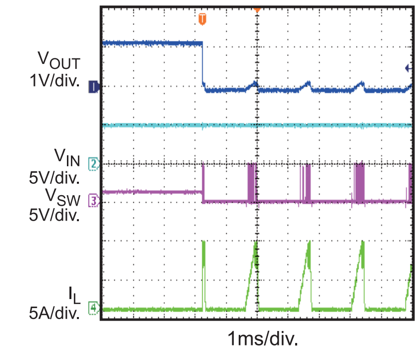
Load Transient Response
I_{OUT}=3A-6A, PFM



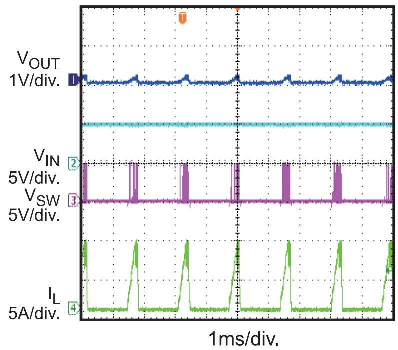
Load Transient Response
I_{OUT}=3A-6A, PWM



Hiccup With Output Short
No Load, PFM, Entry



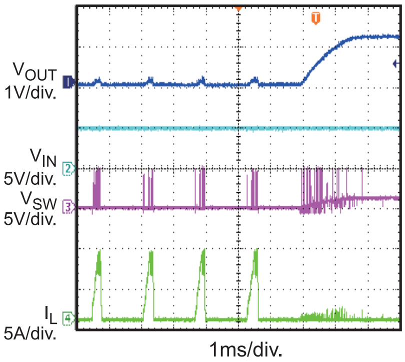
Hiccup With Output Short
No Load, PFM,Steady



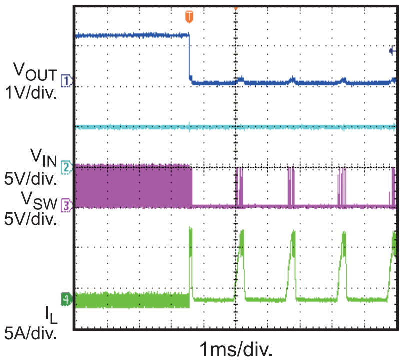
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 0.47µH, C_{OUT} = 22µF×2, T_A = 25°C, unless otherwise noted.

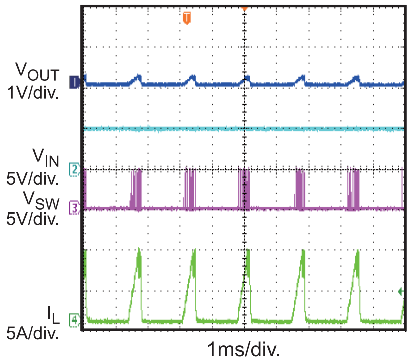
Hiccup With Output Short
No Load, PFM, Recovery



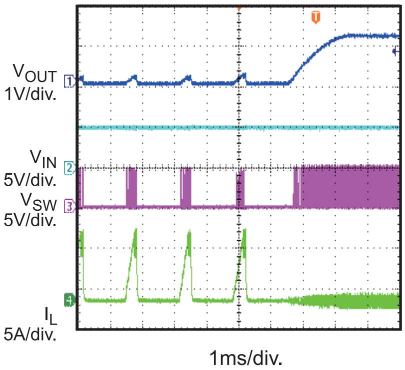
Hiccup With Output Short
No Load, PWM, Entry



Hiccup With Output Short
No Load, PWM,Steady



Hiccup With Output Short
No Load, PWM, Recovery



PIN FUNCTIONS

Package Pin #	Name	Description
1, 9	SW	**Switch Node.** Connect to the inductor. This pin connects to the internal high-side and low-side power MOSFET switches.
2	OUT	**Output Voltage Sensing pin.**
3	FB	**Feedback.** Input to the error amplifier. Connect to an external resistor divider between the output and GND. Comparing the FB voltage to the internal 0.6V reference sets the regulation voltage.
4	RAMP	**External Ramp.** Sets the ramp to optimize the transient performance.
5	EN	**Enable.** EN is high voltage level to enable. For automatic start-up, connect EN pin to VIN pin with a pull-up resistor.
6	MODE /VCON	**Multi-Use Pin.** 1. PWM and PFM Selection. When MODE is more than 1.2V, MP2145 enters PWM mode. When MODE is lower than 0.4V or floating, MP2145 enters PFM mode. 2. Analog Voltage Dynamic Regulation. Analog voltage input pin which control output voltage by PWM mode.
7	PG	**Power Good**. The output of this pin is an open drain with internal pull up resistor to VIN. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level, otherwise it is LOW. There is a 140µs delay between when V_{FB} reach PG threshold to when the PG pin goes HIGH.
8, exposed pad	VIN	**Input Supply.** Requires a decoupling capacitor to ground to reduce switching spikes.
10, 11,12	GND	**IC Ground.** Connect these pins to larger copper areas to the negative terminals of the input and output capacitors.

BLOCK DIAGRAM

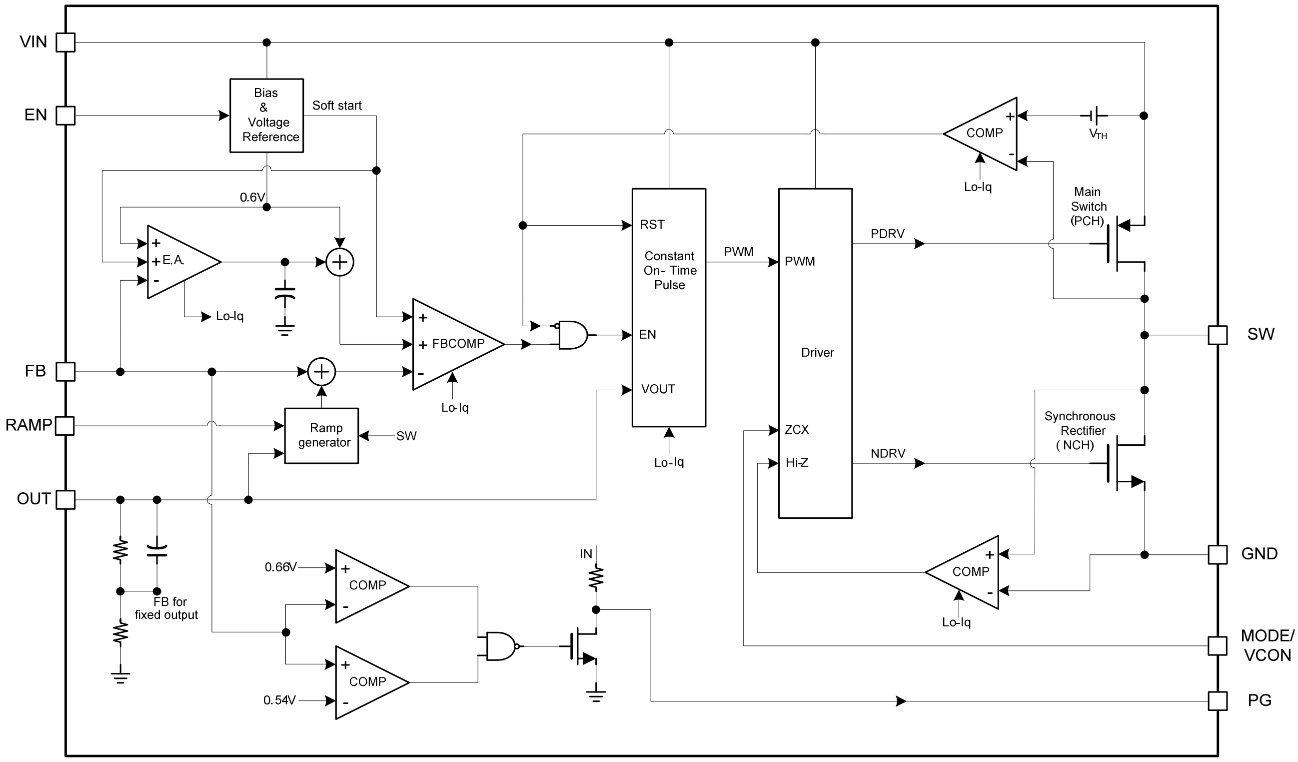


Figure 1: Functional Block Diagram

OPERATION

The MP2145 uses constant on-time control with input voltage feed-forward to stabilize the switching frequency over its full input Voltage range. During light loads, the MP2145 employs a proprietary control over the low-side MOSFET (LS-FET) and inductor current to improve efficiency.

Constant-On-Time Control

When compared to fixed-frequency PWM control, constant-on-time control offers a simpler control loop and faster transient response. The MP2145's input-voltage feed-forward maintains a nearly constant switching frequency across the entire input and output voltage range. The on-time of the switching pulse can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.83\mu s$$

To prevent inductor current runaway during the load transient, the MP2145 has a fixed minimum off time of 60ns. However, this minimum off time limit does not affect the operation of the MP2145 in steady state in any way.

Sleep Mode Operation

MP2145 features sleep mode to get high efficiency at extreme light load. In sleep-mode, most of the circuit blocks are turned off, except the error amplifier and PWM comparator, thus the operation current is reduced to a minimal value, as Figure 2.

When the loading gets lighter, the ripple of the output voltage is bigger and it drives the error amplifier output (EAO) lower. When EAO hits an internal low threshold, it will be clamped at that level, MP2145 enters sleep mode. During sleep mode, the valley of the FB pin voltage is regulated to the internal reference voltage, thus, the average output voltage is slightly higher than the output voltage at DCM or CCM mode. The on-time pulse at sleep mode is around 40% larger than that on DCM or CCM mode. Figure 3 shows the average FB pin voltage relationship with the internal reference at sleep mode.

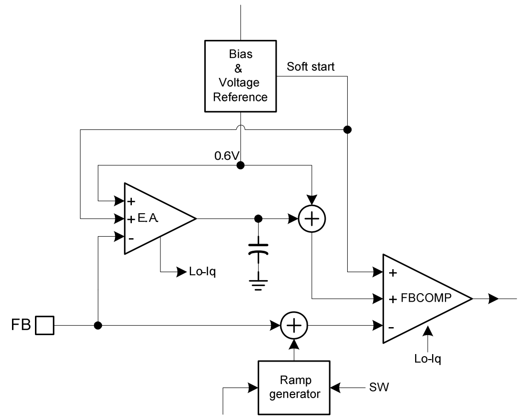


Figure 2: Operation Blocks at Sleep Mode

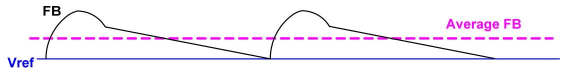


Figure 3: FB Average Voltage at Sleep Mode

When MP2145 is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the loading increases, the PWM switching period decreases in order to keep the output voltage regulated and the output voltage ripple is decrease relatively. Once EAO is more than internal low threshold, MP2145 will be out of sleep mode and enter DCM or CCM mode depending on the loading. In DCM or CCM mode, the EA regulates the average output voltage to the internal reference which is shown in Figure 4.

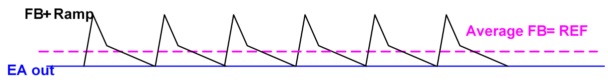


Figure 4: DCM Mode Control

There is always a loading hysteresis of entering sleep mode and leaving sleep mode due to the error amplifier clamping response time.

Light-Load Operation

During light loads, the MP2145 uses a proprietary control scheme to save power and improve efficiency: There is a zero current cross circuit to detect if the inductor current starts to reverse. LS-FET turns off immediately when the inductor current starts to reverse and trigger the ZCD in discontinuous conduction mode (DCM) operation.

Considering the internal circuit propagation time, the typical delay is 50ns. It means the inductor current still fall after the ZCD is trigger in this delay. If the inductor current falling slew rate is fast (V_{OUT} voltage is high or close to Vin), the low side MOSFET is turned off and inductor current may be negative. This phenomena will cause MP2145 can not enter DCM operation. If the DCM mode is required, the off time of low side MOSFET in CCM should be longer than 100ns. For example, Vin is 3.6V and Vo is 3.3V, the off time in CCM is 70ns. It is difficult to enter DCM at light load. And using smaller inductor can improve it and make it enter DCM easily.

Enable

When the input voltage exceeds the under-voltage lockout (UVLO) threshold—typically 2.55V—the MP2145 can be enabled by pulling the EN pin above 1.6V. Leaving EN pin floating or grounded will disable the MP2145. There is an internal 1MΩ resistor from the EN pin to ground.

Mode Selection and Analog Voltage Dynamic Regulation

MP2145 has programmable PWM and PFM work mode. When MODE/VCON is more than 1.2V, MP2145 enters PWM mode. When MODE/VCON is lower than 0.4V or floating, MP2145 enters PFM mode. PFM mode can achieve high efficiency by light-load operation. PWM mode can keep constant switch frequency and smaller Vo ripple, but it has low efficiency at light load.

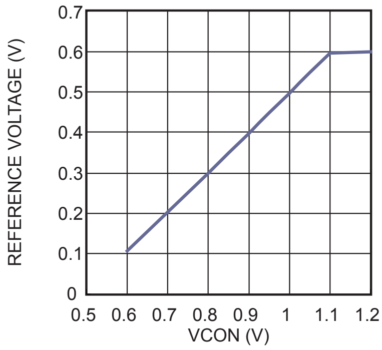


Figure 5: Reference Voltage change with VCON

MP2145 can dynamic regulate output voltage by MODE/VCON pin to meet some situation need change output voltage directly. When MOED/VCON pin get an appropriate voltage value (from 0.6V to 1.1V), MP2145 will work with PWM mode and internal reference voltage changes smoothly to achieve a new output voltage without changing external resistor divider, as Figure 5. When VCON function is enabled, set Ref voltage from 0.35V to 0.6V, the accuracy is 3% typically. When set Ref voltage from 0.1V to 0.35V, the accuracy is 10% typically. Detail Ref voltage calculation formula such as below:

$$Ref(V)=0.985 \times VCON(V)-0.486$$

Soft-Start

The MP2145 has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft-start time is typically about 1.5ms.

Pre-Bias Startup

The MP2145 can start up with a pre-bias output voltage. If the internal SS voltage is lower than the FB voltage, the HS-FET and LS-FET remain off until the SS voltage crosses the FB voltage.

Power-Good Indicator

The MP2145 has an open drain with a 500kΩ pull-up resistor as a power-good (PG) indication. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level. Otherwise the PG pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum R_{dson} of less than 100Ω.

Current Limit

The MP2145 has a 8.1A current limit for the HS-FET. When the HS-FET hits its current limit, the MP2145 enters hiccup mode until the current drops to prevent the inductor current from rising and possibly damaging the components.

Short Circuit and Recovery

The MP2145 enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short circuit by entering hiccup mode. In SCP, the MP2145 disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after soft-start ends, the MP2145 repeats this operation until the short circuit ceases and output rises back to regulation level.

100% Duty Cycle Mode

When the input voltage reduces and is lower than the regulation output voltage, the output voltage drops, and the on time increases. Further reducing the input voltage drives the MP2145 into 100% duty cycle mode. The high-side switch is always on, and the output voltage is determined by the loading current times the $R_{DS(ON)}$ composed by the high-side switch and inductor.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic). Select the feedback resistor R1 which considers reducing VOUT leakage current, typically between 40kΩ to 200kΩ. There is not strict requirement on feedback resistor. R1>10kΩ is reasoned for some application. R2 can be gotten below then:

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 6:

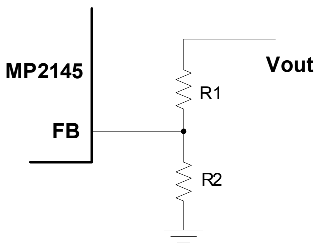


Figure 6: Feedback Network

Table 1 lists the recommended resistors values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

In order to achieve high efficiency at light load, a low value inductor such as 0.47 µH is recommended for most applications. For highest efficiency, chose an inductor with a DC resistance less than 30mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 22µF capacitor is sufficient. For higher output voltage, 47uF may be needed to improve system stability.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = $2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1µF), placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor stabilizes the DC output voltage. Ceramic capacitors are recommended. Low ESR capacitors are preferred to limit the output voltage ripple. Estimate the output voltage ripple as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. For MP2145, 2pcs 22uF Co can satisfy the most application. Add Co can reduce DCM and CCM output ripple effectively. However, a very large Co may cause light group pulse in sleep mode.

Load Transient Optimization

MP2145 can add a capacitor (Cc) between ramp pin and output sense pin to improve load transient. The larger Cc value is, the faster load transient respond speed is. A typical Cc 22pF trades off load transient and loop stability, maximum Cc is less than 200pF in case of SW instability issue. Further, MP2145 internally has optimized compensate block to cover most application. Ramp pin can be floated in normal application.

PCB Layout Recommendation

Proper layout of the switching power supplies is very important, and sometimes critical to make it work properly. Especially, for the high switching converter, if the layout is not carefully done, the regulator could show poor line or load regulation, stability issues.

For MP2145, the high speed step-down regulator, the input capacitor should be placed as close as possible to the IC pins. As shown in Figure 7, the 0805 size ceramic capacitor is used, please make sure the two ends of the ceramic capacitor be directly connected to PIN 8 (the Power Input Pin) and PIN 10/11/12 (the Power GND Pin).

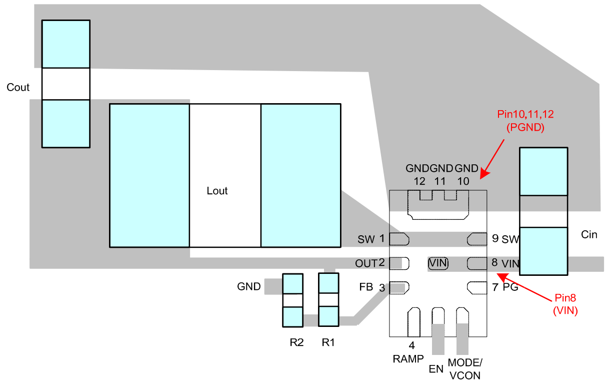


Figure 7: Two ends of Input decoupling Capacitor close to Pin 8 and Pin 10/11/12

TYPICAL APPLICATION CIRCUITS

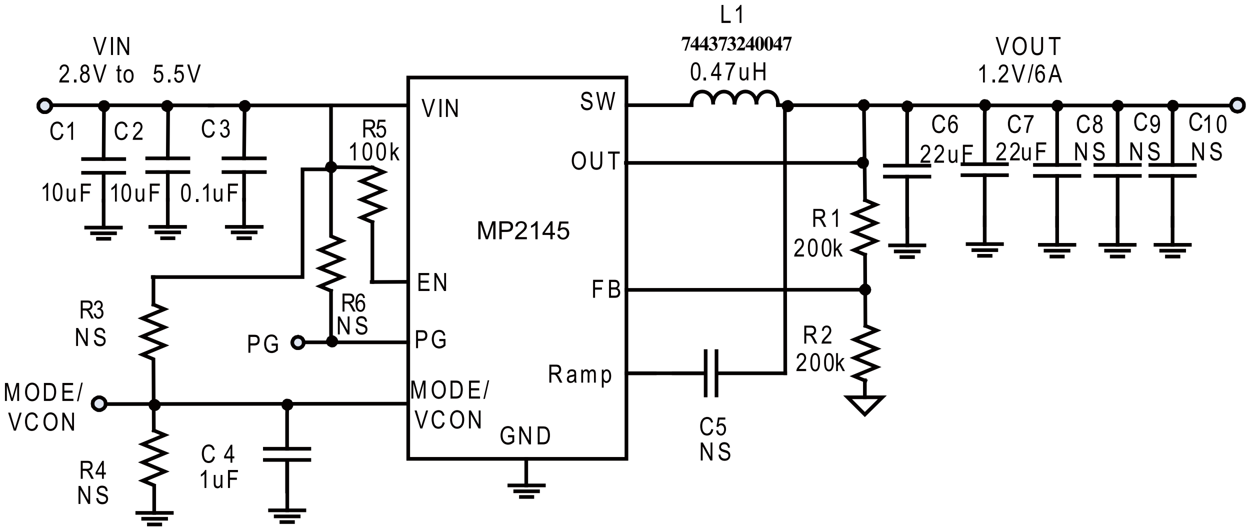
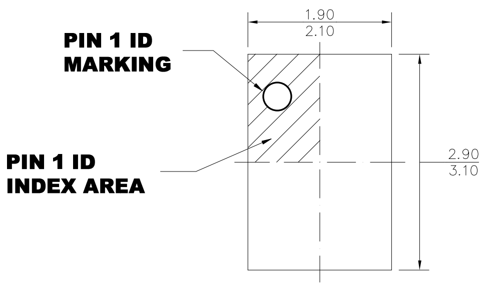


Figure 8: Typical Application Circuit for V_{IN}=5V, I_{OUT}=6A

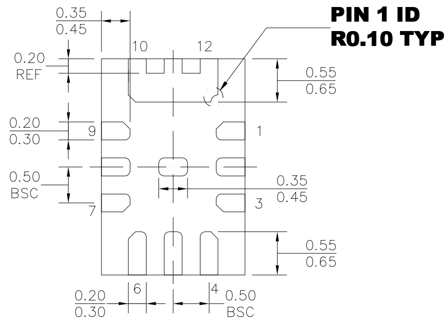
Note: V_{IN}<3.6V may need more input capacitor.

PACKAGE INFORMATION

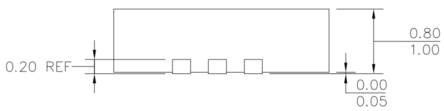
QFN-12 (2mmx3mm)



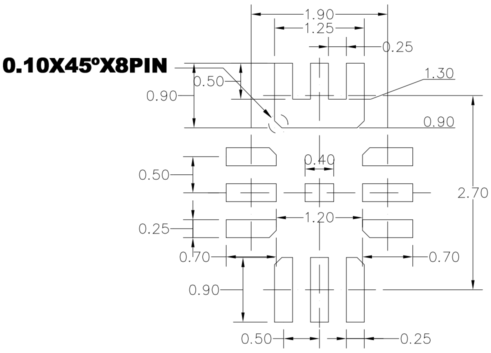
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL PINS' LAND PATTERN WIDTH IS 0.25MM.
2) PIN1,2,3,7,8,9 HAVE THE SAME LAND PATTERN LENGTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4 EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
5) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
6) JEDEC REFERENCE IS MO-220.
7) DRAWING IS NOT TO SCALE.