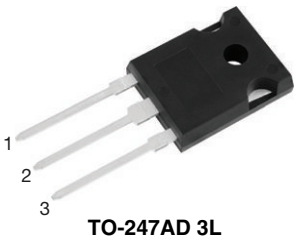
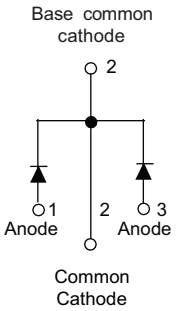
650 V Power SiC Gen 3 Merged PIN Schottky Diode, 2 x 8 A



TO-247AD 3L



FEATURES

- Majority carrier diode using Schottky technology on SiC wide band gap material
- Improved V_F and efficiency by thin wafer technology
- Positive V_F temperature coefficient, for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 1A whisker test
- Solder Bath temperature 275 °C maximum, 10 s per JESD 22-B106
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE

LINKS TO ADDITIONAL RESOURCES

3D Models

Application Notes

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	2 x 8 A
V_R	650 V
V_F at I_F at 25 °C, typ.	1.3 V
T_J max.	175 °C
I_R at V_R at 175 °C	1.9 µA
Q_C (V_R = 400 V)	22 nC
Package	TO-247AD 3L
Circuit configuration	Common cathode

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimum choice for high speed hard switching and efficient operation over a wide temperature range, it is also recommended for all applications suffering from Silicon ultrafast recovery behavior.

Typical applications include AC/DC PFC and DC/DC ultra high frequency output rectification in FBPS and LLC converters.

MECHANICAL DATA

Case: TO-247AD 3L

Molding compound meets UL 94 V-0 flammability rating Base P/N-M3 - halogen-free, RoHS-compliant

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

Mounting torque: 10 in-lbs maximum

MAXIMUM RATINGS (T_A = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Continuous forward current, per leg	I_F (1)	T_C = 136 °C (DC)	8	A
	I_F (2)	T_C = 145 °C (DC)		
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	T_C = 25 °C, f = 50 Hz, square wave, DC = 25 %	35	A
Non-repetitive peak forward surge current, per leg	I_{FSM}	T_C = 25 °C, t_p = 10 ms, half sine wave	54	
		T_C = 110 °C, t_p = 10 ms, half sine wave	52	
Power dissipation, per leg	P_{tot} (1)	T_C = 25 °C	125	W
		T_C = 110 °C	54	
	P_{tot} (2)	T_C = 25 °C	166	W
		T_C = 110 °C	72	
I^2t value, per leg	$\int i^2 dt$	T_C = 25 °C	13.5	A^2s
		T_C = 110 °C	12.5	
Operating junction and storage temperatures	T_J (2), T_{Stg}		-55 to +175	°C

Notes

(1) Based on maximum R_{th}

(2) Based on typical R_{th}

(3) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$

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ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage, per leg	V_F	I_F = 8 A	-	1.3	1.5	V
		I_F = 8 A, T_J = 150 °C	-	1.5	1.8	
		I_F = 8 A, T_J = 175 °C	-	1.58	-	
Reverse leakage current, per leg	I_R	V_R = V_R rated	-	0.25	45	µA
		V_R = V_R rated, T_J = 150 °C	-	1.1	100	
		V_R = V_R rated, T_J = 175 °C	-	1.9	-	
Total capacitance, per leg	C	V_R = 1 V, f = 1 MHz	-	340	-	pF
		V_R = 400 V, f = 1 MHz	-	34	-	
Total capacitive charge, per leg	Q_C	V_R = 400 V, f = 1 MHz	-	22	-	nC

THERMAL - MECHANICAL SPECIFICATIONS (T_A = 25 °C unless otherwise specified)							
PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction-to-case	per leg	R_{thJC}		-	2.0	2.6	°C/W
	per device			-	1.0	1.3	°C/W
Marking device				3C16CP07L			

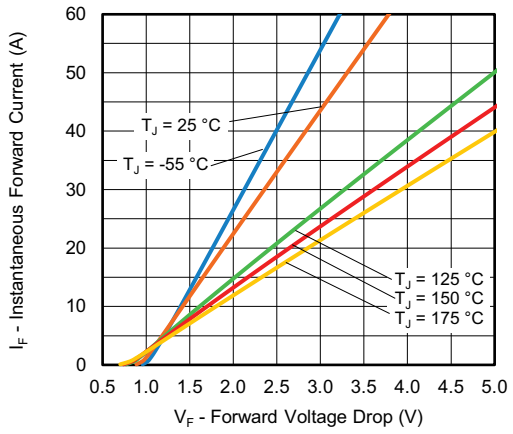


Fig. 1 - Typical Forward Voltage Drop Characteristics, Per Leg

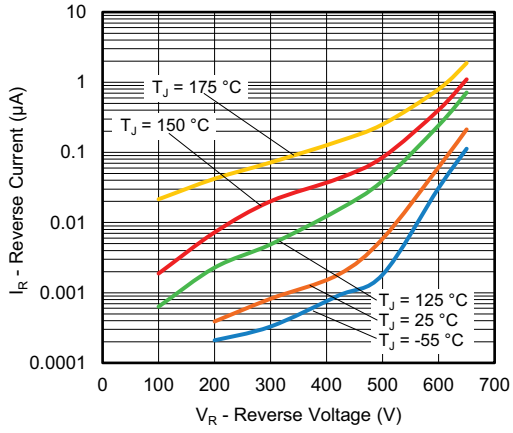


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage, Per Leg

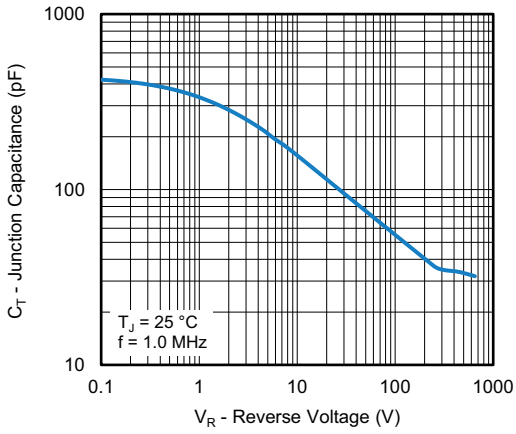


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage, Per Leg

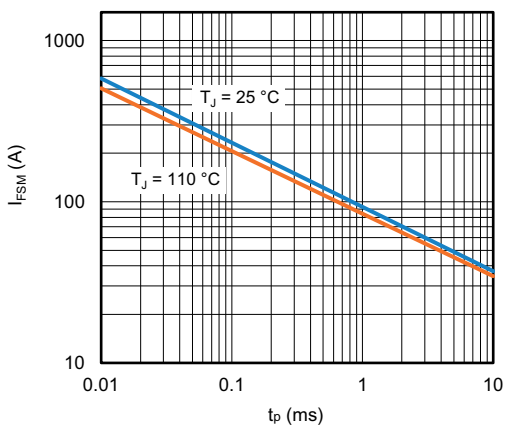


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration, Per Leg (Square Wave)

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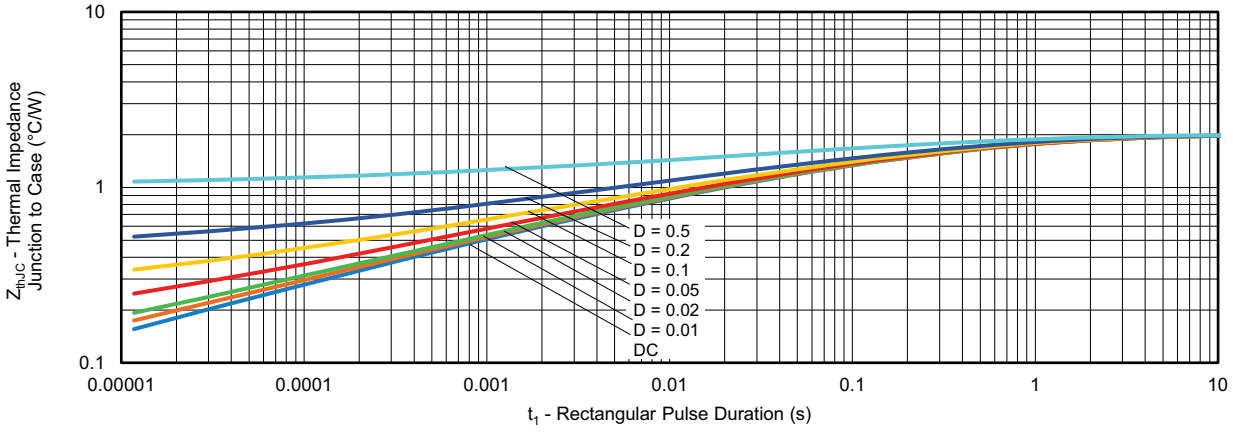


Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics, Per Leg

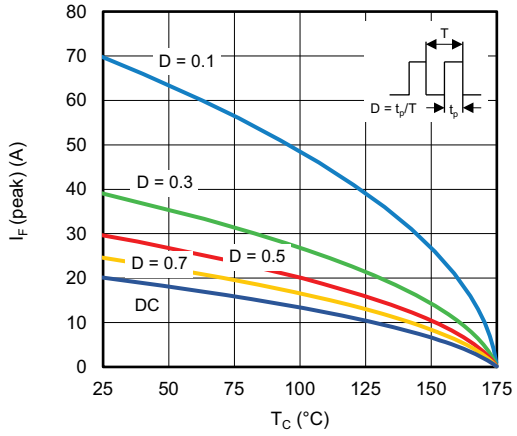


Fig. 6 - Peak Forward Current vs.Maximum Allowable Case Temperature, Per Leg

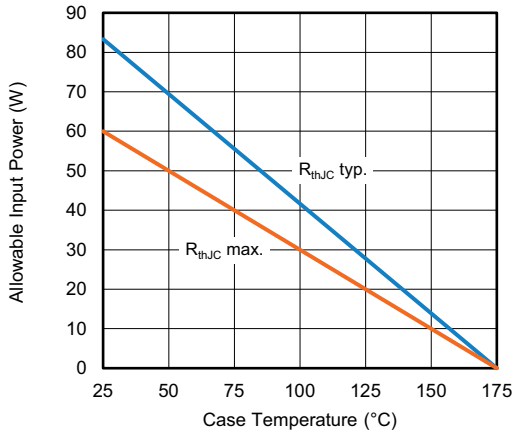


Fig. 7 - Forward Power Loss Characteristics, Per Leg

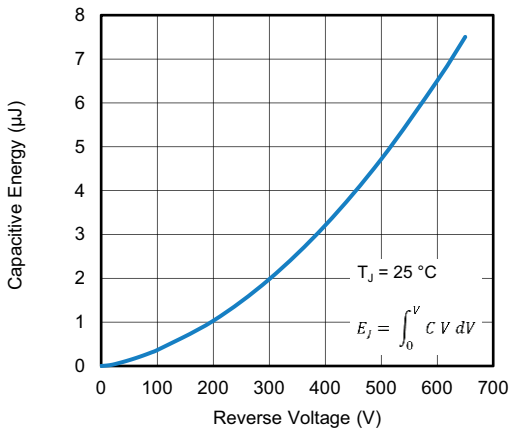


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage, Per Leg

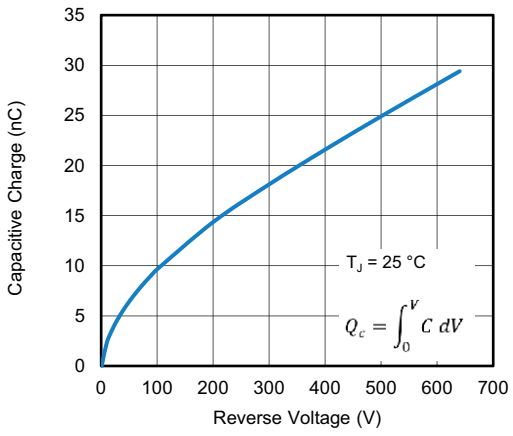
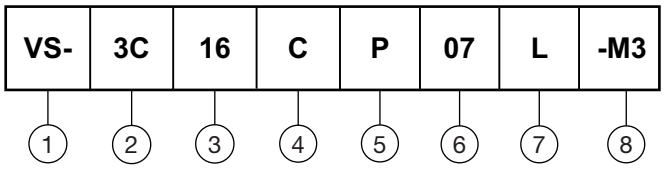


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage, Per Leg

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ORDERING INFORMATION TABLE

Device code



1 - Vishay Semiconductors product
2 - 3C = SiC diode, Generation 3
3 - Current rating (16 = 16 A)
4 - C = common cathode
5 - P = package TO-247
6 - Voltage rating: (07 = 650 V)
7 - L = long lead
8 - Environmental digit:
-M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free

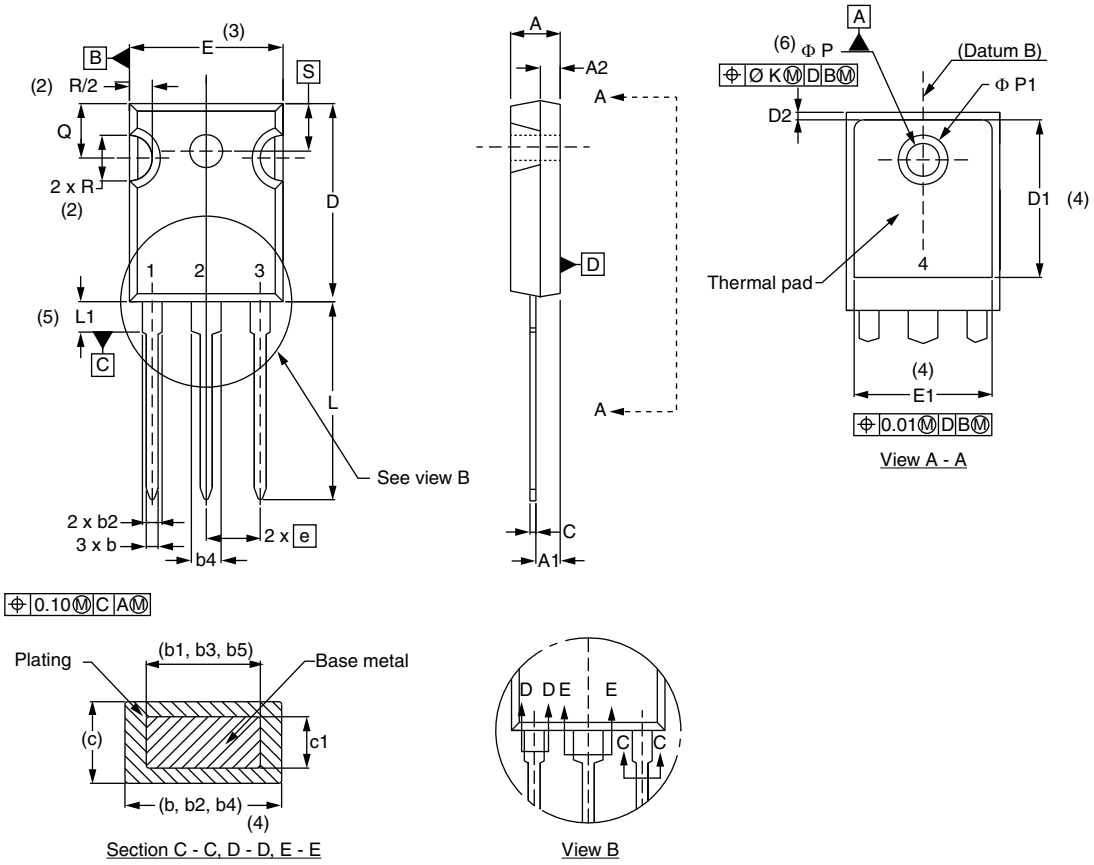
ORDERING INFORMATION		
PREFERRED P/N	**BASE QUANTITY**	**PACKAGING DESCRIPTION**
VS-3C16CP07L-M3	25/tube	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95626
Part marking information	www.vishay.com/doc?95007

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TO-247AD 3L

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.65	5.31	0.183	0.209	
A1	2.21	2.59	0.087	0.102	
A2	1.50	2.49	0.059	0.098	
b	0.99	1.40	0.039	0.055	
b1	0.99	1.35	0.039	0.053	
b2	1.65	2.39	0.065	0.094	
b3	1.65	2.34	0.065	0.092	
b4	2.59	3.43	0.102	0.135	
b5	2.59	3.38	0.102	0.133	
c	0.38	0.89	0.015	0.035	
c1	0.38	0.84	0.015	0.033	
D	19.71	20.70	0.776	0.815	3
D1	13.08	-	0.515	-	4

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D2	0.51	1.30	0.020	0.051	
E	15.29	15.87	0.602	0.625	3
E1	13.46	-	0.53	-	
e	5.46 BSC		0.215 BSC		
Ø K	0.254		0.010		
L	19.81	20.32	0.780	0.800	
L1	3.71	4.29	0.146	0.169	
Ø P	3.56	3.66	0.14	0.144	
Ø P1	-	6.98	-	0.275	
Q	5.31	5.69	0.209	0.224	
R	4.52	5.49	0.178	0.216	
S	5.51 BSC		0.217 BSC		

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
(7) Outline conforms to JEDEC® outline TO-247 with exception of dimension A min., D, E min., Q min., S, and note 4

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