MP4245

36V, 6A Peak, Buck-Boost Converter with I²C Interface for Power Delivery

DESCRIPTION

The MP4245 is a buck-boost converter with four integrated power switches. The device can deliver up to 6A of output current at certain input-voltage supply ranges, with excellent load and line regulation.

The MP4245 is suitable for USB power delivery (USB PD) applications. It can work with an external USB PD controller through the I²C interface. The I²C interface and two-time programmable multiple-time programmable (MTP) memory provide flexible features.

Fault condition protections includes constant current (CC) limiting, output over-voltage protection (OVP), and thermal shutdown (TSD).

The MP4245 requires a minimal number of readily available, standard external components, and is available in a QFN-21 (4mmx5mm) package.

FEATURES

- Supports 60W Buck-Boost or 6A Peak I_{OUT}
- Wide 4V to 36V Operating Input Voltage Range
- 1V to 23V Output Voltage Range
- 250kHz, 350kHz, or 420kHz Selectable Frequency or SYNC Input
- 12mΩ/24mΩ/14mΩ/14mΩ Low $R_{DS(ON)}$ for Switches A, B, C, and D
- Selectable Frequency Spread Spectrum
- Line Drop Compensation
- Accurate Constant Current (CC) Output Current Limit
- **I²C Interface and MTP (PMBus Compatible):**
  - PFM/PWM Mode, Current Limit, Output Voltage, Frequency Spread Spectrum, and Line Drop Compnsation
  - CRC Calculation for MTP Integrity
- Load-Shedding Alert
- EN Shutdown Active Discharge
- Available in a QFN-21 (4mmx5mm) Package with Wettable Flanks

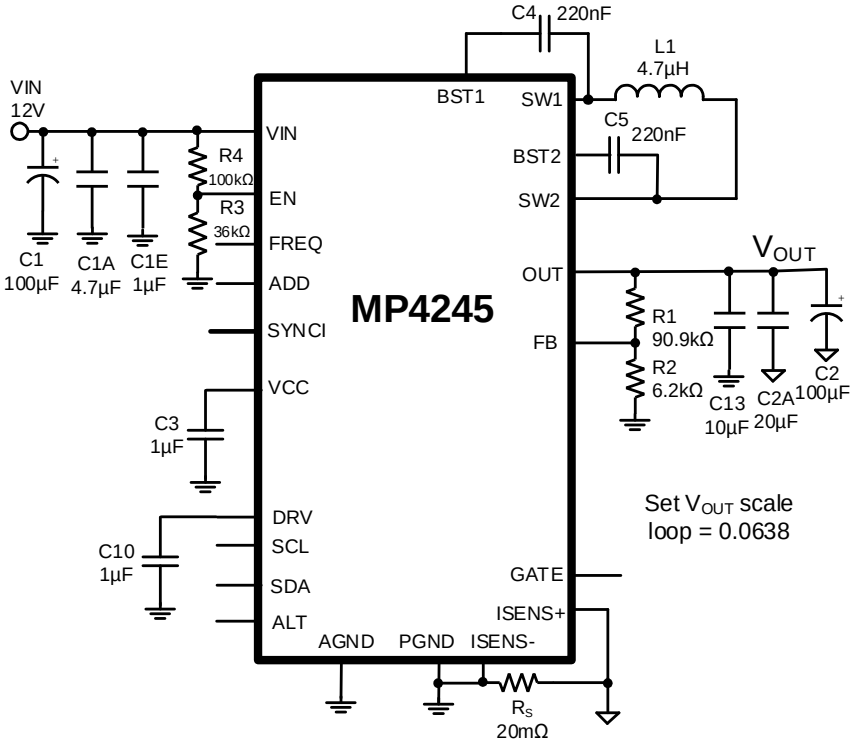
APPLICATIONS

- USB Type-C with PD Charging Only Ports
- 12V Bus Voltage Supplies
- Wireless Charging

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4245GVE-xxxx *	QFN-21 (4mmx5mm)	*See Below*	1
MP4245GVE-0000 **	QFN-21 (4mmx5mm)	*See Below*	
MP4245GVE-0001 **	QFN-21 (4mmx5mm)	*See Below*	
EVKT-MP4245	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP4245GVE-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the MTP. Each "x" can be a hexadecimal value between 0 and F. The MP4245GVE-0000 is the default version.

TOP MARKING

MPSYWW
MP4245
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4245: part number
LLLLLL: Lot number
E: Wettable lead flank

EVALUATION KIT EVKT-MP4245

EVKT-MP4245 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV4245-VE-00A	MP4245 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	MP4245GVE-0001-Z	IC with default configuration	2

Order directly from MonolithicPower.com or our distributors.

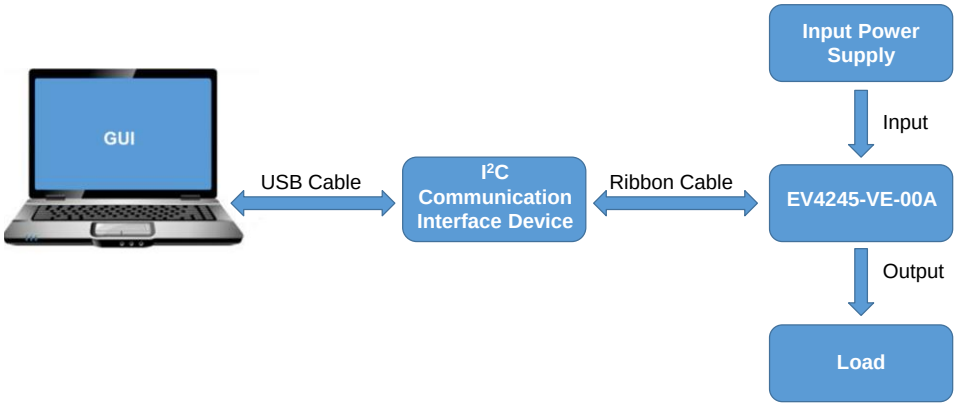
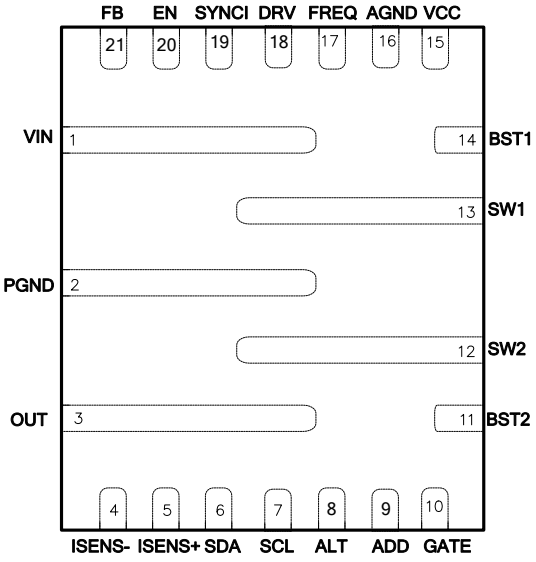


Figure 1: EVKT-MP4245 Evaluation Kit Set-Up

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PACKAGE REFERENCE



QFN-21 (4mmx5mm) with Wettable Flank

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** The MP4245 operates from a 4V to 36V input voltage. An input capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible. VIN is the drain of the first half-bridge's internal power device. VIN supplies power to the entire chip.
2	PGND	**Power ground.** PGND requires extra consideration during PCB layout. Connect PGND to GND with copper traces and vias.
3	OUT	**Buck-boost mode output pin.**
4	ISENS-	**Negative node of the current-sense signal input.** Place a current-sense resistor between the PGND pin and the USB port's GND pin. Connect the ISENS- pin to the PGND side. The sensed signal is used for buck-boost constant current (CC) limiting.
5	ISENS+	**Positive node of current-sense signal input.** Place a current-sense resistor between the PGND pin and the USB port's GND pin. Connect the ISENS+ pin to the USB port's GND. The sensed signal is used for buck-boost constant current (CC) limiting.
6	SDA	**I²C data line.**
7	SCL	**I²C clock signal input.**
8	ALT	**PMBus alert pin.** Open drain output, active low. Pull ALT up to an external supply with a 10kΩ resistor.
9	ADD	**I²C slave address set pin.** Connect a different resistor from the ADD pin to ground to set eight different I²C addresses. The internal ADC reads this pin's voltage to lock the I²C address during start-up. ADD has an internal 20μA current source.
10	GATE	**Gate drive pin to drive external MOSFET.**
11	BST2	**Bootstrap.** A 220nF capacitor is connected between SW2 and BST2 to form a floating supply across the high-side switch driver.
12	SW2	**Switch 2 output.** Use a wide PCB trace to make the SW2 connection.
13	SW1	**Switch 1 output.** Use a wide PCB trace to make the SW1 connection.
14	BST1	**Bootstrap.** A 220nF capacitor is connected between SW1 and BST1 to form a floating supply across the high-side switch driver.
15	VCC	**Internal 5V LDO regulator output.** Decouple VCC with a 1μF capacitor.
16	AGND	**Analog ground.** Connect AGND to PGND, then connect AGND to the VCC capacitor's ground node.
17	FREQ	**Frequency selection pin.** Float the FREQ pin to set the frequency to 350kHz. Pull FREQ to ground set the frequency to 250kHz. Pull FREQ to 5V to set the frequency to 420kHz.
18	DRV	**5.5V to 6.5V adjustable LDO output.** 1mA load capability. DRV starts up at the same time as VCC. Add a 1μF decoupling capacitor to DRV.
19	SYNCI	**SYNC clock input.** Apply a clock on this pin to sync the switching frequency to the external clock. The allowable frequency for the external clock is 250kHz, 350kHz, or 420kHz. If SYNC is not used, it is recommended to connect SYNCI to GND.
20	EN	**Enable control pin.** Apply a logic high voltage on this pin to enable the IC, pull EN to logic low to disable the IC. EN has an internal 2MΩ pull-down resistor.
21	FB	**Feedback pin.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.4V to +40V
$V_{SW1/2}$.....-0.3V (-5V for <10ns)
..... to V_{IN} + 0.3V (+43V for <10ns)
$V_{BST1/2}$.....$V_{SW1/2}$ + 5.5V
V_{OUT}.....-0.3V to +24V
V_{DRV}.....-0.3V to +6.75V
V_{EN}.....-0.3V to +10V (2)
All other pins.....-0.3V to +5.5V
Continuous power dissapation (T_A = 25°C) (3) (6)
QFN-21 (4mmx5mm)..... 5.08W
Junction temperature.....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM) ..... ±2000V
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (5)

Operating input voltage range .....4V to 36V
Operation output voltage range .....1V to 23V
Output power and current……60W or 6A peak
Operating junction temp (T_J)…. -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EV4245-VE-00A (6)	24.6	6.3	°C/W
QFN-21 (4mmx5mm) (7)	44	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) About the details on the EN pin's absolute maximum rating, see the Enable Control (EN) section on page 18.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows for safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on EV4245-VE-00A, 4-layer PCB, 55mmx55mm.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{Q_STD}	V_{EN} = 0V		1	30	μA
Supply current (quiescent)	I_Q	Not switching, PFM mode		300		μA
EN rising threshold	V_{EN_RISING}	V_{OUT} enabled	-5%	1.6	+5%	V
EN hysteresis	V_{EN_HYS}			200		mV
EN pull-down resistor	R_{EN}	V_{EN} = 2V		2		MΩ
Thermal shutdown (8)	T_{STD}			160		°C
Thermal hysteresis(8)	T_{STD_HYS}			20		°C
VCC regulator	V_{CC}		5	5.25	5.5	V
VCC load regulation	V_{CC_LOG}	I_{CC} = 50mA		2	10	%
DRV regulator output	V_{DRV}	I²C-adjustable	5.75	6.0	6.25	V
DRV load regulation	V_{CC_LOG}	I_{CC} = 1mA		2.5	8	%
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}		3.1	3.3	3.5	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			300		mV
FB reference voltage	V_{FB0}	Scale loop = 0.08, set V_{OUT} = 1.25V	0.092	0.100	0.108	V
	V_{FB1}	Scale loop = 0.08, set V_{OUT} = 5V	-2%	0.400	+2%	V
	V_{FB2}	Scale loop = 0.08, set V_{OUT} = 9V	-1.5%	0.720	+1.5%	V
	V_{FB3}	Scale loop = 0.08, set V_{OUT} = 20V	-1.5%	1.600	+1.5%	V
Switch A on resistance	$R_{DS(ON)}$			12	25	mΩ
Switch B on resistance				24	50	
Switch C on resistance				14	30	
Switch D on resistance				14	30	
Output over-voltage protection	V_{OVP_R}		116	121	126	%
Output OVP recovery	V_{OVP_F}			110		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 22V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW1} = 36V, V_{SW2} = 22V, T_J = -40°C to+125°C			30	
Oscillator frequency	f_{SW1}	FREQ = GND	180	250	320	kHz
	f_{SW2}	FREQ pin floating	260	350	440	
	f_{SW3}	FREQ = VCC	330	420	510	
Frequency sync in	f_{SYNC1}	FREQ = GND	220	250	280	kHz
	f_{SYNC2}	FREQ pin floating	310	350	390	kHz
	f_{SYNC3}	FREQ = VCC	370	420	470	
Frequency dithering span (8)	$f_{DITHERING}$			±12		%

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft-start time	t_{SS}	Output from 10% to 90%, V_{REF} = 0.4V, constant slew rate for other V_{REF}		1.4		ms
Minimum on time (8)	$t_{ON_MIN_BT}$			80		ns
ISENS OC threshold	I_{OC1}	OC threshold = 1A, R_{SENS} = 20mΩ	17	20	23	mV
	I_{OC2}	OC threshold = 3.6A, R_{SENS} = 20mΩ	-5%	72	+5%	mV
GND short to battery ISENS threshold	Isc	OC threshold = 20A, R_{SENS} = 20mΩ		420		mV
Short to battery retry delay	t_{SBP}			1		s
Gate pull-down resistance	R_{GATE}			7	20	Ω
High-side A current limit (8)	I_{LIMIT1}	CC limit set-up value = 3.6A		23		A
		1.6A < CC limit set-up value < 3.6A		19		
		CC limit set-up value < 1.6A		15		
Low-side B valley limit	I_{LIMIT2}	Switch B		11.5		A
ADD pin source current	I_{ADD}	Only works during start-up.	-1.5%	20	+1.5%	µA
ADD address 1	ADD1	R_{ADD} = GND, 61h			0.18	V
ADD address 2	ADD2	R_{ADD} = 15kΩ, 62h	0.25		0.38	
ADD address 3	ADD3	R_{ADD} = 25.5kΩ, 63h	0.45		0.59	
ADD address 4	ADD4	R_{ADD} = 35.7kΩ, 64h	0.66		0.79	
ADD address 5	ADD5	R_{ADD} = 45.3kΩ, 65h	0.87		0.99	
ADD address 6	ADD6	R_{ADD} = 56kΩ, 66h	1.07		1.20	
ADD address 7	ADD7	R_{ADD} = V_{CC}, 67h	1.28			
Alert pull-low resistance	R_{ALERT}			8	20	Ω
Alert leakage	LKG_{ALERT}	Pull up with 5V		100		nA
I²C Interface Specifications (HS Mode)						
Input logic high	V_{IH}	I²C pulled up to VDD (can be between 1.8V and 5V)	1.4			V
Input logic low	V_{IL}				0.4	V
SDA output voltage logic low	V_{OUT_L}				0.4	V
SCL clock frequency	f_{SCL}			400	1000	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}		0	60		ns
Set-up time for (repeated) start condition	t_{SU_STA}		160			ns

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ELECTRICAL CHARACTERISTICS *(continued)*

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Parameter	Symbol	Condition	Min	Typ	Max	Units
Hold time for (repeated) start condition	t_{HD_STA}		160			ns
Bus Free Time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	t_{SU_STO}		160			ns
Rise Time of SCL and SDA	t_R		10		300	ns
Fall Time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance for each bus line	C_B				400	pF
PMBus Status Threshold						
VOUT_OV_FAULT_RISING	$VOUT_{OV_F_R}$		116%	121%	126%	V_{OUT}
VOUT_OV_FAULT_FALLING	$VOUT_{OV_F_F}$		105%	110%	115%	V_{OUT}
VOUT_OV_WARNING_RING	$VOUT_{OV_W_R}$		103.5%	108.5%	113.5%	V_{OUT}
VOUT_OV_WARNING_FALLING	$VOUT_{OV_W_F}$		99.5%	104.5%	109.5%	V_{OUT}
VOUT_UV_WARNING_RISING	$VOUT_{UV_W_R}$		81%	86%	91%	V_{OUT}
VOUT_UV_WARNING_FALLING	$VOUT_{UV_W_F}$		69.5%	74.5%	79.5%	V_{OUT}
VOUT_UV_FAULT_RISING	$VOUT_{UV_F_R}$		56%	61%	66%	V_{OUT}
VOUT_UV_FAULT_FALLING	$VOUT_{UV_F_F}$		44.5%	49.5%	54.5%	V_{OUT}
VIN_OV_FAULT_RISING	$VIN_{OV_F_R}$			40		V
VIN_OV_FAULT_FALLING	$VIN_{OV_F_F}$			38		V
VIN_OV_WARNING_RISING	$VIN_{OV_W_R}$			38		V
VIN_OV_WARNING_FALLING	$VIN_{OV_W_F}$			36		V
VIN_UV_WARNING_RISING	$VIN_{UV_W_R}$			3.7		V
VIN_UV_WARNING_FALLING	$VIN_{UV_W_F}$			3.4		V
VIN_UV_FAULT_RSING	$VIN_{UV_F_R}$			3.4		V
VIN_UV_FAULT_FALLING	$VIN_{UV_F_F}$			3.1		V

Notes:

8) Guaranteed by characterization testing.

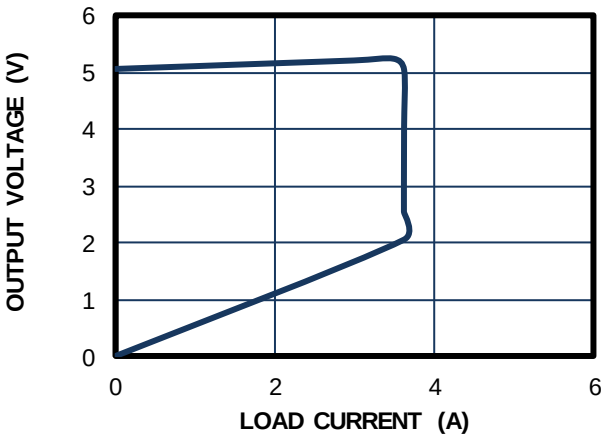
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

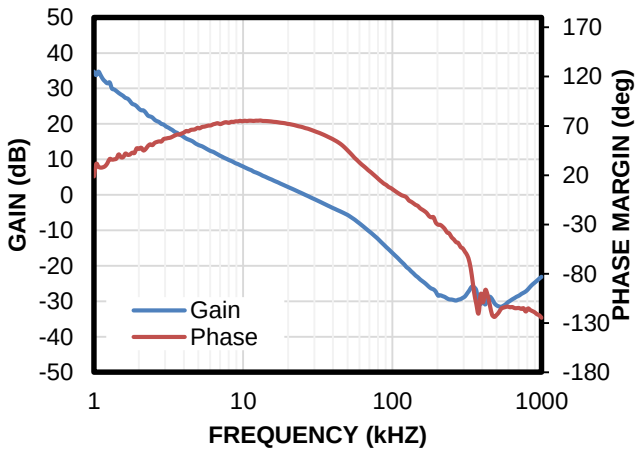
CC/CV Curve

CC limit = 3.6A



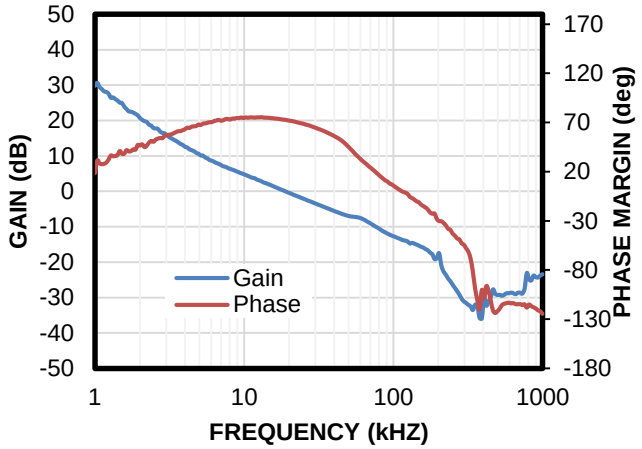
Bode Plot

V_{OUT} = 5V, I_{OUT} = 3A, BW = 26kHz, PM = 68deg



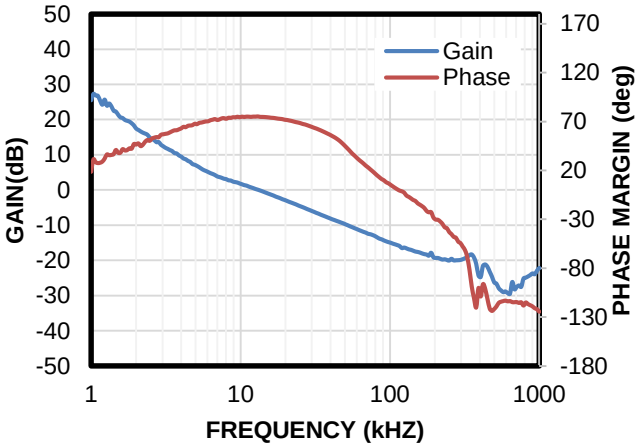
Bode Plot

V_{OUT} = 12V, I_{OUT} = 3A, BW = 19kHz, PM = 71deg



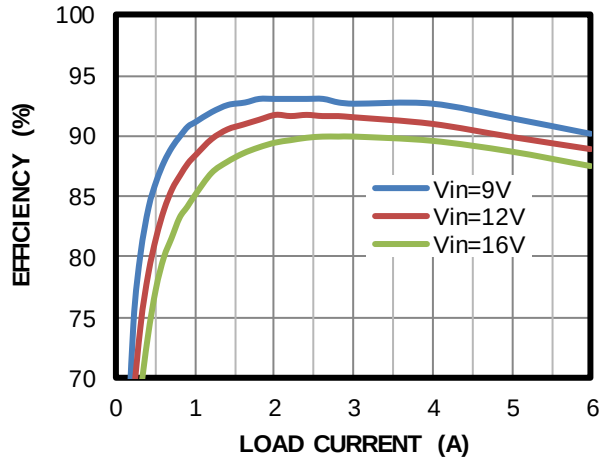
Bode Plot

V_{OUT} = 20V, I_{OUT} = 3A, BW = 13kHz, PM = 76deg



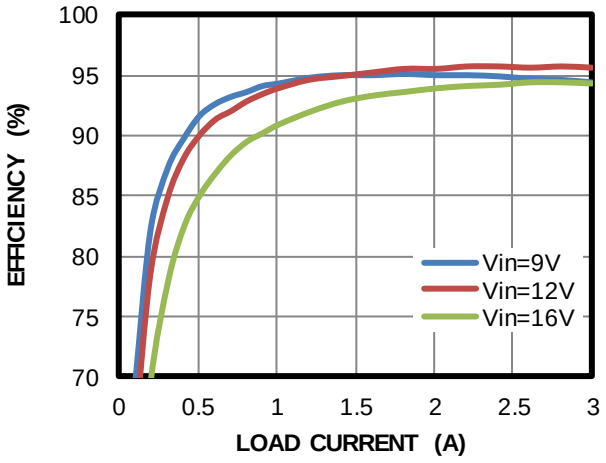
Efficiency vs. Load Current

V_{OUT} = 5V, L = 4.7µH, DCR = 8mΩ, f_{SW} = 420kHz



Efficiency vs. Load current

V_{OUT} = 9V, L = 4.7µH, DCR = 8mΩ, f_{SW} = 420kHz



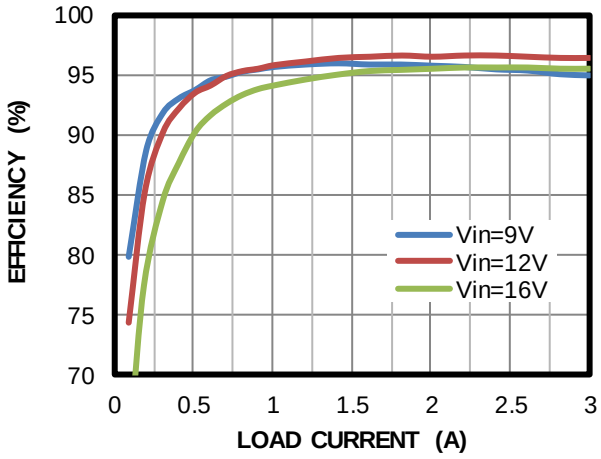
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

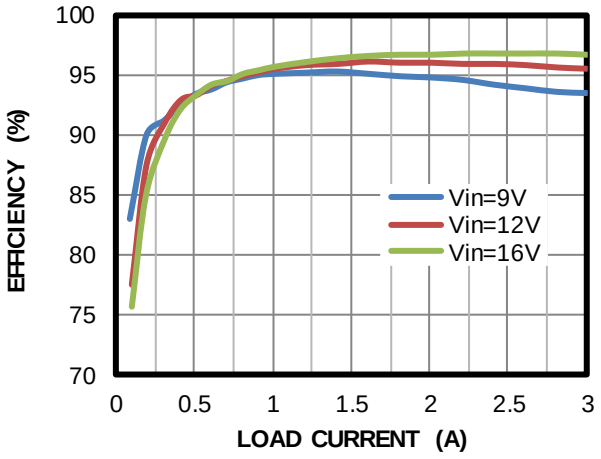
Efficiency vs. Load Current

V_{OUT} = 15V, L = 4.7µH, DCR = 8mΩ, f_{SW} = 420kHz



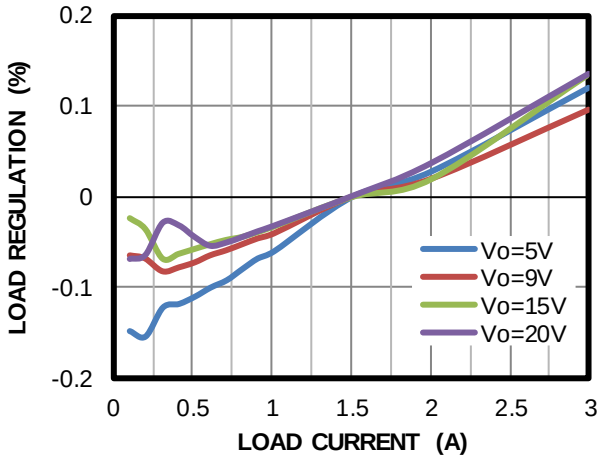
Efficiency vs. Load Current

V_{OUT} = 20V, L = 4.7µH, DCR = 8mΩ, f_{SW} = 420kHz



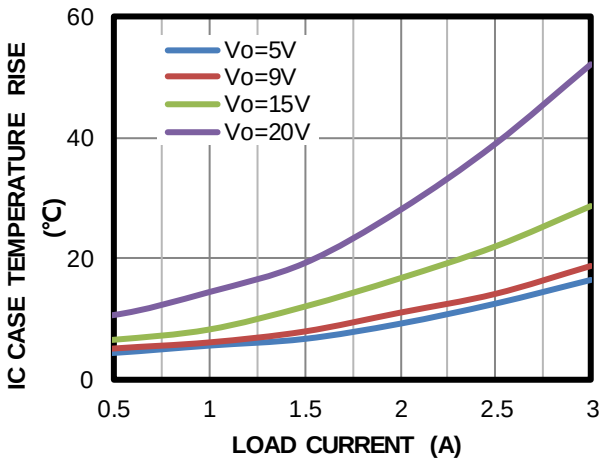
Load Regulation vs. Load Current

V_{IN} = 12V, no line drop compensation



Thermal Rise

V_{IN} = 12V, f_{SW} = 420kHz, based on the EV4245-VE-00A



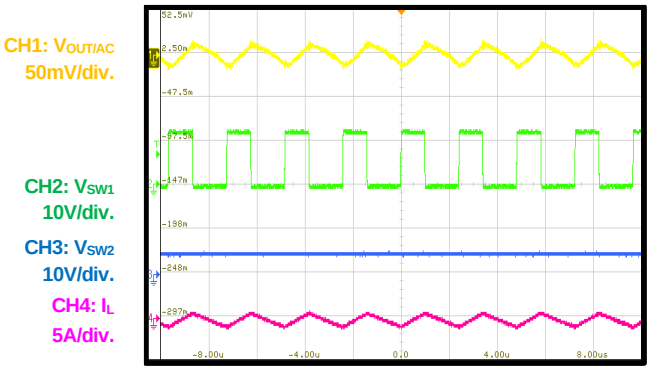
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

Output Ripple

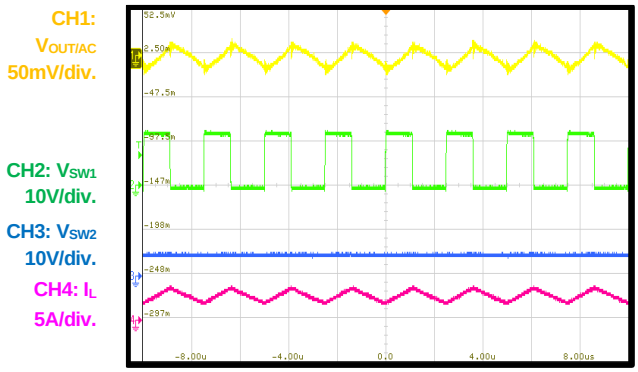
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, PWM mode



2µs/div.

Output Ripple

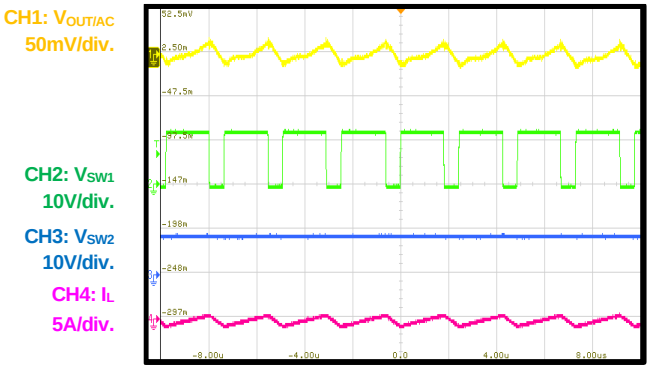
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, PWM mode



2µs/div.

Output Ripple

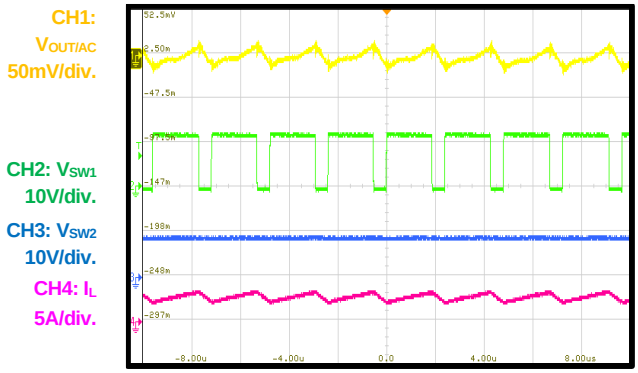
V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 0A, PWM mode



2µs/div.

Output Ripple

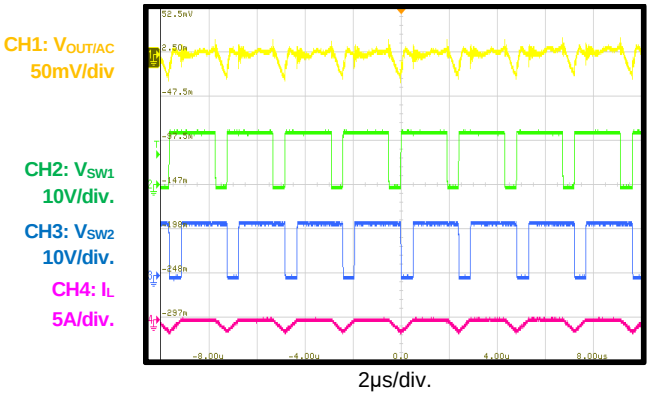
V_{IN} = 12V, V_{OUT} = 9V, I_{OUT} = 3A, PWM mode



2µs/div.

Output Ripple

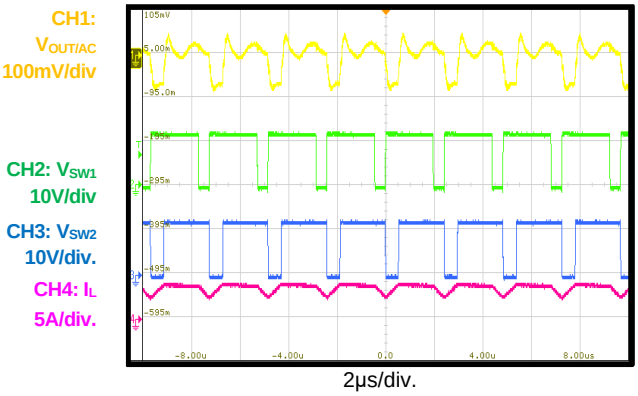
V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 0A, PWM mode



2µs/div.

Output Ripple

V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 3A, PWM mode



2µs/div.

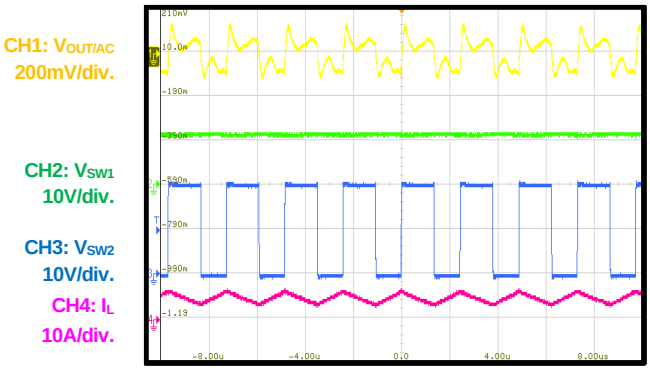
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

Output Ripple

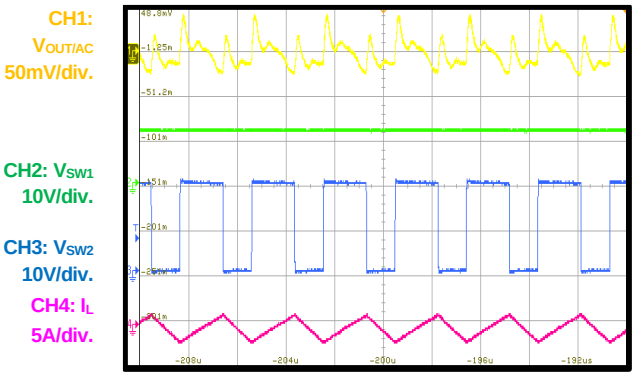
V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 3A, PWM mode



2µs/div.

Output Ripple

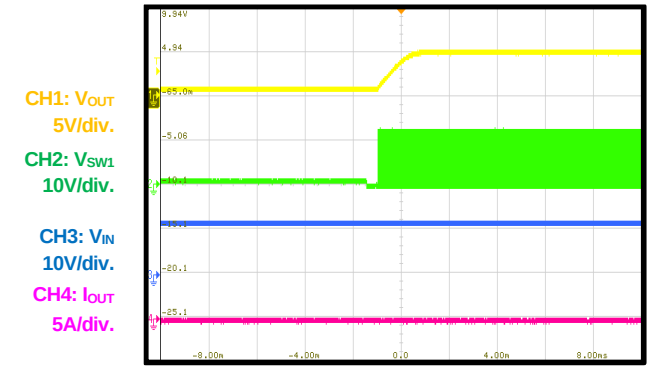
V_{IN} = 12V, V_{OUT} = 20V, I_{OUT} = 0A, PWM mode



2µs/div.

I²C Operation On

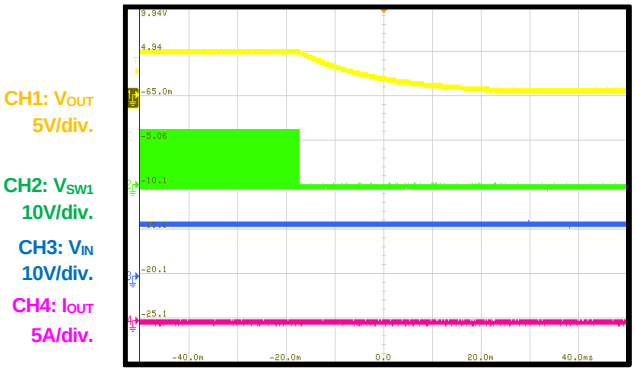
V_{IN} = 12V, V_{OUT} = 5V,I_{OUT} = 0A



2ms/div.

I²C Operation Off

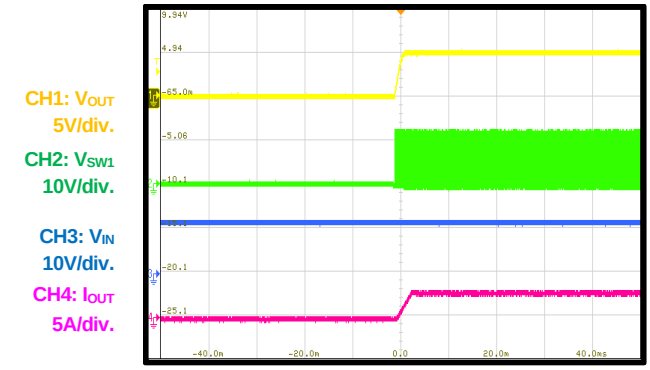
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A



10ms/div.

I²C Operation On

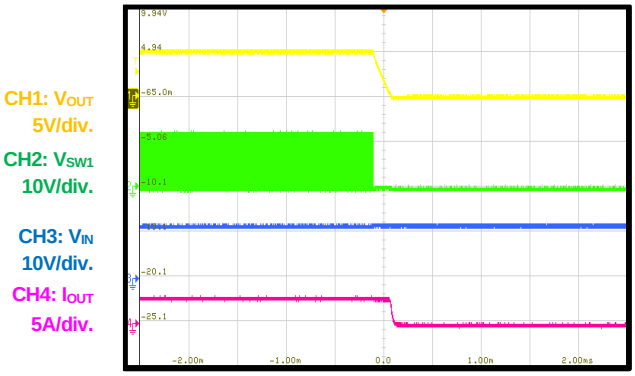
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A



10ms/div.

I²C Operation Off

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A



500µs/div.

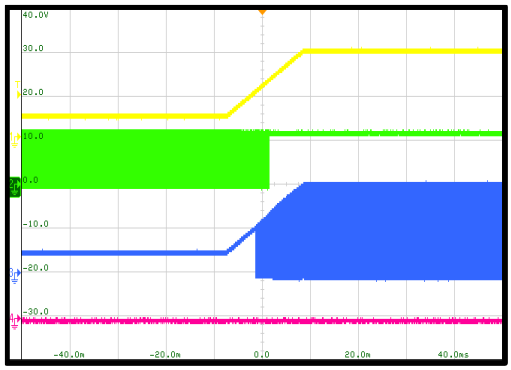
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

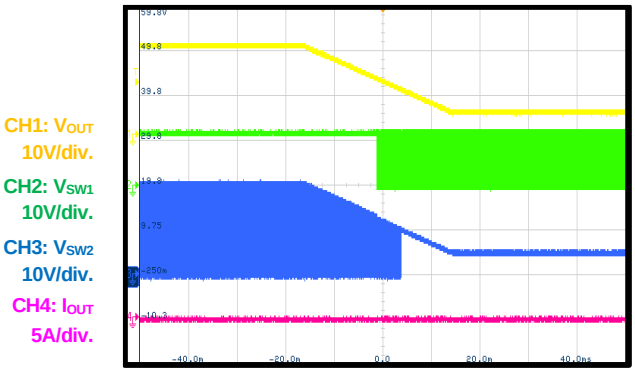
Output Voltage Transition

V_{IN} = 12V, V_{OUT} = 5V to 20V, I_{OUT} = 0A



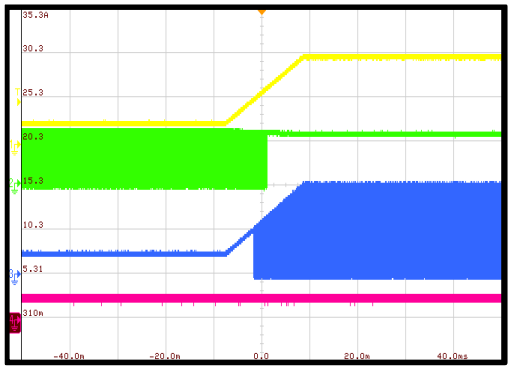
Output Voltage Transition

V_{IN} = 12V, V_{OUT} = 20V to 5V, I_{OUT} = 0A



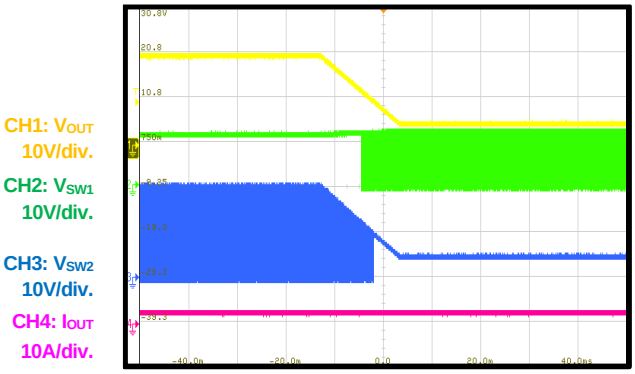
Output Voltage Transition

V_{IN} = 12V, V_{OUT} = 5V to 20V, I_{OUT} = 3A



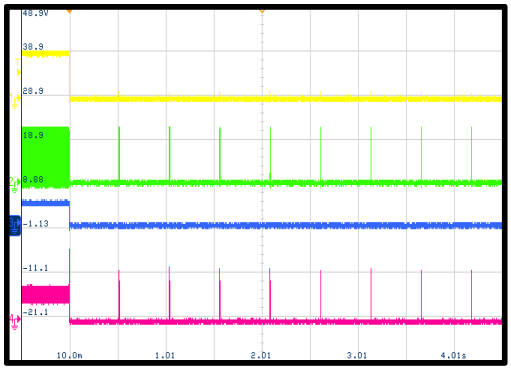
Output Voltage Transition

V_{IN} = 12V, V_{OUT} = 20V to 5V, I_{OUT} = 3A



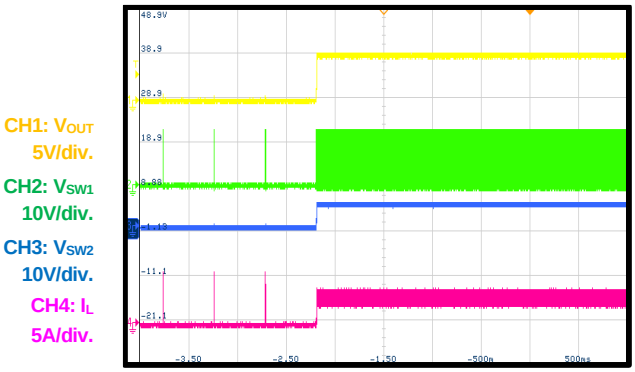
Short Circuit Protection Entry

V_{IN} = 12V, V_{OUT}=5V, I_{OUT} = 3A, 500ms hiccup off time



Short Circuit Protection Recovery

V_{IN} = 12V, V_{OUT}=5V, I_{OUT} = 3A, 500ms hiccup off time



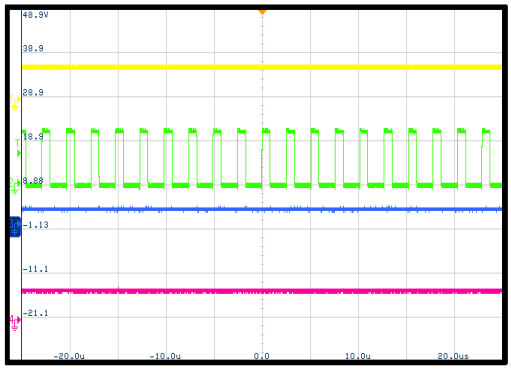
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, forced PWM mode, T_A = 25°C, unless otherwise noted.

Constant Current Limit Protection

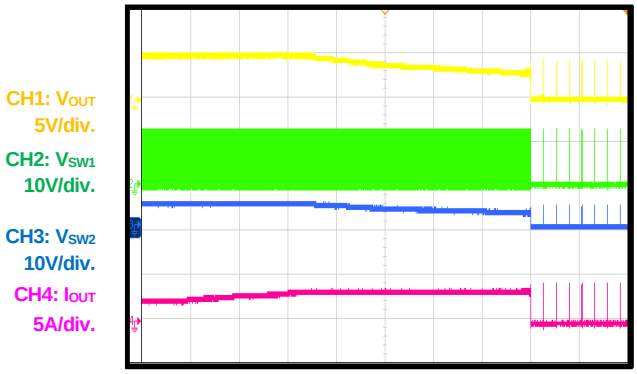
V_{IN} = 12V, V_{OUT} = 5V, CR Load = 1Ω, output current limit = 3A



500µs/div.

CRL Load OCP

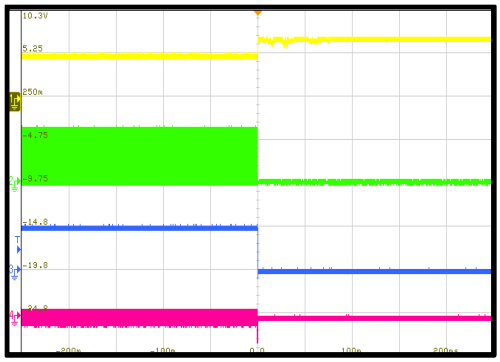
V_{IN} = 12V, V_{OUT} = 5V, CC current limit = 3A, ramp up CRL load slowly



2s/div.

OVP Entry

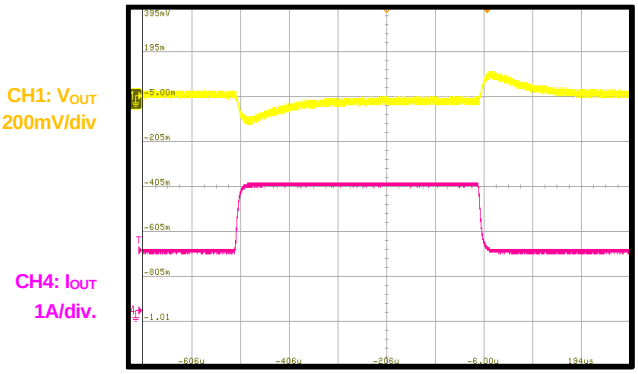
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, Force 7V on Vout



200ms/div.

Load Transient Response

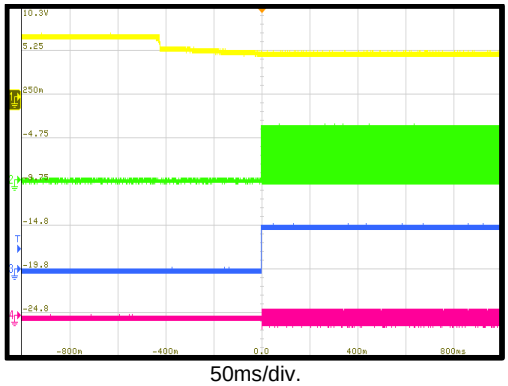
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.5A to 3A, no line drop compensation



100µs/div.

OVP Recovery

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 0A, Force 7V on Vout



50ms/div.

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FUNCTIONAL BLOCK DIAGRAM

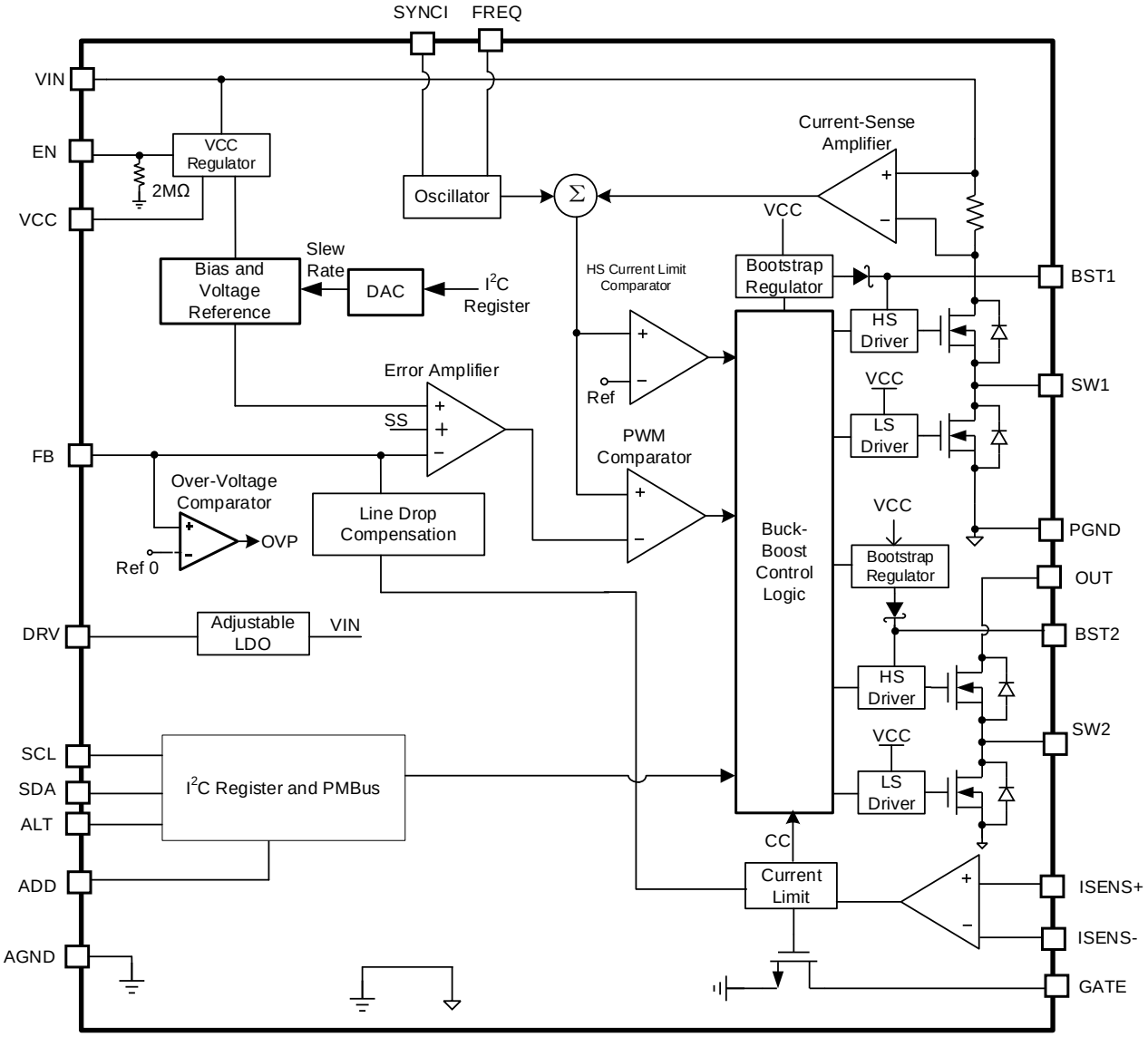


Figure 2: Functional Block Diagram

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OPERATION

The MP4245 is a buck-boost converter with four integrated power MOSFET switches. The device can deliver up to 6A of output current at certain input voltage supply ranges, with excellent load and line regulation.

The MP4245 works with fixed-frequency control logic to provide fast transient response for all operation modes: buck, boost, and buck-boost. There is one special buck-boost control strategy that provides high efficiency across the full input voltage range, and smooths the transient response between different modes.

Buck-Boost Operation

The MP4245 can regulate the output voltage (V_{OUT}) above, below, or equal to the input voltage (V_{IN}). Figure 3 shows a buck-boost power structure with one inductor and four switches (SWA, SWB, SWC, and SWD).

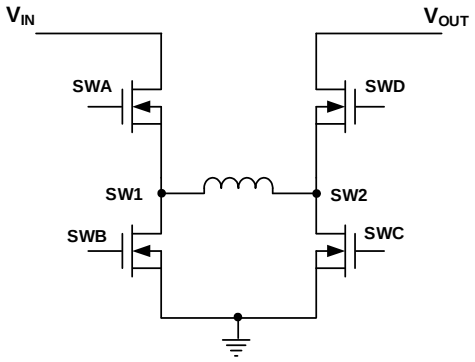


Figure 3: Buck-Boost Topology

Buck mode, boost mode, and buck-boost mode can have different V_{IN} inputs (see Figure 4).

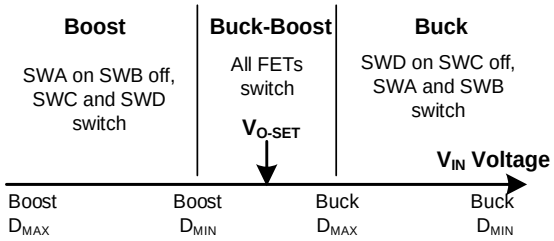


Figure 4: Buck-Boost Operation Range

Buck Mode (V_{IN} > V_{OUT})

When V_{IN} exceeds V_{OUT}, the MP4245 works in buck mode. In buck mode, switch A (SWA) and switch B (SWB) switch for buck regulation. Meanwhile, switch C (SWC) is off, and switch D (SWD) stays on to conduct the inductor current.

In each cycle, SWA turns on to conduct the inductor current. SWA remains on until the inductor current reaches the COMP voltage (V_{COMP}) through R_{SENSE}, then SWB turns on with a calculated off time to conduct the inductor current. An internal oscillator controls the SWA off time to maintain a fixed frequency. The COMP signal is an error amplifier (EA) output from the V_{OUT} feedback and internal FB reference voltage. This means that V_{COMP} controls the inductor current to supply the output terminal voltage. Figure 5 shows the buck mode waveform.

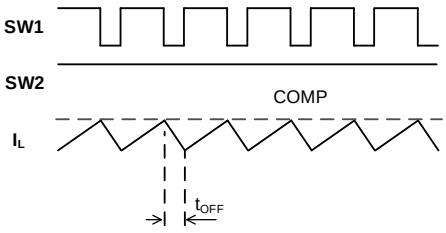


Figure 5: Buck Waveform

Boost Mode (V_{IN} < V_{OUT})

When V_{IN} is significantly lower than V_{OUT}, the MP4245 works in boost mode. In boost mode, SWC and SWD switch for the boost regulation. SWB is off, and SWA remains on to conduct the inductor current.

In each cycle, SWC turns on to conduct the inductor current. When the inductor current rises and triggers the control signal on COMP, SWC turns off and SWD turns on. SWC turns off for a fixed off time before turning on again, and SWD turns on for the current freewheel. An internal oscillator controls the SWC off time to maintain a fixed frequency. Then SWC turns on and off repeatedly to regulate the current to match the COMP signal. The COMP voltage controls the inductor current to supply the output terminal voltage in boost mode. Figure 6 shows the boost work waveform.

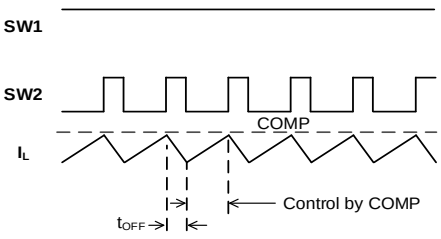


Figure 6: Boost Waveform

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Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

When V_{IN} is almost equal to V_{OUT}, the converter cannot provide enough energy to the load in buck mode due to SWA's minimum off time. In boost mode, the converter supplies too much power to the load due to SWC's minimum on time. Under these conditions, the MP4245 adopts buck-boost control to regulate the output (see Figure 7).

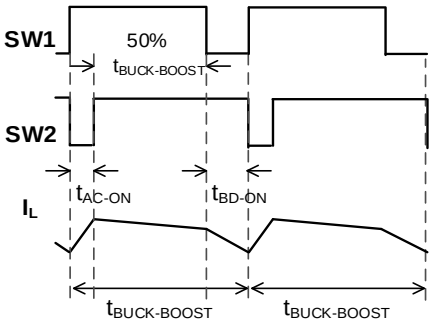


Figure 7: Buck-Boost Waveform

If V_{IN} is almost equal to V_{OUT}, buck-boost mode activates. The MOSFET turn-on sequence is as follows:

1. SWA and SWC
2. SWA and SWD
3. SWD and SWB

Through this process, the inductor current can reach the COMP voltage requirement, and supply enough current to the output.

The SWA and SWD turn-on time is fixed to about 50% of the buck-boost operation frequency. If buck mode nearly reaches the minimum off time, the IC enters buck-boost mode. If V_{IN} is about 15% above V_{OUT} in buck-boost mode, the IC changes to buck mode. If V_{IN} is about 10% below V_{OUT}, the IC enters boost mode. When boost mode nearly reaches the minimum on time, the IC enters buck-boost mode.

Enable Control (EN)

The MP4245 has enable (EN) control. The EN pin has two thresholds. The first threshold is when EN > 0.7V, and VCC is enabled. The second threshold is when EN > 1.6V, and the chip starts to operate normally. The EN pin is clamped internally using a 10V series Zener diode (see Figure 8). Connect the EN input pin through two resistor dividers to the V_{IN} supply and GND. The EN rising threshold is 1.6V, so V_{IN} must exceed 6.05V to enable the circuit. If the EN pin is directly connected to VIN when V_{IN} exceeds 6V, do not add a capacitor exceeding 1nF to EN.

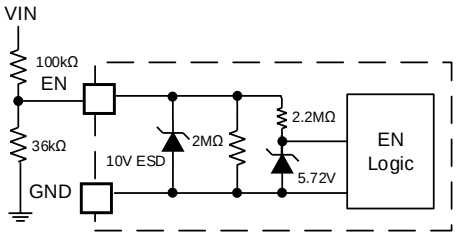


Figure 8: EN Internal Circuit

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.3V; its falling threshold is 3.0V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter's output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage (V_{SS}) that ramps up from 0V to 5V. When V_{SS} is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the output of the MP4245 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side MOSFETs until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Constant Current (CC) Mode Over-Current-Protection (OCP)

The MP4245 senses the ground current with the ISENS+ and ISENS- pins. If I_{OUT} exceeds the set current limit threshold, the MP4245 enters constant current (CC) limit mode. In this mode, the current amplitude is limited. As the load resistance is reduced, the output voltage drops until the feedback voltage falls below the under-voltage (UV) threshold.

If a UV condition is triggered and soft start is ready, the MP4245 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the

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average short circuit current, alleviates thermal issues, and protects the regulator. Once the over-current (OC) condition is removed, the MP4245 exits hiccup mode and resumes normal operation.

When V_{OUT} is set above 6.4V, the MP4245's hiccup UV threshold is about 2.7V. When V_{OUT} is set below 6.4V, the hiccup UV threshold is about 50% of the feedback reference value.

Peak and Valley Current Limit

Besides the output CC limit, the MP4245 also has an SWA peak and SWB valley current limit. The peak current limit is related to the CC limit set-up. When the CC limit increases, the peak current limit increases as well. The valley current limit is fixed, and does not change with the CC limit.

In buck mode and buck-boost mode, both the SWA peak current limit and valley current limit are functional.

In boost mode, only the SWA peak current limit is monitored. In this scenario, the SWA peak current limit is about 23A when V_{IN} = 5V, V_{OUT} = 20V, I_{OUT} = 3A, f_{SW} = 420kHz, and the CC limit = 3.6A.

Output Over-Voltage Protection (OVP)

The MP4245 has output over-voltage protection (OVP). If the output exceeds 121% of V_{REF}, all switches (SWA, SWB, SWC, and SWD) turn off. The discharge path from OUT to ground turns on. When the FB voltage drops to 110% of V_{REF}, the IC resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. The UVLO rising threshold is 2.2V, with a 150mV hysteresis. The BST1 capacitor voltage is regulated internally by VCC through D2, M1, and C4. The BST2 capacitor voltage is regulated internally by VCC through D3, M2, and C5 (see Figure 9).

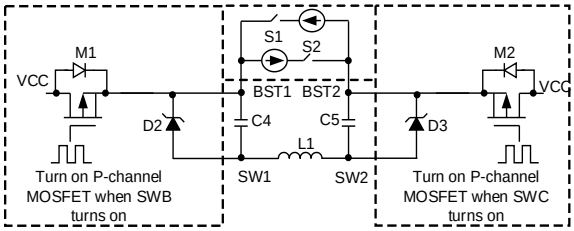


Figure 9: Internal Bootstrap Charging Circuit

In buck mode, S2 always turns on, and BST2 is charged up by BST1; in boost mode, S1 always turns on, and BST1 is charged up by BST2.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current. Then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, VIN going low, thermal shutdown, and an OPERATION off command being received via the I²C. During shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Start-Up Timing for USB PD Applications

If the EN pin is high, the MP4245 powers up VCC, but the default I²C operation bit (OPERATION) is set to off for the MP4245-0000.

When a sink device is plugged in, the PD controller sends the I²C a command to set OPERATION to on.

EN Shutdown Discharge

If the EN pin is pulled low or OPERATION is set to off, all switches (SWA, SWB, SWC, and SWD) turn off. Then the device turns on a 150Ω discharge resistor that is connected from OUT to GND. The discharge path stays on until the FB voltage falls below 50mV.

Gate Pin Logic Table

Table 1 on page 20 shows the GATE pin's logic table. The secondary current limit is about 20A through a current-sense resistor.

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Table 1: GATE Status

Condition	GATE Status
V_{IN} < UVLO threshold	Open drain
EN < UVLO threshold	Open drain
Operation = off	Open drain
I_{SENS} > 20A	0

Configurable Frequency

There are three configurable frequencies: 250kHz, 350kHz, and 420kHz. The frequency can be synchronized to 250kHz, 350kHz, or 420kHz with a ±20% tolerance. When synchronized to a certain frequency, the device's default switching frequency should be set at the same level (e.g. float the FREQ pin). To set f_{SW} to 350kHz, use a 350kHz (±20%) clock to sync the device.

Frequency Spread Spectrum

If the DITHER_ENABLE bit is set to 1, the device has a spread spectrum functionality at 250kHz, 350kHz, or 420kHz. The purpose of spread spectrum is to minimize the peak emissions at specific frequencies.

The MP4245 uses a 4kHz triangle wave (125µs rising, 125µs falling) to modulate the internal oscillator. Spread spectrum operation's frequency span is ±12% of the three available frequencies.

The spread spectrum function is determined by the internal I²C register setting. When frequency spread spectrum is enabled, the frequency sync input is automatically disabled.

Output Line Drop Compensation

The MP4245 can compensate an output voltage drop, such as high impedance caused by a long trace, to keep a fairly constant load-side voltage.

The device uses the load current sensed through R_{SENSE} to sink a current (I_{COMP}) on the FB pin (see Figure 10).

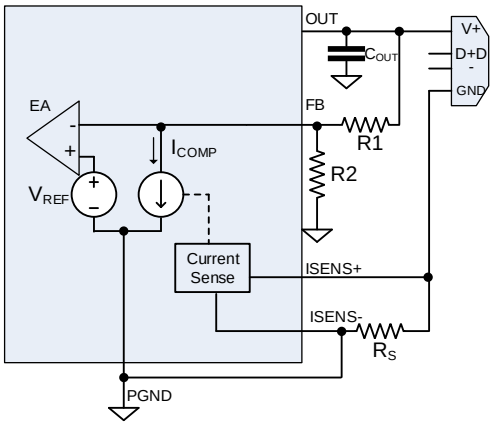


Figure 10: Sinking a Current on FB

I_{COMP} can be calculated with Equation (1):

$$I_{COMP} = G \times I_{OUT} \quad (1)$$

Then V_{OUT} can be estimated with Equation (2):

$$V_{OUT} = \left(\frac{R_1}{R_2} + 1\right) \times V_{REF} + R_1 \times G \times I_{OUT} \quad (2)$$

This means that the line drop compensation amplitude under certain output current conditions is equal to R_1 x G x I_{OUT}.

G is the fixed internal gain, but it can be configured by the I²C. R_1 can also be used to adjust the line drop compensation amplitude.

SYSTEM

Load-Shedding vs. Temperature

The MP4245 monitors the die temperature and alerts the host if a certain thermal threshold is reached. The remaining work is done by a PD controller. For example, the PD controller sends out a new source capability message to lower the output power.

The load-shedding temperature threshold can be configured though the I²C and MTP via the MFR_OT_WARN_LIMIT register.

Thermal Shutdown (TSD)

Thermal shutdown (TSD) prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold, (typically 140°C), the chip is enabled and resumes normal operation. The TSD threshold can be configured via the I²C and MTP.

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ALT Indication

The ALT pin is pulled low if a fault or warning event is triggered. If the related STATUS_MASK register is set to 1, the ALT pin does not respond or pull low if a fault or warning event occurs. Send a byte to the CLEAR_FAULT (0x03) register to reset the STAUS register value and the ALT pin status. If the fault or warning is still present, the alert cannot be cleared (see Figure 11).

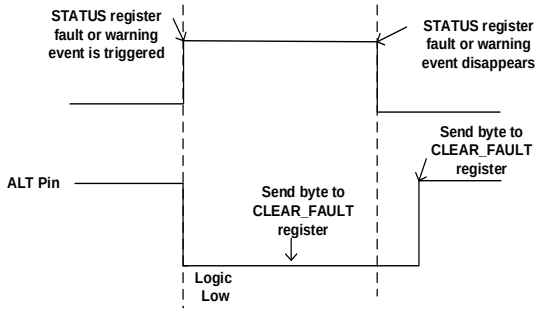


Figure 11: ALT Pin Behaviors

I²C Timing

The I²C is active once VIN and EN both are exceed their under-voltage lockout (UVLO) thresholds.

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PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open standard power management protocol that defines a means of communicating with power converters and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). When idle, the lines are pulled to an external bus voltage. When connecting to the lines, a master device generates an SCL signal and device address, then arranges the communication sequence. This is based on I²C operation principles.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, and signify the beginning and end of a PMBus transfer, respectively. The start condition (S) is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition (P) is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 12).

The master then generates the SCL clocks, andtransmits the device address and the read/write direction bit (R/W) on the SDA. Data is transferred in 8-bit bytes by the SDA. Each byte of data is followed by an acknowledge (ACK) bit.

PMBus Update Sequence

The MP4245 requires a start condition, valid PMBus address, register address byte, and a data byte for a single data update. The device acknowledges that is has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP4245. The device performs an update on the falling edge of the LSB byte.

PMBus Bus Message Format

Figure 13 shows different PMBus operations. Unshaded cells indicate that the bus host is driving the bus actively, and shaded cells indicate that the MP4245 is driving the bus. The symbols are defined below:

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

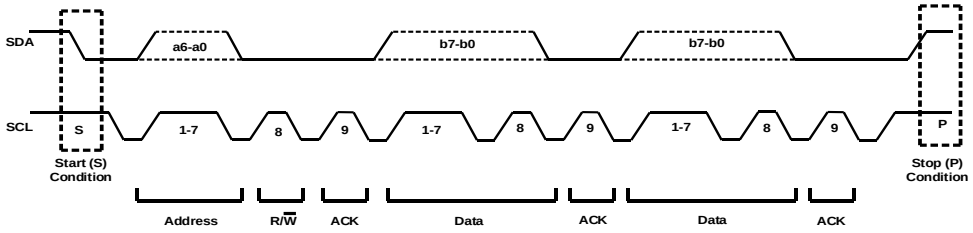


Figure 12: Data Transfer across the PMBus

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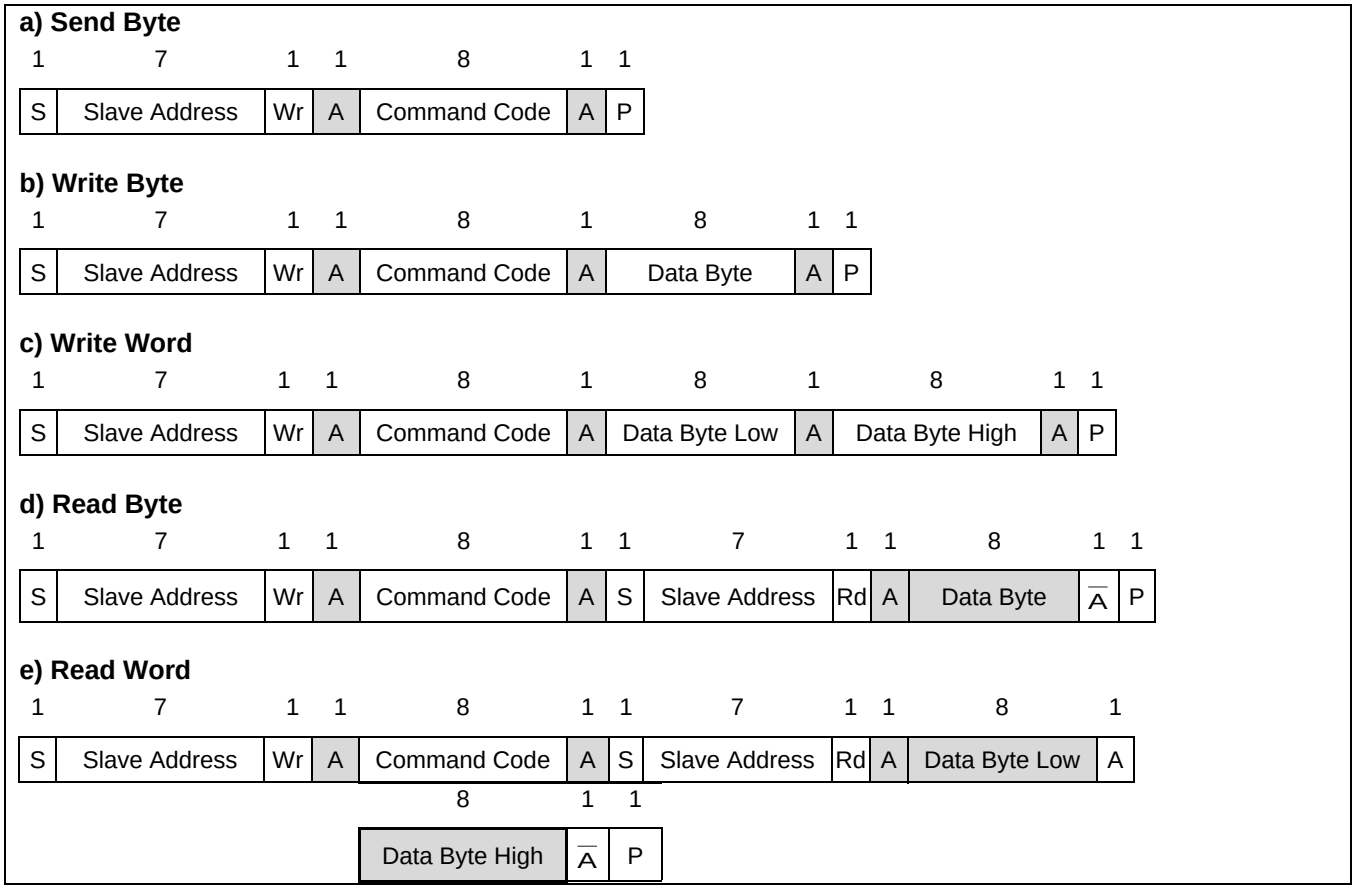


Figure 13: PMBus Message Format

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REGISTER DESCRIPTION

I²C/PMBus Register (9)

CMD Name	CMD Code	Description	Type	Data Format	Unit	MTP
OPERATION	0x01	On/off control	R/W Byte	Reg		Y (1 bit)
CLEAR_FAULTS	0x03		Send Byte	Reg		N
WRITE_PROTECT	0x10		R/W Byte	Reg		N
STORE_USER_ALL	0x15	When sending this command, the converter disables V_{OUT} then enables it again	Send Byte	Reg		N
RESTORE_USER_ALL	0x16		Send Byte	Reg		N
VOUT_MODE	0x20	Output voltage format and exponent (2^{-10})	R Byte	Reg		N
VOUT_COMMAND	0x21		R/W Word	Linear L16	V	Y
VOUT_SCALE_LOOP	0x29		R/W Word	Linear L11		Y
STATUS_BYTE	0x78		R Byte	Reg		N
STATUS_WORD	0x79		R Word	Reg		N
STATUS_VOUT	0x7A		R Byte	Reg		N
STATUS_INPUT	0x7C		R Byte	Reg		N
STATUS_TEMPERATURE	0x7D		R Byte	Reg		N
STATUS_CML	0x7E		R Byte	Reg		N
READ_VIN (1/25V_{IN} to ADC 10 bit, 0V to 1.638V/1.6mV)	0x88	N = -4	R Word	Linear L11	V	N
READ_VOUT	0x8B	N = -10, not including line drop compensation	R Word	Linear L16	V	N
READ_IOUT	0x8C	N = -6	R Word	Linear L11	A	N
READ_TEMPERATURE	0x8D	N = -1, -55°C to +200°C	R Word	Linear L11	°C	N
MFR_MODE_CTRL	0xD0	Selects and enables PWM/PFM, output discharge, hiccup timer, output OVP, dither, and R_{SENS}	R/W Byte	Reg		Y
MFR_CURRENT_LIMIT	0xD1	Sets the continuous constant current (CC) limit	R/W Byte	Reg		Y
MFR_LINE_DROP_COMP	0xD2	Sets line drop compensation	R/W Byte	Reg		Y
MFR_OT_FAULT_LIMIT	0xD3		R/W Byte	Reg	°C	Y
MFR_OT_WARN_LIMIT	0xD4		R/W Byte	Reg	°C	Y
MFR_CRC_ERROR_FLAG	0xD5	Set high when a CRC error occurs while restoring data to the MTP	R Byte	Reg		N
MFR_MTP_ CONFIGURATION_CODE	0xD6	Represents the device	R/W Byte	Reg		Y
MFR_MTP_REVISION_ NUMBER	0xD7	1 Byte, such as “0x01”	R/W Byte	Reg		Y
MFR_STATUS_MASK	0xD8	Masks the ALT pin indication	R/W Byte	Reg		Y

Note:

9) The default register value is based on MP4245-0000.

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PMBUS COMMAND INTRODUCTION

Linear16 (L16) and Linear11 (L11) Data Formats

Linear16 format is used for the V_{OUT} command. For more details, see Figure 14 and the description below.

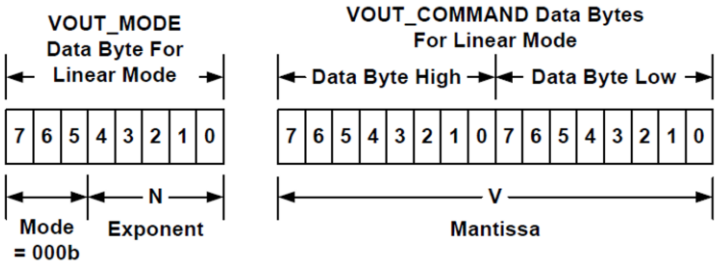


Figure 14: Linear16 Format

The Mode bits are set to 000b. The voltage can be calculated with Equation (3):

$$Voltage = V \times 2^{N} \quad (3)$$

Where Voltage is the parameter of interest (in V); V is a 16-bit unsigned binary integer; and N is a 5-bit, two's complement binary integer.

Linear11 format is used for other commands, such as the V_{OUT} scale loop and temperature monitoring. For more details, see Figure 15 and the description below.

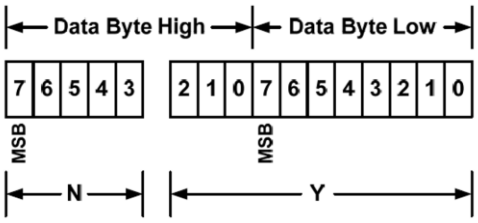


Figure 15: Linear11 Format

The relationship between Y, N, and the real-world value can be calculated with Equation (4):

$$X = Y \times 2^{N} \quad (4)$$

Where X is the real-world value, Y is an 11-bit, two's complement integer, and N is a 5-bit, two's complement integer.

Devices that use linear format must accept and be able to process any value of N.

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OPERATION

The OPERATION command configures the converter's operation state.

Bits	Description
7	This bit sets the on/off state. Note that the EN pin has a higher control priority than this bit. This bit is set to 0 by default. 0: The output is off 1: The output is on
3:0	Reserved.

CLEAR_FAULTS

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. If the device is asserting the ALT signal at the same time, the device clears its ALT signal output.

The CLEAR_FAULTS command does not cause any unit that has latched off for a fault condition to restart. If the fault is still present when the bit is cleared, then the fault bit is immediately set again and the host is notified. This command is write-only. There is no data byte for this command.

WRITE_PROTECT

The WRITE_PROTECT command controls writing to the PMBus device. The intent of this command is to prevent accidental changes. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Data Byte Value	Description
1000 0000	Disable all writes except to the WRITE_PROTECT command
0100 0000	Disable all writes except to the WRITE_PROTECT, OPERATION commands
0010 0000	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR Registers and VOUT_COMMAND commands.
0000 0000	Enable writes to all commands. By default the STORE_USER_ALL is write enabled.

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory (I²C register) to the matching locations in the MTP (non-volatile user store memory). Any items in operating memory that do not have matching locations in the user store are ignored.

The output is initially turned off during this operation. After MTP configuration is complete, the device starts up. While storing user memory to MTP, the device initiates a cyclic redundancy check (CRC) calculation, and stores the CRC check result in a 1-byte MTP cell. The MTP can be configured two times. V_{IN} must exceed 6.5V for MTP configuration.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the non-volatile user store memory (MTP) to the matching locations in the operating memory (I²C register). The values in the operating memory are overwritten by the value retrieved from the user store. Any items in user store that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used even if the device is never configured by the MTP. While restoring MTP data to user memory, the device initiates a CRC calculation, and compares the calculated result with the stored CRC result in the MTP cell. The MTP value is restored to the operating memory only when the values match. After the RESTORE_USER_ALL process is complete, set the

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OPERATION command to off. Set it to on again to refresh the register value. This command is write-only. There is no data byte for this command.

VOUT_MODE

Command	VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R
Function	MODE			N				
Default	0	0	0	1	0	1	1	0

The MP4245 only supports linear mode. The MODE bits are set to 000b by default. N is fixed to -10.

VOUT_COMMAND

The VOUT_COMMAND command sets the output voltage. It follows the Linear16 linear data format.The I²C voltage scaling slew rate is fixed to 0.04mV/μs (V_{REF}). V_{OUT} can be calculated with Equation (5):

$$V_{OUT} = V_{REF} \text{ x feedback ratio} \quad (5)$$

Where the feedback ratio can be estimated with Equation (6):

$$\text{Feedback ratio} = (R1 + R2) / R2 \quad (6)$$

The maximum V_{OUT} command is 0x5800.

Command	VOUT_COMMAND															
Format	Linear16															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default	0x1400 (5V)															

V_{OUT} (in V) can be calculated with Equation (7):

$$V_{OUT} (V) = V \text{ x } 2^{-10} \quad (7)$$

Where V is a 16-bit, unsigned binary integer of VOUT_COMMAND, bits[15:0], K is related to the feedback ratio, and the output resolution (or minimum step) is 0.8mV / K.

For example, if the feedback resistor ratio is V_{OUT} / V_{FB} = 12.5, then K = 1 / 12.5 = 0.08, and the output resolution is 10mV. The internal reference voltage is equal to V_{OUT} x K. The internal reference voltage ranges between 0.1V and 1.63V, with a 0.8mV step.

VOUT_SCALE_LOOP

In typical devices, the output voltage (V_{OUT}) is sensed through a voltage resistor divider (see Figure 16). The resistor divider reduces or scales V_{OUT} so that when V_{OUT} is correct, the value supplied to the control circuit is equal to the reference voltage. This command has 2 data bytes encoded in Linear11 format. This value is unitless.

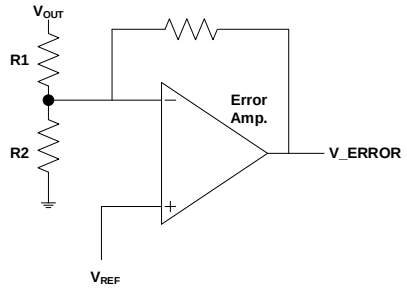


Figure 16: Output Voltage Sensing

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Command	VOUT_SCALE_LOOP															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	Data byte high								Data byte low							
Default	0xB052 (0.08)															

The V_{OUT} scale loop can be estimated with Equation (8):

$$V_{OUT} \text{ scale loop} = X \times 2^{-10} \quad (8)$$

Where X is an 11-bit, unsigned binary integer of VOUT_SCALE_LOOP, bits[10:0]; the V_{OUT} scale loop = R2 / (R1 + R2), and is the reciprocal of the V_{OUT} scale loop (the default value is 0.08).

If another feedback ratio is used, set VOUT_SCALE_LOOP to the new value accordingly.

The feedback ratio should be determined based on the required V_{OUT} resolution. The MP4245's internal reference voltage ranges between 0.1V and 1.638V, with 0.8mV per step. If a 10mV V_{OUT} resolution is required, the feedback ratio should be 10mV / 0.8mV = 12.5. Then VOUT_SCALE_LOOP = 1 / 12.5, or 0.08. The adjustable V_{OUT} range is (0.1V to 1.638V) x 12.5, meaning it is between 1.25V and 20.47V.

If the maximum output voltage is 21V in a USB PD application, the feedback ratio can be set to 0.0638 (R1 = 90.9kΩ, R2 = 6.2kΩ) for a larger output range.

The V_{OUT} scale loop value must match the real output feedback resistor divider value.

STATUS_BYTE

The STATUS_BYTE command returns 1 byte of information with a summary of the most critical fault statuses.

Bit	Bit Name	Description
7	BUSY	Indicates if a fault occurs because the device is busy and unable to respond.
6	OFF	This bit asserts if the unit is not providing power to the output. This includes when the device is not enabled to turn on.
5	VOUT_OV_FAULT	Indicates if an output over-voltage (OV) fault has occurred.
4	IOUT_OC_FAULT	Indicates if an output over-current (OC) fault has occurred. If the devices reaches the constant current (CC) limit or enters hiccup mode, this bit is set.
3	VIN_UV_FAULT	Indicates if an input under-voltage (UV) fault has occurred.
2	TEMPERATURE	Indicates if a temperature fault or warning has occurred.
1	CML	Indicates if a communications, memory or logic fault (e.g. an MTP CRC check error) has occurred.
0	NONE_OF_THE_ ABOVE	Indicates if a fault or warning not listed in bits [7:1] has occurred.

STATUS_WORD

The STATUS_WORD command returns 2 bytes of information with a summary of the MP4245's fault conditions. Based on the information in these bytes, the host can obtain more information by reading the associated status registers.

The lower byte (8 bits) of STATUS_WORD shares its register with the STATUS_BYTE command.

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Byte	Bit	Status Bit Name	Description
Low	7	BUSY	Indicates if a fault occurs because the device is busy and unable to respond.
	6	OFF	This bit asserts if the unit is not providing power to the output. This includes when the device is not enabled to turn on.
	5	VOUT_OV_FAULT	Indicates if an output over-voltage (OV) fault has occurred.
	4	IOUT_OC_FAULT	Indicates if an output over-current (OC) fault has occurred. If the devices reaches the constant current (CC) limit or enters hiccup mode, this bit is set.
	3	VIN_UV_FAULT	Indicates if an input under-voltage (UV) fault has occurred.
	2	TEMPERATURE	Indicates if a temperature fault or warning has occurred.
	1	CML	Indicates if a communications, memory or logic fault (e.g. an MTP CRC check error) has occurred.
	0	NONE_OF_THE_ ABOVE	Indicates if a fault or warning not listed in bits [7:1] has occurred.
High	7	VOUT	Indicates if an output voltage (V_{OUT}) fault or warning has occurred.
	6	IOUT/POUT	Indicates if an output current (I_{OUT}) fault has occurred. This bit is set if an I_{OUT} fault occurs. The MP4245 then enters either hiccup mode or constant current (CC) limiting.
	5	INPUT	Reserved.
	4	OC_EXIT	Indicates if I_{OUT} exits the CC limit mode. This bit is only set high when I_{OUT} changes from CC (before entering hiccup mode) to non-CC. This bit is not set when the device recovers from hiccup mode.
	3	PG_STATUS#	If the power good (PG) signal is present, this bit is ignored.
	2	Reserved	Reserved.
	1	OTHER	Indicates if a bit in the STATUS_OTHER register is set.
	0	UNKNOWN	Indicates if a fault type not listed in bits[15:1] of the STATUS_WORD command has been detected.

The OFF and PG_STATUS# bits are an exception, as they do not remain set. Instead, these bits always reflect the current state of the device or the power good signal (if present).

STATUS_VOUT

The STATUS_VOUT command returns 1 data byte that indicates whether an output under-voltage (UV) or over-voltage (OV) warning or fault has occurred.

Bits	Description
7	VOUT_OV_FAULT indicates whether an output over-voltage (OV) fault has occurred (V_{OUT} >121% of the set V_{OUT}).
6	VOUT_OV_WARNING indicates whether an output OV warning has occurred (V_{OUT} >108.5% of the set V_{OUT}).
5	VOUT_UV_WARNING indicates whether an output under-voltage (UV) warning has occurred (V_{OUT} <75% of the set V_{OUT}).
4	VOUT_UV_FAULT indicates whether an output UV fault has occurred (V_{OUT} <50% of the set V_{OUT}).
3:0	Reserved.

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STATUS_INPUT

The STATUS_INPUT command returns one data byte that indicates whether an input under-voltage (UV) or over-voltage (OV) warning or fault has occurred.

Bits	Description
7	VIN_OV_FAULT indicates whether an input over-voltage (OV) fault has occurred (Input Over-voltage Fault). See the Electrical Characteristics section on page X for more details.
6	VIN_OV_WARNING indicates whether an input OV warning has occurred.
5	VIN_UV_WARNING indicates whether an input under-voltage (UV) warning has occurred.
4	VIN_UV_FAULT indicates whether an input UV fault has occurred.
3:0	Reserved.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns 1 data byte with information about over-temperature (OT) conditions.

Bits	Description
7	OT_FAULT indicates whether an over-temperature (OT) fault has occurred. It shares this information with the bit that sets the OTP threshold (MFR_OT_FAULT_LIMIT).
6	OT_WARNING indicates whether an OT warning has occurred. See the I²C register command MFR_OT_WARN_LIMIT on page X for more details.
5:4	Reserved.
3	OT_WARNING_EXIT. The OT_WARNING falling edge sets this bit high. It has a 20°C hysteresis below MFR_OT_WARN_LIMIT.
2:0	Reserved.

STATUS_CML

The STATUS_CML command returns one data byte that indicates if certain faults have occurred.

Bit	Description
7	An invalid or unsupported command has been received.
6	Invalid or unsupported data has been received.
5	A packet error check (PEC) has failed.
4	A memory fault has been detected.
3	A processor fault has been detected.
2	Reserved.
1	A communication fault other than the ones listed in bits[7:1] or bit[0] has occurred.
0	A different memory or logic fault has occurred.

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READ_VOUT

The READ_VOUT command returns the measured output voltage (V_{OUT}). When generating the value reported in response to the READ_VOUT command, the internal DAC-sensed FB pin value should be divided by VOUT_SCALE_LOOP.

Command	READ_VOUT															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Data byte high								Data byte low							
Default value	V															

V_{OUT} (in V) can be calculated with Equation (9):

$$V_{OUT}\ (V) = V \times 2^{-10} \quad (9)$$

Where V is a 16-bit, unsigned binary integer of READ_VOUT, bits[15:0]. The internal FB ADC sample resolution is 1.6mV/LSB.

In auto-PFM/PWM mode, the user should send the READ_VOUT command twice to obtain the most recent V_{OUT} value. For the most accurate reading, it is recommended to take the average of at least 5 readings.

READ_IOUT

The READ_IOUT command returns the measured output current (I_{OUT}) (in A).

Command	READ_IOUT															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Data byte high								Data byte low							
Default value	Y															

I_{OUT} (in A) can be calculated with Equation (10):

$$I_{OUT}\ (A) = Y \times 2^{-6} \quad (10)$$

Where Y is an 11-bit, unsigned binary integer of READ_IOUT, bits[10:0]. The internal current-sense ADC sample resolution is 8mA/LSB. For the most accurate reading, it is recommended to take the average of at least 5 readings

READ_VIN

The READ_VIN command returns the measured input voltage (V_{IN}).

Command	READ_VIN															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Data byte high								Data byte low							
Default value	Y															

V_{IN} (in V) can be calculated with Equation (11):

$$V_{IN}\ (V) = Y \times 2^{-4} \quad (11)$$

Where Y is a 11-bit, unsigned binary integer of READ_VIN, bits[10:0]. The internal V_{IN} ADC-sample resolution is 1.6mV/LSB. For the most accurate reading, it is recommended to take the average of at least 5 readings.

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READ_TEMPERATURE

The READ_TEMPERATURE command returns the IC's silicon temperature.

Command	READ_TEMPERATURE															
Format	Linear11															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Function	Data byte high								Data byte low							
Default	Y															

The READ_TEMPERATURE value (in °C) can be estimated with Equation (9):

$$READ_TEMPERATURE\ (°C) = Y \times 2^{-1} \quad (9)$$

Where Y is an 11-bit, two's complement integer of READ_TEMPERATURE, bits[10:0].

The internal sample resolution is 0.5°C/LSB. For the most accurate reading, it is recommended to take the average of at least 5 readings.

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MFR COMMAND DESCRIPTION

I²C Register Map

Name	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_MODE_CTRL	D0	R/W	DITHER_ ENABLE	CLK_ MODE	GND_ SENSE_ RESISTOR		OUTPUT _OVP_ EN	HICCUP_ TIMER	OUTPUT_ DISCHARGE _EN	PFM/ PWM_ MODE
MFR_CURRENT_ LIMIT	D1	R/W	Constant current limit (1A to 6.35A/50mA step)							
MFR_LINE_DROP_ COMP	D2	R/W				DRV_VOLTAGE		LINE_DROP_COMPENSATION_ GAIN		
MFR_OT_FAULT_ LIMIT	D3	R/W						OTP_THRESHOLD		
MFR_OT_WARN_ LIMIT	D4	R/W						OT_WARNING_THRESHOLD		
MFR_CRC_ERROR _FLAG	D5	R						MTP_PAGE_ INDEX		CRC_ ERROR _FLAG
MFR_MTP_CONFIG URATION_CODE	D6	R/W	MTP configuration code (defined by MPS)							
MFR_MTP_REV ISION_NUMBER	D7	R/W	MTP software revision number							
MFR_STATUS_ MASK (1 byte)	D8	R/W	Masks the ALT pin indication when a fault event occurs							

I²C Slave: ADDRESS

The ADD pin sets the I²C slave address (see Table 2). There is 20μA current source on the ADD pin.

Table 2: I²C Addresses

ADD Voltage	ADD to GND Resistor (R1), 1% Accuracy	I²C Address A7:A1	
		Binary	Hex
0 to 0.18V	GND	1100 001	61h
0.25V to 0.38V	15kΩ	1100 010	62h
0.45V to 0.59V	25.5kΩ	1100 011	63h
0.66V to 0.79V	35.7kΩ	1100 100	64h
0.87V to 0.99V	45.3kΩ	1100 101	65h
1.07V to 1.20V	56kΩ	1100 110	66h
>1.28V	VCC	1100 111	67h

MFR_MODE_CTRL

Address: 0xD0
Reset value: Set by the MTP
Type: R/W

Bits	Bit Name	Description
D[7]	DITHER_ENABLE	0: No dither (default) 1: Enable frequency spread spectrum at the following frequencies: 250kHz, 350kHz, and 420kHz
D[6]	CLK_MODE	0: The clock turns on if a STATUS bit changes (default) 1: The clock does not turn on if a STATUS bit changes

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D[5:4]	GND_SENSE_ RESISTOR	Ground sensing resistor set-up. For USB PD applications, select a 20mΩ or 30mΩ current-sense resistor. These bits are set to 10 by default. 00: 5mΩ 01: 10mΩ 10: 20mΩ 11: 30mΩ
D[3]	OUTPUT_OVP_EN	Enables over-voltage protection (OVP). This bit is set to 1 by default. 0: OVP is disabled 1: OVP is enabled
D[2]	HICCUP_TIMER	Controls the buck's over-current protection (OCP) hiccup timer. This bit is set to 0 by default. 0: The hiccup timer is 500ms 1: The hiccup timer is 2 seconds
D[1]	OUTPUT_ DISCHARGE_EN	Enables the output discharge function. This bit is set to 1 by default. 0: Disable the output discharge function 1: Enable the output discharge function
D[0]	PFM/PWM_MODE	Sets the work mode to auto-PFM/PWM mode or forced PWM mode. This bit is set to 1 by default. 0: Auto-PFM/PWM mode 1: Forced PWM mode

MFR_CURRENT_LIMIT

Address: 0xD1
Reset value: Set by the MTP
Type: R/W

The MFR_CURRENT_LIMIT command sets the buck-boost output constant current (CC) limit threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0x48 (3.6A)							

The real-world IOUT_OC (in A) can be calculated with Equation (10):

$$IOUT_OC\ (A) = IOUT_LIM \times 0.05 \quad (10)$$

Where IOUT_LIM is an 8-bit, unsigned binary integer of IOUT_LIM, bits D[7:0], and the IOUT_OC resolution (also called the minimum step) is 50mA. The maximum value is 6.35A. Normal performance cannot be guaranteed beyond this range.

The output current is sensed from the ground sensing resistor (typically 20mΩ). Then the sensed signal is used for the output current limit. Choose the correct ground-sense resistance to set the current limit threshold.

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MFR_LINE_DROP_COMP

Address: 0xD2
Reset value: Set by the MTP
Type: R/W

The MFR_LINE_DROP_COMP command sets V_{DRV} and the current gain from I_{OUT} to the FB sink current.

Bits	Bit Name	Description
D[7:5]	RESERVED	Reserved.
D[4:3]	DRV_VOLTAGE	Sets the DRV pin's output voltage (V_{DRV}). These bits are set to 01 by default. 00: 5.5V 01: 6V 10: 6.2V 11: 6.5V
D[2:0]	LINE_DROP_ COMPENSATION_GAIN	000: 0 001: 0.5μA/A 010: 1μA/A (default value) 011: 2μA/A 100: 4μA/A 101: 8μA/A For USB PD applications, it is recommended to use 0.5μA/A line drop compensation. This can compensate for line loss or MOSFET loss.

Line drop compensation is related to the current-sense resistor. It is only valid when V_{OUT} exceeds 5V. The V_{OUT} read operation does not include line drop compensation.

MFR_OT_FAULT_LIMIT

Address: 0xD3
Reset value: Set by the MTP
Type: R/W

The MFR_OT_FAULT_LIMIT command sets the thermal shutdown trigger threshold.

Bits	Bit Name	Description
D[7:3]	RESERVED	Reserved.
D[2:0]	OTP_THRESHOLD	000: 110°C 001: 120°C 010 130°C 011 140°C 100: 150°C 101: 160°C (default) 110: 170°C 111: 180°C

MFR_OT_WARN_LIMIT

Address: 0xD4
Reset value: Set by the MTP
Type: R/W

The MFR_OT_WARN_LIMIT command sets the thermal warning trigger threshold, and has a 20°C recovery hysteresis.

Bits	Bit Name	Description
D[7:3]	RESERVED	Reserved

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D[2:0]	OT_WARNING_ THRESHOLD	000: 60°C 001: 70°C 010: 80°C 011: 90°C 100: 100°C 101: Disabled 110: 120°C (default) 111: 130°C

MFR_CRC_ERROR_FLAG

Address: 0xD5
Reset value: Set by the MTP
Type: Read-only

Bits	Bit Name	Description
D[7:3]	RESERVED	Reserved.
D[2:1]	MTP_PAGE_INDEX	These bits indicate the current MTP page index. 00: The MTP is not used 10: The first page of the multi-page OTP is currently being used 11: The second page of multi-page OTP is currently being used
D[0]	CRC_ERROR_FLAG	This bit is set to 1 if a CRC check error occurs while restoring the MTP to the I²C register. If a CRC error occurs, the MTP data is discarded. The system uses the default I²C or MTP register value.

MFR_MTP_CONFIGURATION_CODE

Address: 0XD6
Reset value: Set by the MTP
Type: Read-only

Bit	Bit Name	Description
D[7:0]	MFR_MTP_ CONFIGURATION_CODE	MTP configuration code, defined by MPS.

MFR_MTP_REVISION_NUMBER

Address: 0XD7
Reset value: Set by the MTP
Type: Read-only

Bit	Bit Name	Description
D[7:0]	MFR_MTP_REVISION_ NUMBER	MTP software revision number.

MFR_STATUS_MASK

Address: 0xD8
Reset value: Set by the MTP
Type: R/W

This register only can mask the ALT pin behavior. The STATUS register still indicates each event.

Bit	Bit Name	Description
7	VOUT_MSK	0: No mask enabled (default) 1: Mask enabled
6	IOUT/POUT_ MSK	0: No mask enabled (default). This bit masks IOUT_OC_FAULT, IOUT/POUT and OC_EXIT 1: Mask enabled

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5	RESERVED	This bit is set to 1 by default.
4	TEMP_MSK	Temperature-related mask bit. This bit is set to 0 by default. 0: No mask enabled 1: Mask enabled
3	PG_STATUS#_MSK	Higher level PG mask off control bit. This bit is set to 0 by default. 0: No mask enabled 1: Mask enabled
2	PG_ALT_EDGE_MSK	0: No mask enabled. The ALT pin indicates the PG_STATUS# rising and falling edges 1: Mask enabled. The ALT pin only indicates the PG_STATUS# falling edge, which means the output voltage transitions from power not good to power good
1	OTHER_MSK	0: No mask enabled (default) 1: Mask enabled
0	UNKNOWN_MSK	0: No mask enabled (default) 1: Mask enabled

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APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

In a buck-boost topology, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. Two critical inductance values can be estimated according to the buck mode and boost mode current ripples with Equation (11) and Equation (12), respectively:

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{REQ} \times \Delta I_L} \quad (11)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times f_{REQ} \times \Delta I_L} \quad (12)$$

Where f_{REQ} is the switching frequency, and ΔI_L is the peak-to-peak inductor current ripple.

As a rule of thumb, the peak-to-peak ripple can be set within 1A to 3A of the inductor current. In addition to the inductance value, the inductor must support the peak currents to avoid saturation. Calculate this value with Equation (13) and Equation (14) for buck and boost mode, respectively:

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times f_{REQ} \times L} \quad (13)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times f_{REQ} \times L} \quad (14)$$

Where η is the estimated efficiency of the MP4245.

Selecting the Input and Output Capacitor

It is recommended to use ceramic capacitors plus an electrolytic capacitor for input and output capacitors. This filters the input and output ripple current and helps achieve stable operation.

Since the input capacitor absorbs the input switching current, it requires sufficient capacitance. For a 15V/3A application, a 100µF electrolytic capacitor, two 4.7µF ceramic capacitors, 0.1µF ceramic capacitor, and a 1µF ceramic capacitor are sufficient.

The output capacitor stabilizes the DC output voltage. Low-ESR capacitors with sufficient capacitance are recommended to limit the output voltage ripple. For a 15V/3A application, it is recommended to use a 100µF, low-ESR (≤160mΩ), aluminum, electrolytic, or polymer capacitor; two 4.7µF ceramic capacitors; a 10µF ceramic capacitor; a 0.1µF ceramic capacitor; and a 1µF ceramic capacitor.

The input and output ceramic capacitors must be placed as close as possible to the device.

Table 3 lists the recommended input and output capacitors for different output power ratings, and also includes detailed descriptions for the capacitors.

Table 3: Recommended C_{IN} and C_{OUT} Values for Different Output Power Ratings

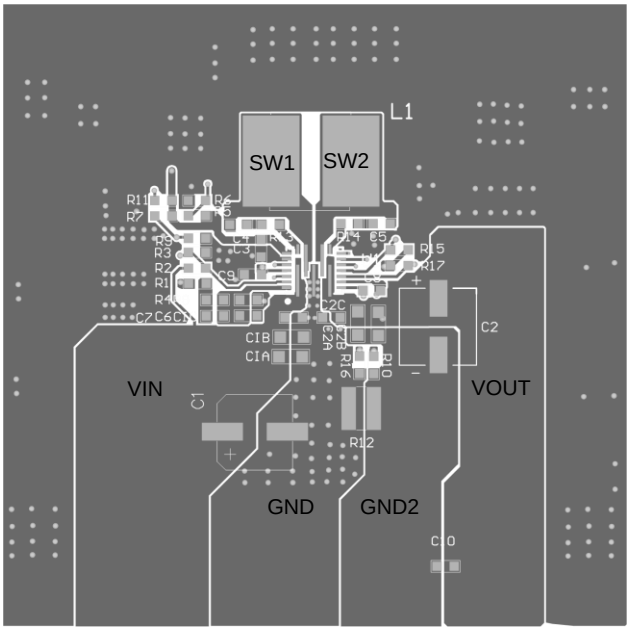
Maximum Output	Input Capacitor (C_{IN})	Output Capacitor (C_{OUT})
20V/2.25A	47µF + 2 x 4.7µF + 0.1µF + 1µF 47µF: Electrolytic capacitor, 50V 4.7µF: Ceramic capacitor, 25V 100nF: Ceramic capacitor, 50V	100µF + 2 x 4.7µF + 0.1µF + 10µF + 1µF 100µF: Hybrid, 25V, 20mΩ 4.7µF: Ceramic capacitor, 16V 10µF: Ceramic capacitor, 50V
15V/3A	47µF + 2 x 4.7µF + 0.1µF + 1µF 47µF: Electrolytic capacitor, 50V 4.7µF: Ceramic capacitor, 25V 100nF: Ceramic capacitor, 50V	100µF + 2 x 4.7µF + 0.1µF + 10µF + 1µF 100µF: Hybrid, 25V, 20mΩ 4.7µF: Ceramic capacitor, 16V 10µF: Ceramic capacitor, 50V
9V/3A	47µF + 2 x 4.7µF + 0.1µF + 1µF 47µF: Electrolytic capacitor, 50V 4.7µF: Ceramic capacitor, 25V 100nF: Ceramic capacitor, 50V	100µF + 2 x 4.7µF + 0.1µF + 1µF 100µF: Hybrid capacitor, 16V, 20mΩ 4.7µF: Ceramic capacitor, 16V
5V/3A	4 x 10µF + 2 x 4.7µF + 0.1µF + 1µF 4x10µF: Ceramic capacitor, 25V 4.7µF: Ceramic capacitor, 25V 100nF: Ceramic capacitor, 50V	100µF + 4.7µF + 0.1µF + 1µF 100µF: Hybrid capacitor, 6.3V, 20mΩ 4.7µF: Ceramic capacitor, 6.3V

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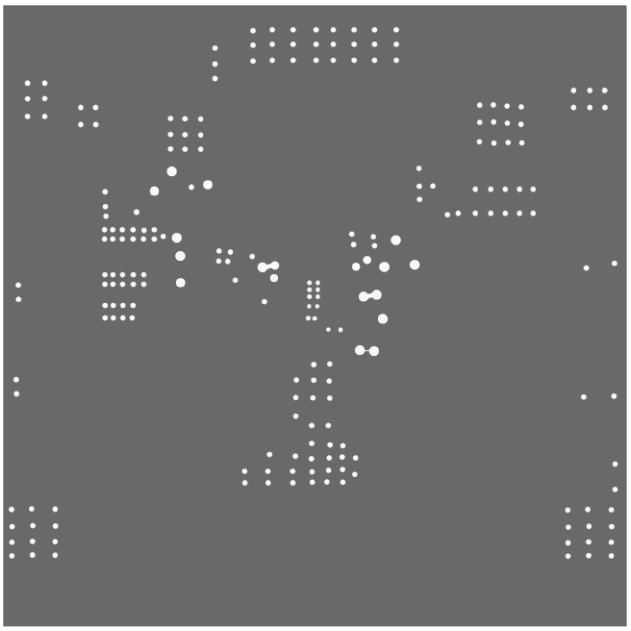
PCB Layout Guidelines

Efficient PCB layout is critical for standard operation and thermal dissipation. For the best results, refer to Figure 17 and follow the guidelines below:

1. Use short, direct, and wide traces to connect OUT.
2. Add vias to GND after the output filter if required.
3. Place a large copper plane on PGND. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. To improve EMI performance, place two ceramic input decoupling capacitors as close as possible to IN and PGND, and place a decoupling ceramic capacitor close to OUT and PGND.
6. Place the input filter on the bottom layer to further improve EMI performance.
7. Place the VCC decoupling capacitor as close as possible to VCC.
8. Use a Kelvin connection for the output current-sense traces (ISENS+ and ISENS-).



Top Layer



Bottom Layer

Figure 17: Recommended PCB layout

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TYPICAL APPLICATION CIRCUITS

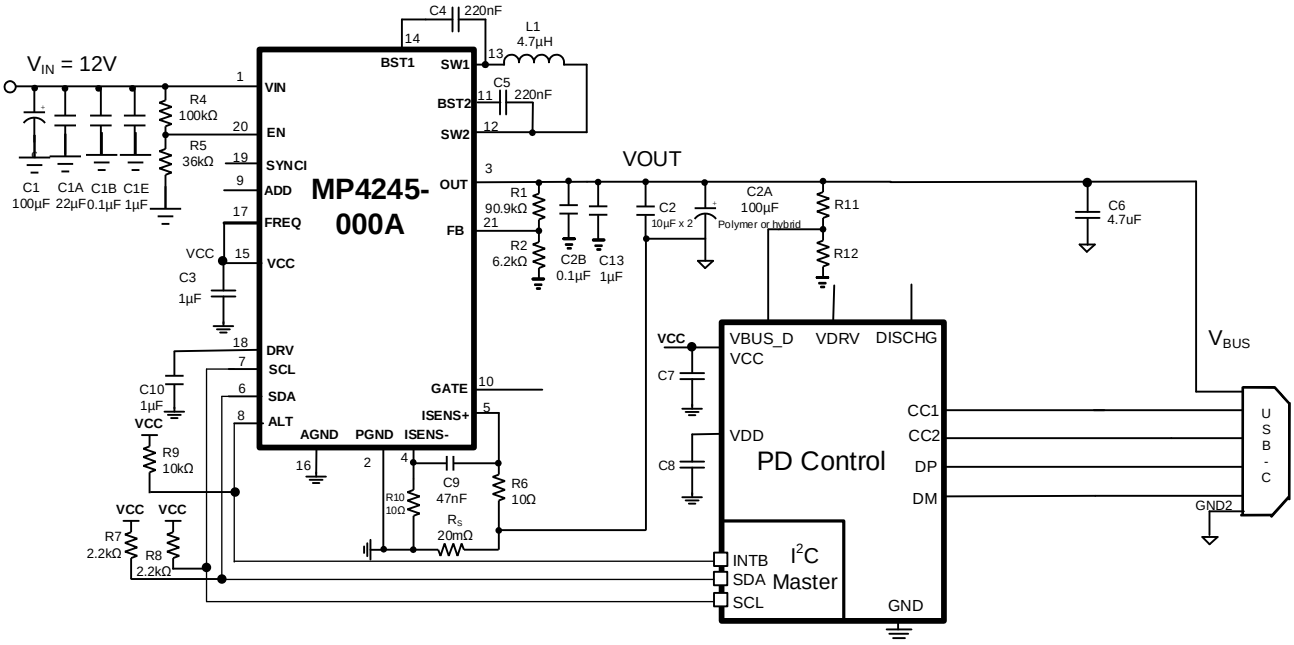


Figure 18: V_{IN} = 12V, V_{OUT} = 3.3V to 21V for USB PD Applications

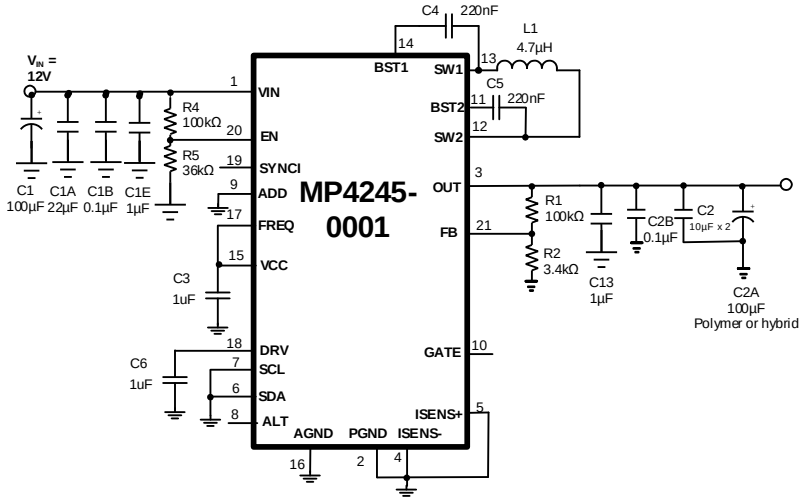


Figure 19: V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 3A without the I²C (10) (11)

Notes:

10) Contact an MPS FAE to apply for a suffix code and modify the MTP register value.
11) When ISENS+ and ISENS- are directly connected to GND, there is no output average current limit, but the switching current limit still functions.

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DEFAULT MTP REGISTER VALUES (MP4245-0000)

OTP Items	Description	Default Value
OPERATION	Sets the MP4245 on or off by default	Off
VOUT_COMMAND	Sets the output voltage (V_{OUT})	5V
VOUT_SCALE_LOOP	Sets the V_{OUT} scale loop (1 / (V_{OUT} feedback ratio))	0.08008
DITHER_ENABLE	Enables frequency spread spectrum	Disabled
GND_SENSE_RESISTOR	Sets the current-sense resistor value	20mΩ
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP)	Enabled
HICCUP_TIMER	Sets the over-current protection (OCP) off timer	500ms
OUTPUT_DISCHARGE_EN	Enables the output discharge function	Enabled
PFM/PWM_MODE	Selects auto-PFM/PWM or forced PWM mode	Forced PWM mode
MFR_CURRENT_LIMIT	Sets the output current limit	3.6A
DRV_VOLTAGE	Sets the DRV pin output voltage (LDO output)	6V
LINE_DROP_COMPENSATION_GAIN	Sets the line drop compensation gain (in µA/A)	1µA/A
OTP_THRESHOLD	Sets the thermal shutdown protection threshold	160°C
OT_WARNING_THRESHOLD	Sets the thermal warning threshold	120°C
VOUT_MSK	Masks the ALT pin indication	No mask
IOUT/POUT_MSK		No mask
INPUT_MASK		Masked
TEMP_MSK		No mask
PG_STATUS#_MSK		No mask
PG_ALT_EDGE_MSK		No mask
OTHER_MSK		No mask
UNKNOWN_MSK		No mask
MFR_MTP_CONFIGURATION_CODE	Returns the MTP configuration code (defined by MPS)	0x08

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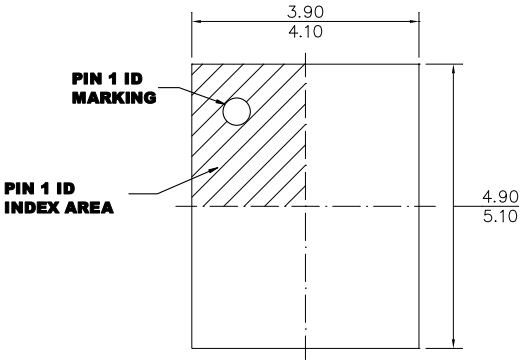
DEFAULT MTP REGISTER VALUES (MP4245-0001)

OTP Items	Description	Default Value
OPERATION	Sets the MP4245 on or off by default	On
VOUT_COMMAND	Sets the output voltage (V_{OUT})	5V
VOUT_SCALE_LOOP	Sets the V_{OUT} scale loop (1 / (V_{OUT} feedback ratio))	0.08008
DITHER_ENABLE	Enables frequency spread spectrum	Disabled
GND_SENSE_RESISTOR	Sets the current-sense resistor value	20mΩ
OUTPUT_OVP_EN	Enables output over-voltage protection (OVP)	Enabled
HICCUP_TIMER	Sets the over-current protection (OCP) off timer	500ms
OUTPUT_DISCHARGE_EN	Enables the output discharge function	Enabled
PFM/PWM_MODE	Selects auto-PFM/PWM or forced PWM mode	Forced PWM mode
MFR_CURRENT_LIMIT	Sets the output current limit	3.6A
DRV_VOLTAGE	Sets the DRV pin output voltage (LDO output)	6V
LINE_DROP_COMPENSATION_GAIN	Sets the line drop compensation gain (in μA/A)	0
OTP_THRESHOLD	Sets the thermal shutdown protection threshold	160°C
OT_WARNING_THRESHOLD	Sets the thermal warning threshold	120°C
VOUT_MSK	Masks the ALT pin indication	No mask
IOUT/POUT_MSK		No mask
INPUT_MASK		Masked
TEMP_MSK		No mask
PG_STATUS#_MSK		No mask
PG_ALT_EDGE_MSK		No mask
OTHER_MSK		No mask
UNKNOWN_MSK		No mask
MFR_MTP_CONFIGURATION_CODE	Returns the MTP configuration code (defined by MPS)	0x01

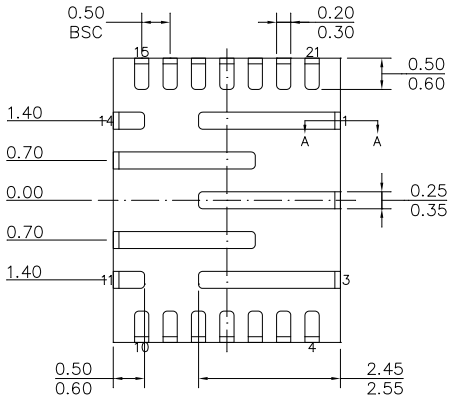
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PACKAGE INFORMATION

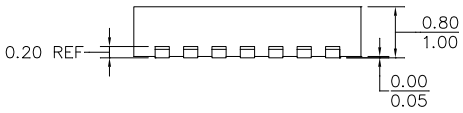
QFN-21 (4mmx5mm)



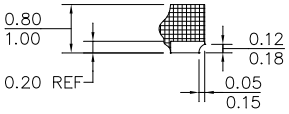
TOP VIEW



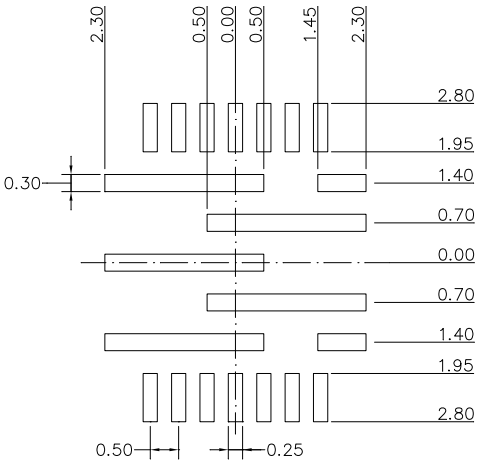
BOTTOM VIEW



SIDE VIEW



SECTION A-A



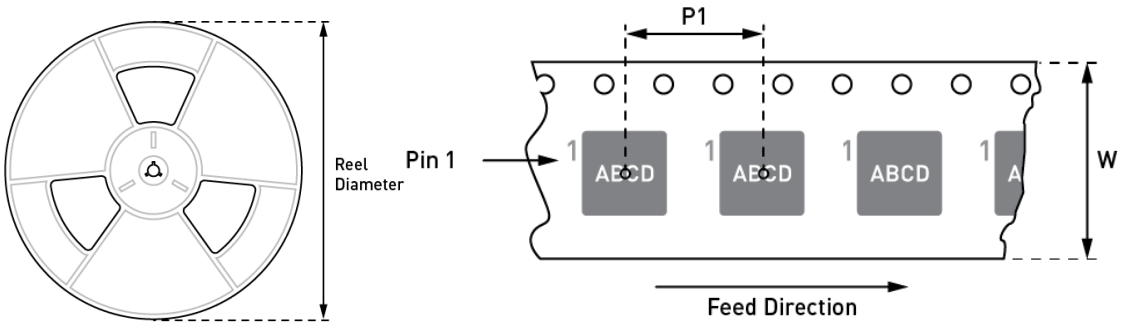
RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PINS 1–3 AND PIN12–13 HAVE THE SAME LENGTH AND WIDTH.
2)ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4245GVE-xxxx-Z	QFN-21 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/19/2021	Initial Release	-

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