



# MP5048A

60V, 4A, 14mΩ  $R_{DS(ON)}$ ,  
Hot-Swap Intelli-Fuse Solution

## DESCRIPTION

The MP5048A is a monolithic, integrated controller and switch. It contains a power MOSFET and circuitry that enable it to operate as a standalone device, or to be controlled by a hot-swap controller. The MP5048A is capable of driving up to 4A of continuous current per device.

The device limits the inrush current to the load when a circuit card is inserted into a live backplane power source. This limits the backplane's voltage drop. The MP5048A also limits the internal MOSFET current by controlling the gate voltage ( $V_{GATE}$ ) via the current-limit reference input.

The MP5048A offers many features to simplify system design. Its integrated solution monitors the output current ( $I_{OUT}$ ) and die temperature, which eliminates the need for an external current-sense resistor, power MOSFET, or thermal sensing.

The MP5048A detects the power MOSFET gate, source, and drain short conditions to provide feedback for the controller. The device can be paralleled for higher current applications.

The MP5048A is available in a QFN-30 (5mmx5mm) package.

## FEATURES

- 24V to 60V Operating Input Voltage ( $V_{IN}$ ) Range
- 4A Maximum Output Current ( $I_{OUT}$ )
- 14mΩ Integrated Power MOSFET
- Built-In MOSFET Driver
- Integrated Current Sensing with Sense Output
- Separate Current-Sense Output to Configure the Over-Current Limit
- Built-In Soft Start (SS) and Insertion Delay
- Output Short-Circuit Protection (SCP)
- Over-Temperature Protection (OTP)
- Built-In Fuse Health Diagnostics
- Fault Signal Output
- Parallel Operation for Higher Current Applications
- Integrated Intelli-Fuse Temperature Sensing
- Output Voltage ( $V_{OUT}$ ) Shutdown Control
- Available in a QFN-30 (5mmx5mm) Package

## APPLICATIONS

- Industrial Applications
- Servers
- Networking

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## TYPICAL APPLICATIONS

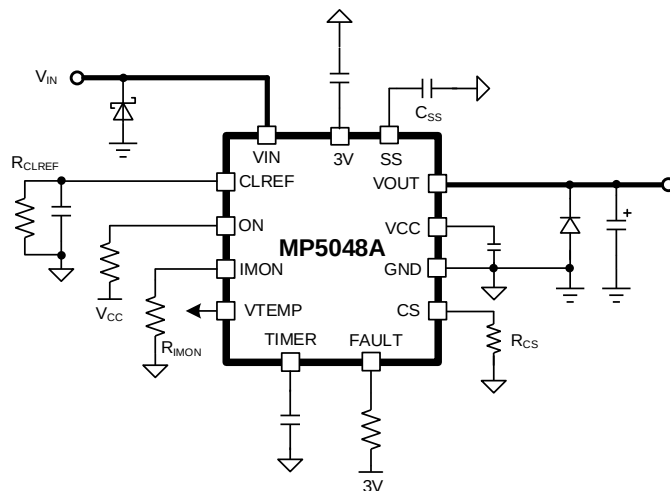
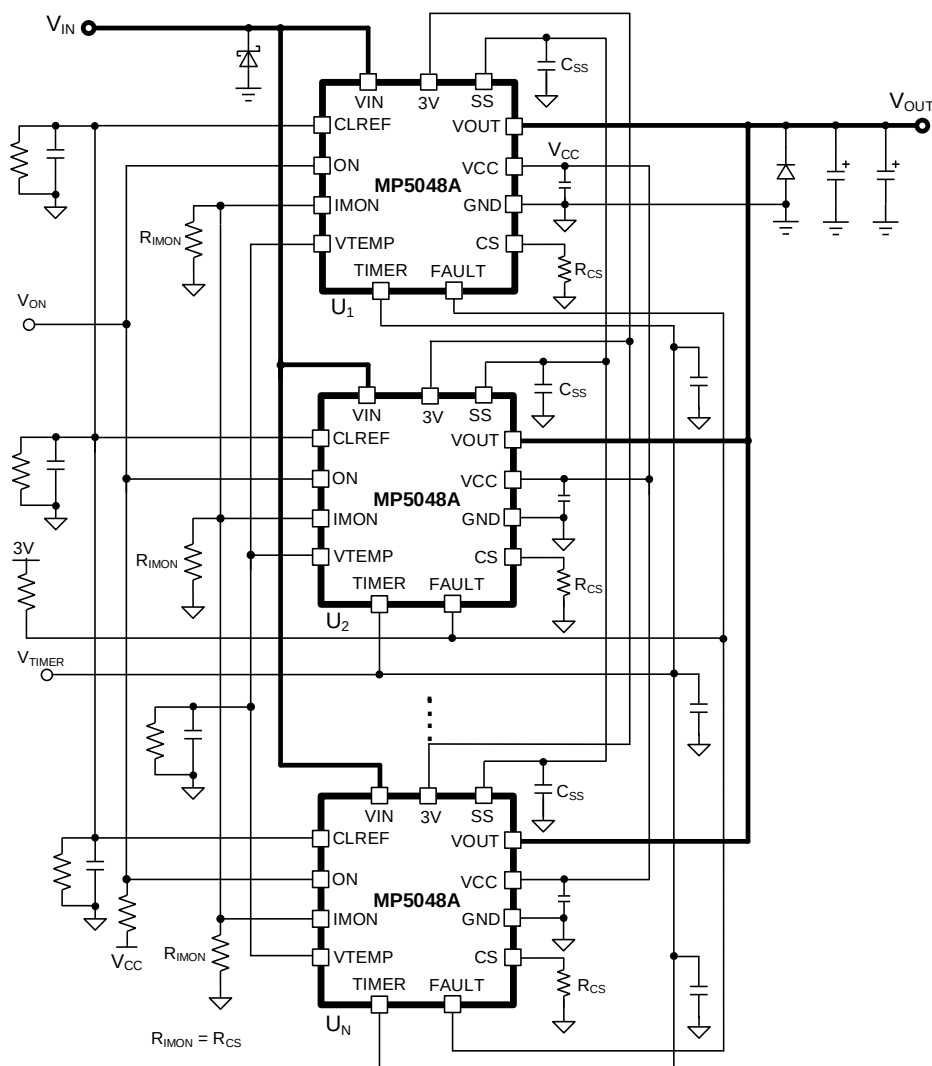


**Figure 1: Standalone Operation ( $R_{IMON} \geq R_{CS}$ )**



### Figure 2: Parallel Operation

## TYPICAL APPLICATIONS (continued)

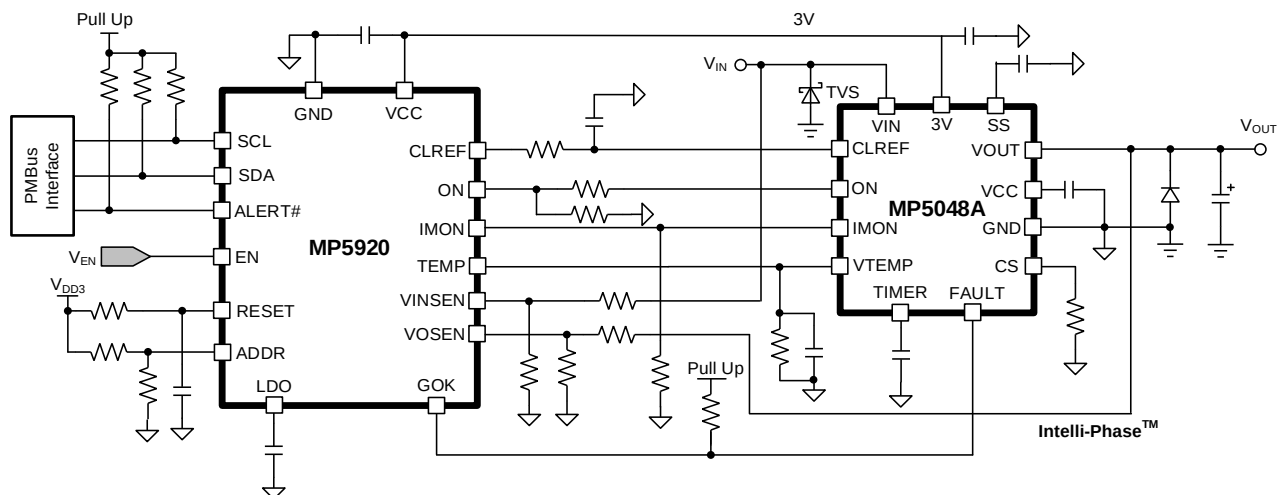


Figure 3: MP5048A Controlled by Hot-Swap Controller (MP5920)

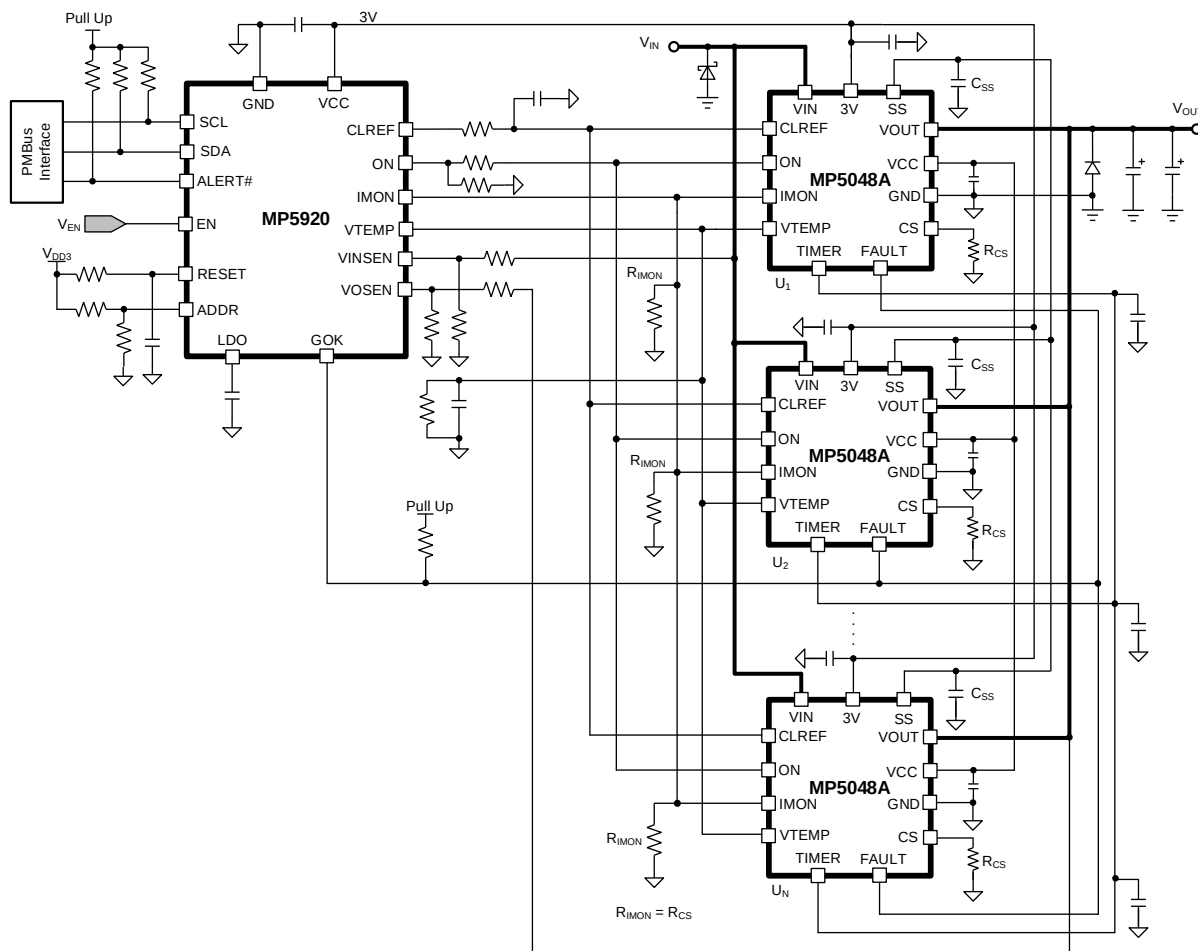


Figure 4: MP5048A Controlled by Hot-Swap Controller (MP5920) in Parallel Operation

## ORDERING INFORMATION

| Part Number* | Package          | Top Marking | MSL Rating |
|--------------|------------------|-------------|------------|
| MP5048AGU    | QFN-30 (5mmx5mm) | See Below   | 1          |

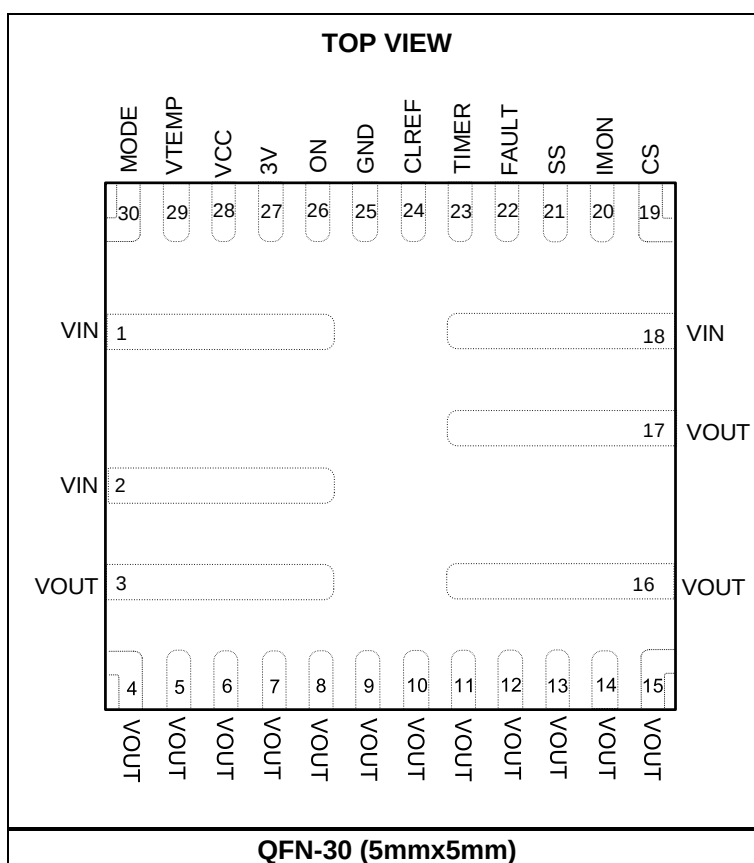
\* For Tape & Reel, add suffix -Z (e.g. MP5048AGU-Z).

## TOP MARKING

**MPSYYWW**  
**MP5048A**  
**LLLLLLL**

MPS: MPS prefix  
 YY: Year code  
 WW: Week code  
 MP5048A: Part number  
 LLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #                                               | Name  | Description                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2, 18                                            | VIN   | <b>System input power supply.</b> The VIN pin is connected to the drain of the integrated power MOSFET.                                                                                                                                                                                                                         |
| 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17 | VOUT  | <b>Output voltage.</b> The VOUT pin is connected to the source of the integrated power MOSFET.                                                                                                                                                                                                                                  |
| 19                                                  | CS    | <b>Current-sense output.</b> The CS voltage (V <sub>CS</sub> ) is compared to the CLREF voltage (V <sub>CLREF</sub> ) to determine the over-current (OC) limit. Connect a resistor between the CS and GND pins to generate V <sub>CS</sub> .                                                                                    |
| 20                                                  | IMON  | <b>Current-monitoring output.</b> The output current (I <sub>OUT</sub> ) is proportional to the current flowing through the powered device. Place a resistor (R <sub>IMON</sub> ) between the IMON and GND pins to set the output gain. Place a 100nF capacitor close to IMON to filter noise.                                  |
| 21                                                  | SS    | <b>Soft start.</b> Place an external capacitor between the SS and GND pins to set the soft-start time (t <sub>SS</sub> ). The internal circuitry controls the slew rate of the output voltage (V <sub>OUT</sub> ) during start-up.                                                                                              |
| 22                                                  | FAULT | <b>Fault indication.</b> The FAULT pin is an open-drain output. If a fault occurs, then FAULT is pulled low and latches.                                                                                                                                                                                                        |
| 23                                                  | TIMER | <b>Timer setting.</b> An external capacitor sets the insertion delay time, start-up short-current protection (SCP) delay time, over-current protection (OCP) delay time, and auto-retry delay time.                                                                                                                             |
| 24                                                  | CLREF | <b>Current-limit reference voltage input.</b> The CLREF pin sets the reference voltage (V <sub>CLREF</sub> ) for the OCP threshold. Connect a resistor between the CLREF and GND pins, or drive CLREF via an external source to generate V <sub>CLREF</sub> . Place a 1nF to 10nF capacitor close to CLREF to filter the noise. |
| 25                                                  | GND   | <b>Ground.</b>                                                                                                                                                                                                                                                                                                                  |
| 26                                                  | ON    | <b>Power MOSFET enable control.</b> Pull the ON pin high to enable the MP5048A; pull ON low to turn it off.                                                                                                                                                                                                                     |
| 27                                                  | 3V    | <b>Internal 3V LDO output.</b> Place a 2.2μF decoupling capacitor close to the 3V and GND pins.                                                                                                                                                                                                                                 |
| 28                                                  | VCC   | <b>Internal 4.5V LDO output.</b> Place a 2.2μF decoupling capacitor close to the VCC and GND pins.                                                                                                                                                                                                                              |
| 29                                                  | VTEMP | <b>Junction temperature sense output.</b> The VTEMP pin is the output of the internal temperature sensor.                                                                                                                                                                                                                       |
| 30                                                  | MODE  | <b>Latch or auto-retry mode selection.</b> If the MODE pin is pulled high, then the part latches off if a fault occurs. Pull MODE up to 5V externally or float MODE to have the part operate in latch mode. Pull MODE low externally to have the part operate in auto-retry mode.                                               |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                     |                 |
|---------------------------------------------------------------------|-----------------|
| V <sub>IN</sub> (DC).....                                           | -0.3V to +65V   |
| V <sub>IN</sub> (25ns) .....                                        | 72V             |
| V <sub>OUT</sub> .....                                              | -0.3V to +65V   |
| All other pins .....                                                | -0.3V to +6.5V  |
| Continuous power dissipation (T <sub>A</sub> = 25°C) <sup>(2)</sup> |                 |
| .....                                                               | 5.58W           |
| Junction temperature .....                                          | 150°C           |
| Lead temperature .....                                              | 260°C           |
| Storage temperature .....                                           | -65°C to +155°C |

## Recommended Operating Conditions <sup>(3)</sup>

|                                                |                 |
|------------------------------------------------|-----------------|
| Input voltage (V <sub>IN</sub> ) .....         | 24V to 60V      |
| Operating junction temp (T <sub>J</sub> ) .... | -40°C to +125°C |

| Thermal Resistance <sup>(4)</sup> | θ <sub>JA</sub> | θ <sub>JC</sub> |
|-----------------------------------|-----------------|-----------------|
| QFN-30 (5mmx5mm).....             | 22.4.....       | 9.6..°C/W       |

### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX) - T<sub>A</sub>) / θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub> = 48V, R<sub>CS</sub> = 2.2kΩ, C<sub>OUT</sub> = 470μF, T<sub>J</sub> = 25°C, unless otherwise noted.

| Parameters                                                                       | Symbol                      | Condition                                          | Min  | Typ  | Max  | Units |
|----------------------------------------------------------------------------------|-----------------------------|----------------------------------------------------|------|------|------|-------|
| Supply Current                                                                   |                             |                                                    |      |      |      |       |
| Quiescent current                                                                | I <sub>Q</sub>              | ON is pulled high, no load                         |      | 2.4  | 3    | mA    |
|                                                                                  |                             | V <sub>ON</sub> = 0V                               |      | 1.8  | 2.4  | mA    |
| VCC Regulator and Under-Voltage Lockout (UVLO) Protection                        |                             |                                                    |      |      |      |       |
| VCC regulator voltage                                                            | V <sub>CC</sub>             |                                                    | 4.45 | 4.6  | 4.75 | V     |
| VCC load regulation                                                              |                             | I <sub>CC</sub> = 10mA                             |      | 5    |      | %     |
| VCC UVLO rising threshold                                                        | V <sub>CC_UVLO_RISING</sub> |                                                    | 3.5  | 3.65 | 3.8  | V     |
| VCC UVLO hysteresis                                                              | V <sub>CC_UVLO_HYS</sub>    |                                                    |      | 380  |      | mV    |
| 3V regulator voltage                                                             | V <sub>3V</sub>             |                                                    | 2.9  | 3    | 3.1  | V     |
| V <sub>IN</sub> Under-Voltage Protection (UVP) and Over-Voltage Protection (OVP) |                             |                                                    |      |      |      |       |
| V <sub>IN</sub> UVP rising threshold                                             | V <sub>IN_UVP_RISING</sub>  | V <sub>CC</sub> = 5V                               |      | 6.2  |      | V     |
| V <sub>IN</sub> UVP falling threshold                                            | V <sub>IN_UVP_FALLING</sub> | V <sub>CC</sub> = 5V                               |      | 5.25 |      | V     |
| V <sub>IN</sub> OVP fault threshold                                              | V <sub>IN_OVP</sub>         | V <sub>ON</sub> = 0V                               |      | 64   |      | V     |
| V <sub>IN</sub> OVP hysteresis                                                   | V <sub>IN_OVP_HYS</sub>     |                                                    |      | 2    |      | V     |
| Power MOSFET                                                                     |                             |                                                    |      |      |      |       |
| On resistance                                                                    | R <sub>DS(ON)</sub>         | T <sub>J</sub> = 25°C                              |      | 14   |      | mΩ    |
|                                                                                  |                             | T <sub>J</sub> = 85°C <sup>(5)</sup>               |      | 18   |      | mΩ    |
| Off state leakage current                                                        | I <sub>OFF</sub>            | V <sub>ON</sub> = 0V                               |      |      | 5    | μA    |
| Maximum continuous output current <sup>(5)</sup>                                 | I <sub>OUT_MAX</sub>        |                                                    |      |      | 5    | A     |
| Thermal Shutdown and Recovery                                                    |                             |                                                    |      |      |      |       |
| Thermal shutdown threshold <sup>(5)</sup>                                        | T <sub>SD</sub>             |                                                    |      | 153  |      | °C    |
| Thermal shutdown hysteresis <sup>(5)</sup>                                       | T <sub>SD_HYS</sub>         | Auto-retry mode only                               |      | 26   |      | °C    |
| Current-Limit Reference Voltage Input (CLREF)                                    |                             |                                                    |      |      |      |       |
| Internal current during normal operation                                         | I <sub>CLREF_NOR</sub>      |                                                    |      | 36   |      | μA    |
| Internal current during soft start (SS)                                          | I <sub>CLREF_SS</sub>       |                                                    |      | 18   |      | μA    |
| Current-Sense Output (CS)                                                        |                             |                                                    |      |      |      |       |
| Current-sense gain accuracy                                                      | G <sub>CS_ACCR</sub>        | 1A ≤ I <sub>OUT</sub> ≤ 4A                         | -2.5 |      | +2.5 | %     |
| Current-sense gain                                                               | G <sub>CS</sub>             |                                                    |      | 144  |      | μA/A  |
| Soft Start (SS)                                                                  |                             |                                                    |      |      |      |       |
| Soft-start pull-up current                                                       | I <sub>SS</sub>             | V <sub>IN</sub> = 48V                              |      | 11.5 |      | μA    |
| Over-Current Protection (OCP) and Short-Circuit Protection (SCP)                 |                             |                                                    |      |      |      |       |
| OCP current limit during normal operation                                        | I <sub>LIMIT_OCP</sub>      | R <sub>CS</sub> = 2.2kΩ, R <sub>CLREF</sub> = 27kΩ |      | 3.1  |      | A     |
| OCP response time <sup>(5)</sup>                                                 | t <sub>OCP_DELAY</sub>      | I <sub>LIMIT_OCP</sub> = 3A                        |      | 10   |      | μs    |
| Short-circuit protection (SCP) current limit <sup>(5)</sup>                      | I <sub>LIMIT_SCP</sub>      | Regardless of R <sub>CS</sub>                      |      | 6.85 |      | A     |
| SCP response time <sup>(5)</sup>                                                 | t <sub>SC</sub>             |                                                    |      | 200  |      | ns    |

## ELECTRICAL CHARACTERISTICS (continued)

V<sub>IN</sub> = 48V, R<sub>ISSET</sub> = 2.2kΩ, C<sub>OUT</sub> = 470μF, T<sub>J</sub> = 25°C, unless otherwise noted.

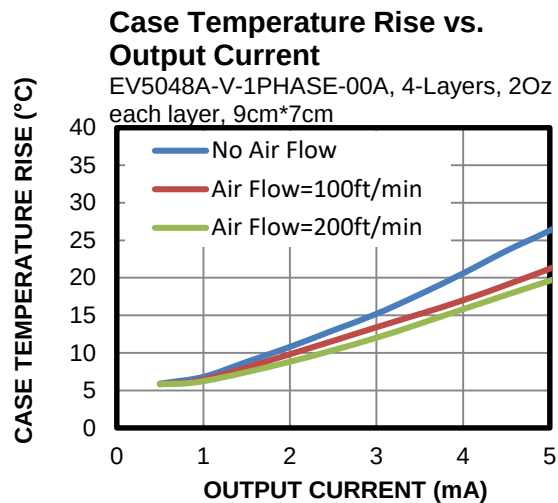
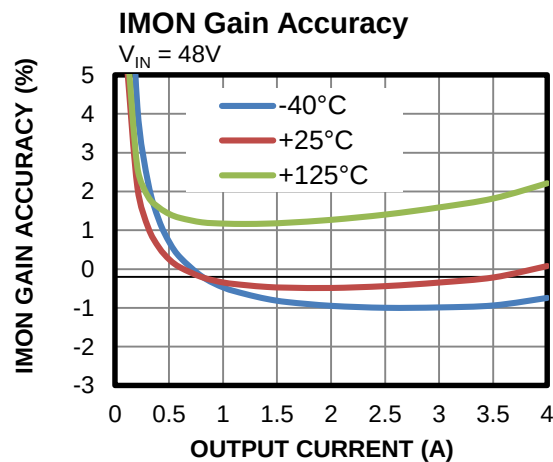
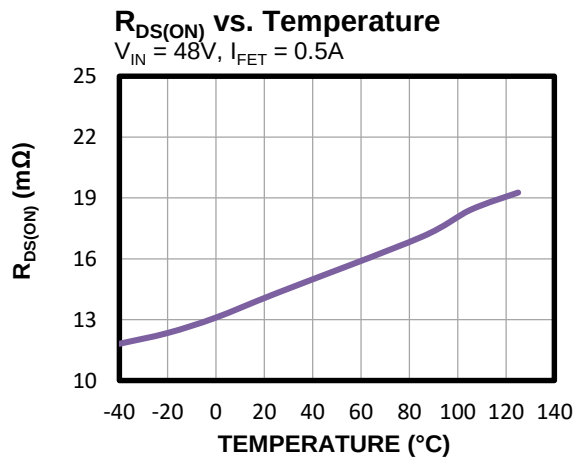
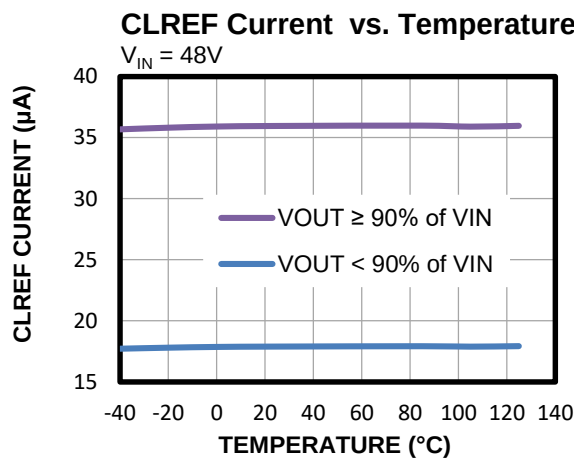
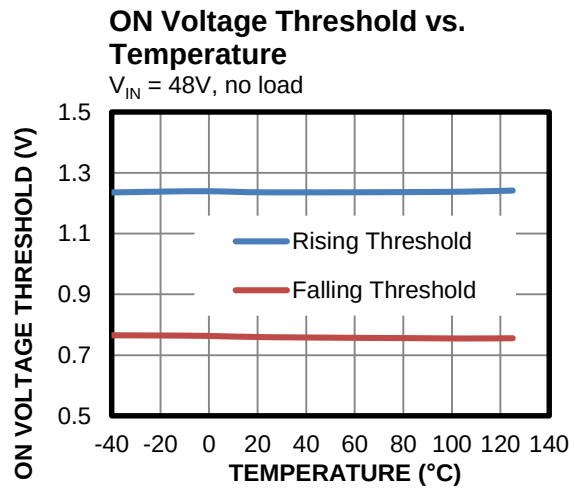
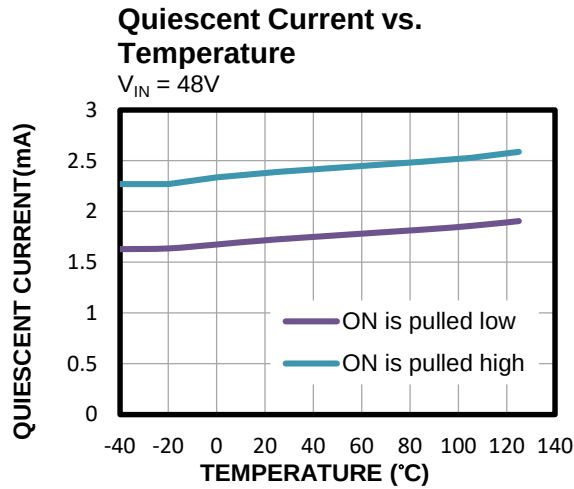
| Parameters                                                   | Symbol                   | Condition                  | Min  | Typ                   | Max  | Units |
|--------------------------------------------------------------|--------------------------|----------------------------|------|-----------------------|------|-------|
| <b>Output Current Monitoring</b>                             |                          |                            |      |                       |      |       |
| I <sub>IMON</sub> / I <sub>OUT</sub> gain                    | G <sub>IMON</sub>        |                            |      | 144                   |      | μA/A  |
| I <sub>IMON</sub> / I <sub>OUT</sub> gain accuracy           | G <sub>IMON_ACCR</sub>   | 1A ≤ I <sub>OUT</sub> ≤ 4A | -1.5 |                       | +1.5 | %     |
| Maximum IMON pin voltage <sup>(5)</sup>                      | V <sub>IMON</sub>        |                            |      |                       | 2    | V     |
| <b>MOSFET Short Detection</b>                                |                          |                            |      |                       |      |       |
| MOSFET drain-to-source short fault flag                      | V <sub>OUT_DSTH</sub>    |                            |      | 0.9 x V <sub>IN</sub> |      | V     |
| Fault release high flag while removing drain-to-source short | V <sub>OUT_FAULTH</sub>  |                            |      | 0.7 x V <sub>IN</sub> |      | V     |
| MOSFET gate-to-source short detection time                   | t <sub>GS_SHRT</sub>     |                            |      | 270                   |      | ms    |
| Maximum soft-start time                                      | t <sub>SS_MAX</sub>      |                            |      | 270                   |      | ms    |
| <b>Power MOSFET Enable Control (ON)</b>                      |                          |                            |      |                       |      |       |
| Rising threshold                                             | V <sub>ON_VTH</sub>      |                            | 1.13 | 1.23                  | 1.31 | V     |
| Hysteresis                                                   | V <sub>ON_HYS</sub>      |                            |      | 450                   |      | mV    |
| <b>Mode Selection (MODE)</b>                                 |                          |                            |      |                       |      |       |
| MODE rising voltage threshold                                | V <sub>MODE_RISING</sub> |                            | 1    | 1.2                   | 1.4  | V     |
| MODE hysteresis                                              | V <sub>MODE_HYS</sub>    |                            |      | 450                   |      | mV    |
| MODE pull-up current                                         | I <sub>MODE_PU</sub>     |                            |      | 4                     |      | μA    |
| <b>Fault</b>                                                 |                          |                            |      |                       |      |       |
| Output low voltage                                           | V <sub>OL_FAULT</sub>    | 1mA sink current           |      |                       | 0.2  | V     |
| Fault off-state leakage current                              | I <sub>FAULT_LKG</sub>   | V <sub>FAULT</sub> = 5V    |      |                       | 5    | μA    |

**Note:**

5) Guaranteed by design.

## TYPICAL CHARACTERISTICS

$V_{IN} = 48V$ ,  $C_{OUT} = 330\mu F$ ,  $R_{CS} = R_{IMON} = 2.2k\Omega$ ,  $C_{TIMER} = 10nF$ ,  $T_J = 25^\circ C$ , unless otherwise noted.

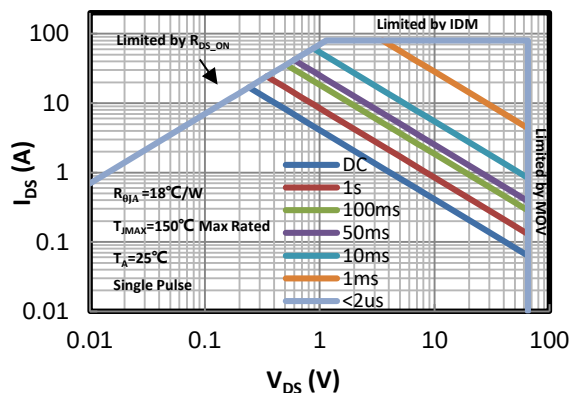


## TYPICAL CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 48V, C<sub>OUT</sub> = 330μF, R<sub>CS</sub> = R<sub>IMON</sub> = 2.2kΩ, C<sub>TIMER</sub> = 10nF, T<sub>J</sub> = 25°C, unless otherwise noted.

### Safe Operating Area (SOA)

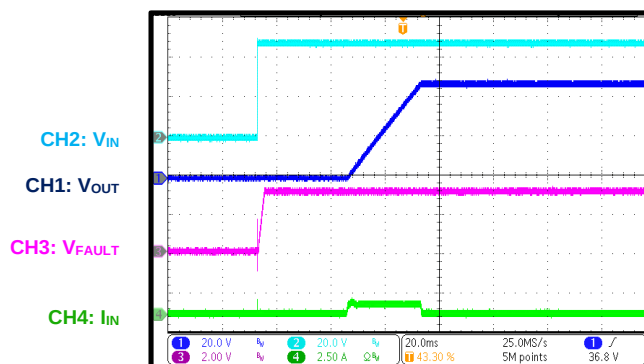
Tested on the EV5048A-V-1PHASE-00A  
(9cmx7cm), 4-layer PCB, 2oz per layer



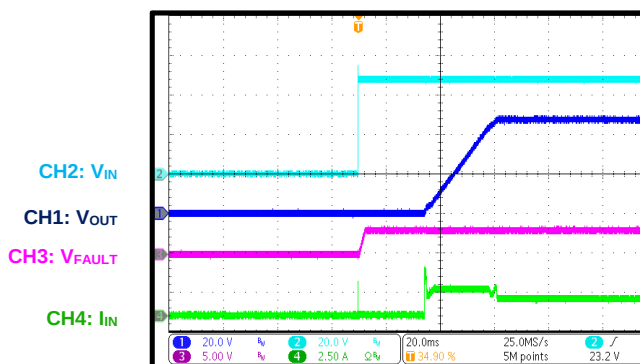
# TYPICAL PERFORMANCE CHARACTERISTICS

V<sub>IN</sub> = 48V, C<sub>OUT</sub> = 330μF, R<sub>CS</sub> = R<sub>IMON</sub> = 2.2kΩ, C<sub>TIMER</sub> = 10nF, T<sub>J</sub> = 25°C, unless otherwise noted.

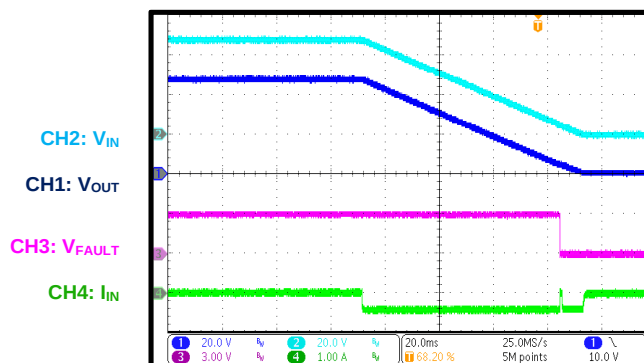
## V<sub>IN</sub> Hot Swap

I<sub>OUT</sub> = 0A


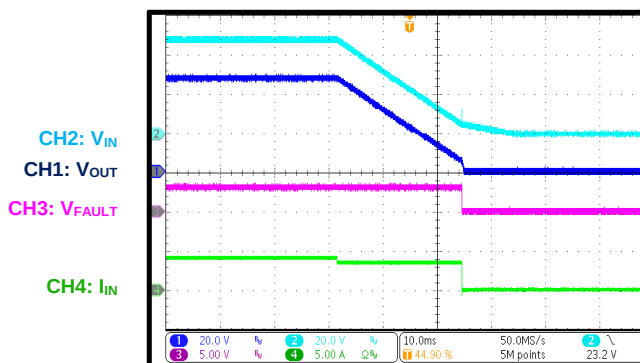
## V<sub>IN</sub> Hot Swap

I<sub>OUT</sub> = 1A


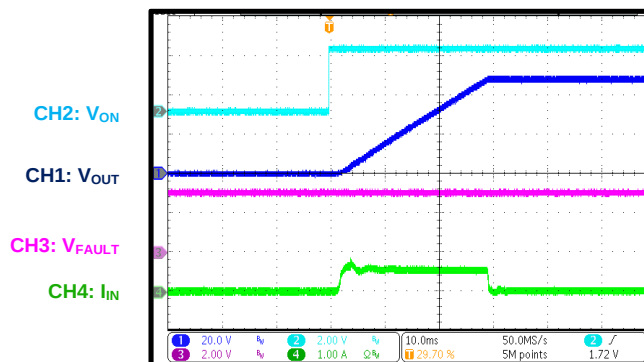
## Shutdown through V<sub>IN</sub>

I<sub>OUT</sub> = 0A


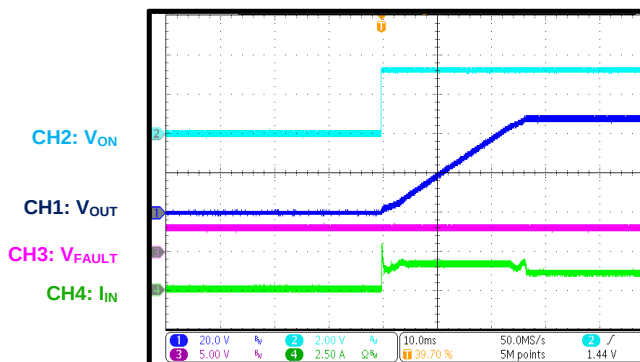
## Shutdown through V<sub>IN</sub>

I<sub>OUT</sub> = 4A


## Start-Up through ON

I<sub>OUT</sub> = 0A


## Start-Up through ON

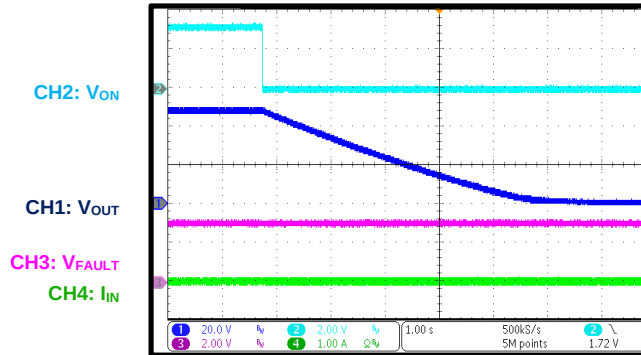
I<sub>OUT</sub> = 1A


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 48V$ ,  $C_{OUT} = 330\mu F$ ,  $R_{CS} = R_{IMON} = 2.2k\Omega$ ,  $C_{TIMER} = 10nF$ ,  $T_J = 25^\circ C$ , unless otherwise noted.

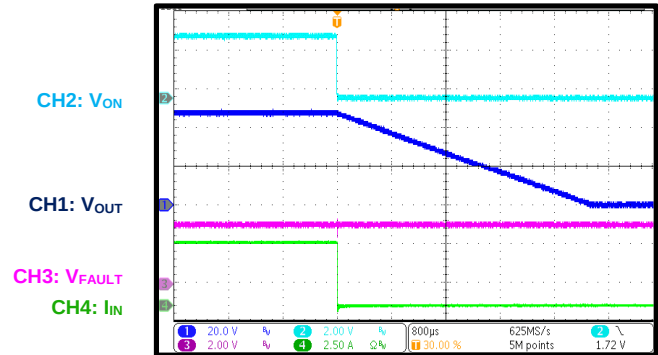
## Shutdown through ON

$I_{OUT} = 0A$



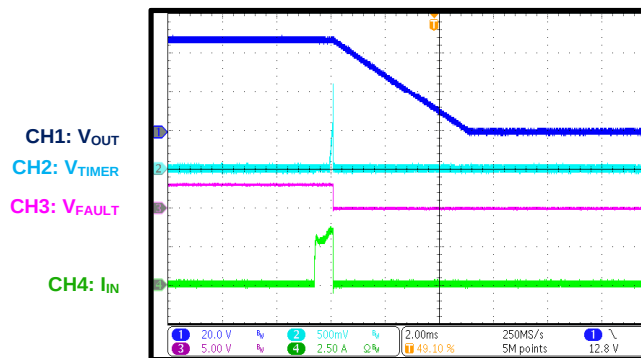
## Shutdown through ON

$I_{OUT} = 4A$



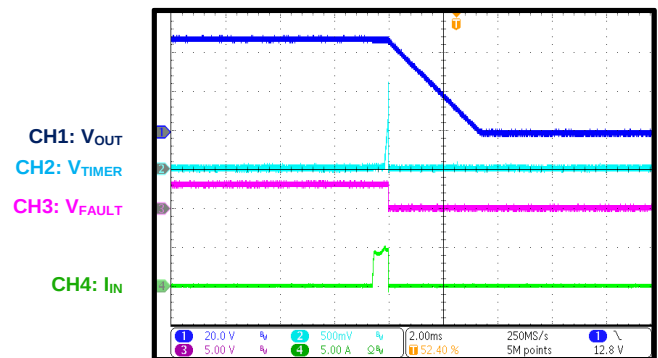
## OCP Entry

$I_{LIMIT\_OCP} = 3A$ , latch mode



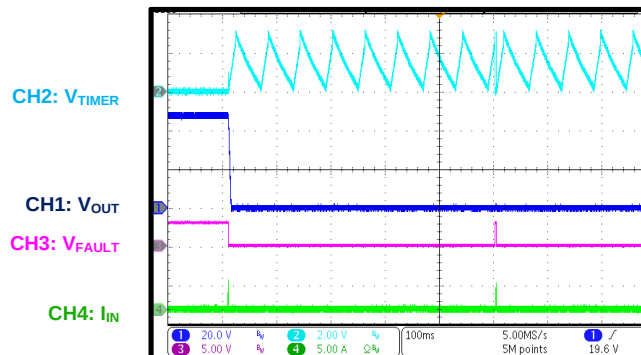
## OCP Entry

$I_{LIMIT\_OCP} = 4.5A$ , latch mode



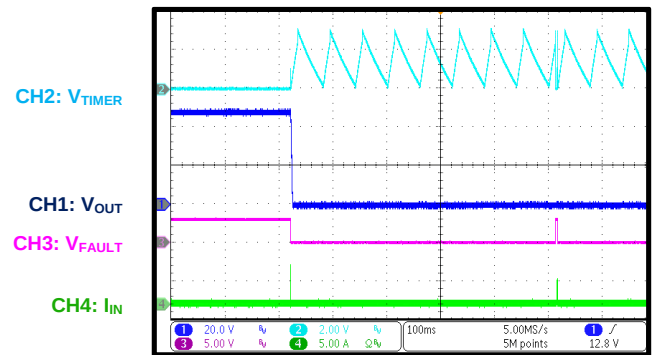
## OCP Entry

$I_{LIMIT\_OCP} = 3A$ , auto-retry mode



## OCP Entry

$I_{LIMIT\_OCP} = 4.5A$ , auto-retry mode

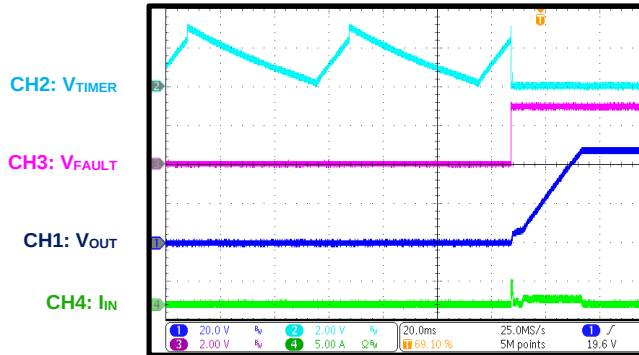


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 48V, C<sub>OUT</sub> = 330μF, R<sub>CS</sub> = R<sub>IMON</sub> = 2.2kΩ, C<sub>TIMER</sub> = 10nF, T<sub>J</sub> = 25°C, unless otherwise noted.

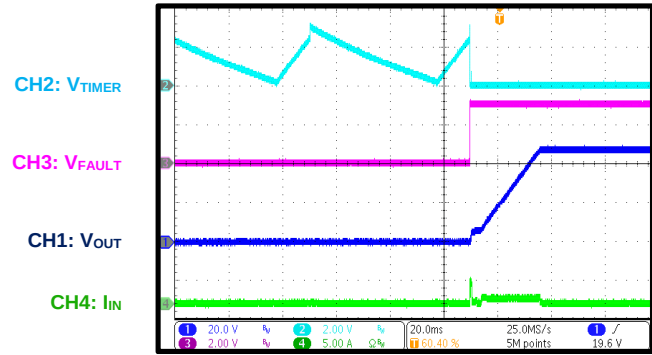
### OCP Recovery

I<sub>LIMIT\_OCP</sub> = 3A, auto-retry mode



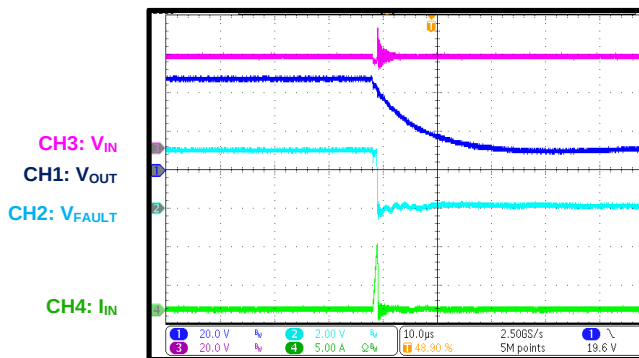
### OCP Recovery

I<sub>LIMIT\_OCP</sub> = 4.5A, auto-retry mode



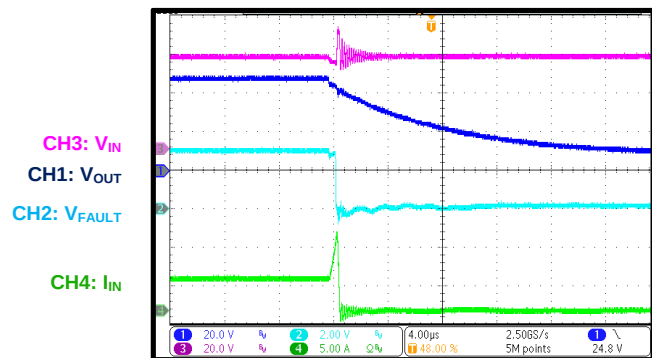
### SCP Entry

Latch mode



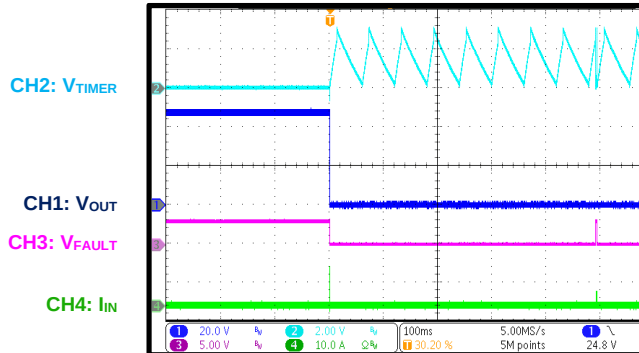
### SCP Entry

I<sub>OUT</sub> = 4A, then short V<sub>OUT</sub> to GND, latch mode



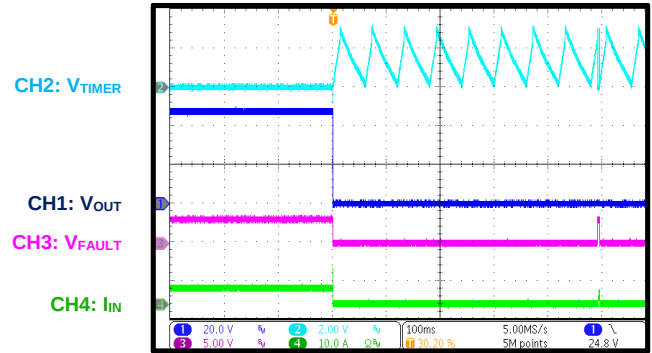
### SCP Entry

Auto-retry mode



### SCP Entry

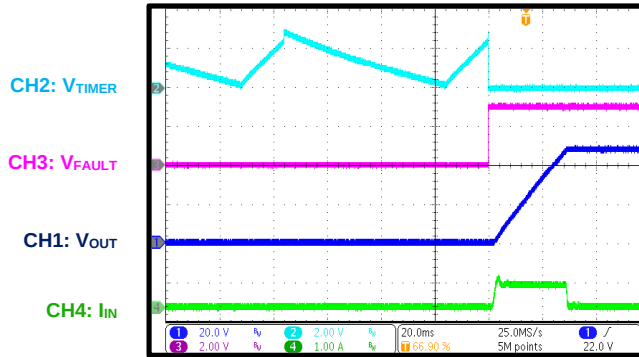
I<sub>OUT</sub> = 4A, then short V<sub>OUT</sub> to GND, auto-retry mode



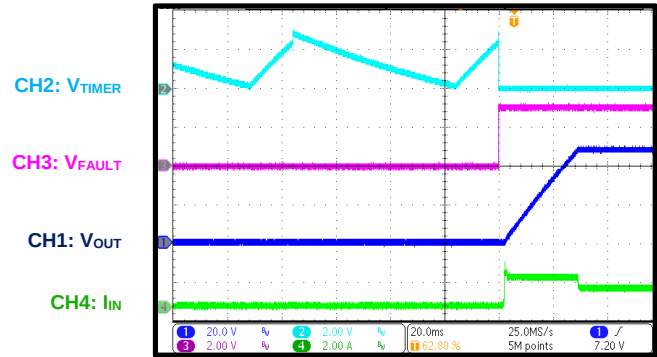
# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V<sub>IN</sub> = 48V, C<sub>OUT</sub> = 330μF, R<sub>CS</sub> = R<sub>IMON</sub> = 2.2kΩ, C<sub>TIMER</sub> = 10nF, T<sub>J</sub> = 25°C, unless otherwise noted.

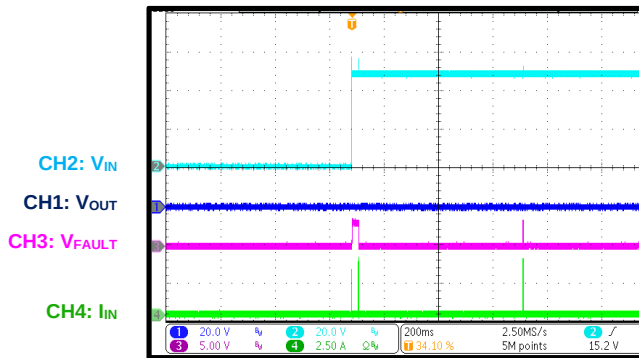
**SCP Recovery**  
Auto-retry mode



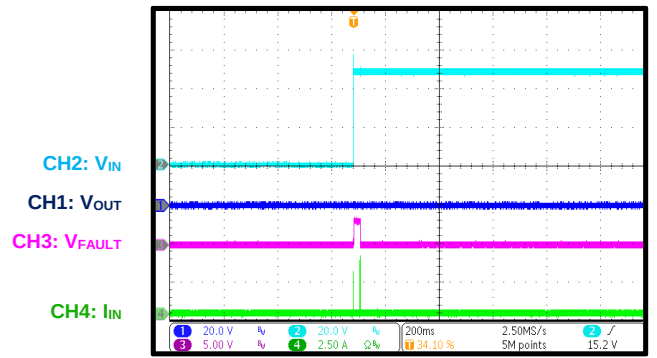
**SCP Recovery**  
I<sub>OUT</sub> = 0.9A, auto-retry mode



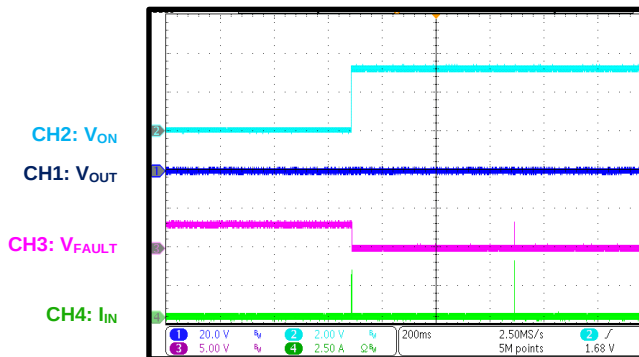
**SCP Start-Up through VIN**  
Auto-retry mode



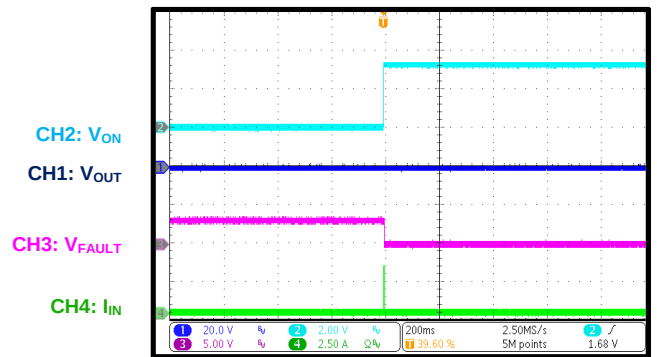
**SCP Start-Up through VIN**  
Latch mode



**SCP Start-Up through ON**  
Auto-retry mode



**SCP Start-Up through ON**  
Latch mode

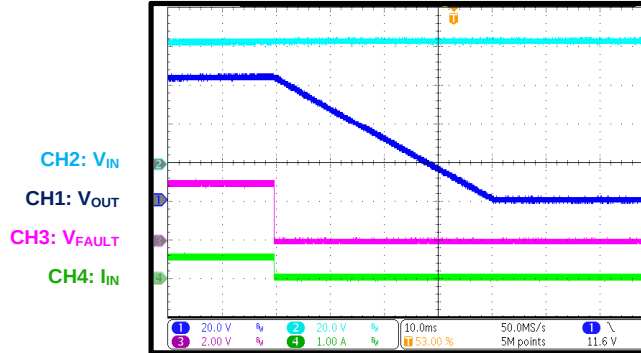


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V<sub>IN</sub> = 48V, C<sub>OUT</sub> = 330μF, R<sub>CS</sub> = R<sub>IMON</sub> = 2.2kΩ, C<sub>TIMER</sub> = 10nF, T<sub>J</sub> = 25°C, unless otherwise noted.

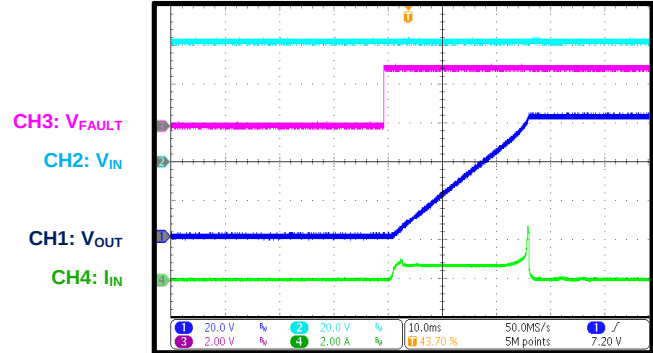
### V<sub>IN</sub> OVP Shutdown

I<sub>OUT</sub> = 0.5A, apply 64V to the VIN pin



### V<sub>IN</sub> OVP Recovery

Auto-retry mode, OVP has been triggered, then V<sub>IN</sub> is reduced



# FUNCTIONAL BLOCK DIAGRAM

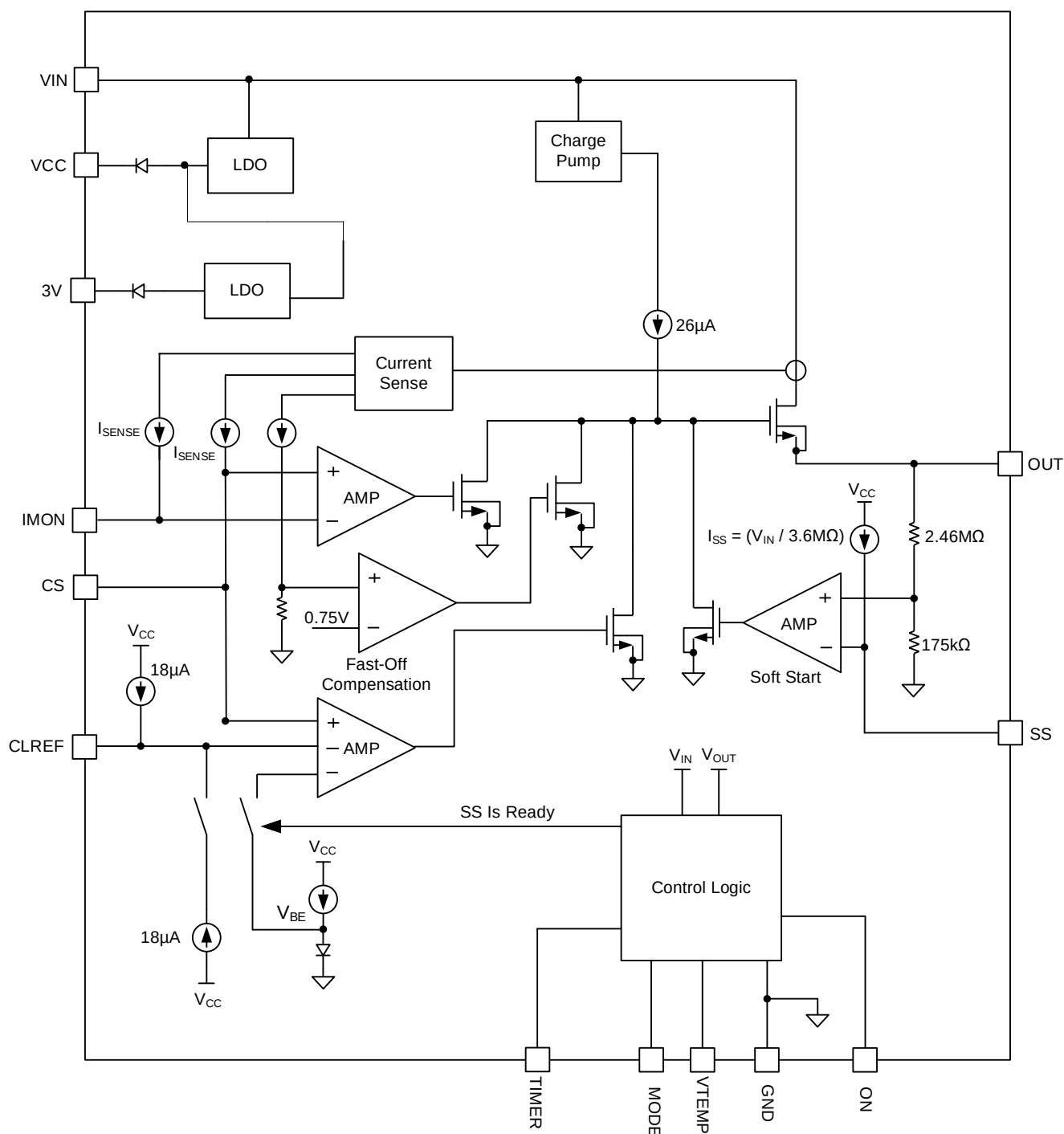


Figure 5: Functional Block Diagram

## OPERATION

The MP5048A is a monolithic, integrated controller and switch. It has a power MOSFET with a 14mΩ on resistance ( $R_{DS(ON)}$ ), which makes it ideal for multi-fuse hot-swap or e-fuse applications. The MP5048A as a standalone device, or it can be sequenced with the hot-swap controller (e.g. the MP5920 or MP5922). Multiple MP5048A devices can be used in parallel to support all power levels required by the system. All devices operating in parallel actively share current during soft start (SS). This distributes the load current ( $I_{LOAD}$ ) evenly during SS. The MP5048A supports 4A of continuous output current ( $I_{OUT}$ ) per device at room temperature.

The MP5048A provides a controlled start-up voltage, and limits the inrush current when a circuit card is inserted into an active power source. The MP5048A provides support for e-fuse and hot-swap applications. It integrates a power MOSFET, temperature sensing, current monitoring, current protection, temperature protection, and power sequencing into a single device. The MP5048A monitors the current flowing through the device, as well as the die temperature, eliminating the need for an external sense resistor and thermal sensing.

### Start-Up Sequence

The MP5048A has two operation modes. It can be controlled by a hot-swap controller, or can act as a standalone device.

If the MP5048A is controlled by a hot-swap controller, then the power MOSFET remains off until the ON pin is pulled high.

A capacitor on the timer pin ( $C_{TIMER}$ ) sets the insertion delay time, start-up short-circuit protection (SCP) delay time, over-current protection (OCP) delay time, and auto-retry delay time. The insertion delay time starts once  $V_{IN}$  exceeds the under-voltage lockout (UVLO) threshold. Once the ON pin is pulled high and the insertion delay time is finished, the power MOSFET is charged up via the internal charge pump. Once the power MOSFET's voltage ( $V_{GS}$ ) reaches its threshold ( $V_{GSTH}$ ), the output voltage ( $V_{OUT}$ ) rises (see Figure 6).

$V_{OUT}$  rises according to the the soft-start slew rate. The rise time is determined by the soft-start capacitor ( $C_{SS}$ ).

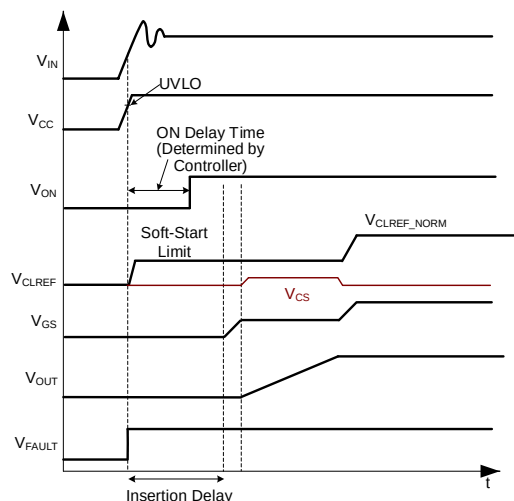


**Figure 6: Start-Up while the MP5048A is Controlled by Hot-Swap Controller**

During SS, the current limit ( $I_{LIMIT}$ ) is reduced via the internal soft-start limit ( $V_{SS\_LIMIT}$ ). Once SS is complete,  $I_{LIMIT}$  increases to the full-scale  $I_{LIMIT}$  set by the CLREF resistor ( $R_{CLREF}$ ).

The ON pin is low by default since it is pulled to GND internally via a 1.1MΩ resistor. If the MP5048A is operating in standalone mode, the ON pin should be pulled up externally to the VCC voltage ( $V_{CC}$ ) (see Figure 7).

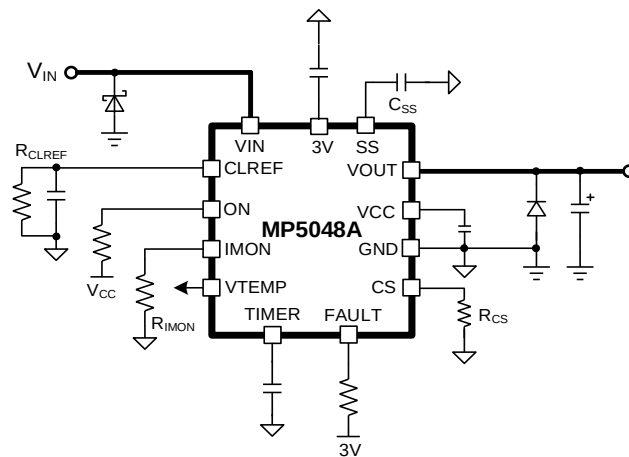


**Figure 7: Standalone Operation**

If the ON voltage ( $V_{ON}$ ) exceeds its rising threshold while the insertion delay time finishes, the power MOSFET is charged up via the internal current source (26μA). The power MOSFET turns on once  $V_{GS}$  reaches  $V_{GSTH}$ , and  $V_{OUT}$  rises (see Figure 8 on page 18).

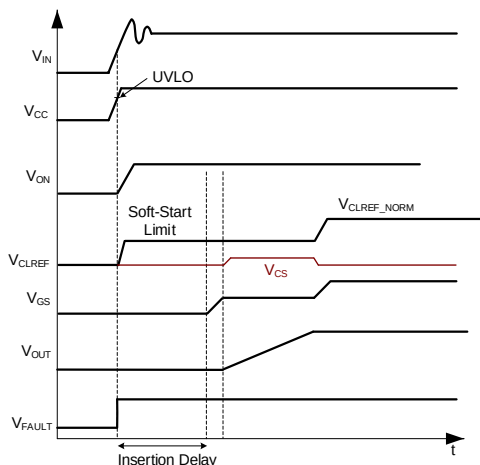


**Figure 8: Start-Up during Standalone Operation**

### Soft Start (SS)

The soft-start capacitor ( $C_{SS}$ ) determines the soft-start time ( $t_{SS}$ ). Once the ON pin is pulled high and the insertion delay time finishes, a constant-current source proportional to the input voltage ( $V_{IN}$ ) charges the soft-start voltage ( $V_{SS}$ ).  $V_{OUT}$  rises at a similar slew rate to  $V_{SS}$ .

$C_{SS}$  can be calculated with Equation (1):

$$C_{SS}(\text{nF}) = \frac{15 \times t_{SS}(\text{mS})}{R_{SS}} \quad (1)$$

Where  $R_{SS}$  is the soft-start resistor (3.6MΩ).

For example, a 100nF capacitor provides a  $t_{SS}$  of 24ms. If the load capacitance is extremely large, then the current required to maintain the preset  $t_{SS}$  exceeds the start-up  $I_{LIMIT}$ . In this case, the rise time is controlled by the load capacitor ( $C_{LOAD}$ ) and the start-up  $I_{LIMIT}$ . Float the SS pin to generate a fast slew rate.

A current source (26μA) pulls up the power MOSFET gate. The gate charge current controls the  $V_{OUT}$  rise time. The minimum  $t_{SS}$  is 1.5ms.

If the MP5048A is used in multi-phase application, all of the SS pins should be connected together. This ensures that all of the devices have the same  $t_{SS}$ .

If a fault occurs, then the FAULT and SS pins are pulled low. If the MP5048A is set to auto-retry mode, then the SS pin is held low until the auto-retry delay time has expired. Once the auto-retry

delay time finishes, the MP5048A turns on the MOSFET, and initiates an SS to resume normal operation.

### TIMER Pin

The TIMER pin has four functions, listed below:

1. Sets the insertion delay time
2. Sets the SCP start-up delay timer
3. Sets the OCP delay time
4. Sets the auto-retry delay time

### Insertion Delay Time

Once the MP5048A's completes the internal power-on reset (POR), then the insertion delay begins by charging the capacitor with a 2μA current source. If the voltage reaches its threshold, then the TIMER pin is pulled up via an internal 4V source for 3.5μs. Then it is pulled to GND for 7.5μs. The timer repeats this, and then the insertion delay time is completed (see Figure 9).

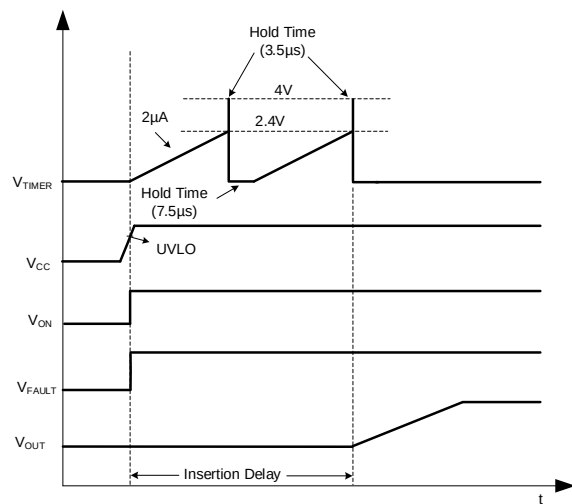


**Figure 9: MP5048A Insertion Delay Time**

The pull-up voltage is determined by the external TIMER capacitor ( $C_{TIMER}$ ).

### Start-Up SCP Delay Time

If  $V_{OUT}$  is below 20% of  $V_{IN}$  during start-up, and  $V_{GS}$  is regulated by  $V_{SS\_LIMIT}$ , then the SCP start-up delay timer starts. Once the SCP start-up delay timer is complete, then the power MOSFET turns off and the FAULT pin is pulled low (see Figure 10 on page 19).

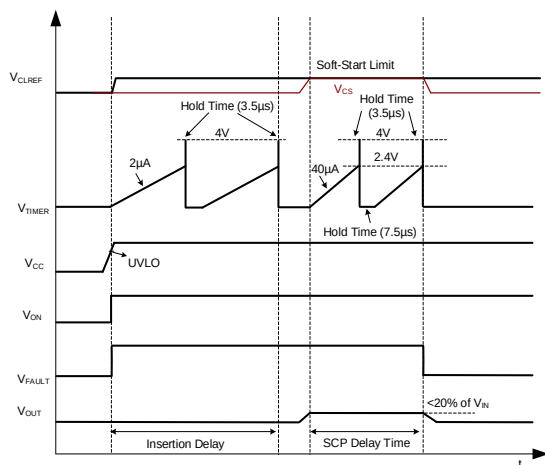


**Figure 10: SCP Delay Time**

If no fault occurs, then the MP5048A follows the normal start-up sequence, and  $V_{OUT}$  rises according to the  $V_{SS}$ .

### OCP Delay Time

An over-current (OC) fault occurs if the current flowing through the MP5048A exceeds the configured threshold, and is held for the duration of the OCP delay time.

If  $V_{CS}$  exceeds the CLREF voltage ( $V_{CLREF}$ ), then a 40μA current source charges  $C_{TIMER}$ . If the TIMER voltage ( $V_{TIMER}$ ) exceeds the trip threshold (0.6V), then the power MOSFET turns off and the FAULT pin is pulled low to indicate an OC fault has occurred (see Figure 11).

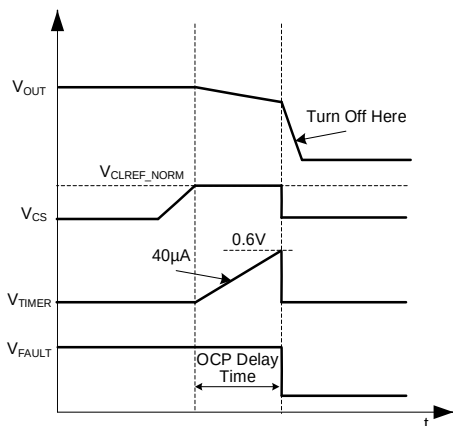


**Figure 11: OCP Delay Time**

The OCP delay time can be adjusted so that the the system can endure a current transient without forcing a shutdown. A current transient

can cause a current that exceeds the OCP threshold for a small amount of time. Adjusting the timer can accommodate this brief OC fault.

### Auto-Retry Delay Time

The FAULT pin is pulled low to indicate a fault has occurred. If the MODE pin is configured for auto-retry mode, then the MP5048A charges and discharges the TIMER pin nine times using the same rates as the insertion delay. After the ninth cycle, the MP5048A automatically retries a start-up sequence (see Figure 12).

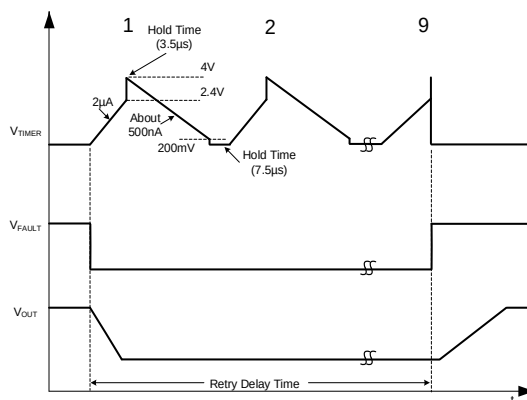


**Figure 12: Auto-Retry**

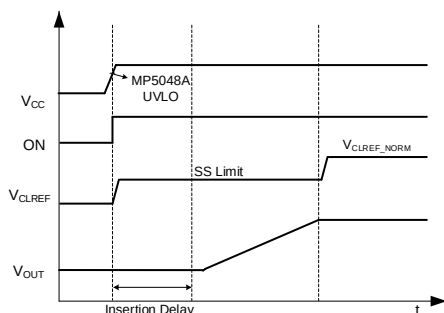
### Over-Current Protection (OCP)

$I_{LOAD}$  is limited by the current-limit reference input and the external current-sense resistor ( $R_{CS}$ ). The CS voltage ( $V_{CS}$ ) is compared to the  $I_{LIMIT}$  reference via an amplifier to regulate the power MOSFET's gate voltage ( $V_{GATE}$ ). This prevents the Intelli-Fuse current from exceeding the  $I_{LIMIT}$  defined by the reference.

The current-limit reference voltage ( $V_{REF}$ ) is set via CLREF, which is clamped low internally during SS to set a low  $I_{LIMIT}$ . Once  $V_{OUT}$  reaches  $V_{IN}$ , the  $I_{LIMIT}$  reference can be increased to the full  $I_{LIMIT}$  set by  $V_{CLREF}$ . At this point, the power MOSFET gate is fully enhanced, and the e-fuse is ready to deliver full power from the input.

### Current Limit at Start-Up

To protect the MP5048A from overheating during start-up, the internal maximum current-limit clamp voltage and CS limit reference configuration current are determined by  $V_{IN}$  and  $V_{OUT}$  (see Figure 13 on page 20).

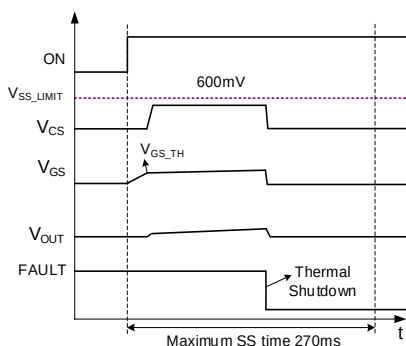

**Figure 13: MP5048A SS Current Limit**

If  $V_{OUT}$  is below 90% of  $V_{IN}$ , then the maximum current-limit reference is clamped to the CLREF clamp voltage ( $V_{CLREF\_CLAMP}$ ) (660mV with a negative temperature coefficient), and the thermal shutdown threshold is 153°C.

The CS current-limit reference configuration current is 18μA if  $V_{OUT}$  is below 90% of  $V_{IN}$ , and  $V_{CLREF}$  is determined by the external CLREF resistor ( $R_{CLREF}$ ). If  $V_{CLREF}$  is below  $V_{CLREF\_CLAMP}$ , then the actual current-limit  $V_{REF}$  is determined by the external  $V_{CLREF}$ . Otherwise,  $V_{REF}$  is determined by  $V_{CLREF\_CLAMP}$ .

If  $V_{OUT} \geq 90\%$  of  $V_{IN}$ , then  $V_{CLREF\_CLAMP}$  (660mV) is disabled. The CS current-limit reference configuration current is between 18μA and 36μA (18μA + 18μA), and CS is limited by the CLREF's externally configured value (typically limited to 2V).

If the power MOSFET remains on while  $V_{OUT}$  is below 90% of  $V_{IN}$  within the maximum  $t_{SS}$  ( $t_{SS\_MAX}$ ), then the power MOSFET shuts down once the  $t_{SS\_MAX}$  (270ms) finishes. If  $I_{LOAD}$  is high (but lower than  $V_{SS\_LIMIT}$ ), then the power MOSFET start-up instantaneous loss is large. Thermal shutdown is triggered before  $t_{SS}$  is complete, and FAULT is pulled low (see Figure 14).


**Figure 14: Failed Start-Up within 270ms**

If  $V_{OUT}$  is below 20% of  $V_{IN}$  during start-up, and  $V_{GS}$  is regulated by  $V_{SS\_LIMIT}$  for the start-up SCP delay time, then the power MOSFET latches off, and FAULT is pulled low.

### Current Limit during Normal Operation

Once the MP5048A detects that start-up is complete, the part enters normal operation.

Once  $V_{CS}$  (configured by an external resistor) exceeds the normal CLREF threshold during normal operation, the internal circuit regulates  $V_{GATE}$  to keep the power MOSFET constant. To limit the current, the gate-to-source voltage ( $V_{GS}$ ) should be regulated between 5V and  $V_{TH}$ . The typical response time is about 10s.  $I_{OUT}$  may have a small overshoot during this period.

If  $I_{LIMIT}$  is reached, then the internal fault timer starts. If  $I_{OUT}$  drops below the  $I_{LIMIT}$  threshold before the end of OCP delay time, then the MP5048A resumes normal operation. If  $I_{OUT}$  exceeds  $I_{LIMIT}$  for longer than the delay time, then the power MOSFET latches off and the FAULT pin is pulled low.

The desired  $I_{LIMIT}$  during normal operation is a function of the CS pin's external resistor ( $R_{CS}$ ).

The MP5048A  $I_{LIMIT}$  value can exceed the normal maximum load current ( $I_{LOAD}$ ) to allow for tolerances in the current-sense value.  $I_{LIMIT}$  can be estimated with Equation (2):

$$I_{LIMIT} = \frac{V_{CLREF\_NORM}}{G_{CS} \times R_{CS}} \quad (2)$$

Where  $V_{CLREF\_NORM}$  is the CLREF voltage during normal operation, and  $G_{CS}$  is the current-sense gain once the power MOSFET is fully on (typically 144μA/A). The OCP limit should not exceed 4.8A.

The MOSFET works in the linear region.

### Short-Circuit Protection (SCP)

If  $I_{LOAD}$  increases rapidly due to a short circuit, then the current may exceed the  $I_{LIMIT}$  threshold before the hot-swap control loop can respond. If the Intelli-Fuse current reaches 6.85A, then a fast turn-off circuit in the Intelli-Fuse is activated to turn the power MOSFET off. The total SCP response time is about 200ns. The FAULT signal is pulled low once the power MOSFET's current reaches the  $I_{LIMIT}$  (6.85A).

If the device is in latch mode, then there is not a retry response after short-circuit detection. The FAULT pin remains low and the device remains off. To clear the fault, pull the ON pin low and then high. This clears the fault condition, and the MP5048A initiates a new SS. If the short circuit is still present, the device repeats this process. Once the short circuit is removed, the MP5048A ramps up  $V_{OUT}$  according to  $V_{SS}$ .

If the device is in auto-retry mode, then the retry timer counts nine cycles on the TIMER pin (see Figure 12 on page 19). At the end of the retry timer count, the MP5048A attempts to start up again. If the short is still present, the process continues at the rate of the retry timer for the auto-retry process. If the short has been removed, then the MP5048A ramps up  $V_{OUT}$  according to  $V_{SS}$ .

### FAULT Report

FAULT is an open-drain, active-low signal to report fault conditions. FAULT monitors the following faults in the Intelli-Fuse:

1. **Over-current (OC) fault:** If the CS voltage exceeds  $V_{CS}$  the CLREF threshold during normal operation, then FAULT is pulled low after a configured gate regulation time.
2. **Short circuit:** If the Intelli-Fuse's  $I_{LOAD}$  reaches 6.85A quickly, then FAULT is pulled low.
3. **Intelli-Fuse's power MOSFET drain-to-source, gate-to-drain, or gate-to-source short detection:** See the Damaged Intelli-Fuse MOSFET Detection section for more details.
4. **Over-temperature (OT) fault:** If an OT fault is detected ( $T_J > 153^{\circ}\text{C}$ ), FAULT is pulled low.

If a fault latch occurs, then FAULT is pulled low. The latch can be released by cycling the power on VIN or ON.

### Damaged Intelli-Fuse MOSFET Detection

Damaged Intelli-Fuse power MOSFET detection includes MOSFET drain-to-source, gate-to-drain, and gate-to-source short detection. These conditions are described below.

#### **Drain-to-Source Short Detection during Start-Up**

Once  $V_{CC}$  on the Intelli-Fuse exceeds its under-voltage lockout (UVLO) rising threshold, and  $V_{ON}$  exceeds its rising threshold, then the Intelli-Fuse

detects the drain-to-source short after the insertion delay ends. In this instance, the Intelli-Fuse treats any  $V_{OUT}$  above 90% of  $V_{IN}$  during start-up as a short on the MOSFET. FAULT remains low while the Intelli-Fuse detects that  $V_{OUT}$  has exceeded 90% of  $V_{IN}$  during start up. Once the short is removed and the Intelli-Fuse detects that  $V_{OUT}$  has dropped below 70% of  $V_{IN}$ , FAULT is pulled high, and the MP5048A starts up and resumes normal operation.

#### **Gate-to-Drain Short Detection during Start-Up**

During start-up, the Intelli-Fuse detects a power MOSFET gate-to-drain short by monitoring its drain-to-gate voltage ( $V_{DG}$ ) and  $V_{GS}$ . If  $V_{GS}$  exceeds a fault threshold voltage, or if  $V_{DG}$  drops below the fault threshold, then FAULT is pulled low until the short is removed.

#### **Gate-to-Source Short Detection during Start-Up**

FAULT is pulled low for gate-to-source short detection during the MOSFET turn-on period (if  $V_{OUT}$  is below 90% of  $V_{IN}$  after the maximum internal 270ms soft-start time). To turn the Intelli-Fuse on again, remove the short and cycle the power on VIN or ON.

#### **Gate-to-Source or Gate-to-Drain Short Detection during Normal Operation**

If  $V_{OUT}$  exceeds 90% of  $V_{IN}$  while the part is operating normally, then the Intelli-Fuse detects the power MOSFET gate-to-to-source or gate-drain short by checking if the difference between the internal charge pump voltage ( $V_{CP}$ ) and  $V_{GATE}$  is below 2V after 270ms (if no other fault has occurred). If this occurs, then FAULT is pulled low. To turn the Intelli-Fuse on again, remove the short and cycle the power on VIN or ON.

### FAULT Reset

To restart the part after a fault has occurred, pull the ON pin low and then high. Once the fault is removed, the MP5048A begins the start-up sequence.

### V<sub>IN</sub> Over-Voltage Protection (OVP)

$V_{IN}$  over-voltage protection (OVP) has a fixed limit of 64V. If this level is reached, then the power MOSFET turns off. If the device is set to latch mode, then the fault can be released by cycling the power on VIN or ON. If the device is set to auto-retry mode, then the power MOSFET

does not turn on until V<sub>IN</sub> drops below 62V.

### Under-Voltage Lockout (UVLO) Protection

The UVLO threshold can be configured via a resistor divider connected between the input and the ON pin. The network can be adjusted by setting the start-up voltage via the VIN pin.

### Current-Sense Output (CS)

The CS pin provides a current proportional to I<sub>OUT</sub> (the current through the powered device). The current-sense gain is 144μA/A once the power MOSFET is fully on. There is a resistor (R<sub>CS</sub>) connected to CS that forms an external voltage. The CS current (I<sub>CS</sub>) can be estimated with Equation (3):

$$I_{CS} = I_{OUT} \times 144\mu A/A \quad (3)$$

The CS reference voltage (V<sub>CS</sub>) can be calculated with Equation (4):

$$V_{CS} = I_{CS} \times R_{CS} \quad (4)$$

If V<sub>CS</sub> reaches the CLREF I<sub>LIMIT</sub> threshold, then the internal circuit regulates V<sub>GATE</sub> to keep the current in the power MOSFET constant.

### Current-Monitoring Output (IMON)

The current monitor gain is 144μA/A. There is a resistor (R<sub>IMON</sub>) connected between the IMON and GND pins. The IMON voltage (V<sub>IMON</sub>) should be between 0V and 2V to keep IMON's current (I<sub>IMON</sub>) linearly proportional to I<sub>OUT</sub>. I<sub>IMON</sub> can be calculated with Equation (5):

$$I_{IMON} = I_{OUT} \times 144\mu A/A \quad (5)$$

The IMON reference voltage (V<sub>IMON</sub>) can be estimated with Equation (6):

$$V_{IMON} = I_{IMON} \times R_{IMON} \quad (6)$$

The MP5048A current-monitoring output can be used by the controller to accurately monitor the I<sub>OUT</sub>. Place a 100nF capacitor between the IMON and GND pins to smooth the indicator voltage.

### Temperature-Sense Output (VTEMP)

The VTEMP pin reports the junction temperature (T<sub>J</sub>) when there is no thermal gradient on the IC. If V<sub>CC</sub> exceeds its UVLO threshold and the MP5048A is in active mode, then VTEMP has a voltage output proportional to T<sub>J</sub>. The VTEMP

voltage (V<sub>TEMP</sub>) is 11.8mV/°C, which can be calculated with Equation (7):

$$V_{TEMP} = (T_J \times 11.8 + 100)mV \quad (7)$$

For example, if T<sub>J</sub> is 100°C, then V<sub>TEMP</sub> is about 1.3V. If V<sub>TEMP</sub> is 0V, then T<sub>J</sub> is about -8°C. The total temperature-sense range is between -8°C and +150°C. If T<sub>J</sub> drops below -8°C, then V<sub>TEMP</sub> remains at 0V.

In multi-fuse operation, the VTEMP pins of each Intelli-Fuse can be connected to the temperature monitor pin of the controller (see Figure 15).

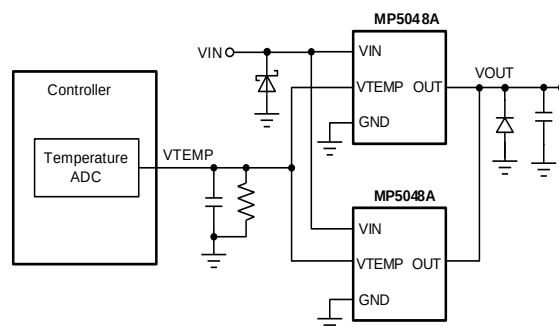


**Figure 15: Multi-Fuse Temperature-Sense Utilization during Parallel Operation**

### Current Balancing during Parallel Operation

Multiple MP5048A devices can be used in parallel for high-current applications. The current balance loop balances the start-up current per active channel. All IMON pins should be connected together for current balancing in parallel operation.

The sensed currents from each active MP5048A's IMON are summed together and divided by the number of active channels. The resulting average I<sub>LOAD</sub> provides a measure of the total I<sub>LOAD</sub>.

Current balancing is achieved by comparing the sensed current of each CS pin to the average current, which makes an appropriate adjustment to the power MOSFET V<sub>GATE</sub> of each Intelli-Fuse during start-up. The equivalent average IMON resistor (R<sub>IMON</sub>) can be calculated with Equation (8):

$$R_{IMON\_AVG} = R_{CS} / N \quad (8)$$

Where N is the number of active MP5048A devices (see Figure 16 on page 23).

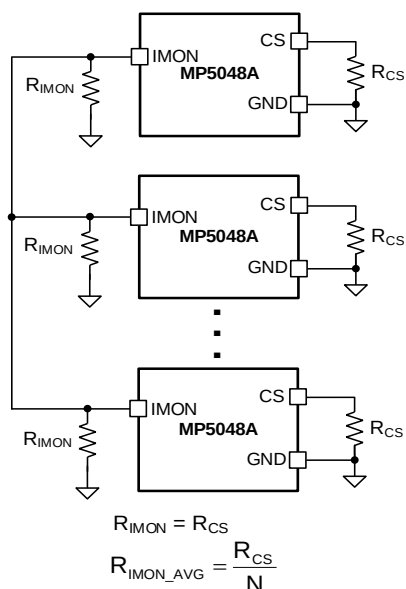


**Figure 16: IMON and CS Connections in Multi-Phase Application**

The start-up current balance is essential to achieving the thermal advantage of parallel

operation. With good current balancing, the power loss is dissipated across multiple devices equally over a greater area.

### MP5048A and MP5920 Controller Operation

The MP5048A can be combined with the MP5920 to provide PMBus telemetry, power sequencing, and black box capabilities (see Figure 17).

Using the internal 3V LDO, the MP5920 can be powered directly by the MP5048A, which allows for power sequencing when only 48V is available. The 3V LDO can be used as a bootstrap source to start up the MP5920; however, it cannot be used for continuous operation. It is expected that a 3.3V source starts up the MP5920 after initial start-up. The 3V LDO can be connected to the main system 3.3V supply via a diode. This disables the current being drawn from the internal 3V LDO, and instead uses the system's 3.3V to power the MP5920.

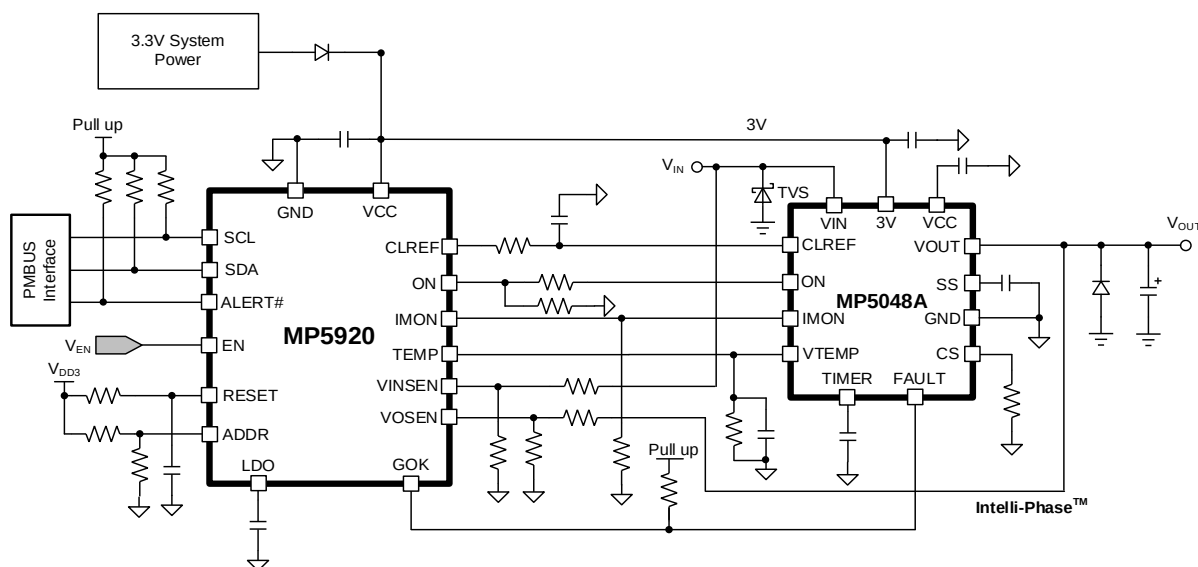


**Figure 17: MP5048A and MP5920 Operation**

## APPLICATION INFORMATION

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 18 and follow the guidelines below:

1. Place the MP5048A close to the board's input connector to minimize trace inductance.
2. Place a small input capacitor (e.g. 100nF) close to the MP5048A's VIN and GND pins to reduce transients on the input supply line. (Transients can occur if I<sub>LOAD</sub> is shut off.)
3. Place a 2.2μF capacitor as close to VCC as possible.
4. Keep the high-current path between the board's input and load close to and in parallel to the return path to reduce loop inductance.
5. Connect the analog signal ground (AGND) plane to the PCB's power ground (PGND) planes at a single point.
6. If the MP5048A is controlled by a hot-swap device, connect the reference ground of all of the signal pins to the reference ground of the controller.

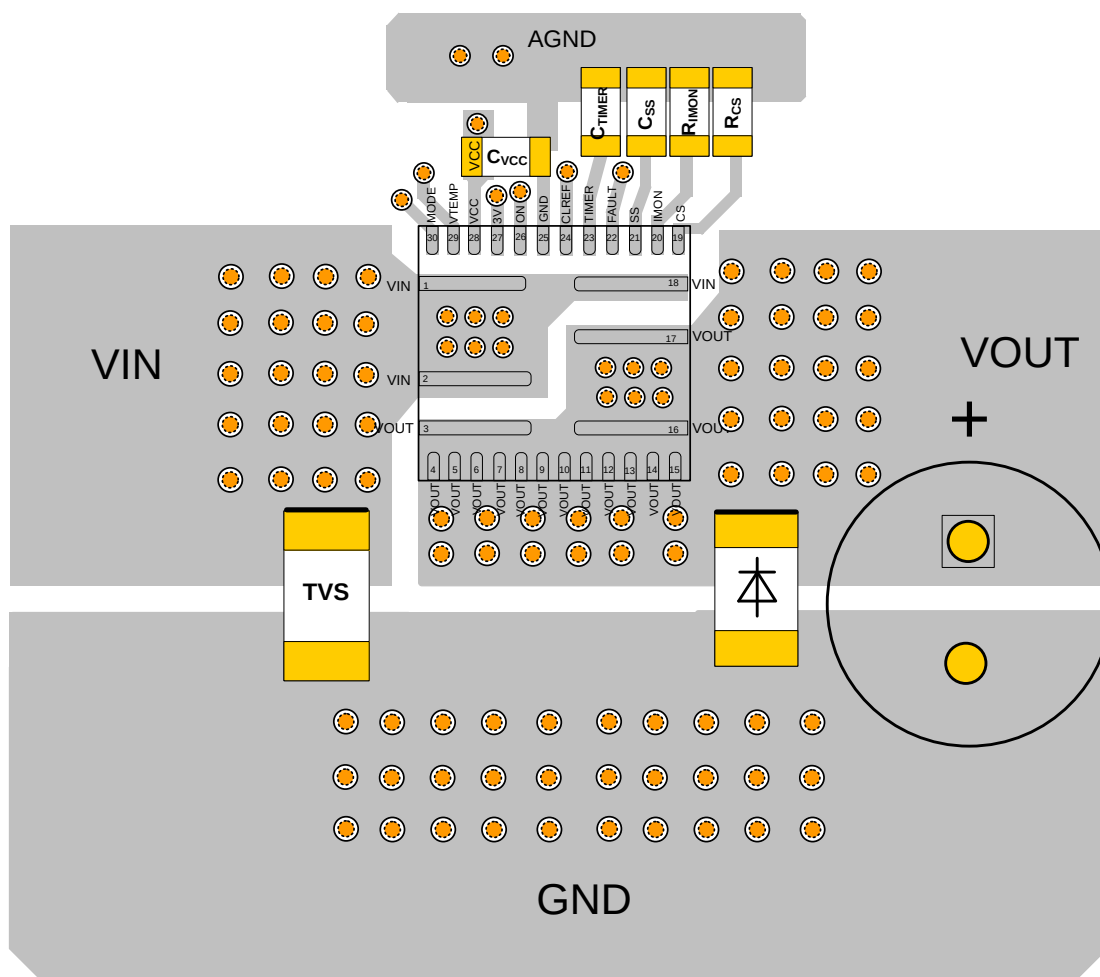


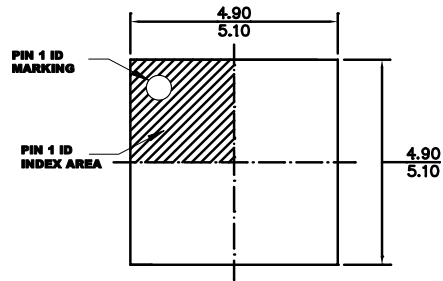
**Figure 18: Recommended PCB Layout**

VIN TVS Diode: 5.0SMDJ51A

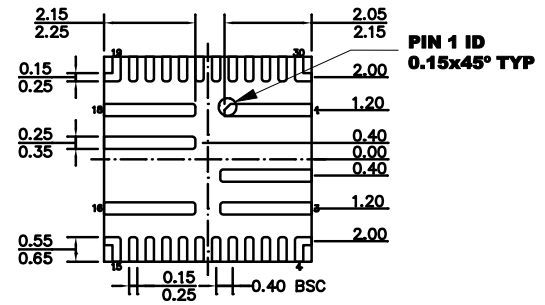
VOUT Diode: B380-13-F

# PACKAGE INFORMATION

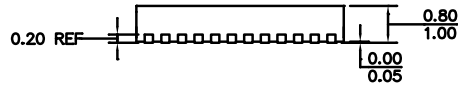
## QFN-30 (5mmx5mm)



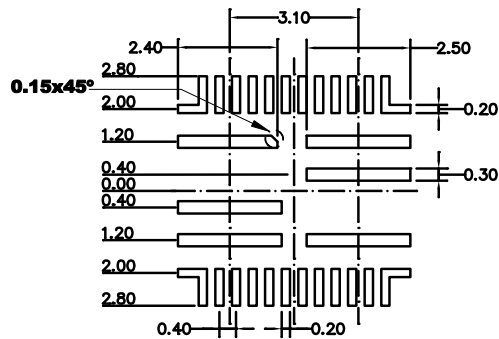
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

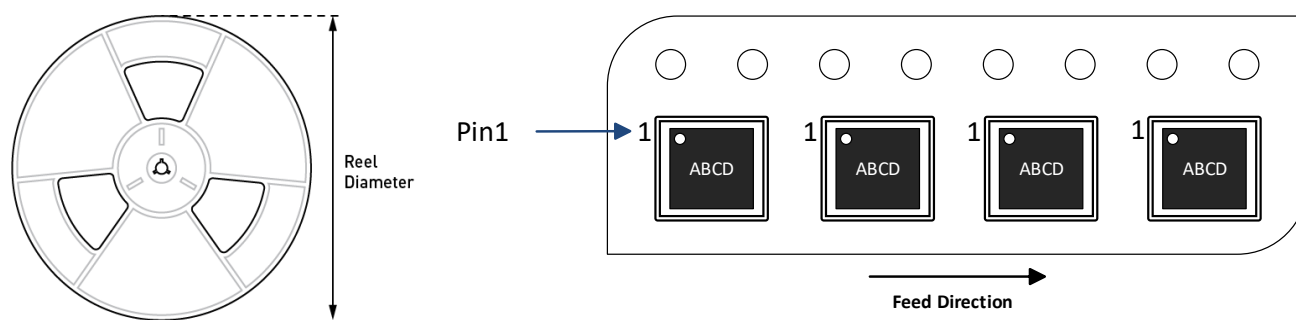


**RECOMMENDED LAND PATTERN**

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MP5048AGU-Z | QFN-30 (5mmx5mm)    | 5000           | N/A            | N/A            | 13in          | 12mm               | 8mm                |

**REVISION HISTORY**

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 9/8/2022      | Initial Release | -             |

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