MPQ6532

5V to 60V, Three-Phase Brushless DC Motor Pre-Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6532 is a gate driver IC designed for three-phase brushless DC (BLDC) motor driver applications. It is capable of driving three half-bridges, consisting of six N-channel power MOSFETs, up to 60V.

The MPQ6532 integrates a regulated charge pump to generate gate drive power, and uses a bootstrap (BST) capacitor to generate a supply voltage for the high-side MOSFET (HS-FET) driver. An internal trickle-charge circuit maintains a sufficient HS-FET driver voltage even when the output is at 100% duty cycle.

Internal safety features include configurable short-circuit protection (SCP), over-current protection (OCP), adjustable dead-time (DT) control, under-voltage lockout (UVLO), and thermal shutdown.

The MPQ6532 integrates 120° commutation using three Hall sensor inputs. The pulse-width modulation (PWM), DIR, and nBRAKE inputs control the motor speed, direction, and braking, respectively.

The MPQ6532 is available in a QFN-28 (4mmx5mm) package with an exposed thermal pad, and is AEC-Q100 qualified.

FEATURES

- Wide 5V to 60V Input Voltage (V_{IN}) Range
- Built-in Hall Sensor Inputs and 120° Commutation Logic
- Charge Pump Gate Drive Supply
- Bootstrap (BST) High-Side (HS) Driver with Trickle-Charge Circuit Supports 100% Duty Cycle Operation
- Low-Power Sleep Mode
- Configurable Short-Circuit Protection (SCP)
- Over-Current Protection (OCP)
- Adjustable Dead-Time (DT) Control to Prevent Shoot-Through
- Pulse-Width Modulation (PWM) Speed Control Input
- Brake Control Input
- Motor Start-Up Current Limit
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package
- Available in a QFN-28 (4mmx5mm) Package
- Available in AEC-Q100 Grade 1

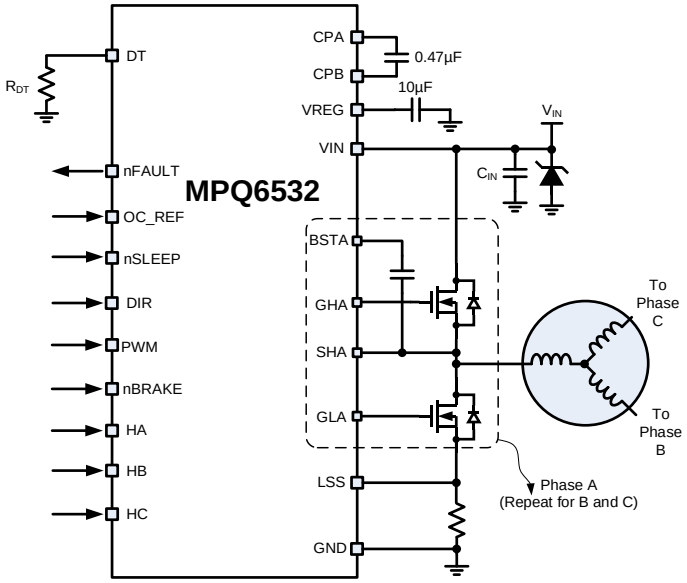
APPLICATIONS

- Three-Phase Brushless DC (BLDC) Motors and Permanent Magnet Synchronous Motors (PMSMs)
- Automotive Actuators, Pumps, and Fans

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6532GVE-AEC1**	QFN-28 (4mmx5mm)	*See Below*	2

* For Tape & Reel, add suffix -Z (e.g. MPQ6532GVE-AEC1-Z).

** Wettable Flank

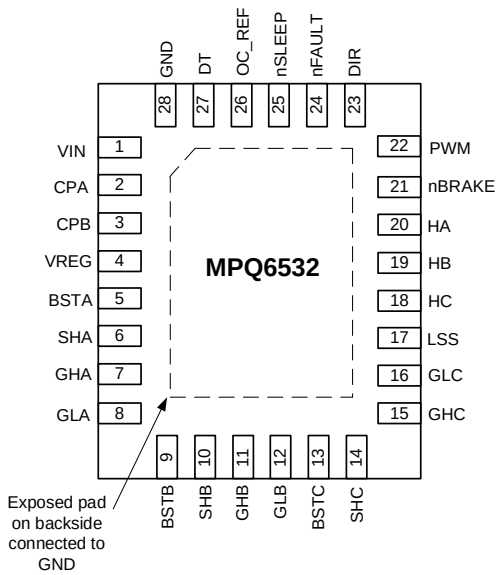
TOP MARKING

MPSYWW
MP6532
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6532: Part number
LLLLLL: Lot number
E: Wettable lead flank

PACKAGE REFERENCE

TOP VIEW



Wettable Flank

QFN-28 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input supply voltage.** Bypass VIN to ground using a ceramic capacitor. Additional bulk capacitance may be required. See the Application Information section on page 15 for more details.
2	CPA	**Charge pump capacitor.** Connect a ceramic capacitor between the CPA and CPB pins. See the Application Information section on page 15 for more details.
3	CPB	**Charge pump capacitor connection terminal.**
4	VREG	**Gate drive supply output.** Connect a ceramic capacitor to ground. See the Application Information section on page 15 for more details.
5	BSTA	**Bootstrap for phase A.** Connect a ceramic capacitor from this pin to SHA. See the Application Information section on page 15 for more details.
6	SHA	**High-side (HS) source connection for phase A.**
7	GHA	**HS gate drive for phase A.**
8	GLA	**Low-side (LS) gate drive for phase A.**
9	BSTB	**Bootstrap for phase B.** Connect a ceramic capacitor from this pin to SHB. See the Application Information section on page 15 for more details.
10	SHB	**HS source connection for phase B.**
11	GHB	**HS gate drive for phase B.**
12	GLB	**LS gate drive for phase B.**
13	BSTC	**Bootstrap for phase C.** Connect a ceramic capacitor from this pin to SHC. See the Application Information section on page 15 for more details.
14	SHC	**HS source connection for phase C.**
15	GHC	**HS gate drive for phase C.**
16	GLC	**LS gate drive for phase C.**
17	LSS	**LS source connection.**
18	HC	**Hall-sensor input for phase C.** HC has an internal pull-down resistor.
19	HB	**Hall-sensor input for phase B.** HB has an internal pull-down resistor.
20	HA	**Hall-sensor input for phase A.** HA has an internal pull-down resistor.
21	nBRAKE	**Brake input.** Pull nBRAKE active low to turn on all low-side MOSFETs (LS-FETs) and stop the motor; pull it high for normal operation. This pin has an internal pull-down resistor.
22	PWM	**External pulse-width modulation (PWM) input.** Pull PWM active high to drive the phase selected by the commutation logic high; pull it low to drive the phase low. This pin has an internal pull-down resistor.
23	DIR	**Direction input.** Pull this pin high or low to set the motor rotation direction. See Table 2 on page 13 for more details.
24	nFAULT	**Fault indication.** This pin is the open-drain output. nFAULT is pulled logic low if a fault condition occurs.
25	nSLEEP	**Sleep mode input.** Pull nSLEEP logic low to enter low-power sleep mode; pull it high to enable the device. This pin has an internal pull-down resistor.
26	OC_REF	**Over-current protection (OCP) reference voltage input.**
27	DT	**Dead time setting.** Connect a resistor to ground to set the dead time. See the Application Information section on page 15 for more details.
28	GND	**Ground.**

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ABSOLUTE MAXIUM RATINGS (1)

Input voltage (V_{IN}) ..... -0.3V to +62V
CPA ..... -0.3V to +55V
CPB ..... -0.3V to +12.5V
CPB (transient, <2µs) ..... -0.3V to +13V
VREG ..... -0.3V to +13V
BSTA, BSTB, and BSTC..... -0.3V to +70V
GHA, GHB, and GHC (continuous)..... ..... -0.3V to +70V
GHA, GHB, and GHC (transient, <2µs)..... ..... -8V to +70V
SHA, SHB, and SHC (continuous)..... ..... -0.3V to +65V
SHA, SHBC, and SHC (transient, <2µs) .... -8V to +65V
GLA, GLB, and GLC (continuous)..... ..... -0.3V to +13V
GLA, GLB, GLC (transient, <2µs) ....-2V to +13V
LSS (continuous) ..... -0.3V to +1V
LSS (transient, <2µs)..... -2V to +2V
All other pins to AGND..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
QFN-28 (4mmx5mm)…….....3.1W
Storage temperature..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human body model (HBM) 1.8kV
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Input voltage (V_{IN}) ..... 5V to 60V
OC_REF voltage (V_{OC_REF})..... 0.125V to 2.4V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm) ..... 40 ..... 9 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5		60	V
Quiescent current	I_Q	nSLEEP = 1, gate not switching		1.8	4	mA
	I_{SLEEP}	nSLEEP = 0			2.5	µA
Control Logic						
Low input logic threshold	V_{IL}				0.8	V
High input logic threshold	V_{IH}		2			V
Input current logic	$I_{IN(H)}$	V_{IH} = 5V	-20		+20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		+20	µA
nSLEEP pull-down current	$I_{SLEEP-PD}$			1		µA
Internal pull-down resistance	R_{PD}	All logic inputs except nSLEEP		880		kΩ
Fault Output (Open-Drain Output)						
Low-voltage output	V_{OL}	I_{OUT} = 5mA			0.5	V
High leakage current output	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuit						
Under-voltage lockout (UVLO) rising threshold	V_{IN_RISING}		3.2	3.9	5	V
UVLO hysteresis	V_{IN_HYS}			200		mV
VREG rising threshold	V_{REG_RISING}		6.8	7.6	8.4	V
VREG hysteresis	V_{REG_HYS}			0.65	1	V
VREG start-up delay	t_{REG}			880		µs
OC_REF threshold	V_{OC_REF}	V_{OC_REF} = 1V	0.8	1	1.2	V
		V_{OC_REF} = 2.4V	2.18	2.4	2.62	V
Over-current protection (OCP) deglitch time	t_{OC}			3		µs
SLEEP wake-up time	t_{SLEEP}			1		ms
LSS OCP threshold	$V_{LSS-OCP}$		0.4	0.5	0.6	V
LSS current limit fixed off time	t_{OFF}			70		µs
LSS current limit high-side (HS) minimum on time	t_{ON}			1		µs
Thermal shutdown	T_{TSD}			190		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			30		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Drive						
Bootstrap (BST) diode forward voltage	V_{FBOOT}	I_D = 10mA			1	V
		I_D = 100mA			1.4	V
VREG output voltage	V_{REG}	V_{IN} = 5.5V - 60V	9.5	11.5	13	V
		V_{IN} = 5V	2 x V_{IN} - 1			V
Maximum source current (5)	I_{OSO}			0.8		A
Maximum sink current (5)	I_{OSI}			1		A
Gate drive pull-up resistance	R_{UP}	V_{DS} = 1V		8		Ω
HS gate drive pull-down resistance	R_{HS-DN}	V_{DS} = 1V	1		5	Ω
Low-side (LS) gate drive pull-down resistance	R_{LS-DN}	V_{DS} = 1V	0.7		6.7	Ω
LS automatic turn-on time	t_{LS}	At each commutation time		2		µs
Charge pump frequency	f_{CP}			110		kHz
Dead time (DT)	t_{DEAD}	R_{DT} = 10kΩ		700		ns
		DT tied to GND		90		ns
		R_{DT} = 100kΩ		5.7		µs

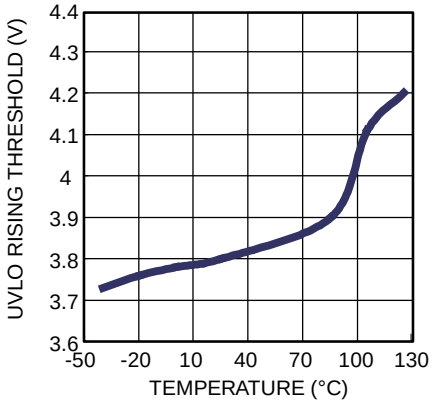
Note:

5) Not tested in production.

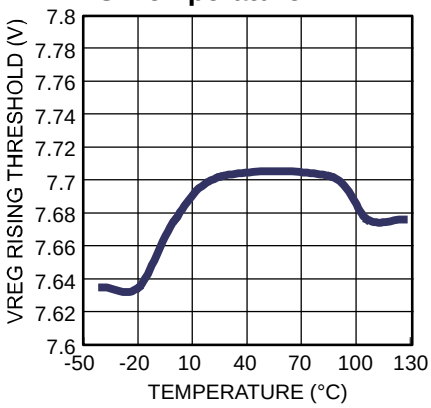
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TYPICAL CHARACTERISTICS

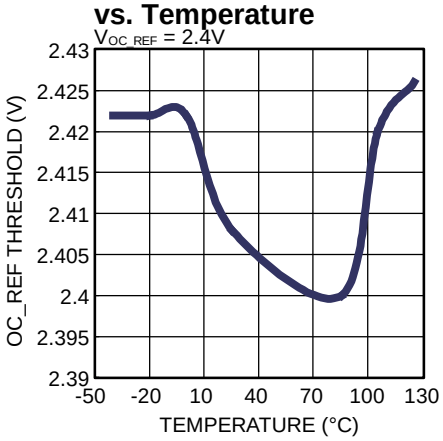
UVLO Rising Threshold vs. Temperature



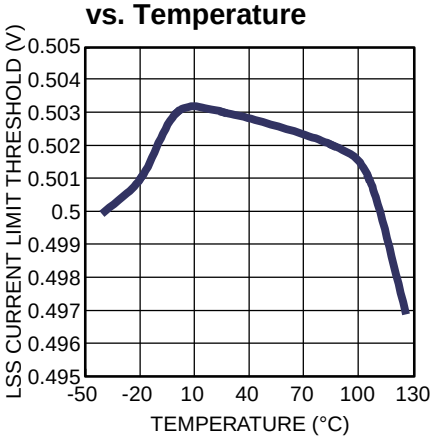
VREG Rising Threshold vs. Temperature



OC_REF Threshold vs. Temperature



LSS Current Limit Threshold vs. Temperature

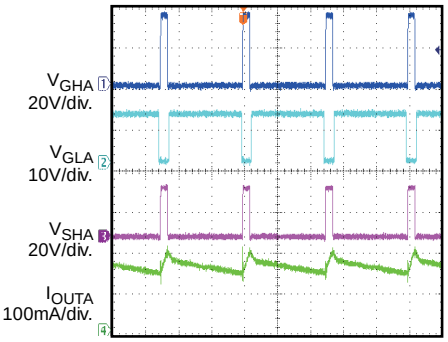


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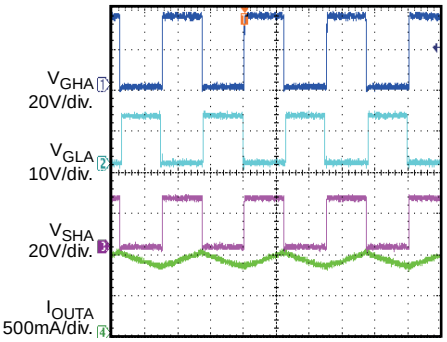
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, OC_REF = 0.5V, R_{DT} = 20kΩ, DIR = nBRAKE = H, HA = HC = H, HB = L, f_{PWM} = 20kHz, T_A = 25°C, resistor + inductor load is 5Ω + 1mH/phase with a star connection, unless otherwise noted.

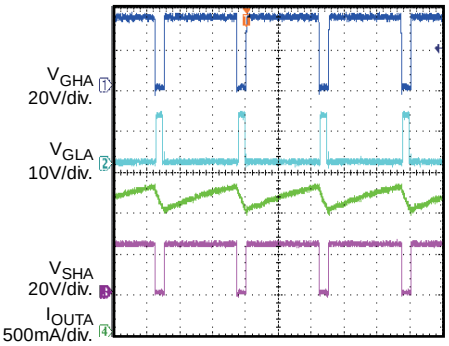
Steady State
Duty = 10%



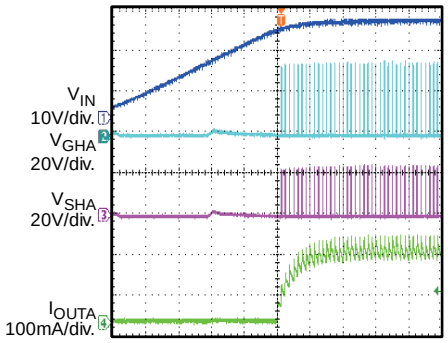
Steady State
Duty = 50%



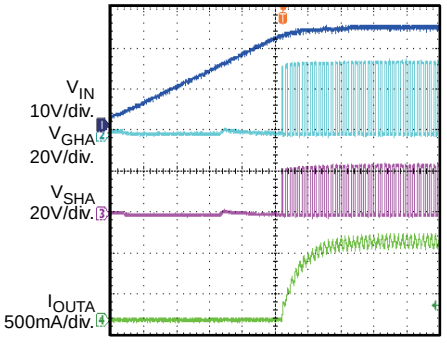
Steady State
Duty = 90%



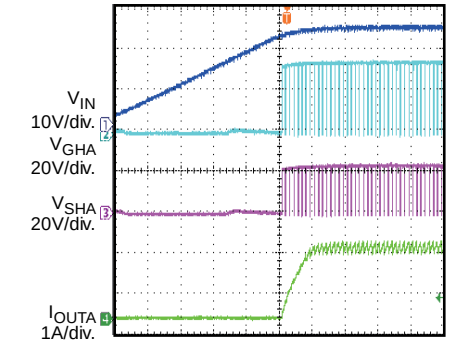
Power Ramping Up
Duty = 10%



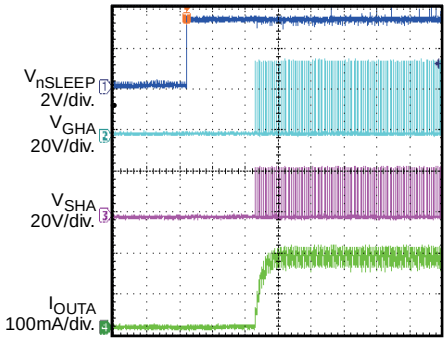
Power Ramping Up
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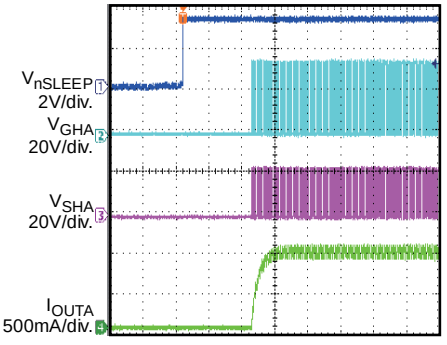
Power Ramping Up
Duty = 90%



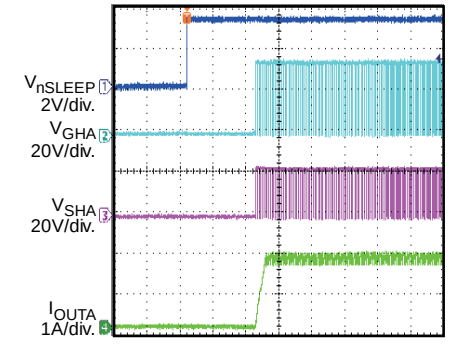
Sleep Recovery
Duty = 10%



Sleep Recovery
Duty = 50%



Sleep Recovery
Duty = 90%

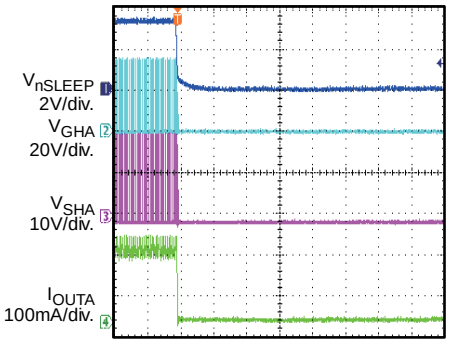


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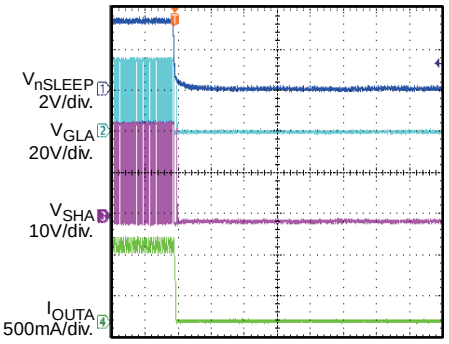
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, OC_REF = 0.5V, R_{DT} = 20kΩ, DIR = nBRAKE = H, HA = HC = H, HB = L, f_{PWM} = 20kHz, T_A = 25°C, resistor + inductor load is 5Ω + 1mH/phase with a star connection, unless otherwise noted.

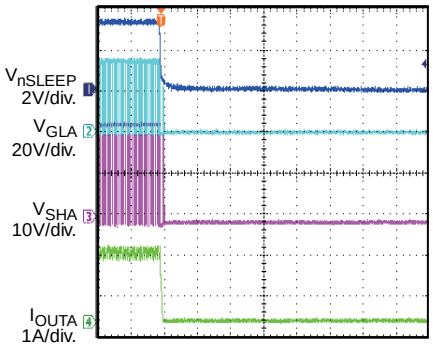
Sleep Mode Entry
Duty = 10%



Sleep Mode Entry
Duty = 50%



Sleep Mode Entry
Duty = 90%



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FUNCTIONAL BLOCK DIAGRAM

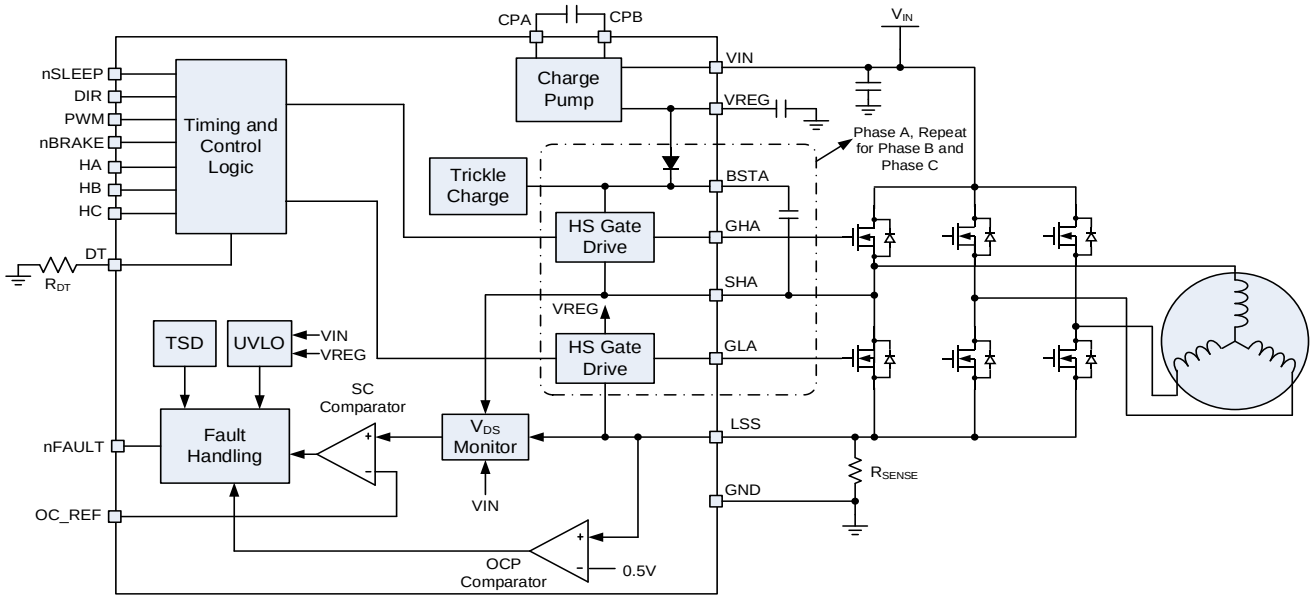


Figure 1: Functional Block Diagram

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OPERATION

The MPQ6532 is a three-phase brushless DC (BLDC) motor pre-driver with built-in commutation logic that drives three external N-channel MOSFET half-bridges with 0.8A source current and 1A sink current capability. It operates across a wide 5V to 60V input voltage (V_{IN}) range, generating a boost gate drive voltage when the input supply is below 12V. The MPQ6532 features low-power sleep mode, which disables the device and draws a very low supply current.

The MPQ6532 provides several flexible functions, such as adjustable dead-time (DT) control and over-current protection (OCP), which support a wide range of applications.

Start-Up Sequence

Apply voltage to VIN to initiate the start-up sequence. V_{IN} must exceed the under-voltage lockout (UVLO) threshold (V_{IN_RISE}) to initiate start-up.

After start-up begins, the VREG supply starts operating and must exceed the VREG rising threshold (V_{REG_RISING}) before the device becomes functional.

The start-up process takes between 1ms and 2ms. Once start-up is complete, the MPQ6532 responds to logic inputs and drives the outputs.

Gate Drive Power Supplies

Gate drive voltages are generated from V_{IN}. A regulated charge pump doubler circuit supplies a voltage (about 11.5V to V_{REG}). This voltage is used for the low-side (LS) gate drive supply. The charge pump requires external capacitors placed between CPA and CPB, and from VREG to ground.

The high-side (HS) gate drive is generated by a combination of a bootstrap (BST) capacitor (C_{BST}) and an internal trickle-charge pump. C_{BST} is charged to the VREG voltage (V_{REG}) when the low-side MOSFET (LS-FET) is turned on. This charge is then used to drive the high-side MOSFET (HS-FET) gate when it is turned on.

To keep C_{BST} charged and allow operation at 100% duty cycle, an internal trickle-charge pump supplies a small current (about 5µA) to overcome leakages that would discharge C_{BST}.

See the Application Information section on page 15 for details on selecting external components.

Sleep Mode (nSLEEP Input)

Pull nSLEEP low to put the device into a low-power sleep state. In this state, all internal circuits are disabled, and all inputs are ignored. nSLEEP has an internal pull-down resistor, so the pin must be pulled high for the MPQ6532 to operate. To exit sleep mode, the MPQ6532 initiates the start-up sequence.

Input Logic

The pulse-width modulation (PWM) input is typically connected to a PWM signal, which controls the motor's speed. DIR controls the direction of rotation. When nBRAKE is pulled active low, all LS-FETs turn on to stop the motor. Table 1 shows the logic of the PWM and nBRAKE inputs.

Table 1: Input Logic Truth Table

PWM	nBRAKE	Operation
X	L	Brake (all LS-FETs on)
L	H	Drive selected phase low
H	H	Drive selected phase high

Commutation Logic and Hall Inputs

The commutation logic is driven by three Hall-sensor inputs. These inputs are connected to sensors in the motor that are spaced 120° apart. See Table 2 on page 13 for the commutation logic.

At each Hall input transition, the relevant phase (pulled high or low, depending on the PWM input) is first pulled low for a short period of time (t_{LS}). This ensures that C_{BST} is charged at the beginning of each commutation cycle. Consequently, even if the PWM input is held high, each phase pulses low before being pulled high.

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Table 2: Commutation Table (nBRAKE = 1 (6))

Logic Inputs				Driver Outputs						Motor Terminals		
HA	HB	HC	DIR	GLA	GLB	GLC	GHA	GHB	GHC	SHA	SHB	SHC
1	0	1	1	/PWM	0	1	PWM	0	0	H	Z	L
1	0	0	1	0	/PWM	1	0	PWM	0	Z	H	L
1	1	0	1	1	/PWM	0	0	PWM	0	L	H	Z
0	1	0	1	1	0	/PWM	0	0	PWM	L	Z	H
0	1	1	1	0	1	/PWM	0	0	PWM	Z	L	H
0	0	1	1	/PWM	1	0	PWM	0	0	H	L	Z
1	0	1	0	1	0	/PWM	0	0	PWM	L	Z	H
1	0	0	0	0	1	/PWM	0	0	PWM	Z	L	H
1	1	0	0	/PWM	1	0	PWM	0	0	H	L	Z
0	1	0	0	/PWM	0	1	PWM	0	0	H	Z	L
0	1	1	0	0	/PWM	1	0	PWM	0	Z	H	L
0	0	1	0	1	/PWM	0	0	PWM	0	L	H	Z

Note:

6) If nBRAKE = 0, the braking function is active, and all low-side gates are turned on.

nFAULT

nFAULT reports to the system if a fault condition, such as over-current (OC) or over-temperature (OT), is detected. nFAULT is an open-drain output, and is pulled low if a fault condition occurs. Once the fault condition is removed, an external pull-up resistor drives nFAULT high.

Short-Circuit Protection (V_{DS} Sensing)

To protect the power stage from high currents, the MPQ6532 implements drain-to-source voltage (V_{DS}) sensing circuitry, which senses the voltage drop across each MOSFET. This voltage is proportional to the MOSFET's $R_{DS(ON)}$ and the drain-to-source current (I_{DS}) passing through the MOSFET. If the voltage drop exceeds the voltage supplied to the OC_REF terminal, then a short circuit is recognized.

In the event of a short circuit, the MPQ6532 disables all of the gate drive outputs. nFAULT is pulled active low. The device remains latched off until it is reset by nSLEEP or V_{IN} UVLO.

Short-circuit protection (SCP) can be disabled by connecting a 100kΩ resistor between VREG and OC_REF.

Over-Current Protection (OCP)

The MPQ6532 implements output OCP by monitoring the current through an LS shunt resistor connected to the LS-FETs. This resistor is connected to the LSS input pin and the LS-FET source terminals. If the OCP function is not necessary, connect LSS and the LS-FET source terminals directly to ground.

The LSS voltage (V_{LSS}) is the voltage across the shunt resistor. If V_{LSS} exceeds the LSS OCP threshold voltage ($V_{LSS-OCP}$), the HS-FET turns off and the corresponding LS-FET turns on for a fixed off time (t_{OFF}). After t_{OFF}, the HS-FET turns back on, and the cycle repeats until LSS no longer exceeds the current limit threshold.

The OCP current limit level is set by the current-sense resistor's value at LSS. See the Application Information section on page 15 for more information.

OCP limits the stall current of a BLDC motor.

Short-Circuit and OCP Deglitch Time

A current spike often occurs during switching transitions, caused by the body diode's reverse-recovery current or the distributed capacitance of the load. This current spike requires filtering to prevent it from erroneously triggering OCP. An internal, fixed deglitch time (t_{OC}) blanks the VDS monitor's output when the outputs are switched.

Dead Time (DT) Adjustment

To prevent shoot-through in any phase of the bridge, it is necessary to have a dead time (t_{DEAD}) between the HS-FET or LS-FET turning off and the next complementary turn-on event. t_{DEAD} for all three phases is set by a single DT resistor (R_{DT}) between DT and ground, and can be estimated using Equation (1):

$$t_{DEAD}\ (ns) = 60 \times R(k\Omega) \quad (1)$$

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If DT is directly connected to ground, apply an internal minimum t_{DEAD} (90ns).

Under-Voltage Lockout (UVLO) Protection

If V_{IN} falls below the UVLO threshold (V_{IN_RISING}), all circuitry in the MPQ6532 is disabled and the internal logic is reset. Once V_{IN} exceeds V_{IN_RISING} again, operation resumes with the start-up sequence.

If for any reason V_{REG} drops below V_{REG_RISING}, the gate drive outputs are disabled, and nFAULT is pulled active low. Once V_{REG} exceeds V_{REG_RISING}, normal operation resumes.

Thermal Shutdown

If the die temperature exceeds safe limits (typically 190°C), the MPQ6532 disables its outputs. Once the temperature has fallen to a safe level, the device resumes normal operation.

PCB Mounting

To comply with IPC-2221 or IPC-9592 standards, conformal coating may be required after mounting the device on the PCB.

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APPLICATION INFORMATION

Input Voltage (V_{IN})

V_{IN} supplies all power to the device, and must be properly bypassed with a capacitor to ground. The normal operating range of V_{IN} is 5V to 60V.

V_{IN} must never exceed the absolute maximum ratings, even under short-term transient conditions, or damage to the device may result. In some cases, especially when mechanical energy can transform a motor into a generator, it may be necessary to use some form of over-voltage protection (OVP), such as a TVS diode, between VIN and ground.

Selecting the MOSFET

Correctly selecting the power MOSFETs for driving a motor is crucial for successful motor drive design.

The MOSFET must have a breakdown voltage (V_{DS}) that exceeds the supply voltage. A considerable margin (10V to 15V) should be added to prevent damage to the MOSFET from transient voltages, which are caused by parasitic inductance in the PCB layout and wiring. For example, MOSFETs in 24V power supply applications should have a minimum V_{DS} between 40V and 60V. Additional margin is ideal for high-current applications, as the transients caused by parasitic inductance may be larger. Conditions such as regenerative braking can also inject current back into the power supply. Care must be taken to ensure that such conditions do not increase the power supply voltage enough to damage components.

The MOSFETs should be able to safely pass the current necessary to run the motor. The motor's stall current is the highest current condition (typically when the motor is first started or stalled) that must be supported.

$R_{DS(ON)}$ is the MOSFET's on resistance, and is similar to the MOSFET's current capability. The power dissipated by the MOSFET is proportional to $R_{DS(ON)}$ and the motor current, and can be calculated using Equation (2):

$$P = I^2R \quad (2)$$

$R_{DS(ON)}$ must be selected to support safe heat dissipation for the desired motor current. In some cases, this may require special PCB design considerations, or implementing external heatsinks for the MOSFETs.

Considerations should be made for the safe operating area (SOA) of the MOSFETs during fault conditions, such as a short circuit. The IC acts quickly in the event of a short. However, large currents can flow in the MOSFETs for a short time period (about 3µs), before the protection circuits recognize the fault and disable the outputs.

Selecting the External Capacitor

The MPQ6532 can provide a gate drive voltage (V_{REG}) between 9.5V and 13V, even if the input supply voltage drops as low as 5V. V_{REG} is generated by a charge pump inside the IC using external capacitors.

The charge pump flying capacitor (C_{CP}) should have a capacitance of 470nF. The capacitor must be rated to withstand the maximum V_{IN} supply voltage. An X7R or X5R ceramic capacitor is recommended. With a 470nF capacitor, VREG can output approximately 10mA when V_{IN} is 5V. If operation below 10V is not necessary, a 220nF capacitor can be used.

Use BST capacitors to provide the large peak currents required to turn on the HS-FET. These capacitors are charged when the output is pulled low, then the C_{BST} charge turns on the HS-FET when the output is pulled high. Note that an internal charge pump keeps C_{BST} charged when the output is held high for an extended period.

Select the BST capacitors based on the MOSFET total gate charge. When the HS-FET is on, the charge stored in C_{BST} is transferred to the HS-FET gate. For simplification, the minimum BST capacitance (C_{BOOT}) can be estimated using Equation (3):

$$C_{BOOT} > 8 \times Q_G \quad (3)$$

Where Q_G is the total gate charge of the MOSFET (in nC), and C_{BOOT} is the minimum BST capacitance (in nF).

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C_{BST} should not exceed 1µF, or it may cause improper operation at start-up.

For most applications, C_{BST} should be between 0.1µF and 1µF, X5R or X7R ceramic, and rated for at least 25V.

VREG requires placing a bypass capacitor to ground, as close to the device as possible. This capacitor should be a 10µF, X7R or X5R ceramic capacitor rated for at least 16V.

VIN requires placing a bypass capacitor to ground, as close as possible to the device. It is recommended to use a 0.1µF, X5R or X7R ceramic capacitor that is rated for V_{IN}.

Depending on the power supply impedance and the distance between the MOSFETs and the power supply, additional bulk capacitance may be required. Low-ESR electrolytic capacitors between 47µF and 470µF are recommended.

Selecting the Dead-Time Resistor

During the transition between driving an output low and high, t_{DEAD} is the short period during which neither the HS-FET nor LS-FET turn on. t_{DEAD} is necessary to prevent shoot-through, a condition in which overlaps in conduction between HS-FETs and LS-FET create a short circuit between the power supply and ground. Shoot-through causes large transient currents and can destroy the MOSFETs.

Since motors are naturally inductive, once current is flowing in the motor, it cannot stop immediately, even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field decays.

When the MOSFETs turn off, the recirculation current flows through the body diode in the MOSFET.

MOSFET body diodes have a significantly greater voltage drop than the MOSFET during conduction, so more power is dissipated during body diode conduction than during the MOSFET's on time. Therefore, it is ideal to minimize t_{DEAD}. However, t_{DEAD} must still be long enough to guarantee that the HS-FETs and LS-FETs are never turned on at the same time.

t_{DEAD} can be set to a large range of times by selecting the value of the external resistor connected to DT. Typically, a good t_{DEAD} is about 1µs, which requires a 20kΩ resistor on DT. If faster switching or a high PWM frequency (f_{PWM}) (above ~30kHz) is used, a shorter t_{DEAD} may be ideal. If switching is slowed using external gate resistors, a longer t_{DEAD} may be necessary.

Figure 2 shows a waveform with a t_{DEAD} of ~300ns between the LS gate turn-off and the HS gate turn-on.

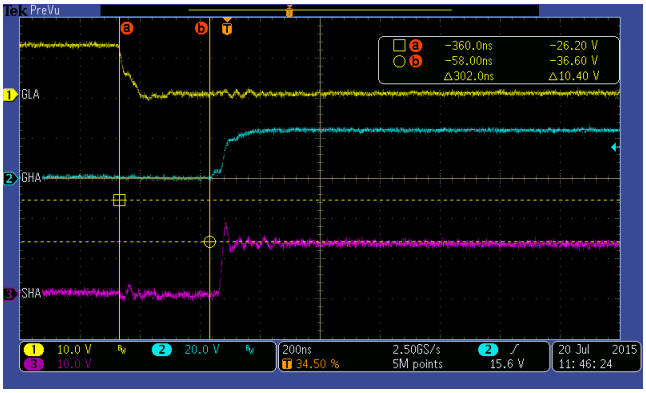


Figure 2: Dead Time

Selecting the LSS Resistor

If V_{LSS} exceeds 500mV, an OC event is recognized. The external sense resistor is sized to provide a drop below 500mV at the maximum expected motor current. For example, if a 50mΩ resistor is used, then a 10A current causes a 500mV drop and activates OCP.

If this function is not necessary, connect LSS directly to ground.

Selecting the OC_REF Voltage

An internal comparator compares the voltage drop across each MOSFET with a voltage externally provided on the OC_REF input pin. This voltage is typically provided by an external resistor divider from a logic power supply. If the drop across any MOSFET exceeds the voltage on OC_REF, this is considered a short-circuit event.

If this function is not necessary, connect OC_REF to VREG through a 100kΩ resistor.

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Gate Drive Considerations

The selected MOSFETs' gate characteristics affect how fast the MOSFETs are switched on and off. The MPQ6532's gate drive outputs can be directly connected to the gates of the power MOSFETs, which results in the fastest possible turn-on and turn-off times. However, it may be advantageous to add external components (resistors and/or diodes) to modify the MOSFET turn-on and turn-off characteristics.

Adding external series resistance (typically 10Ω to 100Ω) limits the current that charges and discharges the MOSFET gate, slowing down the turn-on and turn-off times. This is sometimes useful to control EMI and noise. However, slowing down the transition too much results in a large power dissipation in the MOSFET during switching.

In some cases, it is desirable to have a slow turn-on, but a fast turn-off. This can be implemented by using a series resistor in parallel with a diode (see Figure 3). During turn-on, the resistor limits the current flow into the gate. During turn-off, the gate is discharged quickly through the diode.

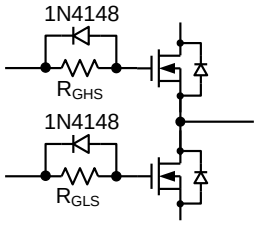


Figure 3: Gate Circuit for Fast Turn-Off

Figure 4 shows a waveform representing the LS-FET and HS-FET gates, and the phase node (output) with no series resistance. The gates transition quickly, and the resulting rise time on the phase node is quite fast. The scale of Figure 4 is 100ns/div.

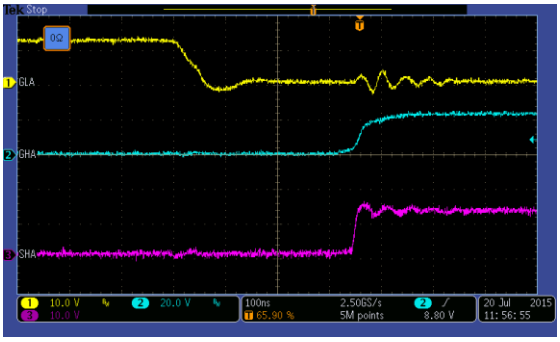


Figure 4: Switching with No Series Resistance

Figure 5 shows the waveform that results from adding a 100Ω series resistor between the GLA pin and the LS-FET gate, and between the GHA pin and the HS-FET gate, respectively. The rise time on the phase node has been slowed significantly. The scale of Figure 5 is 200ns/div.

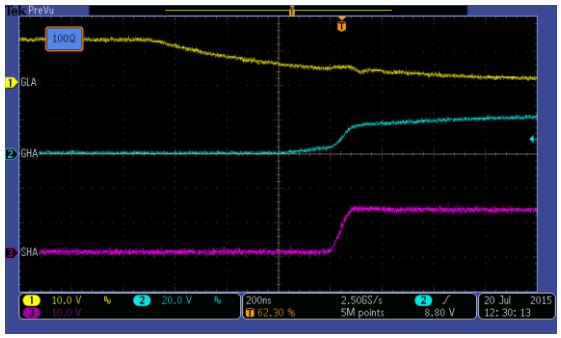


Figure 5: Switching with 100Ω Series Resistance

Figure 6 shows the waveform that results from adding a 1N4148 diode in parallel with the 100Ω resistors (and the cathode connected to the IC). The LS gate fall time is fast compared to the HS gate rise time. The phase node moves even slower because of a longer time period between when the LS-FET turns off and the HS-FET turns on.

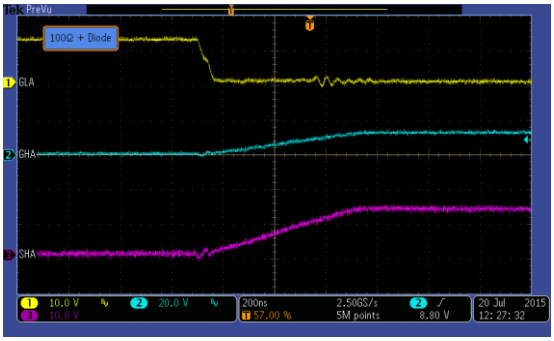


Figure 6: Switching with 100Ω Resistance and Diode

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PCB Layout Guidelines

Efficient PCB layout is critical for optimal performance. The pre-driver is designed to accommodate negative undershoot; however, excessive undershoot can lead to unpredictable operation or damage to the IC. For the best results, refer to Figure 7 and follow the guidelines below:

1. Make the connection between the HS source and LS drain as direct as possible to avoid a negative undershoot on the phase node due to parasitic inductance.
2. Use surface-mount N-channel MOSFETs that allow for a very short connection between the HS-FETs and LS-FETs.
3. Use wide copper areas for all of the high-current paths.
4. Connect the LS sense resistor, which is composed of three resistors in parallel (R25, R26, and R27), to the input supply ground and LS-FET source terminals with wide copper areas.
5. Place the charge pump and supply bypass capacitors as close to the IC as possible. Connect the grounded side of these capacitors to a ground plane, which should be connected to the device ground pin and exposed pad.
6. Keep the high-current ground path between the input supply, input bulk capacitor (C19), and MOSFETs away from the ground plane of the IC.

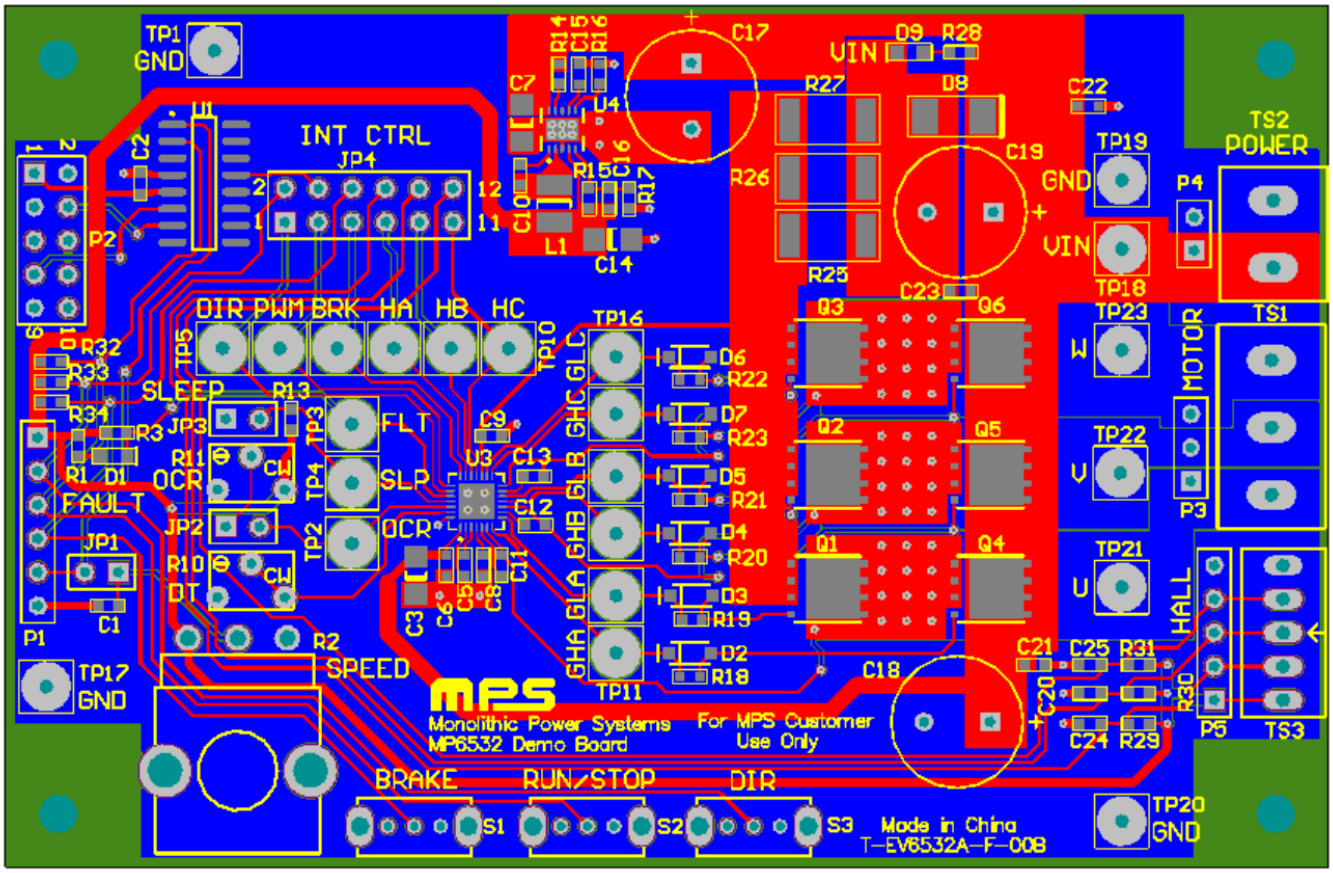


Figure 7: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

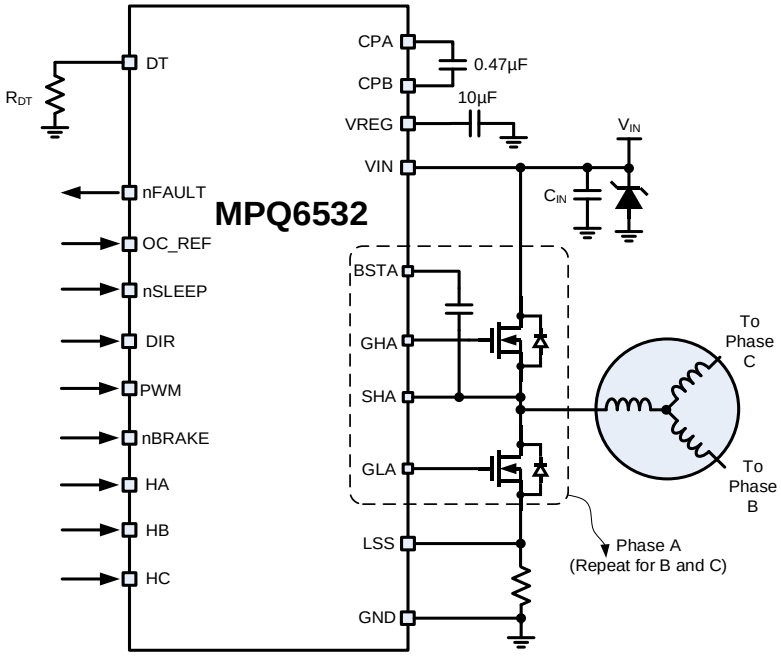
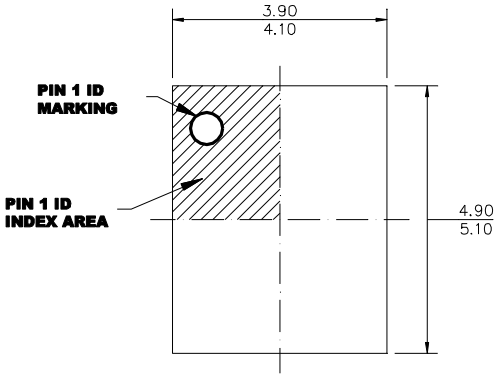


Figure 8: Typical Application Circuit

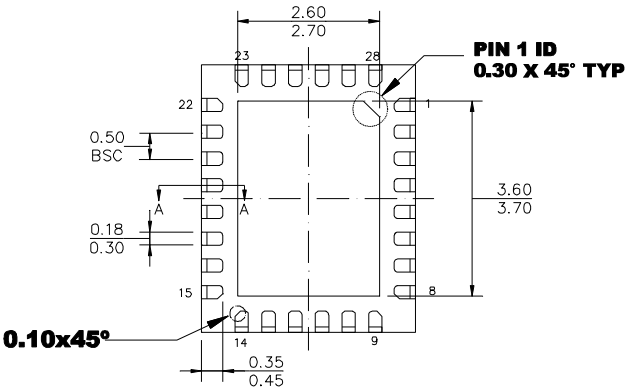
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PACKAGE INFORMATION

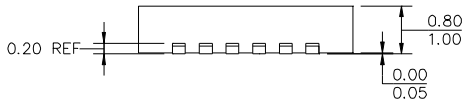
QFN-28 (4mmx5mm)
Wettable Flank



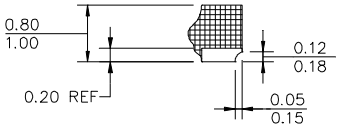
TOP VIEW



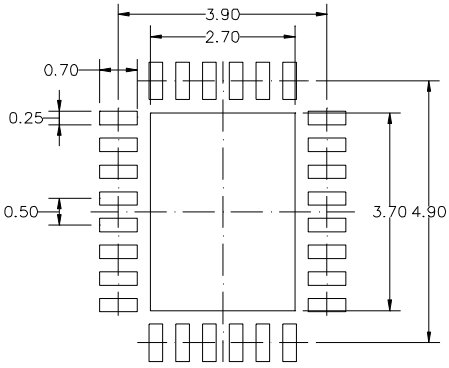
BOTTOM VIEW



SIDE VIEW



SECTION A-A



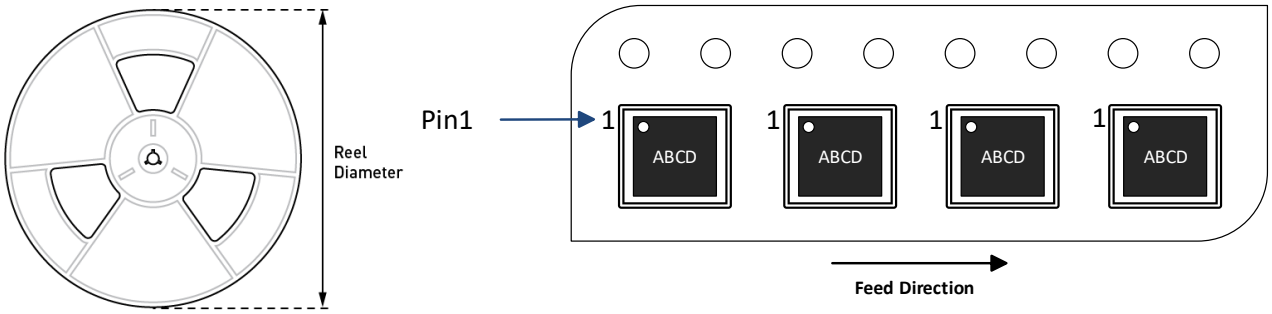
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6532GVE-AEC1-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/04/2021	Initial Release	-

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