MPQ6528

5V to 60V, H-Bridge Gate Driver, AEC-Q100 Qualified

DESCRIPTION

The MPQ6528 is an H-bridge gate driver IC that can drive two half-bridges with four N-channel power MOSFETs across a wide 5V to 60V input voltage (V_{IN}) range.

The device's integrated, regulated charge pump generates gate driver power (V_{REG}), and a bootstrap (BST) capacitor generates the supply voltage for the high-side MOSFET (HS-FET) driver. An internal trickle-charge circuit maintains a sufficient HS-FET gate driver voltage even at 100% duty cycle.

Full protection features include configurable short-circuit protection (SCP), over-current protection (OVP), under-voltage lockout (UVLO) protection, adjustable dead time (DT) control, and thermal shutdown.

The MPQ6528 is available in a QFN-28 (4mmx5mm) package with an exposed thermal pad.

FEATURES

- Wide 5V to 60V Input Voltage (V_{IN}) Range
- Charge Pump Gate Driver Supply
- Bootstrap (BST) High-Side MOSFET (HS-FET) Driver with Trickle-Charge Circuit for 100% Duty Cycle Operation
- Low-Power Sleep Mode
- Configurable Short-Circuit Protection (SCP)
- Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO) Protection
- Adjustable Dead Time (DT) Control to Prevent Shoot-Through
- Thermal Shutdown
- Fault Indication Output
- Thermally Enhanced Surface-Mount Package
- Available in a QFN-28 (4mmx5mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

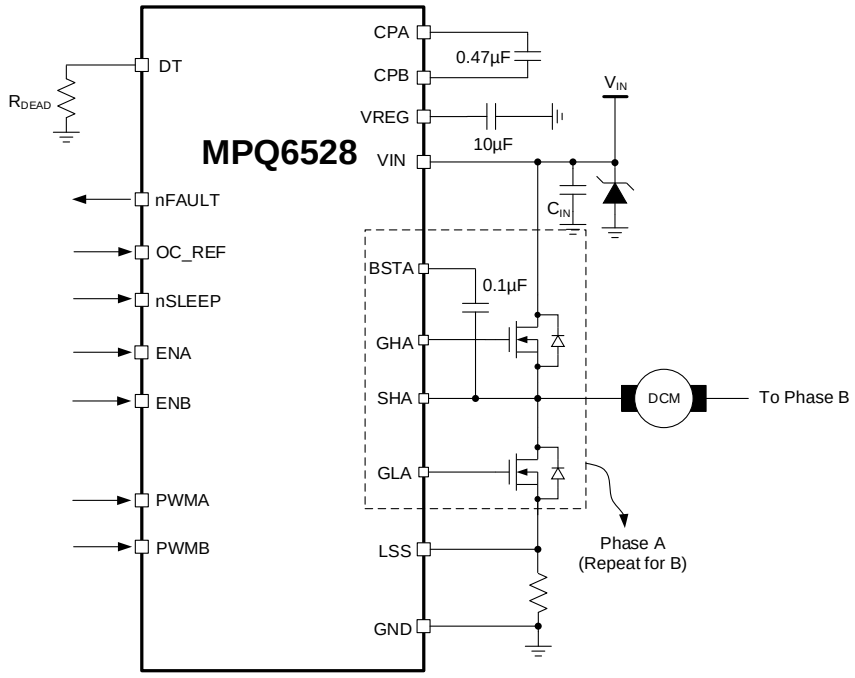
APPLICATIONS

- Brushed DC Motors
- Automotive Actuators
- Gate Openers
- Audio Amplifiers
- Power Converters

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPQ6528GVE-AEC1*	QFN-28 (4mmx5mm)	*See Below*	2

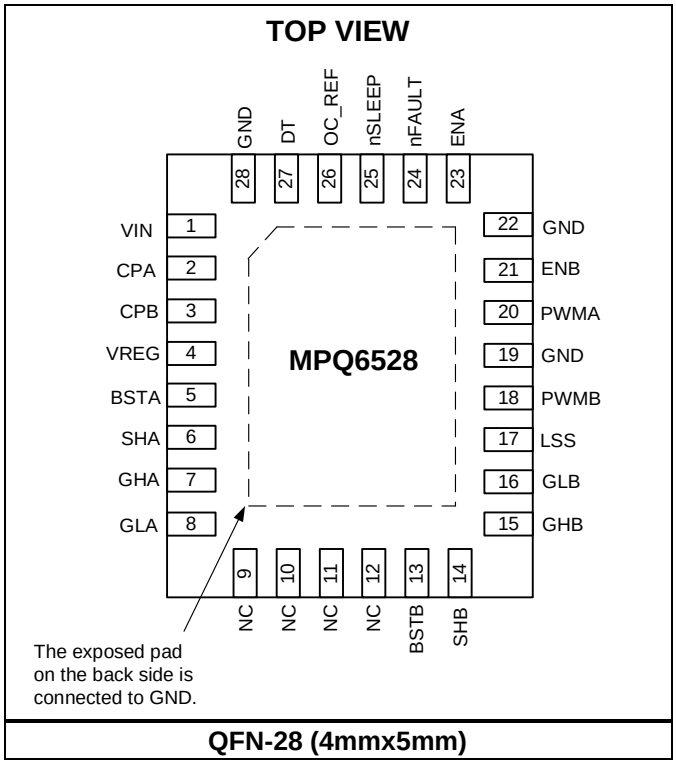
* For Tape & Reel, add suffix -Z (e.g. MPQ6528GVE-AEC1-Z).

TOP MARKING

MPSYWW
MP6528
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP6528: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-28 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Input supply voltage.** Use a ceramic capacitor to bypass the VIN pin to ground. Additional bulk capacitors may be required. (1)
2	CPA	**Charge pump capacitor.** Connect a ceramic capacitor between the CPA and CPB pins. (1)
3	CPB	**Charge pump capacitor connection terminal.**
4	VREG	**Gate driver output.** Connect a ceramic capacitor between the VREG pin and ground. (1)
5	BSTA	**Phase A bootstrap (BST).** Connect a ceramic capacitor between the BSTA and SHA pins. (1)
6	SHA	**Phase A high-side MOSFET (HS-FET) source connection.**
7	GHA	**Phase A HS-FET gate driver.**
8	GLA	**Phase A low-side MOSFET (LS-FET) gate driver.**
9, 10, 11, 12	NC	**No connection.**
13	BSTB	**Phase B bootstrap (BST).** Connect a ceramic capacitor between the BSTB and SHB pins. (1)
14	SHB	**Phase B HS-FET source connection.**
15	GHB	**Phase B HS-FET gate driver.**
16	GLB	**Phase B LS-FET gate driver.**
17	LSS	**Phase A and phase B LS-FETs source connection.**
18	PWMB	**Phase B pulse-width modulation (PWM) input.** Pull the PWMB pin high to drive phase B high; pull PWMB low to drive phase B low. PWMB has an internal pull-down resistor.
19, 22, 28	GND	**Ground.**
20	PWMA	**Phase A PWM input.** Pull the PWMA pin high to drive phase A high; pull PWMA low to drive phase A low. PWMA has an internal pull-down resistor.
21	ENB	**Phase B Enable (EN).** Pull the ENB pin high to turn the gate driver on for phase B; pull ENB low to turn the gate driver off for phase B. ENB has an internal pull-down resistor.
23	ENA	**Phase A Enable (EN).** Pull the ENA pin high to turn the gate driver on for phase A; pull ENA low to turn the gate driver off for phase A. ENA has an internal pull-down resistor.
24	nFAULT	**Fault indicator.** The nFAULT pin is an open-drain output. If a fault occurs, nFAULT is pulled low.
25	nSLEEP	**Sleep mode input.** Pull the nSLEEP pin low to enter low-power sleep mode; pull nSLEEP high to exit sleep mode. nSLEEP has an internal pull-down resistor.
26	OC_REF	**Over-current protection (OCP) reference voltage (V_{REF}) input.**
27	DT	**Dead time (DT) setting.** Connect a resistor to ground to set the dead time (DT). (1)

Note:

1) For more information, see the Application Information section on page 14.

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ABSOLUTE MAXIMUM RATINGS (2)

Input voltage (V_{IN}) ..... -0.3V to +62V
CPA ..... -0.3V to +55V
CPB ..... -0.3V to +12.5V
CPB (transient, <2µs) ..... -0.3V to +13V
VREG ..... -0.3V to +13V
BSTA/B ..... -0.3V to +70V
GHA, GHB (continuous) ..... -0.3V to +70V
GHA, GHB (transient, <2µs) ..... -8V to +70V
SHA, SHB (continuous) ..... -0.3V to +65V
SHA, SHB (transient, <2µs) ..... -8V to +65V
GLA, GLB (continuous) ..... -0.3V to +13V
GLA, GLB (transient, <2µs) ..... -2V to +13V
LSS (continuous) ..... -0.3V to +1V
LSS (transient, <2µs) ..... -2V to +2V
All other pins to AGND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (3)
QFN-28 (4mmx5mm) 3.1W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human body model (HBM) ..... ±1.8kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions (4)

Input voltage (V_{IN}) ..... 5V to 60V
OC_REF voltage (V_{OC_REF}) ..... 0.125V to 2.4V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance (5) θ_{JA} θ_{JC}

QFN-28 (4mmx5mm) ..... 40 ..... 9 .... °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are tested at T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input voltage	V_{IN}		5		60	V
Quiescent current	I_Q	nSLEEP = 1, gate driver is not switching		1.8	4	mA
	I_{SLEEP}	nSLEEP = 0, sleep mode			2.5	µA
Control Logic						
Input logic low threshold	V_{IN_LOW}				0.8	V
Input logic high threshold	V_{IN_HIGH}		2			V
Input current	I_{IN_HIGH}	V_{IN_HIGH} = 5V	-20		+20	µA
	I_{IN_LOW}	V_{IN_LOW} = 0.8V	-20		+20	µA
nSLEEP pull-down current	I_{PD_SLEEP}			1		µA
Internal pull-down resistance	R_{PD}	All logic inputs except nSLEEP		880		kΩ
Fault Outputs (Open-Drain Outputs)						
Output low voltage	V_{OUT_LOW}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OUT_HIGH}	V_{OUT} = 3.3V			1	µA
Protection Circuit						
Under-voltage lockout (UVLO) rising threshold	V_{IN_RISING}		3.2	3.9	5	V
UVLO hysteresis	V_{IN_HYS}			200		mV
V_{REG} rising threshold	V_{REG_RISING}		6.8	7.6	8.4	V
V_{REG} hysteresis	V_{REG_HYS}			0.65	1	V
VREG start-up delay	t_{DELAY_REG}			880		µs
OC_REF threshold	V_{OC_REF}	V_{OC_REF} = 1V	0.8	1	1.2	V
		V_{OC_REF} = 2.4V	2.18	2.4	2.62	V
Over-current protection (OCP) deglitch time	t_{OCP}			3		µs
Sleep mode wake-up time	t_{SLEEP}			1		ms
LSS OCP threshold	V_{OCP_LSS}		0.4	0.5	0.6	V
Thermal shutdown	T_{SD}			190		°C
Thermal shutdown hysteresis (6)	ΔT_{SD}			30		°C
Gate Driver						
Bootstrap (BST) diode forward voltage	V_{BST_FOR}	I_D = 10mA			1	V
		I_D = 100mA			1.4	V
VREG output voltage	V_{REG}	V_{IN} = 5.5V - 60V	9.5	11.5	13	V
		V_{IN} = 5V - 5.5V	2 x V_{IN} - 1			V
Maximum source current (6)	I_{SOURCE_MAX}			0.8		A
Maximum sink current (6)	I_{SINK_MAX}			1		A
Gate driver pull-up resistance	R_{PU}	V_{DS} = 1V		8		Ω
High-side MOSFET (HS-FET) gate driver pull-down resistance	R_{PD_HS}	V_{DS} = 1V	1		6	Ω
Low-side MOSFET (LS-FET) gate driver pull-down resistance	R_{PD_LS}	V_{DS} = 1V	0.7		6.7	Ω
LS-FET passive pull-down resistance	R_{PPD_LS}			590		kΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted. Typical values are tested at T_J = 25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LS-FET automatic on time	t_{LS}	At ENx rising edge		2		µs
Charge pump frequency	f_{CP}			110		kHz
Dead time	t_{DEAD}	R_{DT} = 10kΩ		700		ns
		DT tied to GND		90		ns
		R_{DT} = 100kΩ		5.7		µs

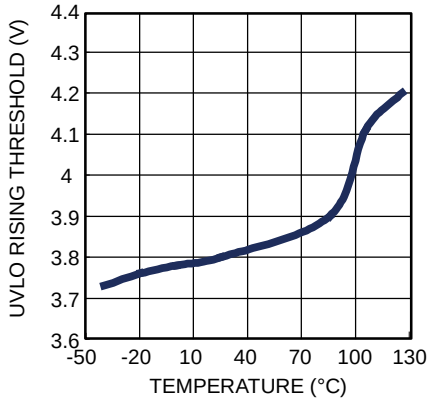
Note:

6) Not tested in production.

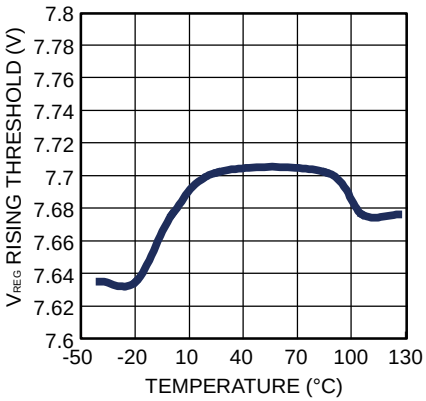
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TYPICAL PERFORMANCE CHARACTERISTICS

UVLO Rising Threshold vs. Temperature

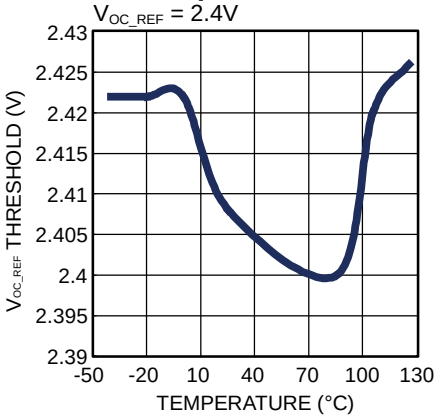


V_{REG} Rising Threshold vs. Temperature

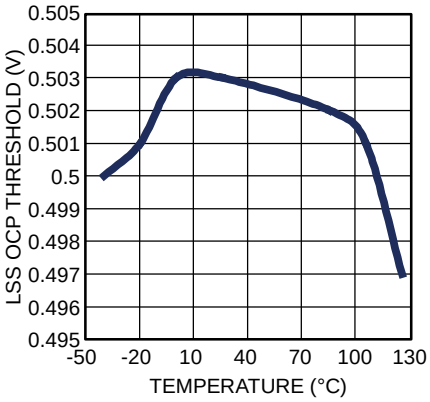


V_{OC_REF} Threshold vs. Temperature

V_{OC_REF} = 2.4V



LSS OCP Threshold vs. Temperature

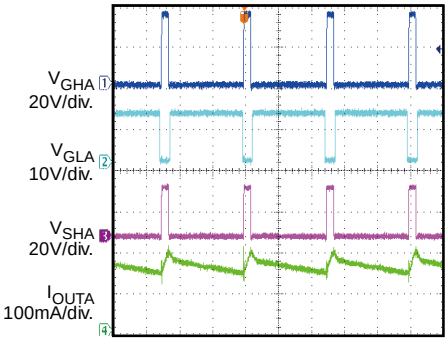


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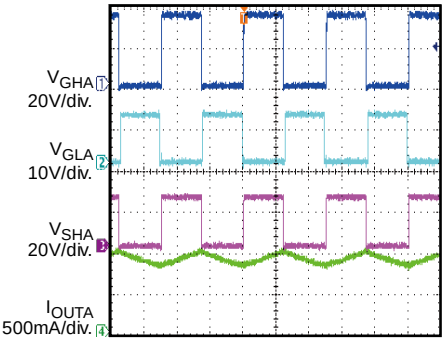
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OC_REF} = 0.5V, R_{DT} = 20kΩ, ENA = ENB = H, f_{PWMA} = 20kHz, PWMB = L, T_A = 25°C, resistor + inductor load = 10Ω + 2mH, unless otherwise noted.

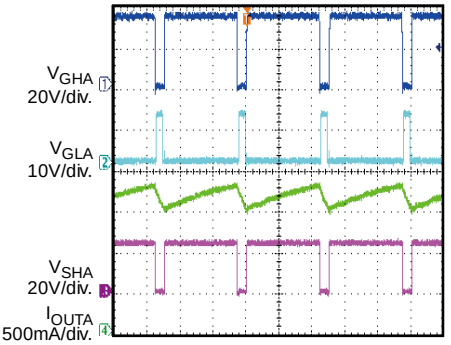
Steady State
Duty = 10%



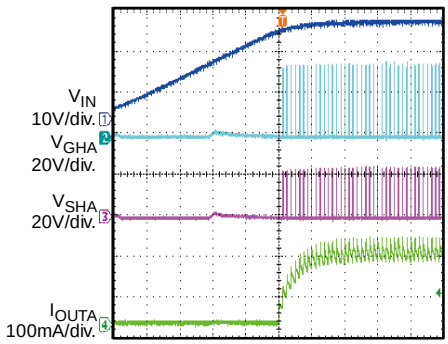
Steady State
Duty = 50%



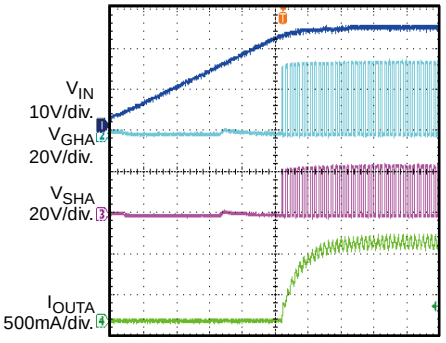
Steady State
Duty = 90%



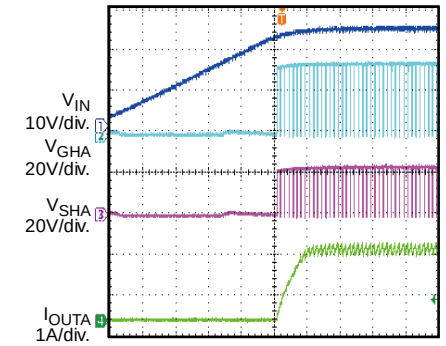
Power Ramps Up
Duty = 10%



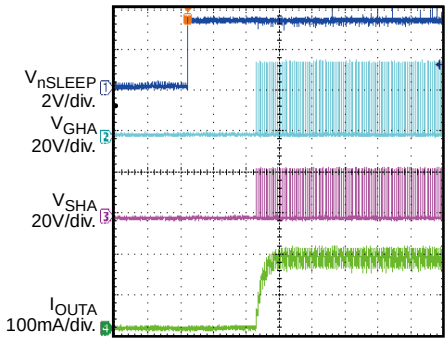
Power Ramps Up
Duty = 50%



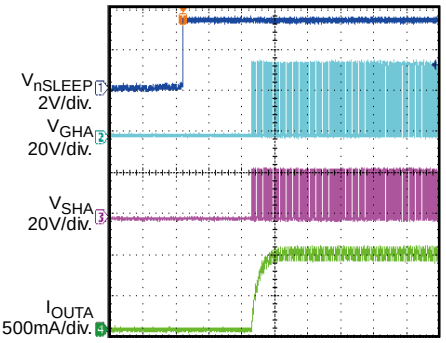
Power Ramps Up
Duty = 90%



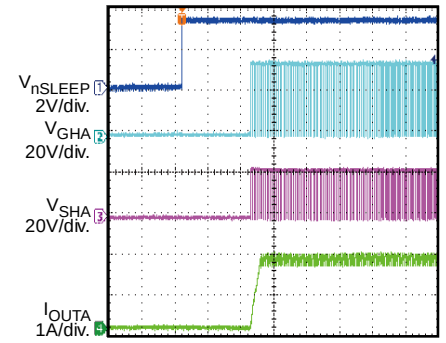
Sleep Mode Recovery
Duty = 10%



Sleep Mode Recovery
Duty = 50%



Sleep Mode Recovery
Duty = 90%

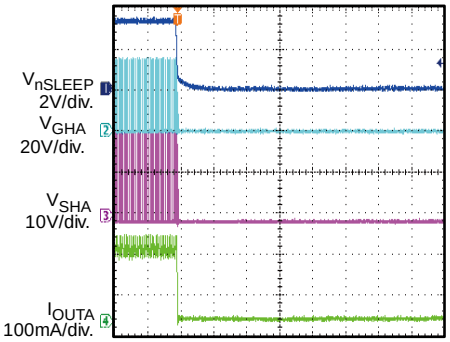


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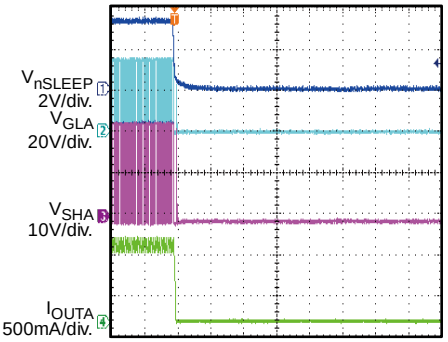
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OC_REF} = 0.5V, R_{DT} = 20kΩ, ENA = ENB = H, f_{PWMA} = 20kHz, PWMB = L, T_A = 25°C, resistor + inductor load = 10Ω + 2mH, unless otherwise noted.

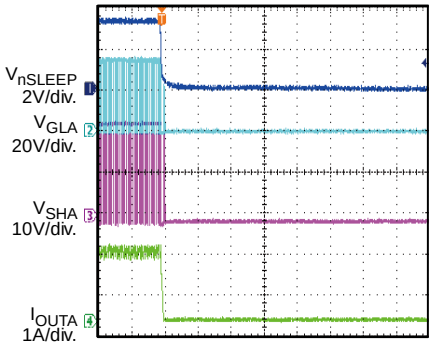
Sleep Mode Entry
Duty = 10%



Sleep Mode Entry
Duty = 50%



Sleep Mode Entry
Duty = 90%



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FUNCTIONAL BLOCK DIAGRAM

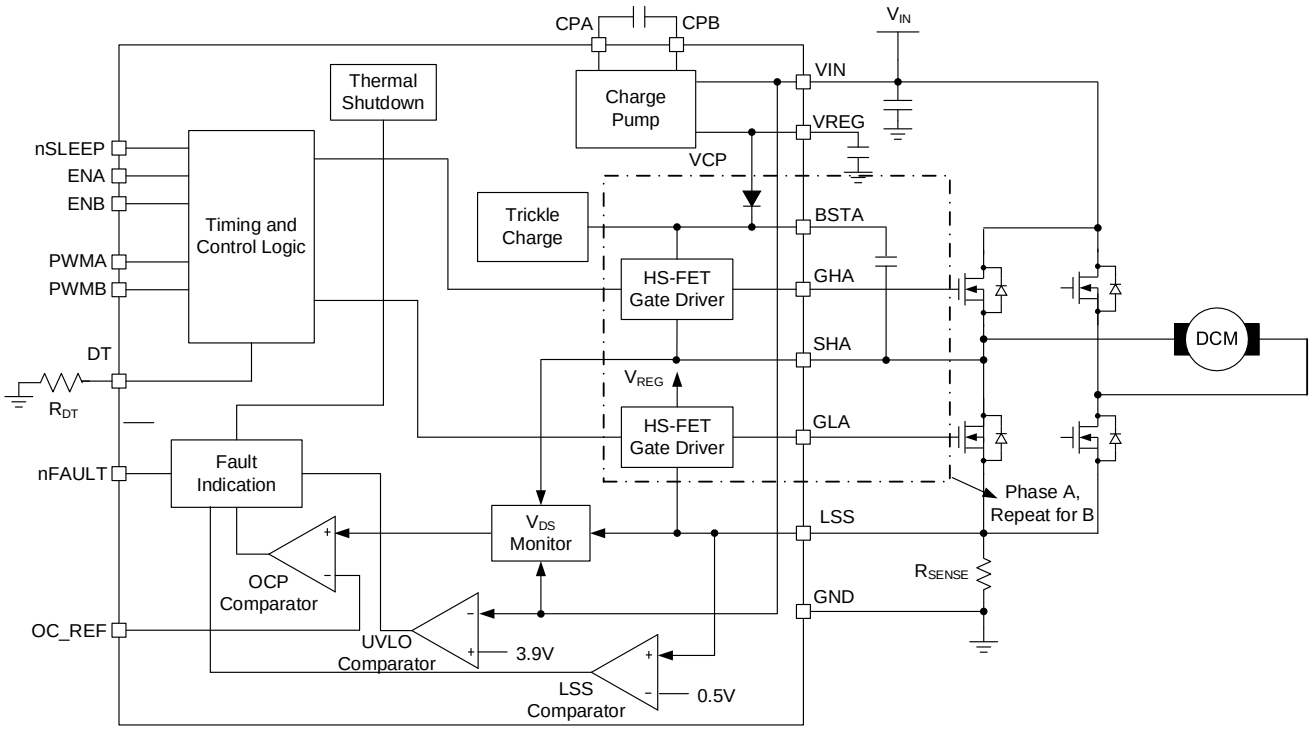


Figure 1: Functional Block Diagram

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OPERATION

The MPQ6528 is an H-bridge gate driver that can drive two external N-channel MOSFET half-bridges with 0.8A of source current (I_{SOURCE}) and 1A of sink current (I_{SINK}) across a wide 5V to 60V input voltage (V_{IN}) range. It can generate a boosted gate driver voltage (V_{REG}) while the V_{IN} supply is below 12V. The MPQ6528 is designed for use in battery-powered equipment. Low-power sleep mode disables the device and draws a very low supply current.

The device provides several flexible functions, such as adjustable dead time (DT) control and over-current protection (OCP). This allows the MPQ6528 to handle a wide range of applications.

Start-Up Sequence

The gate driver starts up once V_{IN} exceeds the under-voltage lockout (UVLO) rising threshold (typically 3.9V). The gate driver's output (GLx) is enabled once V_{REG} exceeds its rising threshold (typically 7.6V).

After the start-up sequence (about 1ms to 2ms), the MPQ6528 responds to the logic inputs and begins driving the outputs.

Gate Driver Power Supplies

The gate driver voltages are generated by V_{IN}. A regulated charge pump doubler circuit supplies a voltage (about 11.5V to V_{REG}) to the low-side MOSFET (LS-FET) gate driver. The charge pump requires an external capacitor between the CPA and CPB pins. External capacitor is also required between the VREG pin and ground.

The high-side MOSFET (HS-FET) gate driver supply is generated by both a bootstrap (BST) capacitor (C_{BST}) and an internal trickle-charge pump. Once the LS-FET turns on, the BST capacitors are charged to V_{REG}. This charge drives the HS-FET gate driver.

To keep the BST capacitors charged and to allow for 100% duty cycle, an internal trickle-charge pump supplies a small current (about 5µA) to overcome leakages that could discharge the BST capacitors. (7)

Sleep Mode

Pulling the nSLEEP pin low makes the device enter low-power sleep mode. In sleep mode, all internal circuits are disabled and all inputs are ignored. nSLEEP has an internal pull-down resistor. Pull nSLEEP high to make the device exit sleep mode. While exiting sleep mode, the MPQ6528 initiates a start-up sequence.

Input Logic

The ENx input pins (ENA and ENB) control the HS-FET and LS-FET gate driver outputs of each phase. If ENx is low, then the gate driver outputs are disabled and the phase's PWMx input is ignored. If ENx is high, the gate driver outputs are enabled and the PWMx input is recognized (see Table 1).

Table 1: Input Logic Truth Table

ENx	PWMx	SHx
High	High	V_{IN}
High	Low	GND
Low	x	Hi-Z

Fault Indication

The MPQ6528 has a fault indication pin (nFAULT) that indicates whether a fault has occurred (e.g. an over-current (OC) or over-temperature (OT) event). nFAULT is an open-drain output. If a fault occurs, nFAULT is pulled low. Once the fault condition is removed, nFAULT is pulled high via an external pull-up resistor.

Short-Circuit Protection (SCP) (Drain Source Voltage Sensing)

The MOSFET's drain-source voltage (V_{DS}) sensing circuitry protects the power stage from damage caused by high currents. It senses the voltage drop across each MOSFET. This voltage is proportional to the on resistance ($R_{DS(ON)}$) of the MOSFET and the current (I_{DS}) passing through it. If this voltage exceeds the OC_REF voltage (V_{OC_REF}), then short-circuit protection (SCP) is triggered.

If a short circuit occurs, the gate driver outputs are latched off and the nFAULT pin is pulled low. The device remains latched off until it is reset by pulling nSLEEP high or by V_{IN} exceeding the UVLO threshold.

SCP can be disabled by connecting a 100kΩ resistor between the VREG and OC_REF pins.

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Over-Current Protection (OCP)

Output over-current protection (OCP) monitors the current through a low-side (LS) shunt resistor connected to the LS-FETs. This resistor is connected to the LSS input pin and the LS-FET source terminals. To disable OCP, connect the LSS pin and LS-FET source terminals directly to ground.

If the LSS voltage (V_{LSS}) (i.e. the voltage across the shunt resistor) exceeds the LSS OCP threshold (V_{OCP_LSS}, typically 0.5V), then OCP is triggered and the MPQ6528 latches off. The device remains latched off until it is reset by pulling nSLEEP high or by V_{IN} exceeding the UVLO threshold.

The LSS pin's shunt resistor sets the OCP current limit. (7)

OCP can be disabled by connecting a 100kΩ resistor between the VREG and OC_REF pins.

OCP Deglitch Time

Current spikes during switching transitions can be caused by the body diode reverse-recovery current or the load's distributed capacitance. This current spike requires filtering to prevent it from unintentionally triggering OCP. To avoid triggering OCP, an internal fixed deglitch time (t_{OCP}) blanks the V_{DS} monitor output while the outputs are switched.

Dead Time Adjustment

To prevent shoot-through in either phase, a dead time (t_{DEAD}) is inserted between when the HS-FET turns off and the LS-FET turns on, and vice versa.

Both phases' dead times are set by a dead-time resistor (R_{DT}) connected between the DT pin and ground. t_{DEAD} can be calculated with Equation (1):

$$t_{DEAD}(ns) = 60 \times R_{DT}(k\Omega) \quad (1)$$

If the DT pin is connected directly to ground, there is a minimum internal dead time (90ns).

Under-Voltage Lockout (UVLO) Protection

If V_{IN} drops below the UVLO threshold (typically 3.9V), then UVLO protection is triggered. The device's circuitry is disabled, and the internal logic is reset. Once V_{IN} exceeds 3.9V, the part starts up again and resumes normal operation.

If V_{REG} drops below its threshold (typically 7.6V), the gate driver outputs are disabled and the nFAULT pin is pulled low. Once V_{REG} exceeds 7.6V, the part resumes normal operation.

Thermal Shutdown

If the die temperature exceeds its safe threshold (190°C), the MPQ6532 shuts down. Once the die temperature drops below 160°C, the part starts up again and resumes normal operation. There is a hysteresis of 30°C.

PCB Mounting

Conformal coating may be required after mounting the device on the PCB to comply with IPC-2221 or IPC-9592 standards.

Note:

7) For more information, see the Application Information section on page 14.

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APPLICATION INFORMATION

Selecting the Input Voltage (V_{IN})

V_{IN} supplies power to the device, and must be properly bypassed via a capacitor connected to ground. The MPQ6532 has a 5V to 60V operating V_{IN} range.

To avoid damaging the device, V_{IN} should not exceed the absolute maximum ratings (see the Absolute Maximum Ratings section on page 5). In some applications, especially when mechanical energy is turning a generator motor, it may be necessary to use some form of over-voltage protection (OVP) (e.g. a TVS diode between the VIN pin and ground).

Selecting the Power MOSFETs

Proper power MOSFET selection is critical to designing a successful motor driver. To prevent damage from transient voltages caused by parasitic inductance, the MOSFET's breakdown voltage should exceed V_{IN} by at least 10V to 15V. For example, for 24V power supply applications, the MOSFETs' minimum breakdown voltage should be between 40V and 60V. A larger margin is recommended in high-current applications, as the transient voltages may also be higher.

Other factors, such as regenerative braking, can also inject current back into the power supply. Ensure that these factors do not increase V_{IN} enough to damage the components.

The MOSFETs should be able to safely pass the current required to run the motor. The highest current condition (typically as the motor starts up or is stalled) should be supported. This is called the motor stall current (I_{MOTOR}).

The MOSFET's on resistance ($R_{DS(ON)}$) should also be taken into consideration. The MOSFET dissipates power proportional to its $R_{DS(ON)}$ and the I_{MOTOR}. The MOSFET's power dissipation (P) can be calculated with Equation (2):

$$P = I_{MOTOR}^2 \times R_{DS(ON)} \quad (2)$$

Select an $R_{DS(ON)}$ that dissipates the generated heat safely for the desired I_{MOTOR}. In some applications, this may require special PCB design considerations and external heatsinks for the MOSFETs.

The MOSFETs' safe operating area (SOA) during a fault (e.g. a short circuit) should be considered.

The IC responds quickly in the event of a short; however, there is still a brief amount of time (about 3µs) where large currents may flow into the MOSFETs before the protection circuits identify the fault and shut down the part.

Selecting the External Capacitor

The MPQ6528 can provide a 9.5V to 13V V_{REG}, even if V_{IN} drops as low as 5V. V_{REG} is generated by an internal charge pump with an external capacitor.

The charge pump flying capacitor (C_{CP}) should be 470nF and rated to withstand the maximum V_{IN}. It is recommended to use a ceramic capacitor with X7R or X5R dielectrics. With a 470nF capacitor, V_{REG} can output approximately 10mA while V_{IN} is 5V. If the application does not require operation below 10V, then a 220nF capacitor can be used for C_{CP}.

A bootstrap (BST) capacitor (C_{BST}) provides the peak current required to turn on the HS-FET. C_{BST} is charged while the output is pulled low. Once the HS-FET turn on signal comes, C_{BST} turns on the HS-FET. If the output remains high for an extended period of time, then C_{BST} is charged via an internal trickle-charge pump.

Select a capacitor that meets the application's total charge requirement. If the HS-FET is on, then the charge stored in C_{BST} is transferred to the HS-FET gate. For simplification, C_{BST} can be estimated with Equation (3):

$$C_{BST}(nF) > 8 \times Q_G(nC) \quad (3)$$

Where Q_G is the total gate charge.

To avoid improper start-up, C_{BST} should not exceed 1µF.

For most applications, a 0.1µF to 1µF ceramic capacitor with X5R or X7R dielectrics and a minimum 25V rating is sufficient.

Place a bypass capacitor between the VREG pin and ground, as close to the device as possible. For most applications, a 10µF ceramic capacitor with X5R or X7R dielectrics and a minimum 25V rating is sufficient.

Place another bypass capacitor between the VIN pin and ground, as close to the device as possible. For most applications, a 0.1µF ceramic capacitor with X5R or X7R dielectrics and rating

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that accounts for V_{IN} is sufficient. A 0.1µF X5R or X7R ceramic capacitor rated for V_{IN} is recommended.

Depending on the power supply impedance, as well as the distance between the MOSFETs and the power supply, additional bulk capacitors may be required. It is recommended to use low-ESR, 47µF to 470µF electrolytic capacitors.

Selecting the Dead Time Resistor (R_{DT})

During the transition between when the HS-FET turns off and the LS-FET turns on (and vice versa), there is a short period of time during which neither the HS-FET or LS-FET is on. This dead time (t_{DEAD}) is required to prevent conduction overlap between the HS-FET and LS-FET, which can create a short circuit between the power supply and ground, known as shoot-through. Shoot-through causes large transient currents and can damage the MOSFETs.

Since motors are naturally inductive, I_{MOTOR} cannot stop immediately even if the MOSFETs are turned off. This recirculation current continues to flow in the original direction until the magnetic field has decayed.

Once the MOSFETs are turned off, this current flows through the body diode, which is an internal parasitic component of the MOSFET.

The body diodes have a higher voltage drop than the MOSFETs during conduction, which means that more power is dissipated during body diode conduction than during the MOSFET's on time. It is recommended to minimize t_{DEAD} to reduce the body diode conductance time; however, t_{DEAD} must be long enough to guarantee that the HS-FET and LS-FET do not turn on simultaneously.

t_{DEAD} can be set via the external resistor connected to the DT pin. Typically, a 1µs t_{DEAD} is sufficient. A 1µs t_{DEAD} requires a 20kΩ resistor on the DT pin. If a faster switching speed or a ≥30kHz pulse-width modulation (PWM) frequency is desired, set a shorter t_{DEAD}. If switching speed is reduced by the external gate resistors, a longer t_{DEAD} may be required.

Figure 2 shows a t_{DEAD} of about 300ns between the LS-FET off time and the HS-FET on time.

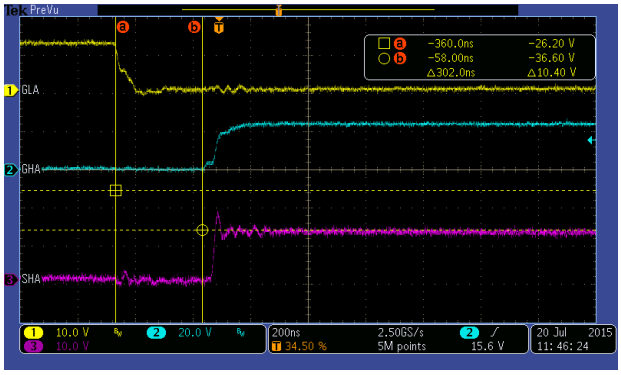


Figure 2: Dead Time between the LS-FET Off Time and HS-FET On Time

Selecting the LSS Resistor (R_{LSS})

If the LSS voltage (V_{LSS}) exceeds 500mV, then OCP is triggered. To avoid triggering OCP unintentionally, the external sense resistor should provide a voltage drop below 500mV at the maximum I_{MOTOR}. For example, when a 50mΩ resistor is used, a 10A current would cause a 500mV drop, triggering OCP.

This function can be disabled by connecting the LSS pin to ground.

Selecting the OC_REF Voltage (V_{OC_REF})

An internal comparator compares the voltage drop across each MOSFET to an external voltage on the OC_REF input pin. This voltage is typically provided by an external resistor divider from a power supply. If the drop across any MOSFET exceeds V_{OC_REF}, then SCP is triggered.

This function can be disabled by connecting the OC_REF and VREG via a 100kΩ resistor.

Gate Driver Considerations

The MOSFET gate characteristics affect the switching speed. For the maximum switching speed, connect the gate driver outputs to the MOSFET gates. It is recommended to add external components (e.g. resistors and diodes) to modify the MOSFET's turn-on and turn-off speed.

Adding external series resistance (typically 10Ω to 100Ω) limits the current that charges and discharges the MOSFET gate. This slows down the MOSFET's turn-on and turn-off speed. Slower turn-on and turn-off speed can reduce EMI and noise; however, slowing down the transition speed too much can result in large power dissipation during switching.

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In some applications, a slow turn-on and a fast turn-off are desired. To achieve this, place a series resistor in parallel with the diode (see Figure 3). During turn-on, the resistor limits the current flowing into the gate. During turn-off, the gate is discharged through the diode.

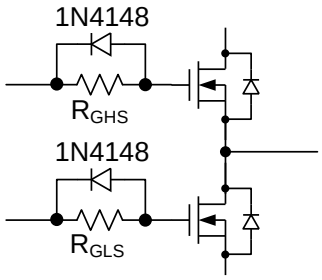


Figure 3: Gate Circuit for Fast Turn-Off

Figure 4 shows the LS-FET gate, HS-FET gate, and phase node (output) without any series resistance. The gates transition quickly, and the resulting phase node rise time (t_{RISE}) is fast. (8)

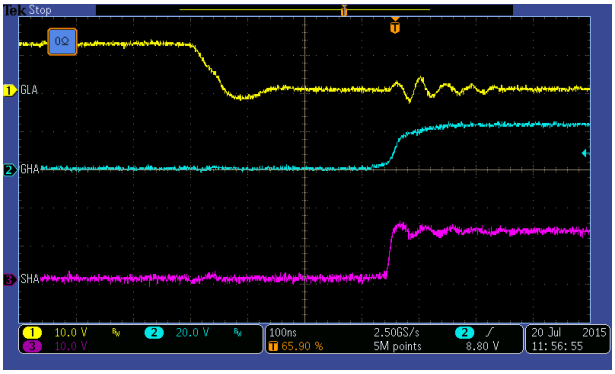


Figure 4: Switching with No Series Resistance

Figure 5 shows the effect of adding a 100Ω series resistor between the GLA pin and the LS-FET gate, as well as the GHA pin and the HS-FET gate. Adding the series resistor slows the phase node's t_{RISE}. (9)

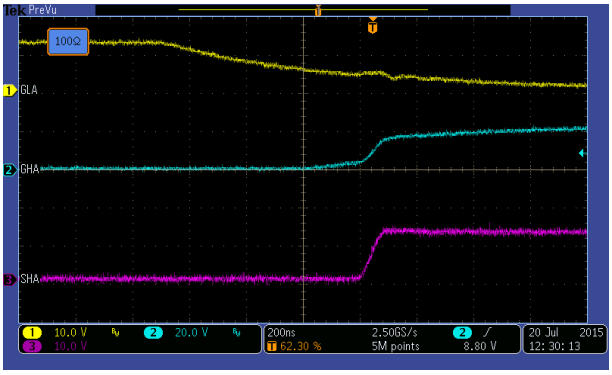


Figure 5: Switching with 100Ω Series Resistance

Figure 6 shows the effect of adding a 1N4148 diode in parallel with the 100Ω series resistor, and the cathode connected to the IC. The LS-FET gate's fall time (t_{FALL}) is fast compared to the HS-FET gate's t_{RISE}.

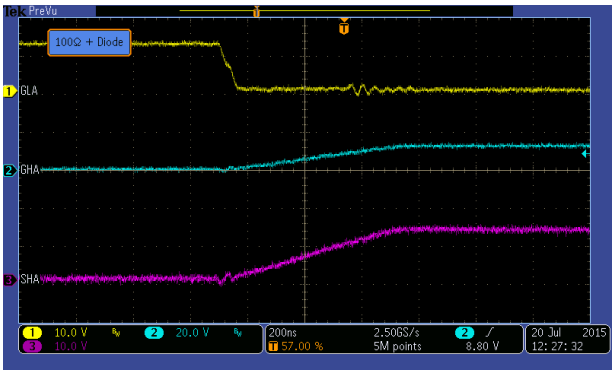


Figure 6: Switching with Resistance and a Diode

Notes:

8) Scale is 100ns/div.
9) Scale is 200ns/div.

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. The pre-driver is designed to accommodate negative undershoot; however, excessive undershoot can result in unpredictable operation and damage to the IC. For the best results, refer to Figure 7 and follow the guidelines below:

1. Connect the HS-FET source and the LS-FET drain. Use surface-mounted N-channel MOSFETs to make the connection as short and direct as possible in order to reduce parasitic inductance and avoid a negative undershoot.
2. Use wide copper areas for the high-current paths.
3. Use wide copper traces to connect the low-side sense resistor, which is composed of five resistors in parallel (R13, R14, R15, R16 and R17), to GND and the LS-FET source terminals.
4. Place the charge pump and the VIN bypass capacitors as close to the IC as possible.
5. Connect the bypass capacitors' grounded side to a ground plane (the ground plane should be connected to the GND pin and the exposed pad).
6. Keep the high-current ground path that runs between VIN, the input bulk capacitor (C1), and the MOSFETs away from the ground plane.

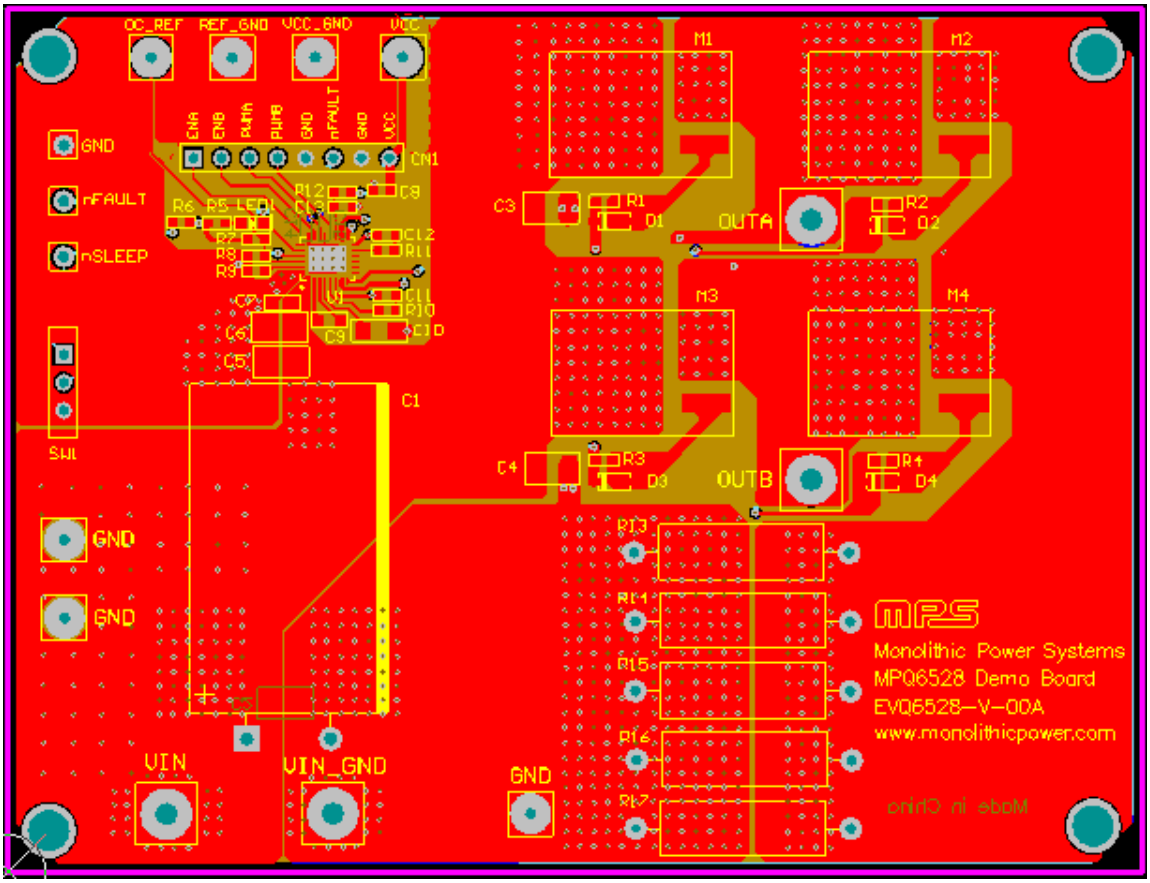


Figure 7: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

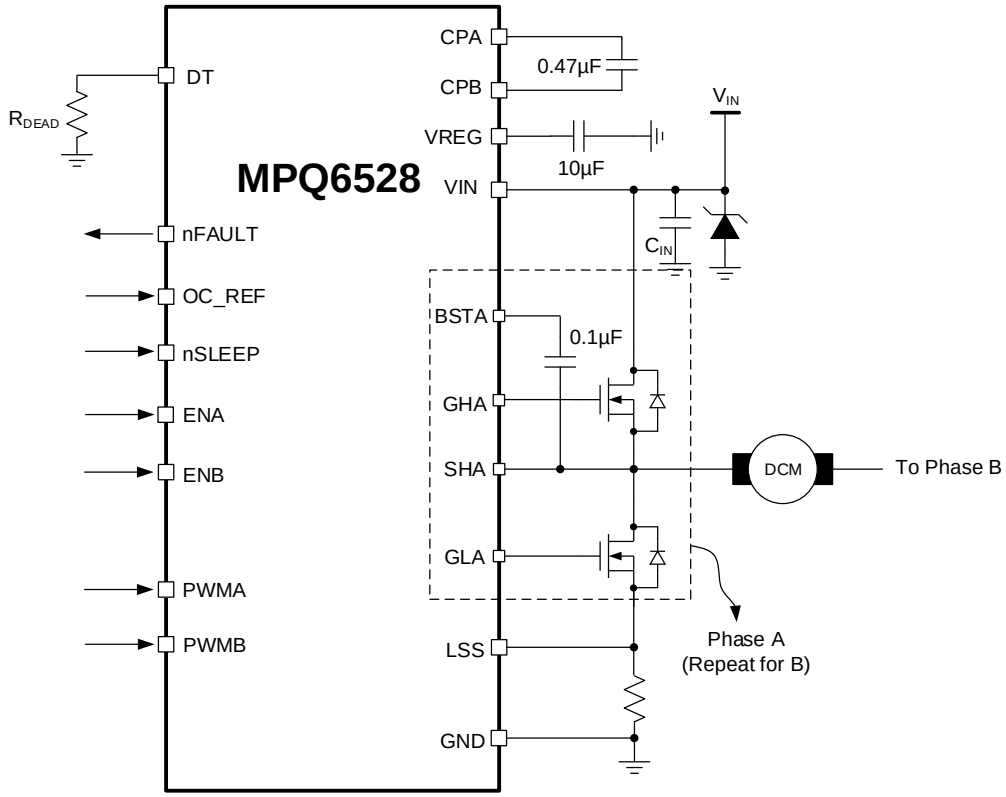
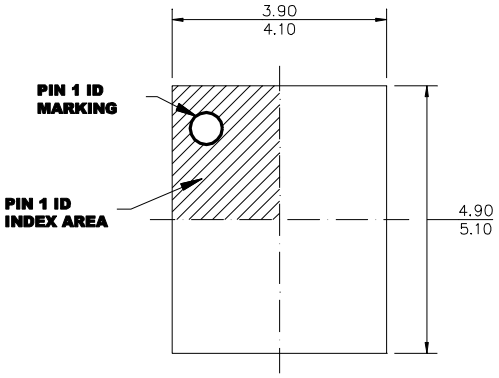


Figure 8: Typical Application Circuit

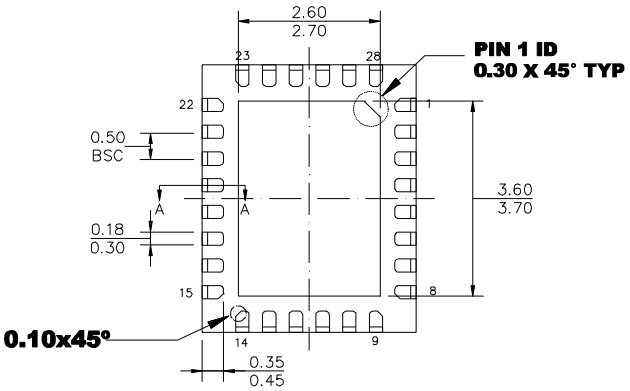
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PACKAGE INFORMATION

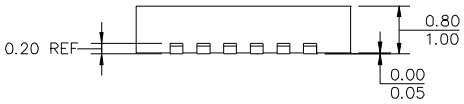
QFN-28 (4mmx5mm)
Wettable Flank



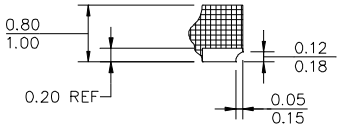
TOP VIEW



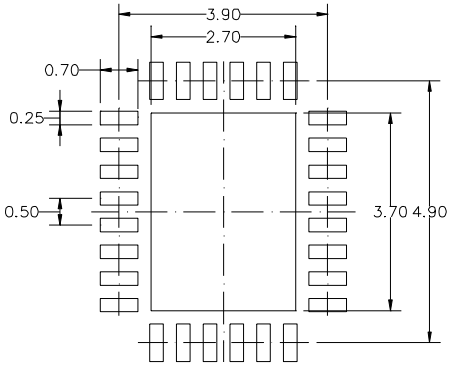
BOTTOM VIEW



SIDE VIEW



SECTION A-A



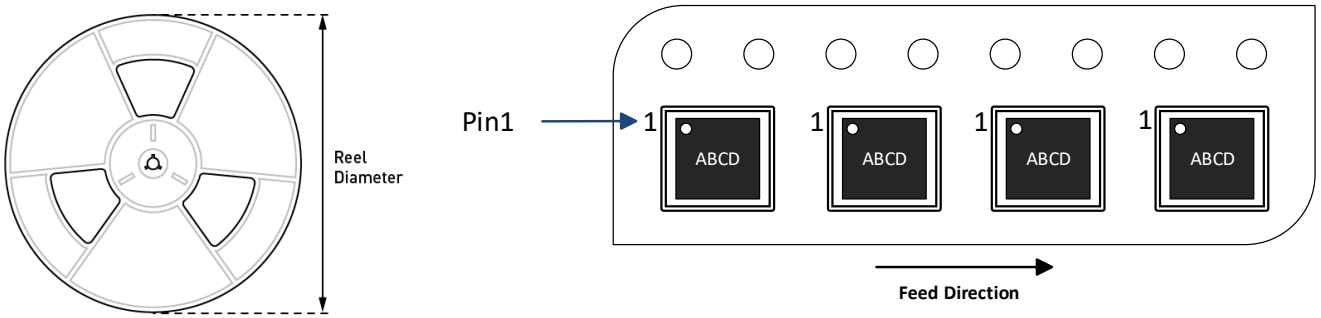
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package	Quantity /Reel	Quantity /Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6528GVE-AEC1-Z	QFN-28 (4mmx5mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	09/08/2021	Initial Release	-

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