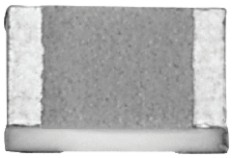
ESCC (e) 4001/023 Qualified R Failure Rate High Precision (10 ppm/°C, 0.05 %) Thin Film Chip Resistors



DESIGN SUPPORT TOOLS

click logo to get started

3D Models Available

Vishay Sfernice Thin Film division holds ESCC QML qualification (ESCC technology flow qualification).

These HiRel components are ideal for low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics Y (± 10 ppm/°C).

FEATURES

HALOGEN FREE

- Load life stability at ± 70 °C for 2000 h: 0.25 % under Pn
- Temperature coefficient to: 10 ppm/°C
- Very low noise (< -35 dB) and voltage coefficient (< 0.01 ppm/V)
- Resistance range: 100 Ω to 3.01 MΩ (depending on size)
- Tolerances down to 0.05 %
- SnPb terminations over nickel barrier
- ESCC 4001 (generic specification)
- ESCC 4001/023 (detail specification)
- ESCC qualified
- R failure rate (0.01 % per 1000 h)
- SMD wraparound chip resistor
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	ESCC VARIANT NUMBER	RESISTANCE RANGE Ω	RATED POWER AT +70 °C (Pn) W	LIMITING ELEMENT VOLTAGE (UL) V	INSULATION VOLTAGE (U_i) V	TOLERANCE ± %	TEMPERATURE COEFFICIENT ± ppm/°C
PFRR 0402 (e)	0402	15	100 to 150K	0.05	40	50	0.05, 0.1	10, 25
PFRR 0603 (e)	0603	09	100 to 500K	0.1	50	100	0.05, 0.1	10, 25
PFRR 0805 (e)	0805	10	100 to 750K	0.125	100	200	0.05, 0.1	10, 25
PFRR 1206 (e)	1206	11	100 to 3.5M	0.25	150	300	0.05, 0.1	10, 25
PFRR 2010 (e)	2010	12	100 to 6M	0.50	200	300	0.05, 0.1	10, 25

CLIMATIC SPECIFICATIONS

Operating temperature range	-55 °C; +155 °C
Soldering temperature (T_{sol})	260 °C, immersion 10 s

MECHANICAL SPECIFICATIONS

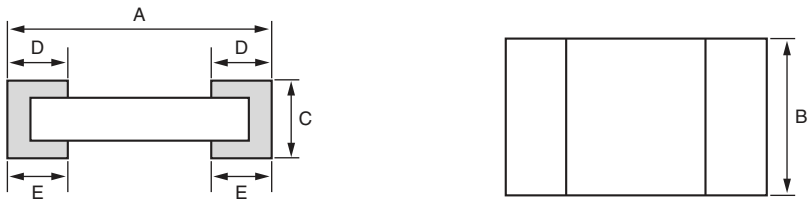
Substrate material	Alumina
Technology	Thin Film
Film	**Nickel Chromium** with mineral passivation
Protection	Epoxy and Silicon
Terminations	**B type:** SnPb over nickel barrier for solder reflow

QUALIFIED OHMIC RANGE: MAX. VALUE

PFRR0402	PFRR0603	PFRR0805	PFRR1206	PFRR2010
100 kΩ	261 kΩ	301 kΩ	1 MΩ	3.01 MΩ

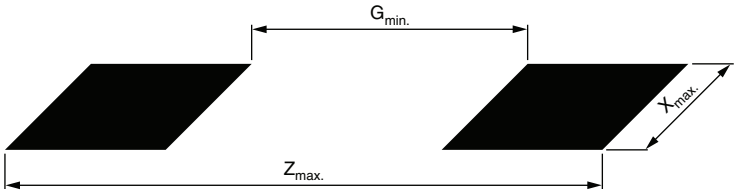
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DIMENSIONS in millimeters



VARIANT NUMBER	STYLE	A		B		C		D		E	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
09	0603	1.39	2.16	0.62	1.01	0.25	1.02	0.17	0.51	0.25	0.51
10	0805	1.78	2.55	1.14	1.53	0.25	1.02	0.17	0.51	0.25	0.51
11	1206	2.87	3.64	1.47	1.86	0.25	1.02	0.17	0.51	0.25	0.51
12	2010	4.95	5.72	2.41	2.8	0.25	1.02	0.35	0.85	0.35	0.85
15	0402	0.87	1.64	0.47	0.86	0.25	1.02	0.09	0.38	0.12	0.38

LAND PATTERN DIMENSIONS in millimeters



CHIP SIZE	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0402	1.55	0.15	0.73
0603	2.37	0.35	0.98
0805	2.76	0.74	1.40
1206	3.91	1.85	1.73
2010	5.93	3.71	2.67

Note

- Suggested land pattern: According to IPC-7351

TRACEABILITY DEFINITIONS

The two major traceability elements are defined as:

- The primary process lot number named Front End lot (FE lot). One “FE lot”is composed of several wafers issued from the same thin film deposition sequence.
- The date code named Batch Number(BN). The “BN” is defined after completion of the end of production testing sequence.

The lot homogeneity is given by the “FE lot” and not by the “BN”.

According to the applied rules validated by the ESCC through the product qualification, the following situations are agreed:

- Parts coming from different “FE lost” might have the same “BN”.
- A maximum of two different “BN” might be applied to the same “FE lot” to enable the use of overruns from a previous PO.
- Unless requested / approved by the customer the “BN” will be 2 years old maximum.

SPECIFIC TRACEABILITY REQUIREMENTS

The following specific requirements have to be treated as:

- A customer who requires “Lot Homogeneity” has to mention it on the PO as “SINGLE PRODUCTION LOT”.
- A customer who requires “Lot Homogeneity” in addition to a “Single Batch Number” has to mention it on the PO as “SINGLE PRODUCTION LOT AND OPTION R0101”.

END OF PRODUCTION TESTING

Mandatory testing performed at the end of the production process:

- 100 % overload: Voltage $\sqrt{(6.25\ P_n \times R_n)}$ or 2 U_L whichever is less - duration 2 s

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GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: PFRR0603Y1003BBT (preferred part number format)

P	F	R	R	0	6	0	3	Y	1	0	0	3	B	B	T

TYPE	TCR	OHMIC VALUE	TOLERANCE	TERMINATION	PACKAGING
PFRR0402 **PFRR0603** **PFRR0805** **PFRR1206** **PFRR2010**	**Y** = ± 10 ppm/°C **E** = ± 25 ppm/°C	The first three digits are significant figures and the last digit specifies the number of zeros to follow. Example: **3901** = 3900 Ω **1004** = 1 MΩ	**W** = ± 0.05 % **B** = ± 0.10 %	**B**: SnPb over nickel barrier	For more information see Codification of Packaging table

CODIFICATION OF PACKAGING

CODE 18	PACKAGING
WAFFLE PACK	
W	100 min., 1 mult
WA	100 min., 100 mult (available only in size 1206)
PLASTIC TAPE (in standard for all sizes)	
T	100 min., 1 mult
TA	100 min., 100 mult
TB	250 min., 250 mult
TC	500 min., 500 mult
TD	1000 min., 1000 mult
TE	2500min., 2500 mult
TF	Full tape (quantity depending on size of chips)
PAPER TAPE (Available for 0402, 0603, 0805 and 1206. Please consult Vishay Sfernice for 2010 size.)	
PT	100 min., 1 mult
PA	100 min., 100 mult
PB	250 min., 250 mult
PC	500 min., 500 mult
PD (not available for size 0402)	1000 min., 1000 mult
PE (not available for size 0402)	2500min., 2500 mult
PF (not available for size 0402)	Full tape (quantity depending on size of chips)

GLOBAL PART NUMBER INFORMATION

ESCC Code

4	0	0	1	0	2	3	0	9	R	1	0	0	3	B	1

ESCC SPEC	VARIANT	FAILURE RATE	OHMIC VALUE	TOLERANCE	TCR
4001023	**0402** = 15 **0603** = 09 **0805** = 10 **1206** = 11 **2010** = 12	**R**	The first three digits are significant figures and the last digit specifies the number of zeros to follow. Example: **3901** = 3900 Ω **1004** = 1 MΩ	**W** = ± 0.05 % **B** = ± 0.10 %	**1** = ± 10 ppm/°C **2** = ± 25 ppm/°C

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Vishay Sfernice thin film is the first passive manufacturer to hold the ESCC Technology Flow Qualification, official certificate is available on ESCIES web site https://escies.org/ReadArticle?docId=727).

This qualification open the door to a new concept at ESA: The Failure Rate option (similar to the one offered in the MIL system), for instance R failure rate: 0.01 % per 1000 h.

New specifications describing this new concept have been released by the ESA:

2544001: Requirements for the Technology Flow Qualification of Film Resistors
https://escies.org/escc/specifications/2544001.pdf

26000: Failure Rate Level Sampling Plans and Procedures
https://escies.org/escc/specifications/26000.pdf

21300: Terms, Definitions, Abbreviations, Symbols and Units
https://escies.org/escc/specifications/21300.pdf

21700: General Requirements for the Marking of the ESCC Components
https://escies.org/escc/specifications/21700.pdf

4001: Generic Specification Resistors Fixed Film
https://escies.org/escc/specifications/4001.pdf

4001023: Resistors, Fixed, Chip, Thin Film, Type PHR and PFRR
https://escies.org/escc/specifications/4001023.pdf

Parts are delivered with space C.O.C.

Parts undergo 100 % overload at end of production process.

ESCC/PFRR CODIFICATION CORRESPONDANCE TABLES

VARIANT	MODEL	CASE SIZE	TERMINATION
15	PFRR	0402	B (tin/lead)
09	PFRR	0603	B (tin/lead)
10	PFRR	0805	B (tin/lead)
11	PFRR	1206	B (tin/lead)
12	PFRR	1210	B (tin/lead)

TEMPERATURE COEFFICIENT	ESCC CODE	PFRR CODE
10 ppm/°C (- 55 °C; + 155 °C)	1	Y
25 ppm/°C (- 55 °C; + 155 °C)	2	E

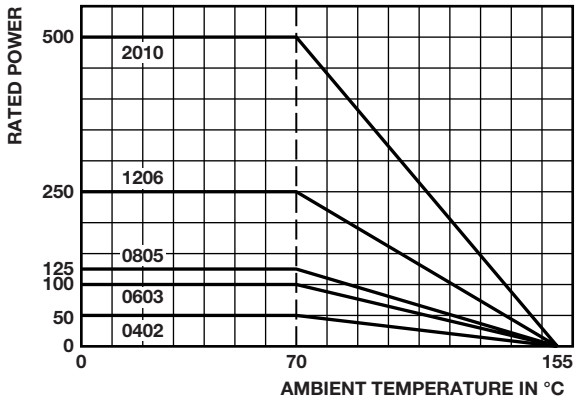
TOLERANCE	MODEL	CASE SIZE
0.1 %	B	B
0.05 %	W	W

PACKAGING

Two types of packaging are available: waffle-pack and tape and reel.

SIZE	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
	WAFFLE PACK 2" × 2"	TAPE AND REEL		
		MIN.	MAX.	
0402	340	100	5000	8 mm
0603	100			
0805			4000	
1206	140			
2010	60		1000	

POWER DERATING CURVE



EXTENDED FEATURES

You may consult Vishay Sfernice for chip sizes, ohmic values and tolerances outside of the qualified range.

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PERFORMANCE				
TEST	CONDITIONS	REQUIREMENTS		TYPICAL
		ESA/SCC 4001/023	MIL-PRF-55342G	
Short time overload	$U = \sqrt{(6.25 \text{ Pr x Rn})}$ $U_{max.} < 2$ UL - 2 s	± 0.05 % + (0.05 Ω x 100/Rn)	0.10 %	± 0.01 %
Rapid temperature change	- 55 °C/+ 155 °C 5 cycles CEI 66-2-14 Test Na	± 0.05 % + (0.05 Ω x 100/Rn)	0.1 % (for 100 cycles)	± 0.01 % ± 0.015 % (for 500 cycles)
Soldering (thermal shock)	260 °C/10 s CEI 68-2-20 A Test T6 (met. 1A)	± 0.05 % + (0.05 Ω x 100/Rn)	-	± 0.005 %
Terminal strength: Adhesion bend strength of end plated facing	CEI 115-1 Clause 4.32 CEI 115-1 Clause 4.33	± 0.05 % + (0.05 Ω x 100/Rn)	-	± 0.01 %
Climatic sequence	CEI 67-2-1/CEI 68-2-2 CEI 67-2-13/CEI 68-2-30	± 0.10 % + (0.05 Ω x 100/Rn)	-	± 0.02 % Insulation resistance > 1 GΩ
Load life	2000 h Pr at + 70 °C 90'/30' cycle 8000 h	± 0.25 % + (0.05 Ω x 100/Rn) 1 % + (0.05 Ω x 100/Rn)	0.5 %	± 0.05 % (8000 h) Insulation resistance > 1 GΩ
High temperature exposure	2000 h Pr at + 155 °C CEI 68-2-20A Test B	± 0.15 % + (0.05 Ω x 100/Rn)	± 0.10 % (duration 1000 h)	± 0.05 % Insulation resistance > 1 GΩ

CODIFICATION OPTIONS ON TWO DIGITS	
OPTION	OPTION 2 DIGITS
...	...
0099	99
0100	0A
0101	0B
0102	0C
0103	0D
0104	0E
0105	0F
...	...
0124	0Y
0125	0Z
0126	1A
0127	1B
0128	1C
...	...
0320	8M
0321	8N
0322	8O
0323	8P
0324	8Q
0325	8R
...	...

CODIFICATION OF SIZES	
CODE 18	CODE 40
9	0402
C	0603
D	0805
H	1206
J	2010

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