MP1567

1.2A Synchronous Rectified Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1567 is a 1.2A, 800KHz DC to DC converter designed for low voltage applications requiring high efficiency. Capable of providing output voltages as low as 0.9V from a 3.3V supply voltage, the MP1567 eliminates the need for a 5V rail, providing over 90% efficiency via synchronous rectification and eliminating heat issues in confined spaces. Soft-start operation protects internal circuitry from hard turn on issues. Switching at 800KHz reduces the size of external components and thereby reduces board space.

The MP1567 includes cycle-by-cycle current limiting and under voltage lockout. Internal power switches combined with the tiny 10-pin MSOP or QFN packages provide a solution requiring a minimum of space.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV0033 (MP1567DK)	2.5"X x 2.0"Y x 0.7"Z
EV0059 (MP1567DK)	2.5"X x 2.0"Y x 0.4"Z
EV0060 (MP1567DQ)	2.5"X x 2.0"Y x 0.4"Z

FEATURES

- 1.2A Output Current
- Synchronous Rectified
- Internal 180mΩ and 220mΩ Power Switches
- V_{IN} Range of 2.6V to 6V
- Over 90% Efficiency
- Zero Current Shutdown Mode
- Under Voltage Lockout Protection
- Soft-Start Operation
- Thermal Shutdown
- Internal Current Limit (Source & Sink)
- Tiny 10-Pin MSOP or QFN Packages
- **Evaluation Boards Available**

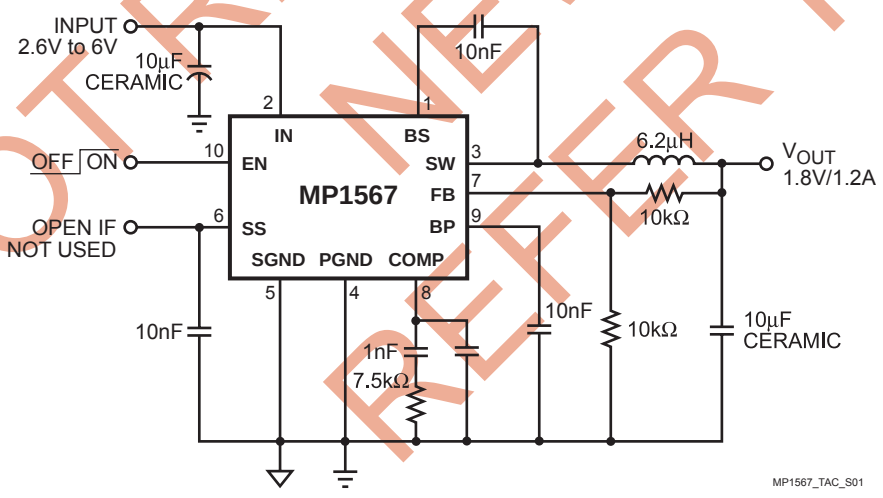
APPLICATIONS

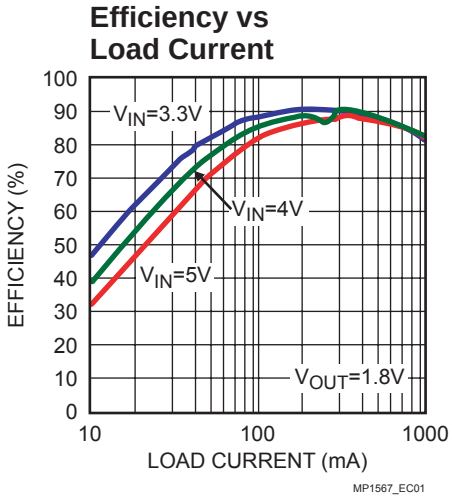
- SOHO Routers, PCMCIA Cards, Mini PCI
- Handheld Computers, PDAs
- Cell Phones
- Digital Video Cameras
- Small LCD Displays

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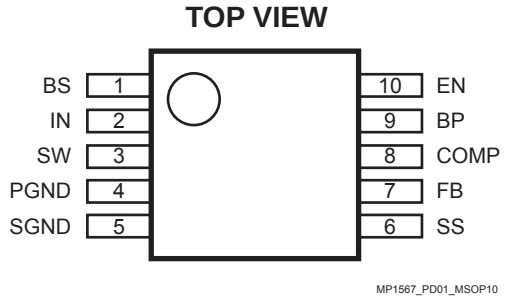
TYPICAL APPLICATION





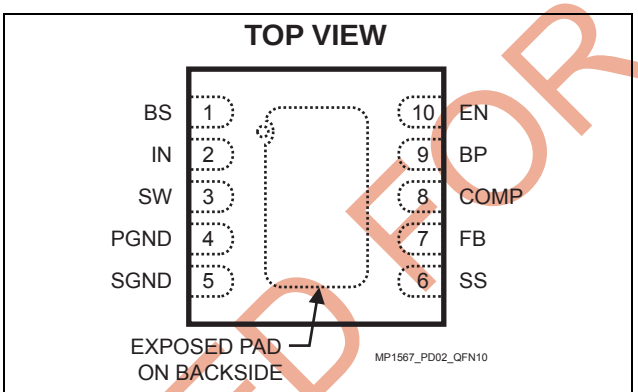
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PACKAGE REFERENCE



Part Number*	Package	Temperature
MP1567DK	MSOP10	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP1567DK–Z)
For Lead Free, add suffix –LF (eg. MP1567DK–LF–Z)



Part Number**	Package	Temperature
MP1567DQ	QFN10 (3mm x 3mm)	–40°C to +85°C

** For Tape & Reel, add suffix –Z (eg. MP1567DQ–Z)
For Lead Free, add suffix –LF (eg. MP1567DQ–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Input Supply Voltage V_{IN} 6.5V
SW Voltage V_{SW} ..... –0.3V to V_{IN} + 0.3V
BS to SW Voltage ..... –0.3V to +6V
Voltage at All Other Pins ..... –0.3V to +6V
Storage Temperature..... –55°C to +150°C

Recommended Operating Conditions (2)

Input Supply Voltage V_{IN} ..... 2.6V to 6V
Output Voltage V_{OUT} ..... 0.9V to 4.5V
Operating Temperature..... –40°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
MSOP10	150	65	°C/W
3x3 QFN10	50	12	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.6		6	V
Input Undervoltage Lockout				2.2		V
Input Undervoltage Lockout Hysteresis				100		mV
Shutdown Supply Current		V_{EN} ≤ 0.3V		0.5	1.0	µA
Operating Supply Current		V_{EN} > 2V, V_{FB} = 1.1V		1.2	1.8	mA
BP Voltage	V_{BP}	V_{IN} = 2.6 to 6V		2.4		V
EN Input Low Voltage	V_{IL}				0.4	V
EN Input High Voltage	V_{HL}		1.5			V
EN Hysteresis				100		mV
EN Input Bias Current					1	µA
Oscillator						
Switching Frequency	f_{SW}			800		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	85			%
Minimum On Time	t_{ON}			200		ns

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ELECTRICAL CHARACTERISTICS *(continued)*

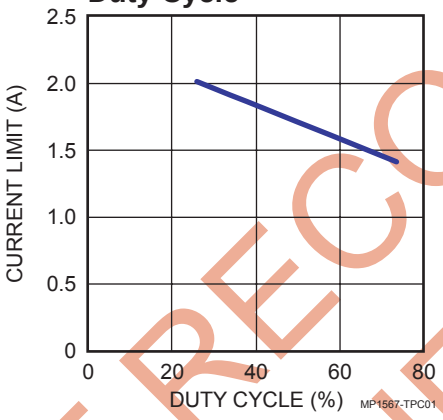
V_{IN} = 5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Error Amplifier						
Voltage Gain	A_{VEA}			400		V/V
Transconductance	G_{EA}			300		µA/V
COMP Maximum Output Current				±30		µA
FB Regulation Voltage	V_{FB}		875	905	935	mV
FB Input Bias Current	I_{FB}	FB = 0.9V		–100		nA
Soft-Start						
Soft-Start Current	I_{SS}			2		µA
Output Switch On-Resistance						
Switch On Resistance		V_{IN} = 5V		265		mΩ
		V_{IN} = 3V		330		mΩ
Synchronous Rectifier On Resistance		V_{IN} = 5V		220		mΩ
		V_{IN} = 3V		270		mΩ
Switch Current Limit (Source)			1.5	2.0		A
Synchronous Rectifier Current Limit (Sink)				350		mA
Thermal Shutdown				160		°C

TYPICAL PERFORMANCE CHARACTERISTICS

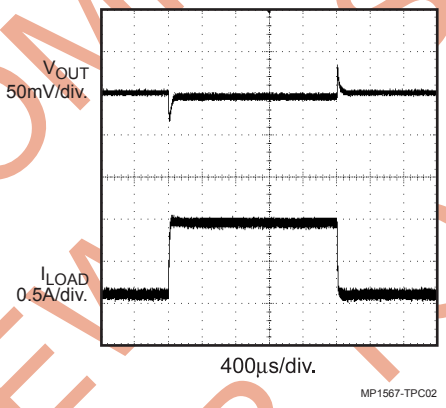
V_{IN} = 3.3V, V_{OUT} = 1.8V, T_A = +25°C, unless otherwise noted.

Current Limit vs. Duty Cycle



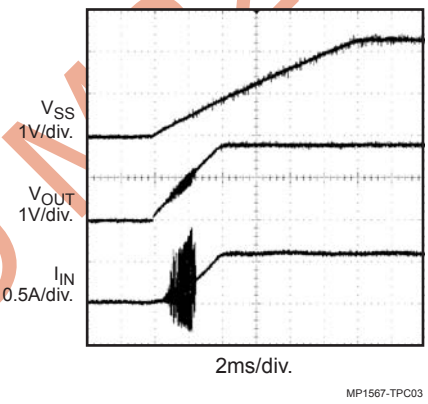
Load Transient

0.1A to 1A Load Step



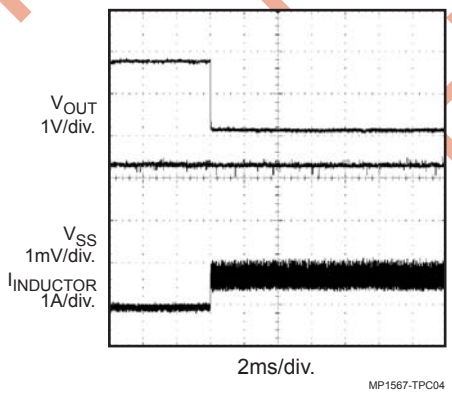
Soft-Start

R_{OUT} = 1.8Ω

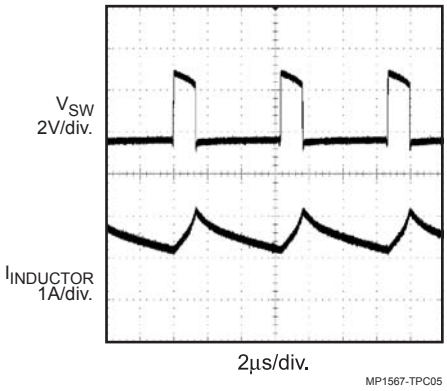


Output Short Circuit

I_{OUT} = 1.2A



Steady State



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PIN FUNCTIONS

Pin#	Name	Function
1	BS	Power Switch Boost. BS powers the gate of the high-side N-Channel power MOSFET switch. Connect a 10nF or greater capacitor between BS and SW.
2	IN	Internal Power Input. IN supplies the power to the MP1567 through the internal LDO regulator. Bypass IN to PGND with a 10µF or greater capacitor. Connect IN to the input source voltage.
3	SW	Output Switching Node. SW is the source of the high-side N-Channel switch and the drain of the low-side N-Channel switch. Connect the output LC filter between SW and the output.
4	PGND	Power Ground. PGND is the source of the N-Channel MOSFET synchronous rectifier. Connect PGND to SGND as close to the MP1567 as possible.
5	SGND	Signal Ground.
6	SS	Soft-Start Input. Place a capacitor from SS to SGND to set the soft-start period. The MP1567 sources 2µA from SS to the soft-start capacitor at start up. As the voltage at SS rises, the feedback threshold voltage increases to limit inrush current at start up.
7	FB	Feedback Input. FB is the inverting input of the internal error amplifier. Connect a resistive voltage divider from the output voltage to FB to set the output voltage.
8	COMP	Compensation Node. COMP is the output of the error amplifier. Connect a series RC network to compensate the regulation control loop.
9	BP	Internal 2.4V Regulator Bypass. Connect a 10nF capacitor between BP and SGND to bypass the internal regulator. Do not apply any load to BP.
10	EN	On/Off Control Input. Drive EN high to turn on the MP1567; low to turn it off. For automatic startup, connect EN to IN.

OPERATION

The MP1567 measures the output voltage through an external resistive voltage divider and compares that to the internal 0.9V reference to generate the error voltage at COMP. The current-mode regulator uses the voltage at COMP and compares it to the inductor current to regulate the output voltage. The use of current-mode regulation improves transient response and improves control loop stability.

At the beginning of each cycle, the high-side N-Channel MOSFET is turned on, forcing the inductor current to rise. The current at the drain of the high-side MOSFET is internally measured and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage at COMP. When the inductor current raises sufficiently, the PWM comparator turns off the high-side switch and turns on the low-side switch, forcing the inductor current to decrease. The average inductor current is controlled by the voltage at COMP, which in turn, is controlled by the output voltage. Thus the output voltage controls the inductor current to satisfy the load.

Since the high-side N-Channel MOSFET requires voltage above V_{IN} to drive its gate, a bootstrap capacitor from SW to BS is required to drive the high-side MOSFET gate. When SW is driven low (through the low-side MOSFET), the BS capacitor is internally charged. The voltage at BS is applied to the high-side MOSFET gate to turn it on, and maintains that voltage until the high-side MOSFET is turned off and the low-side MOSFET is turned on, and the cycle repeats. Connect a 10nF or greater capacitor from BS to SW to drive the high-side MOSFET gate. Using a larger capacitor does little to improve performance.

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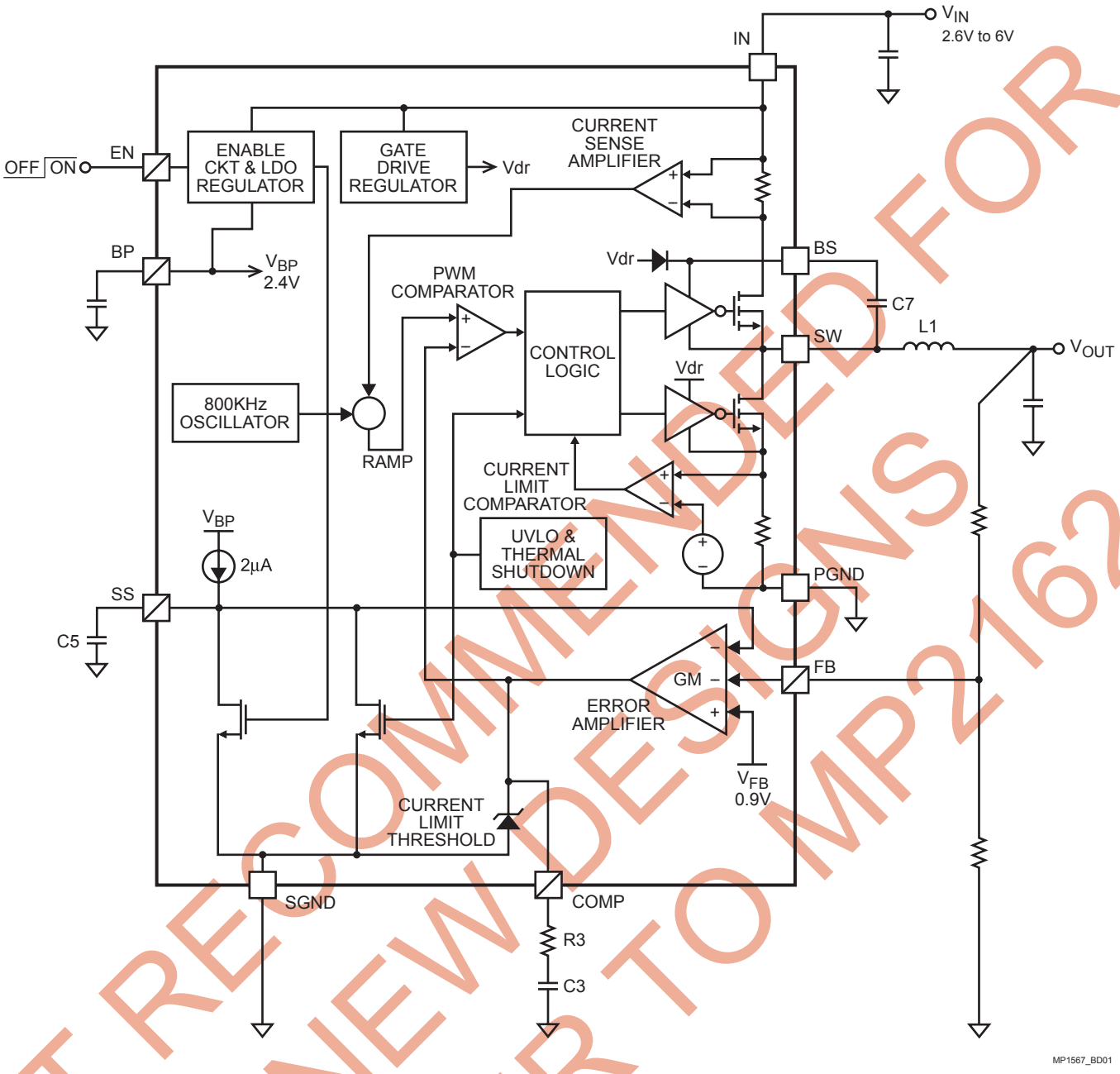


Figure 1—Functional Block Diagram

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APPLICATION INFORMATION

COMPONENT SELECTION

Internal Low-Dropout Regulator

The internal power to the MP1567 is supplied from the input voltage through an internal 2.4V low-dropout linear regulator, whose output is BP. Bypass BP to SGND with a 10nF or greater capacitor to insure the MP1567 operates properly. The internal regulator cannot supply more current than is required to operate the MP1567, therefore do not apply any external load to BP.

Soft-Start

The MP1567 includes a soft-start timer that slowly ramps the output voltage at startup to prevent excessive current at the input. This prevents premature termination of the battery voltage at startup due to input current overshoot at startup.

When power is applied to the MP1567 a 2μA internal current source charges the external capacitor at SS. As the capacitor charges, the voltage at SS will rise. The MP1567 internally limits the feedback threshold voltage at FB to that of the voltage at SS. This forces the output voltage to rise at the same rate as the voltage at SS, forcing the output voltage to ramp linearly from 0V to the desired regulation voltage during soft-start. The soft-start period is determined by the equation:

$$t_{SS} = 0.45 \times C5$$

Where C5 (in nF) is the soft-start capacitor from SS to GND, and t_{SS} (in ms) is the soft-start period. Determine the capacitor required for a given soft-start period by the equation:

$$C5 = 2.22 \times t_{SS}$$

Use values for C5 between 10nF and 22nF to set the soft-start period (between 4ms and 10ms).

Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.9V feedback threshold voltage. Use 10kΩ for the low-side resistor of the voltage divider. Determine the high side resistor by the equation:

$$R2 = \frac{V_{OUT} - V_{FB}}{\left(\frac{V_{FB}}{R1}\right)}$$

Where R2 is the high-side resistor, R1 is the low-side resistor, V_{OUT} is the output voltage and V_{FB} is the feedback regulation threshold.

For R1 = 10kΩ and V_{FB} = 0.9V, then

$$R2(k\Omega) = 11.1k\Omega\ (V_{OUT} - 0.9V)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, so a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will also suffice.

Use an input capacitor with a value greater than 10μF. The capacitor can be electrolytic, tantalum or ceramic. However, since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with a RMS current rating greater than 1/2 of the DC load current.

For insuring stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller high quality 0.1μF ceramic capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the MP1567.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum or low ESR electrolytic capacitors are recommended.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, and so the

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Out put voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated to be:

$$V_{RIPPLE} = 1.4 \times V_{IN} \times \left(\frac{f_{LC}}{f_{SW}}\right)^2$$

Where V_{RIPPLE} is the output ripple voltage, V_{IN} is the input voltage, f_{LC} is the resonant frequency of the LC filter and f_{SW} is the switching frequency. In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE} = \Delta I \times R_{ESR}$$

Where ΔI is the inductor ripple current, and R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple requirements of the design. A 10μF ceramic capacitor is suitable for most applications.

Selecting the Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current that will results in lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance and/or lower saturation current. Choose an inductor that does not saturate under the worst-case load conditions. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum load current. Make sure that the peak inductor current (the load current plus half the peak-to-peak inductor ripple current) is below 2A to prevent loss of regulation due to the current limit.

Calculate the required inductance value by the equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I}$$

Compensation

The system stability is controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system.

The DC loop gain is:

$$A_{VDC} = A_{VEA} \times G_{CS} \times R_{LOAD} \times \left(\frac{V_{FB}}{V_{OUT}}\right)$$

Where A_{VEA} is the transconductance error amplifier voltage gain, G_{CS} is the current sense gain (roughly the output current divided by the voltage at COMP) and R_{LOAD} is the load resistance (V_{OUT}/I_{OUT} where I_{OUT} is the output load current)

The system has 2 poles of importance, one is due to the compensation capacitor (C3), and the other is due to the load resistance and the output capacitor (C2). The first is:

$$f_{P1} = \frac{G_{EA}}{2\pi \times A_{VEA} \times C3}$$

Where P1 is the first pole and G_{EA} is the error amplifier transconductance (300μA/V). The second is:

$$f_{P2} = \frac{1}{2\pi \times R_{LOAD} \times C2}$$

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). The zero is:

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C3}$$

If large value capacitors with relatively high equivalent-series-resistance (ESR) are used, the zero due to the capacitance and ESR of the output capacitor can be compensated by a third pole set by R3 and C4. This pole is:

$$f_{P3} = \frac{1}{2\pi \times R3 \times C4}$$

The system crossover frequency (the frequency where the loop gain drops to 1, or 0dB) is important. Set the crossover frequency to

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75KHz or lower to insure stable operation. Lower crossover frequencies result in slower response and worse transient load recovery. Higher crossover frequencies degrade the phase and/or gain margins and can result in instability.

Choosing the Compensation Components

The values of the compensation components given in Table 1 yield a stable control loop for the output voltage and capacitor given.

Table 1—Compensation Values for Typical Output Voltage/Capacitor Combinations

V_{OUT}	C2	R3	C3	C4
1.8V	4.7µF Ceramic	3.3kΩ	2.2nF	None
2.5V	4.7µF Ceramic	5.1kΩ	1.5nF	None
3.3V	4.7µF Ceramic	6.8kΩ	1.2nF	None
1.8V	10µF Ceramic	7.5kΩ	1nF	None
2.5V	10µF Ceramic	10kΩ	820pF	None
3.3V	10µF Ceramic	10kΩ	820pF	None
1.8V	47µF Tantalum (300mΩ)	10kΩ	2.2nF	1.5nF
2.5V	47µF Tantalum (300mΩ)	10kΩ	3.3nF	1.5nF
3.3V	47µF Tantalum (300mΩ)	10kΩ	4.7nF	1.5nF

To optimize the compensation components for conditions not listed in Table 1, use the following procedure.

Choose the compensation resistor to set the desired crossover frequency. Determine the value by the following equation:

$$R3 = \frac{2\pi \times C2 \times V_{OUT} \times f_C}{G_{EA} \times G_{CS} \times V_{FB}}$$

Putting in the known constants and setting the crossover frequency to the desired 75KHz:

$$R3 \approx 4.36 \times 10^8 \times C2 \times V_{OUT}$$

In this case, the actual crossover frequency is less than the desired 75KHz, and it is calculated by:

$$f_C = \frac{R3 \times G_{EA} \times G_{CS} \times V_{FB}}{2\pi \times C2 \times V_{OUT}}$$

Choose the compensation capacitor to set the zero to one fourth of the crossover frequency. Determine the value by the following equation:

$$C3 = \frac{4 \times C2 \times V_{OUT}}{R3^2 \times G_{EA} \times G_{CS} \times V_{FB}}$$

Determine if the second compensation capacitor, C4, is required. It is required if the ESR zero of the output capacitor occurs at less than four times the crossover frequency, or:

$$8\pi \times C2 \times R_{ESR} \times f_C \geq 1$$

Where R_{ESR} is the equivalent series resistance of the output capacitor.

If this is the case, then add the second compensation capacitor. Determine the value by the equation:

$$C4 = \frac{C2 \times R_{ESR(MAX)}}{R3}$$

Where $R_{ESR(MAX)}$ is the maximum ESR of the output capacitor.

For Example:

Given:

V_{OUT} = 1.8V

C2 = 10µF Ceramic (ESR = 10mΩ max.)

Calculate:

$$R3 \approx 4.36 \times 10^8 (10\mu F) \times (1.8V) = 7.85k\Omega$$

(Use the nearest standard value of 7.5kΩ.)

$$C3 = \frac{1.9 \times 10^{-14}}{10\mu F \times 1.8V} = 1.05nF$$

(Use 1nF since it is a standard value.)

$$8\pi \times C2 \times R_{ESR} \times f_C = 0.19$$

which is less than 1, therefore the second compensation capacitor (C4) is not required.

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External Boost Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: D= $\frac{V_{OUT}}{V_{IN}}$ >65%

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Fig.2

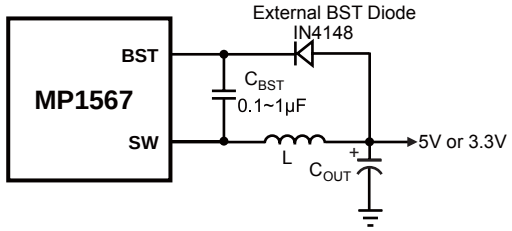


Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

TYPICAL APPLICATION CIRCUITS

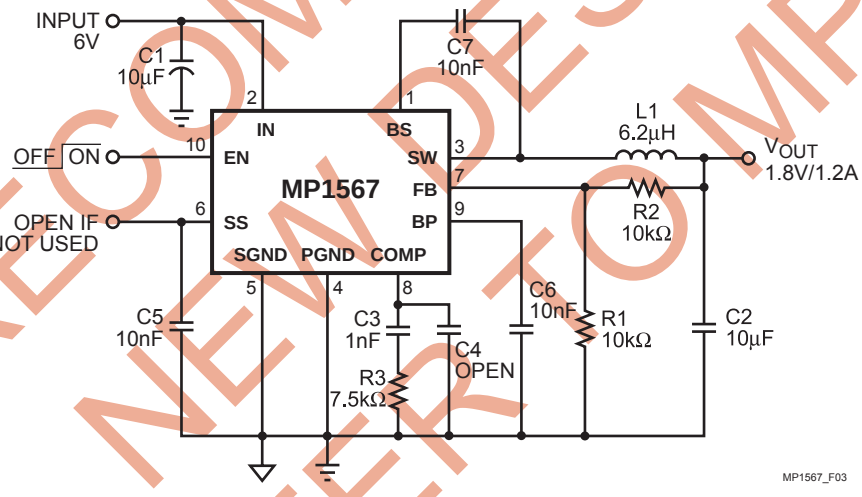


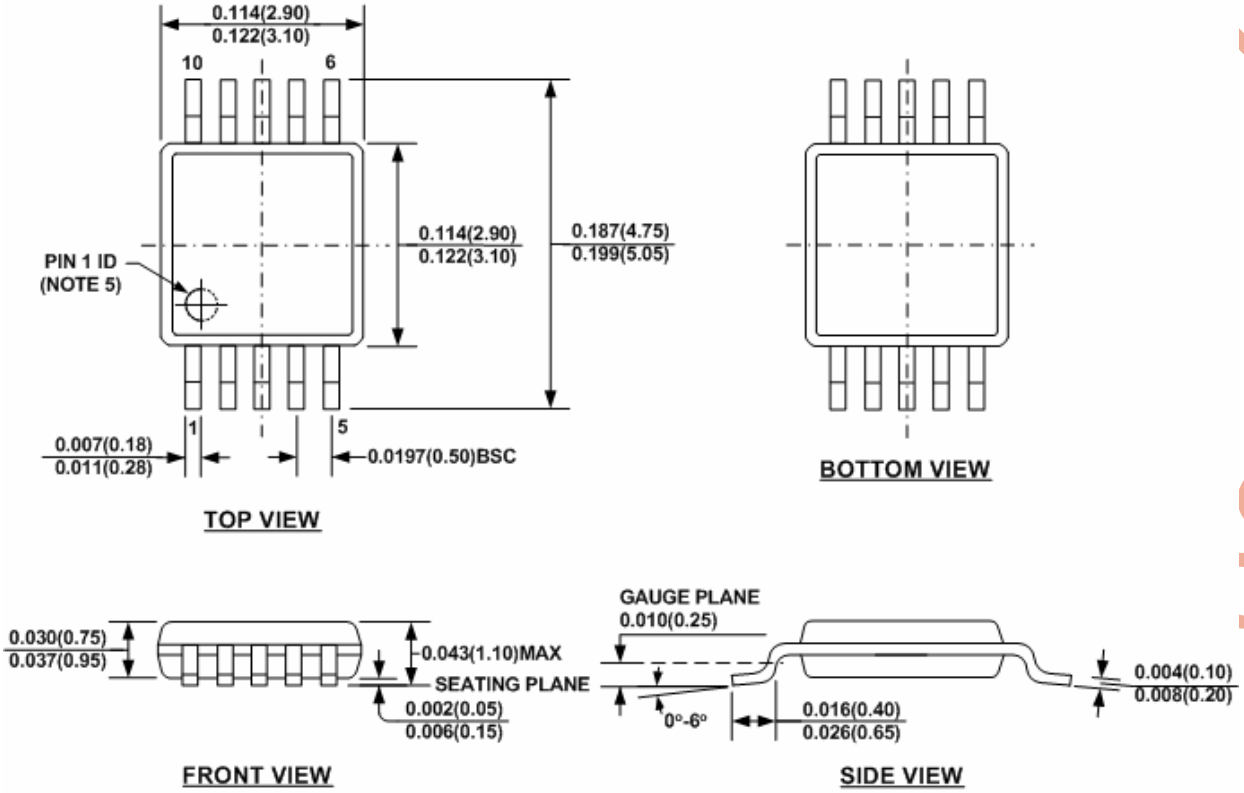
Figure 3—6V Input Application Circuit

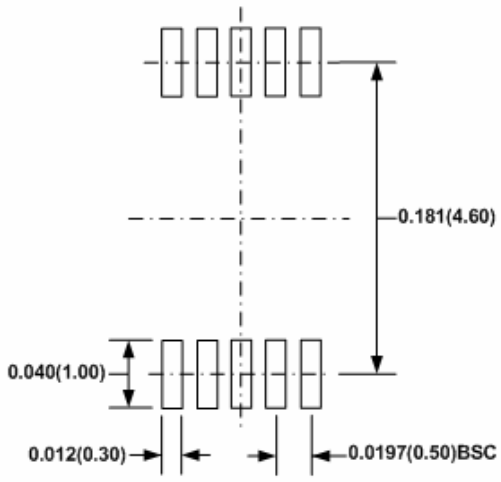
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PACKAGE INFORMATION

MSOP10





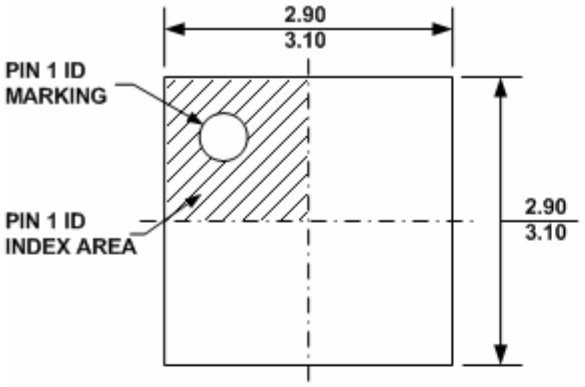
RECOMMENDED LAND PATTERN

NOTE:

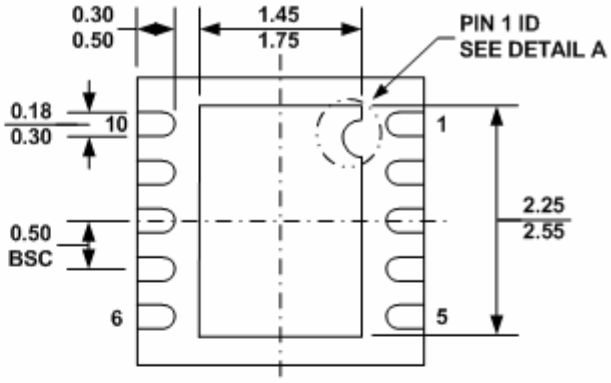
1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) PIN 1 IDENTIFICATION HAS THE HALF OR FULL CIRCLE OPTION.
6) DRAWING MEETS JEDEC MO-817, VARIATION BA.
7) DRAWING IS NOT TO SCALE.

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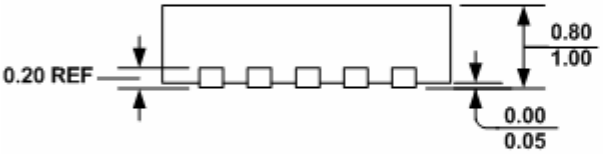
QFN10 (3mm x 3mm)



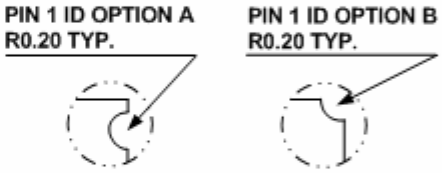
TOP VIEW



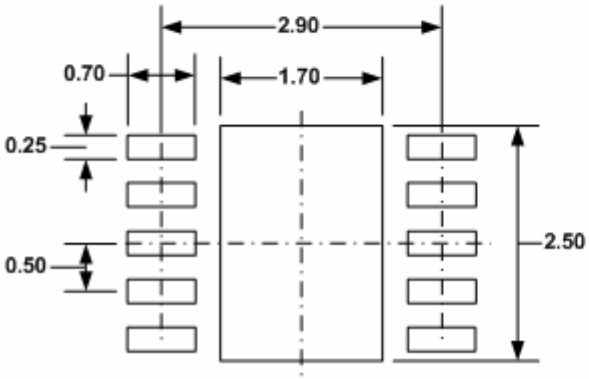
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

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