MP8770C

3V to 17V, 8A, Synchronous Step-Down Converter with Forced CCM

DESCRIPTION

The MP8770C is a fully integrated, high-frequency, synchronous rectified step-down switch-mode converter with internal power MOSFETs. The MP8770C offers a very compact solution to achieve 8A of continuous output current with excellent load and line regulation over a wide input range. The MP8770C uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response and easy loop design, as well as very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8770C requires a minimal number of readily available, standard external components, and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

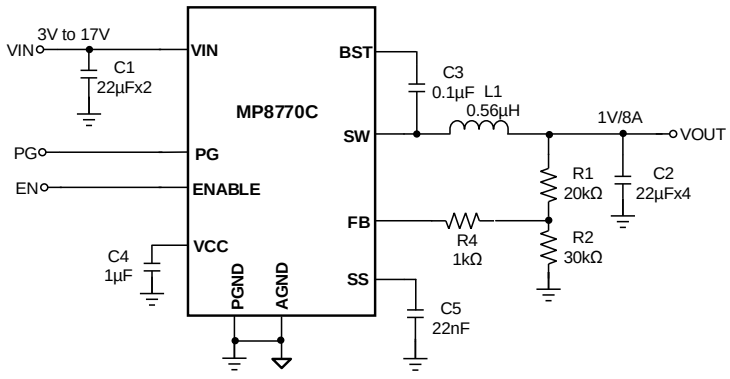
- Wide 3V to 17V Operating Input Range
- 8A Output Current
- 22mΩ/10mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 100μA Quiescent Current
- Output Adjustable from 0.6V
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- Forced PWM Operation
- External Programmable Soft-Start Time
- EN and Power Good for Power Sequencing
- Over-Current Protection (OCP) and Hiccup Mode
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purpose

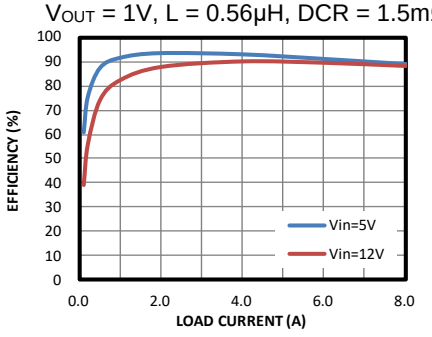
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TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.56μH, DCR = 1.5mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8770CGQ	QFN-16 (3mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8770CGQ–Z).

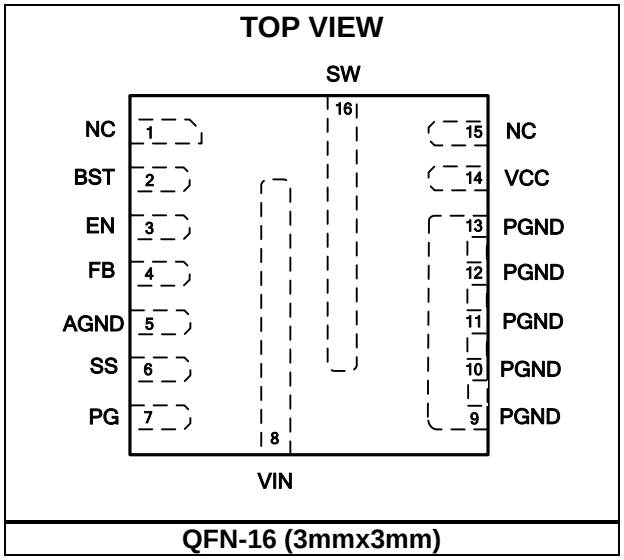
TOP MARKING

BGCY

LLL

BGC: Product code of MP8770CGQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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PIN FUNCTIONS

Pin #	Name	Description
1, 15	NC	**No connection.** Pin must be left floating.
2	BST	**Bootstrap.** A capacitor connected between the SW and BS pins is required to form a floating supply across the high-side switch driver. It is recommended for the BST resistor to be less than 4.7Ω.
3	EN	**Enable.** Pull EN high to enable the MP8770C. When floating, EN is pulled down to GND by an internal 1.2MΩ resistor so it is disabled.
4	FB	**Feedback.** Sets the output voltage when connected to the tap of an external resistor divider that is connected between output and GND.
5	AGND	**Signal ground.** AGND is not internally connected to the system ground. Ensure that AGND is connected to the system ground in PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time and avoid start-up inrush current.
7	PG	**Power good output.** The output of this pin is an open drain. It will change state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8770C operates from a 3V to 17V input rail. C1 is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9, 10, 11, 12, 13	PGND	**System ground.** This pin is the reference ground of the regulated output voltage, so care must be taken during PCB layout. It is recommended to connect it to GND with copper pours and vias.
14	VCC	**Internal bias supply output.** Decouple with a 1µF capacitor. The VCC capacitor should be placed close to the VCC and GND pins.
16	SW	**Switch output.** Use a wide PCB trace to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +20V
V_{SW} - 0.3V (-5V < 10ns) to + V_{IN} +0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = 25°C) (2) (4) 3.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +125°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 17V
Output voltage (V_{OUT}) ..... 0.6V to V_{IN} * D_{MAX} or 12V max
Operating junction temp ..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)		
EV8770C-Q-00A (4)	38	10 °C/W
JESD51-7 (5)	50	12 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV8770C-Q-00A, 4-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		17	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			5	µA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	µA
MOSFET						
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		22		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 3.3V		10		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V			1	µA
Current Limit						
Valley current limit	I_{LIMIT_VY}		8	10		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
Switching Frequency and Minimum On/Off Timer						
Switching frequency	f_{SW}		600	700	800	kHz
Minimum on time (7)	t_{ON_MIN}			50		ns
Minimum off time (7)	t_{OFF_MIN}			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	µA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pin pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout rising threshold	VCC_{Vth}		2.6	2.8	3	V
VCC under-voltage lockout threshold	VCC_{HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%

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ELECTRICAL CHARACTERISTICS *(continued)* (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{vth_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by design and characterization test.

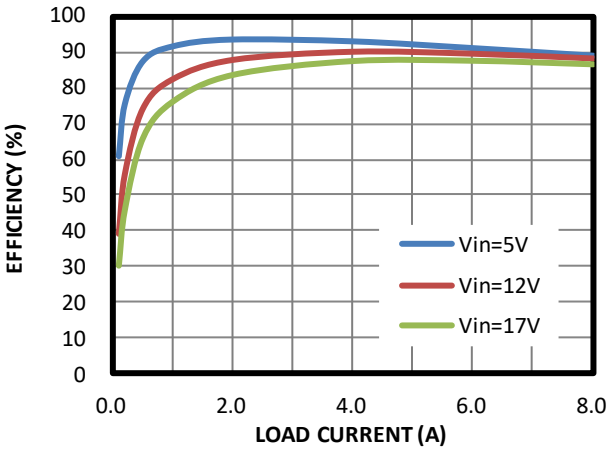
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

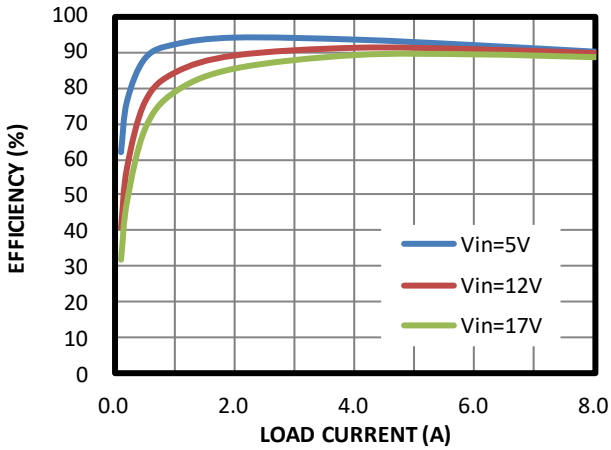
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.56µH, DCR = 1.5mΩ



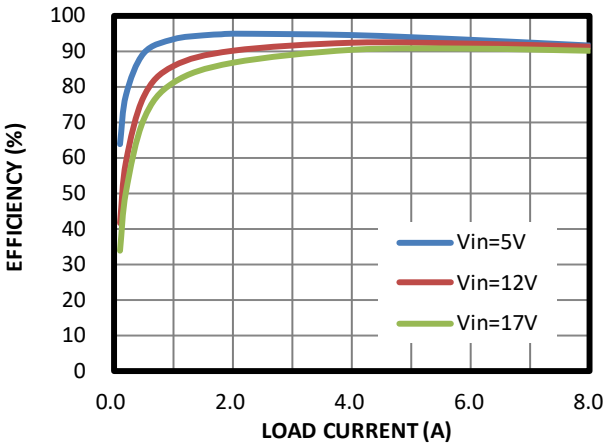
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.56µH, DCR = 1.5mΩ



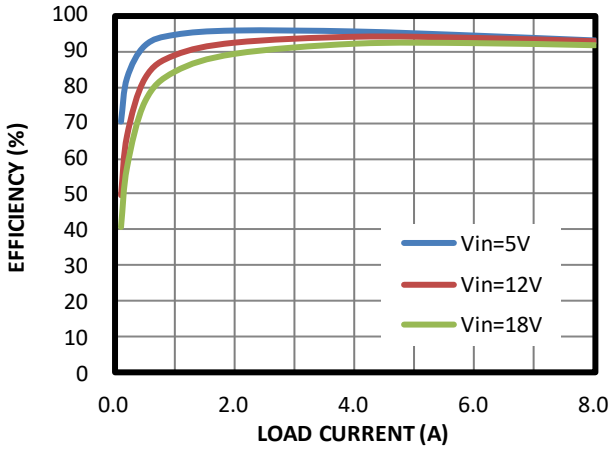
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 0.56µH, DCR = 1.5mΩ



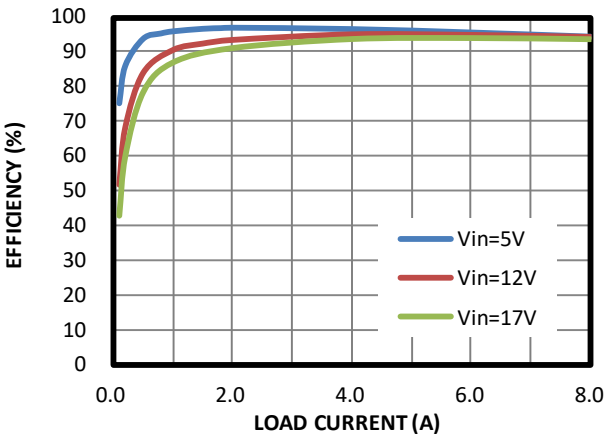
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 0.82µH, DCR = 0.9mΩ



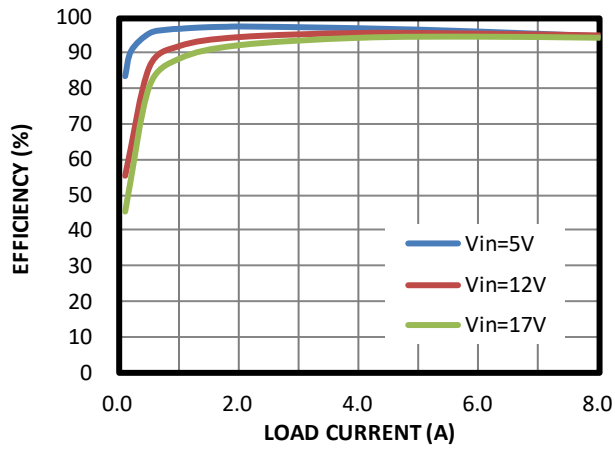
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 0.82µH, DCR = 0.9mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1µH, DCR = 1.35mΩ



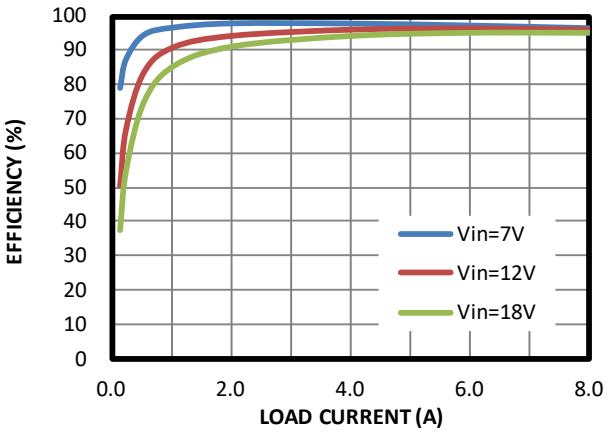
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

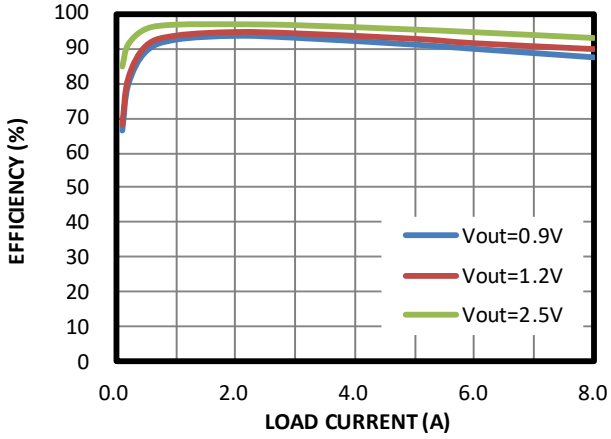
Efficiency vs. Load Current

V_{OUT} = 5V, L = 1.2µH, DCR = 1.8mΩ



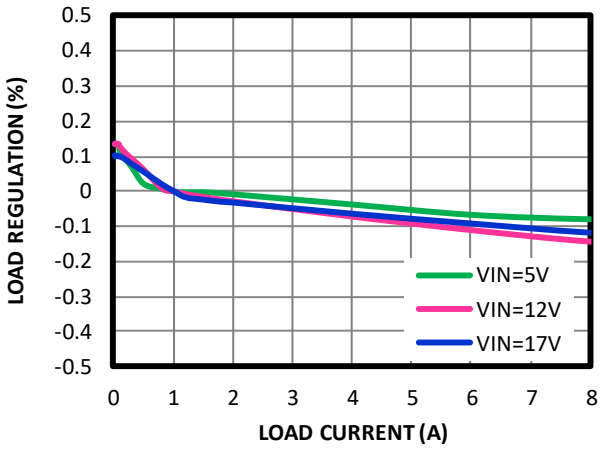
Efficiency vs. Load Current

V_{IN} = 3.3V, L = 0.68µH, DCR = 1.58mΩ



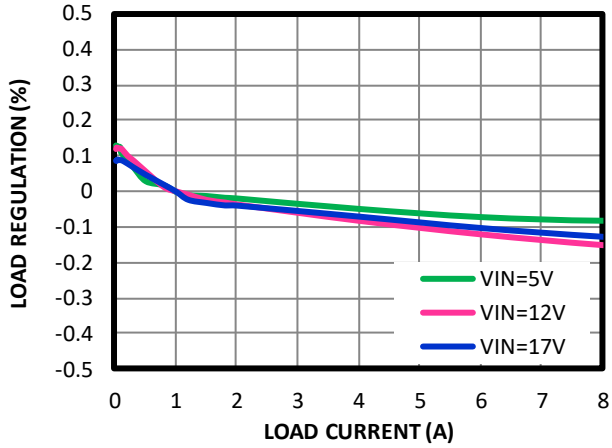
Load Regulation vs. Load Current

V_{OUT} = 1V



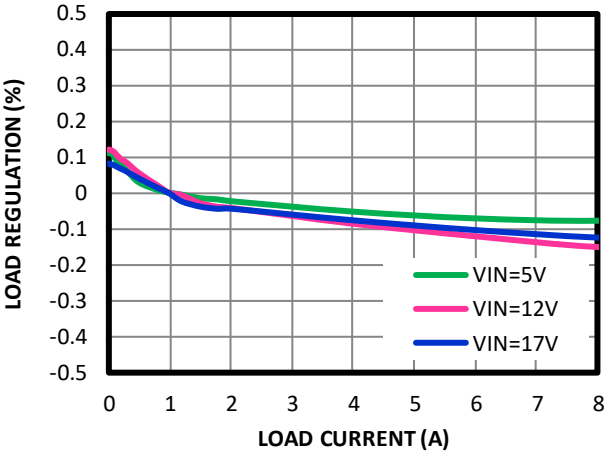
Load Regulation vs. Load Current

V_{OUT} = 1.2V



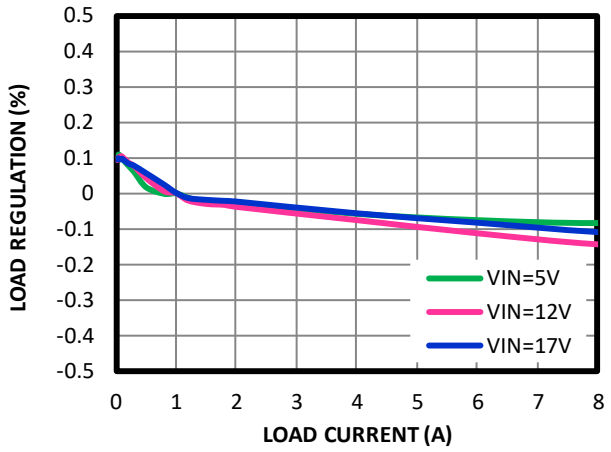
Load Regulation vs. Load Current

V_{OUT} = 1.5V



Load Regulation vs. Load Current

V_{OUT} = 1.8V



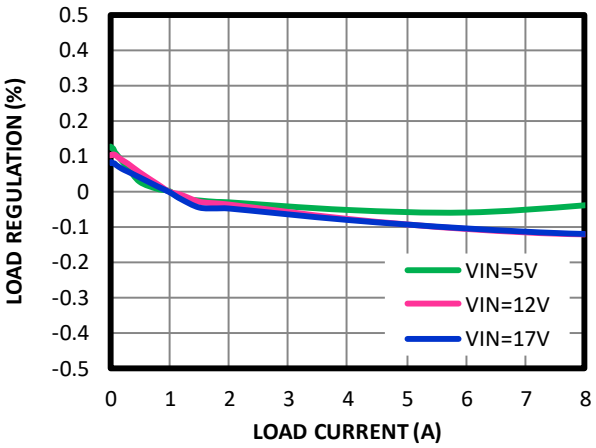
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

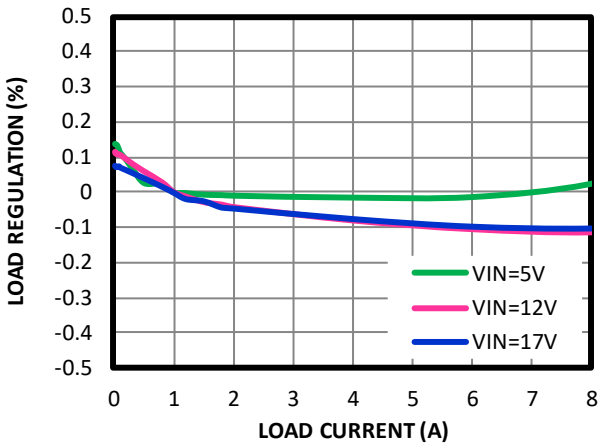
Load Regulation vs. Load Current

V_{OUT} = 2.5V



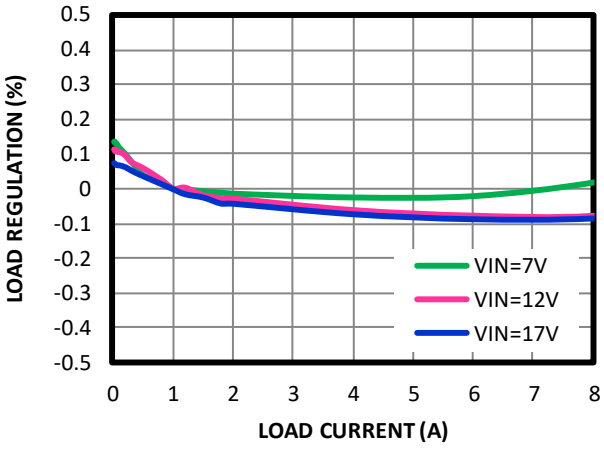
Load Regulation vs. Load Current

V_{OUT} = 3.3V

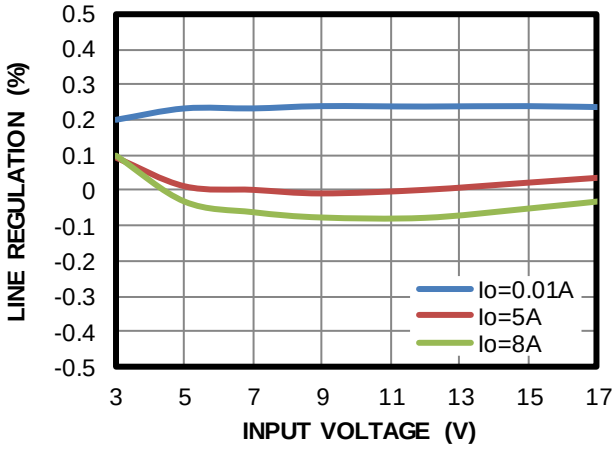


Load Regulation vs. Load Current

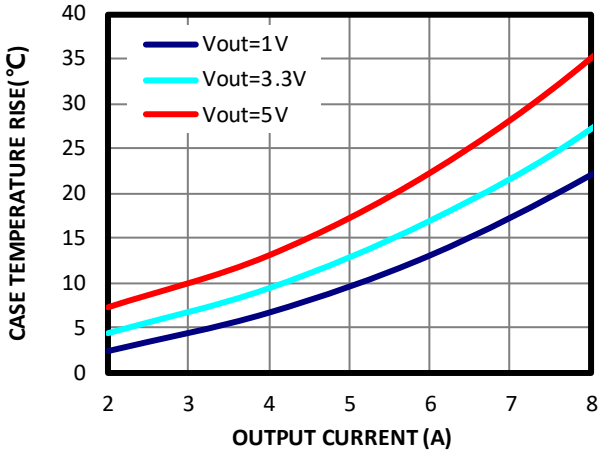
V_{OUT} = 5V



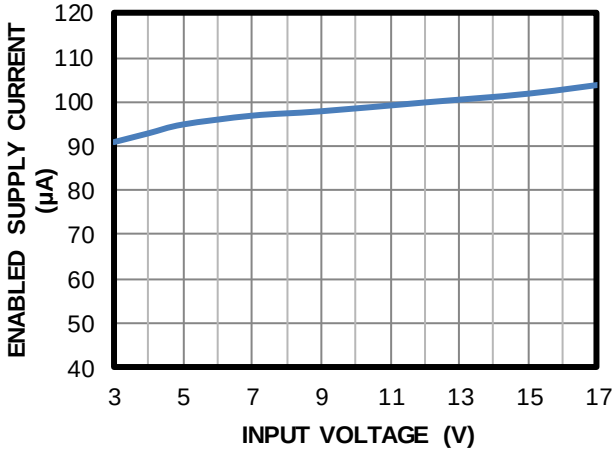
Line Regulation vs. Input Voltage



Case Temperature Rise vs. Output Current



Enabled Supply Current vs. Input Voltage

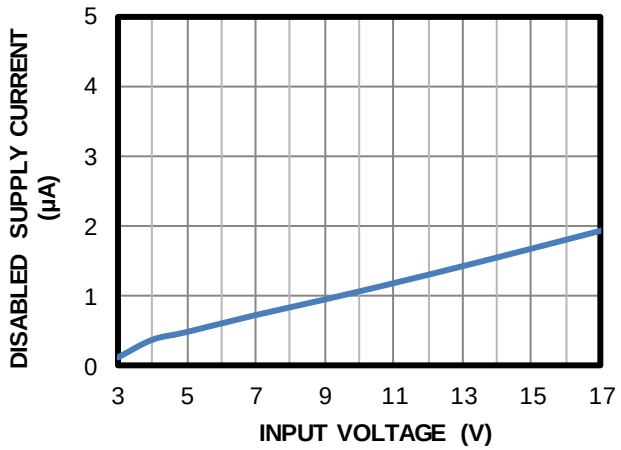


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

Disabled Supply Current vs. Input Voltage



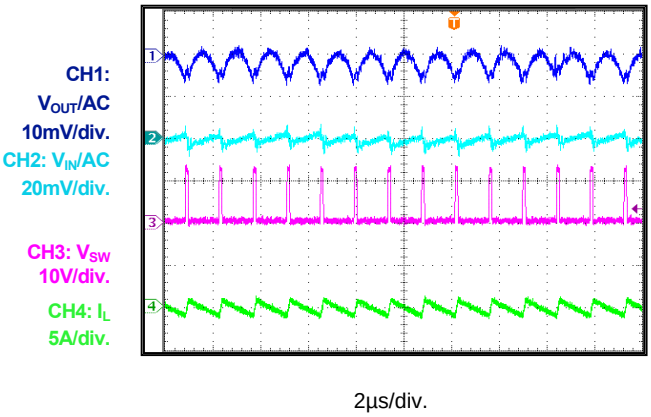
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

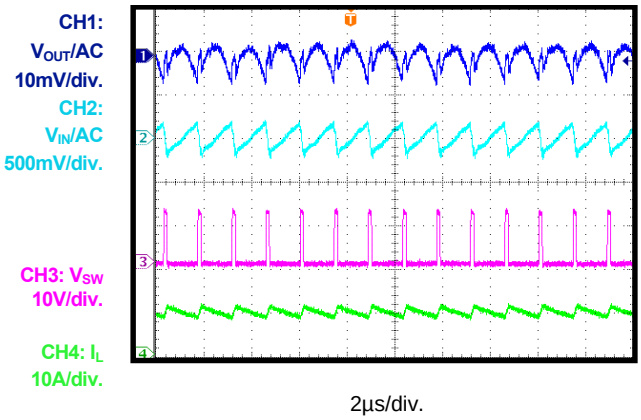
Input/Output Ripple

I_{OUT} = 0A



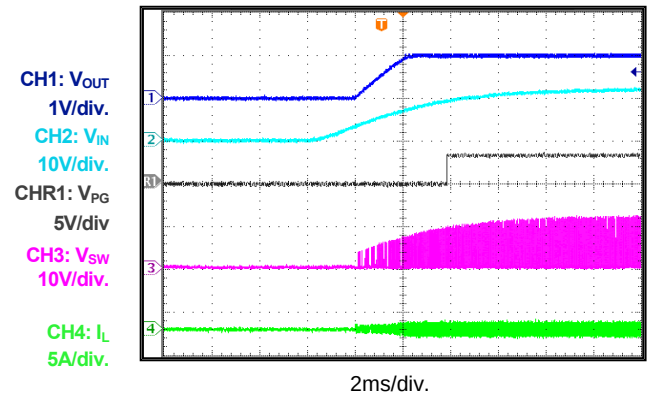
Input/Output Ripple

I_{OUT} = 8A



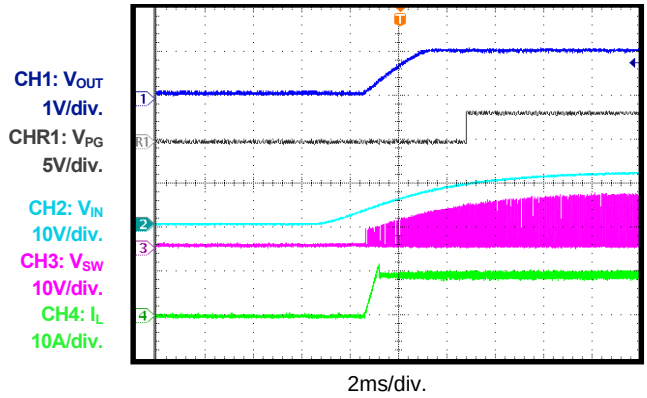
Start-Up through Input Voltage

I_{OUT} = 0A



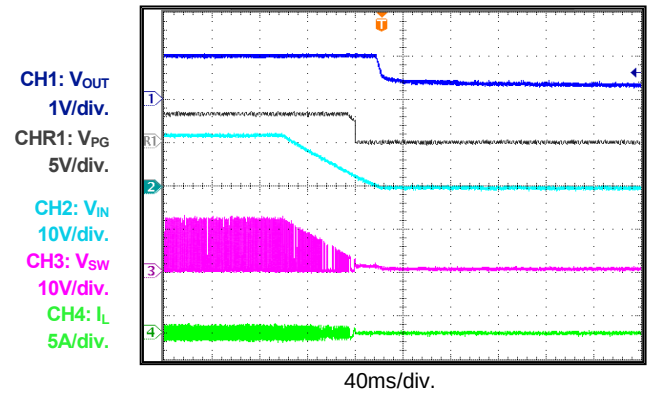
Start-Up through Input Voltage

I_{OUT} = 8A



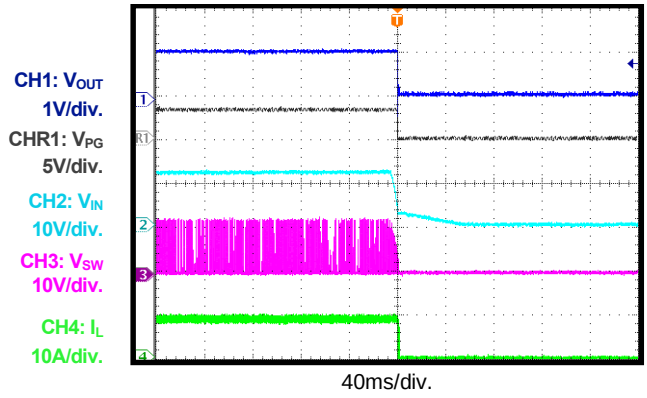
Shutdown through Input Voltage

I_{OUT} = 0A



Shutdown through Input Voltage

I_{OUT} = 8A



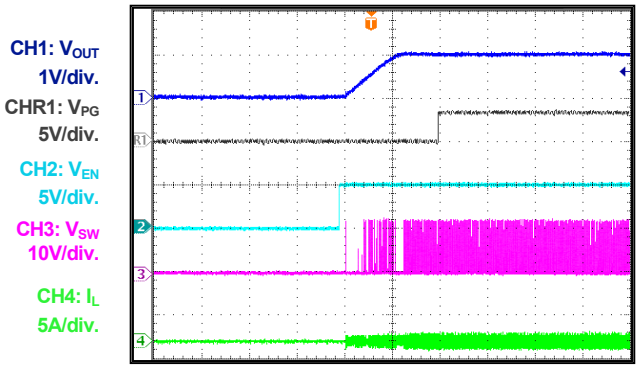
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

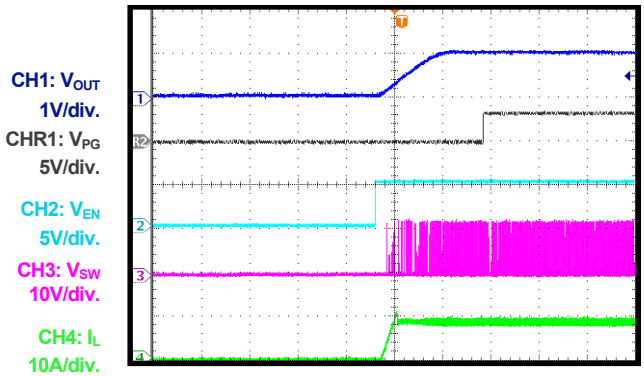
Start-Up through EN

I_{OUT} = 0A



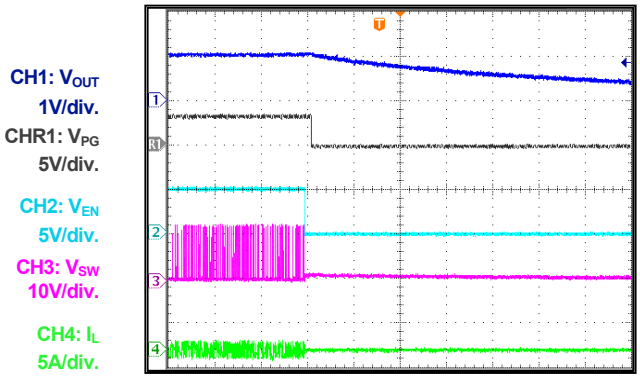
Start-Up through EN

I_{OUT} = 8A



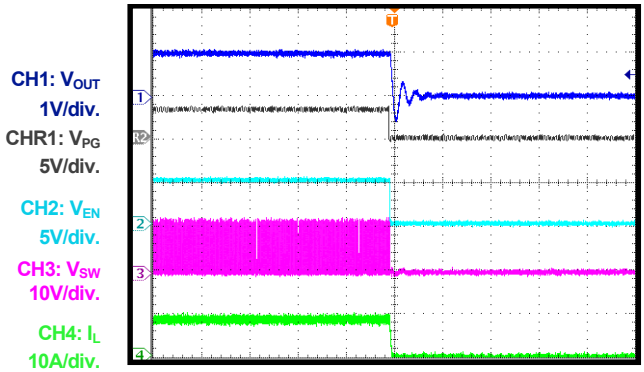
Shutdown through EN

I_{OUT} = 0A



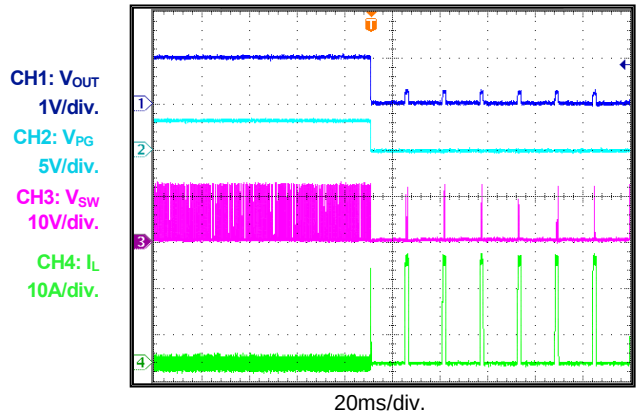
Shutdown through EN

I_{OUT} = 8A



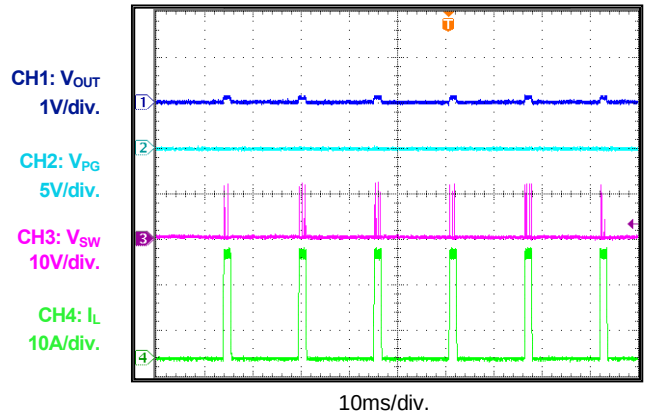
Short-Circuit Protection Entry

I_{OUT} = 0A



Short-Circuit Protection Steady State

Short output to GND



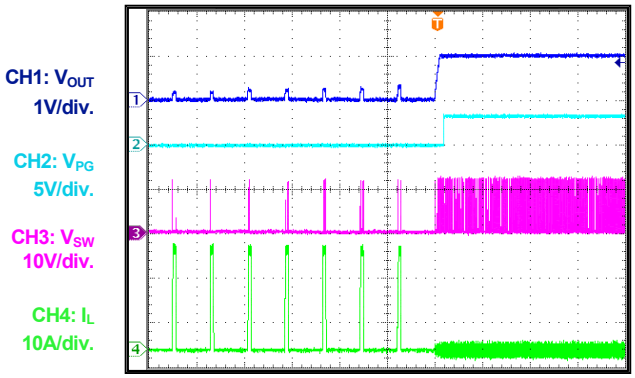
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

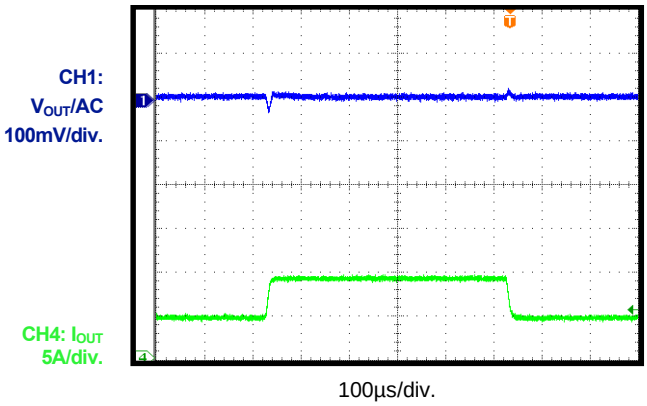
Short-Circuit Protection Recovery

I_{OUT} = 0A



Load Transient

I_{OUT} = 4A to 8A



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FUNCTIONAL BLOCK DIAGRAM

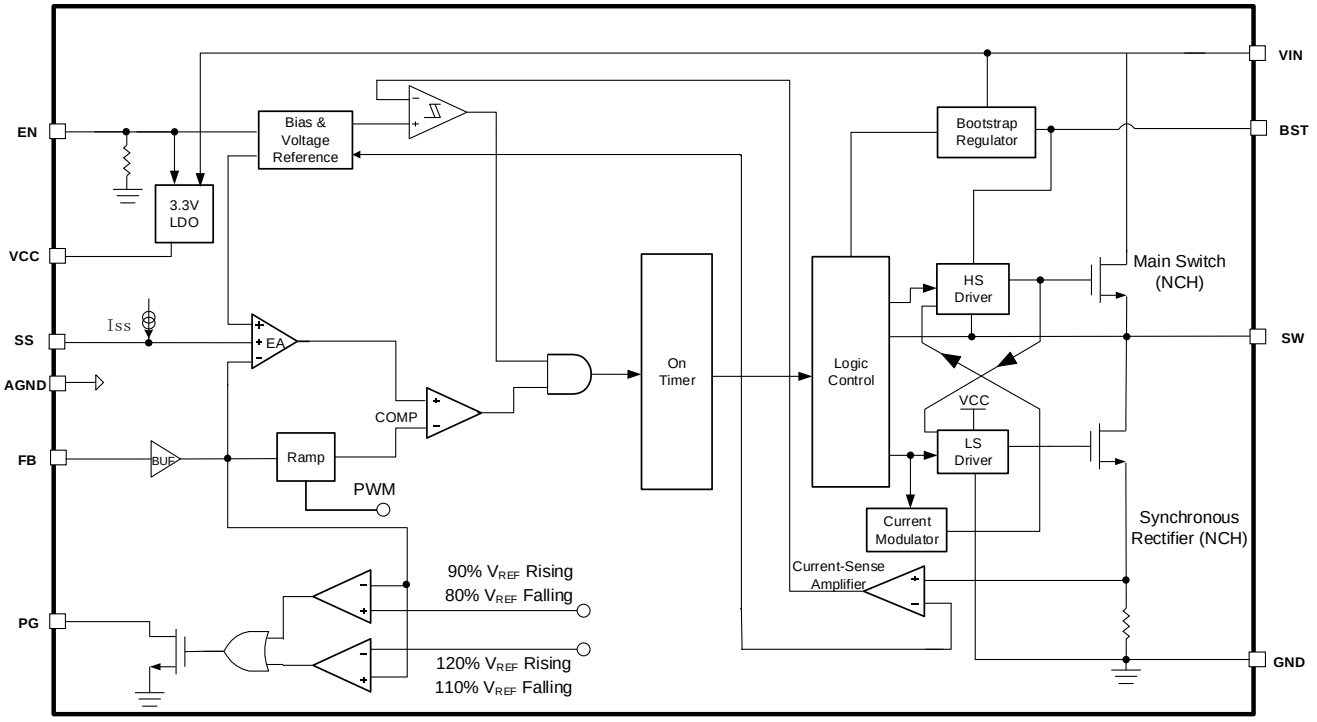


Figure 1: Functional Block Diagram

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OPERATION

The MP8770C is a fully integrated, synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP8770C. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant across the entire input voltage range.

After the on period elapses, the HS-FET turns off. The HS-FET turns on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage.

The MP8770C operates in continuous conduction mode (CCM). The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. If both the HS-FET and LS-FET are turned on at the same time, a dead short occurs between input and GND. This is called shoot-through. In order to avoid shoot-through, a dead time (DT) is internally generated between the HS-FET off and LS-FET on periods, or vice versa.

An internal compensation is applied for COT control for more stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

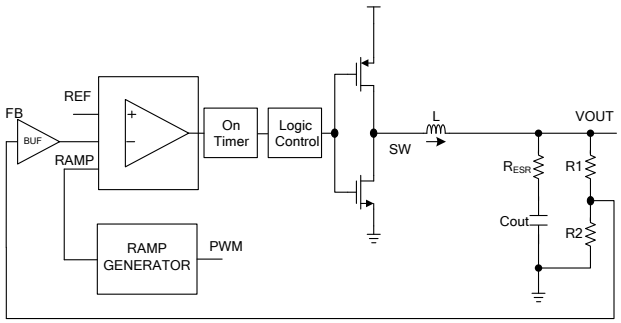


Figure 2: Simplified Ramp Compensation Block

VCC Regulator

The 3.4V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 3.4V, the output of the regulator is in full regulation. When V_{IN} falls below 3.4V, the regulator output decreases following V_{IN}. A 1µF decoupling ceramic capacitor is needed at the pin.

Enable

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.25V to turn on the regulator, drive it below 1V to turn it off.

When floating, EN is pulled down to GND by an internal 1.2MΩ resistor.

EN can be connected directly to V_{IN}. It supports a 17V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8770C's UVLO comparator monitors the output voltage of the internal regulator's VCC.

The VCC UVLO rising threshold is about 2.8V, while its falling threshold is 2.45V.

When the input voltage exceeds the UVLO rising threshold voltage, the MP8770C powers up. It shuts off when the input voltage falls below the UVLO falling threshold voltage. This is a non-latch protection.

Soft Start

The MP8770C employs a soft start (SS) mechanism to ensure smooth output ramping during power-up. When the EN pin goes high, an internal (6µA) current source charges up the SS capacitor. The SS capacitor voltage takes over V_{REF} to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once SS voltage (V_{SS}) rises above V_{REF}, it continues to ramp up and V_{REF} takes over. At this point, soft start finishes and the device enters steady state operation.

The SS capacitor value can be determined with Equation (1):

$$C_{ss}(nF) = 0.83 \times \frac{t_{ss}(ms) \times I_{ss}(uA)}{V_{REF}(V)} \quad (1)$$

If the output capacitance is a large value, it is not recommended to set the SS time too short. This

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avoids accidentally reaching the current limit during SS. An SS capacitor less than 4.7nF should be avoided.

Power Good Indicator (PG)

The PG pin is the open drain of a MOSFET that connects to VCC or some other voltage source through a resistor (e.g. 100kΩ). The MOSFET turns on with the application of an input voltage so that the PG pin is pulled to GND before SS is ready. After V_{FB} reaches 90% of V_{REF}, the PG pin is pulled high after a 50μs delay. When the V_{FB} drops to 80% of V_{REF}, the PG pin is pulled low.

When UVLO or OTP occurs, the PG pin is pulled low immediately. If OC (over-current) occurs, the PG pin is pulled low when V_{FB} drops below 80% of V_{REF} after a 0.05ms delay. When OV occurs, PG is pulled low when V_{FB} rises above 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls back below 110% of V_{REF}, PG is pulled high after a 0.05ms delay.

If the input supply fails to power the MP8770C, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. Figure 3 shows the relationship between the PG voltage and the pull-up current.

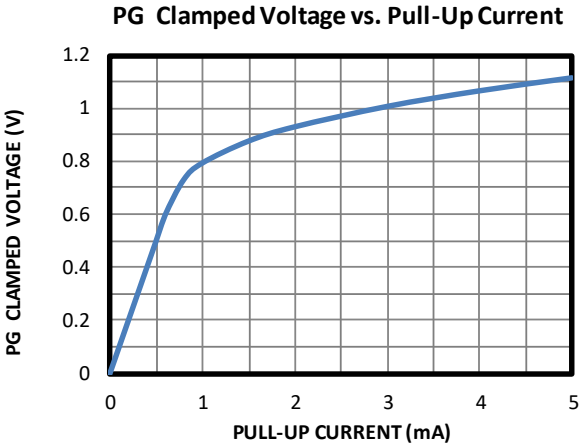


Figure 3: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP8770C has valley limit control. The LS-FET monitors the current flowing through it. The HS-FET waits until the valley current limit disappears to turn on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold, typically 50% below the reference. Once UV is triggered, the MP8770C enters hiccup mode to periodically restart the part.

During OCP, the device tries to recover from an over-current fault with hiccup mode. This means the chip disables the output power stage, discharges the soft-start capacitor, then automatically tries to soft start again.

If the over-current condition still remains after soft start ends, the device repeats this operation cycle until the over-current conditions disappear and the output rises back to regulation level. OCP is a non-latch protection.

Pre-Bias Start-Up

The MP8770C has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is also charged. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at the FB pin, the part starts to work normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection, with a rising threshold of 1.7V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, L_O, and C_O (see Figure 4). If V_{IN} - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C4. It is recommended for the BST resistor (R4) to be less than 4.7Ω.

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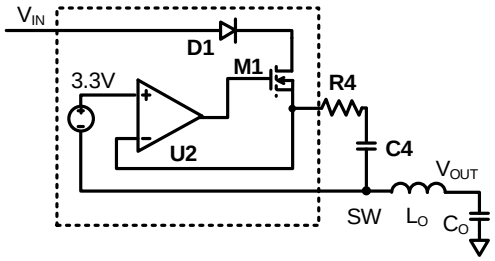


Figure 4: Internal Bootstrap Charger

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by initially blocking the signaling path to avoid any fault triggering, and then the internal supply rail is pulled down.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, as a small R2 value leads to considerable quiescent current loss and too large a value makes the FB noise sensitive. It is recommended to choose a value between 2kΩ and 100kΩ for R2. Typically, a current less than 250μA through R2 offers a good balance between system stability and no load loss. R1 is then determined with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

Figure 5 shows the feedback circuit.

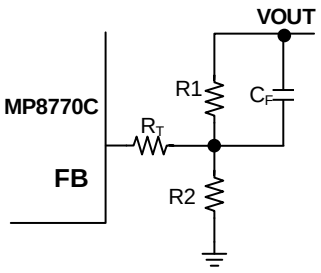


Figure 5: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_F (pF)	R_T (kΩ)
1.0	20	30	0.56	56	1
1.2	20	20	0.56	56	1
1.5	20	13	0.56	56	1
1.8	20	10	0.82	56	1
2.5	20	6.34	0.82	56	1
3.3	20	4.42	1	56	1
5	20	2.7	1.2	56	1

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current and a lower output ripple voltage. However, it also has a larger physical footprint, higher series resistance, and a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 40% of the maximum output current. The peak inductor current should also be below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance, and should be placed as close to the VIN pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

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The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Besides considering the output ripple, a larger output capacitor also can get better load transient response. However, maximum output capacitor limitation should be also considered in design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time, and the device will fail to regulate. The maximum output capacitor value C_{O_MAX} can be limited with Equation (12):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (12)$$

Where I_{LIM_AVG} is the average start-up current during soft-start period, and t_{ss} is the soft-start time.

Design Example

A design example is provided below when the ceramic capacitors are applied:

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	8A

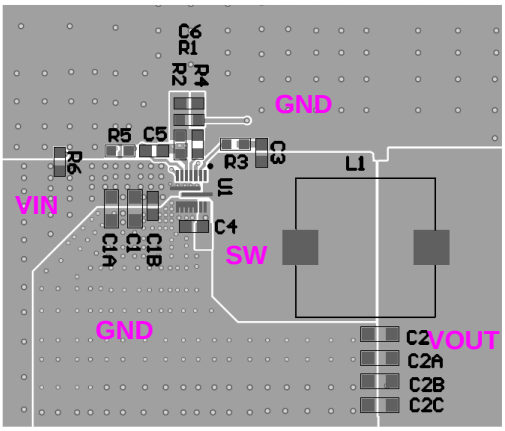
For detailed application schematics, see the Typical Application Circuits section on page 20. For the typical performance and waveforms, see the Typical Characteristics section on page 6. For more device applications, refer to the related evaluation board datasheet.

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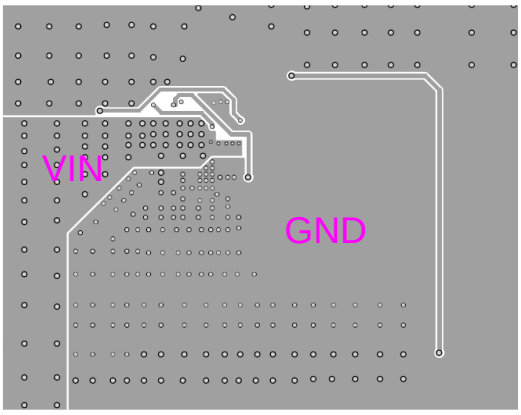
PCB Layout Guidelines

Efficient layout is very important for proper device function. Poor layout design can result in poor line or load regulation and stability issues. It is strongly recommended to use a 4-layer board layout, with the two middle layers being GND. For best performance, refer to Figure 6 and follow the guidelines below:

1. Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close as possible to the IN and GND pins.
3. Place the VCC decoupling capacitor close to the device.
4. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
5. Place the external feedback resistors next to the FB pin.
6. Keep the switching node (SW) short and away from the feedback network.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

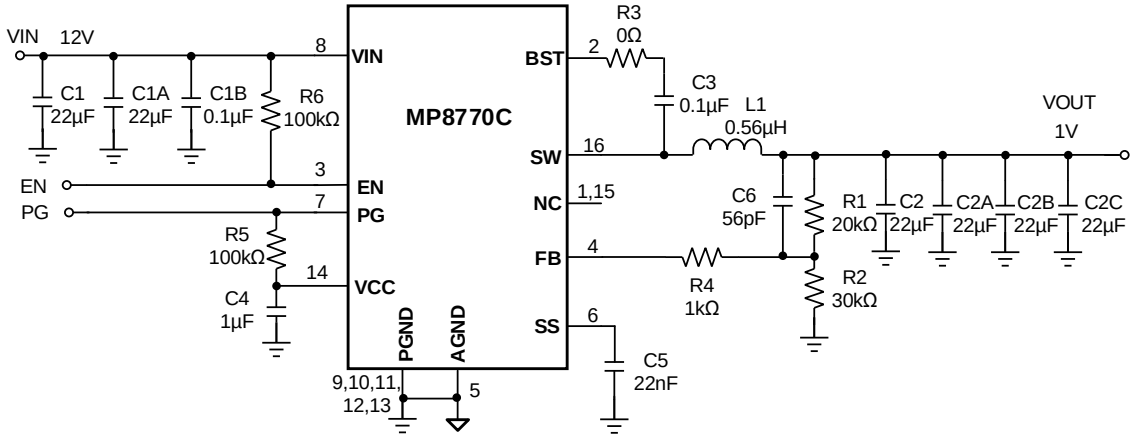


Figure 7: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 8A (8)

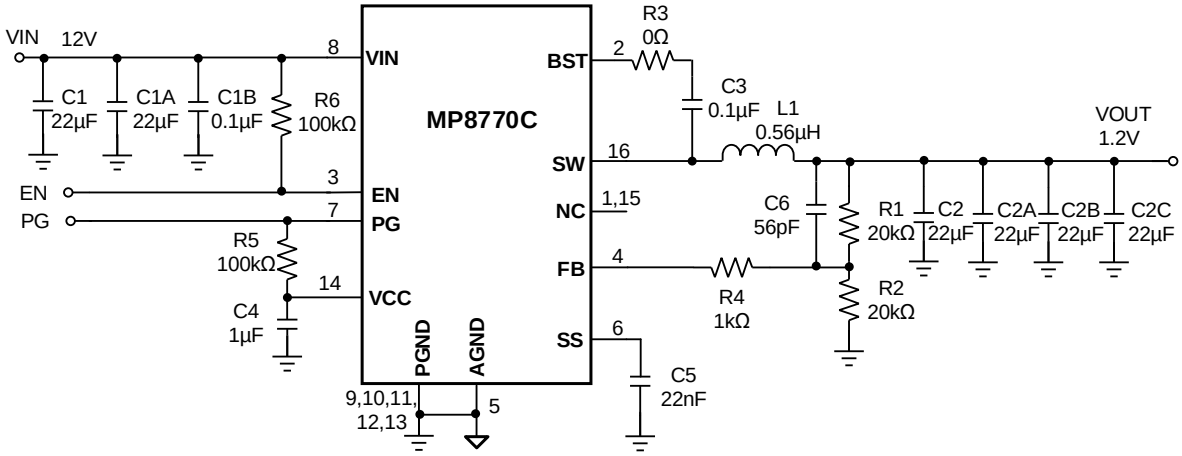


Figure 8: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 8A (8)

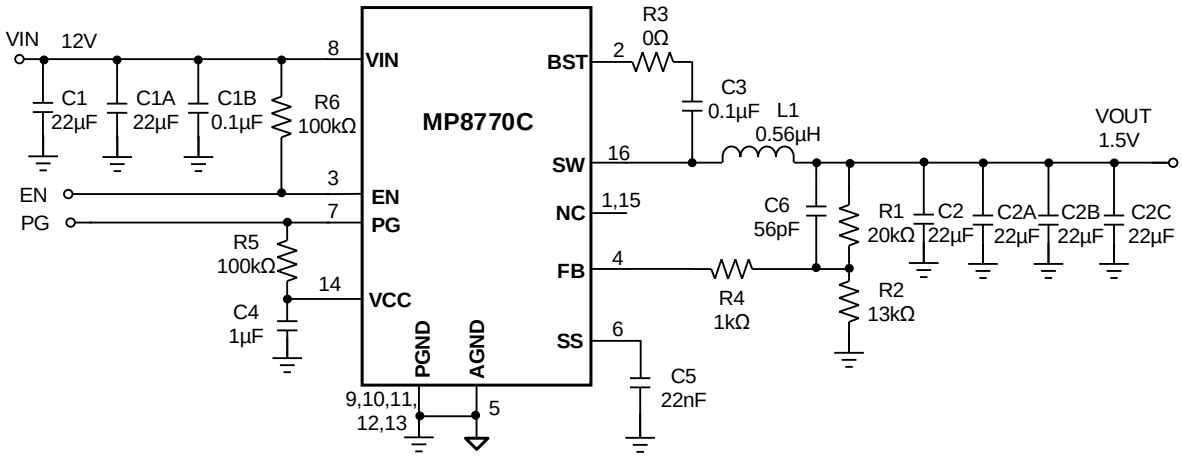


Figure 9: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 8A (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

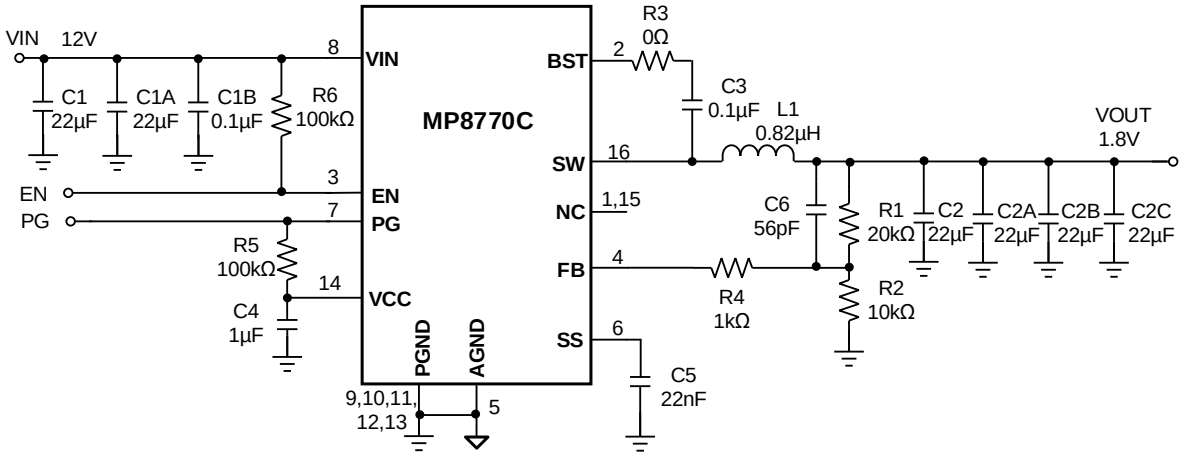


Figure 10: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 8A (8)

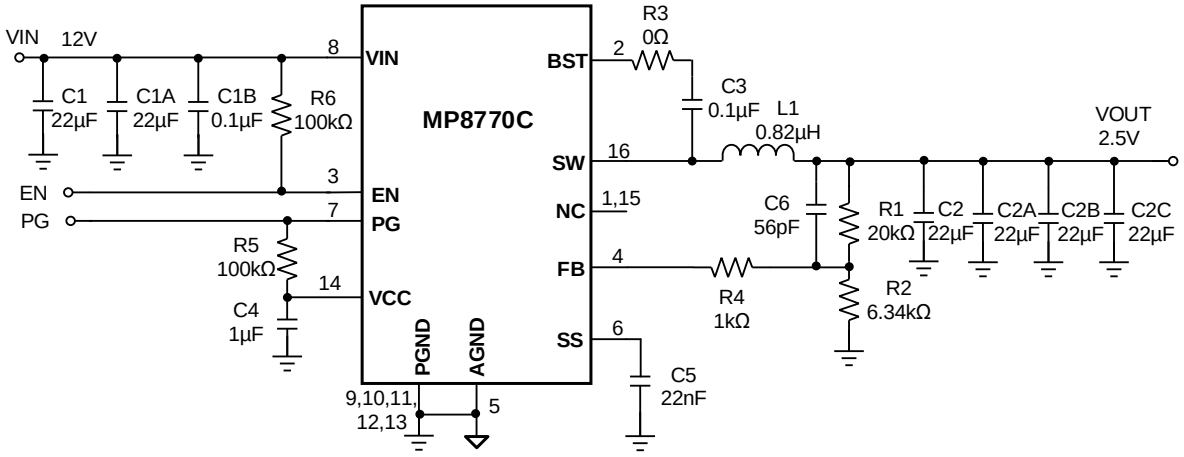


Figure 11: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 8A (8)

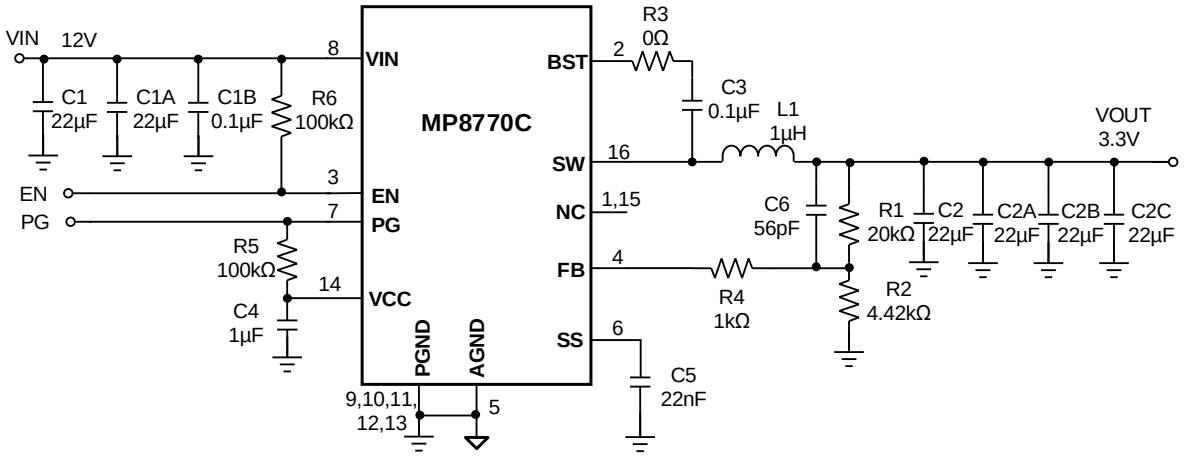


Figure 12: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 8A (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

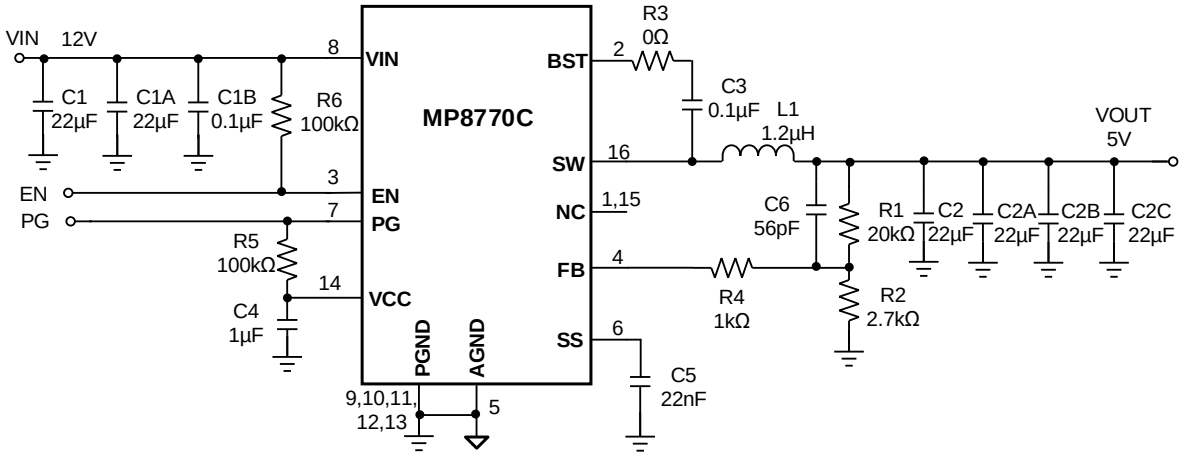


Figure 13: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A (8)

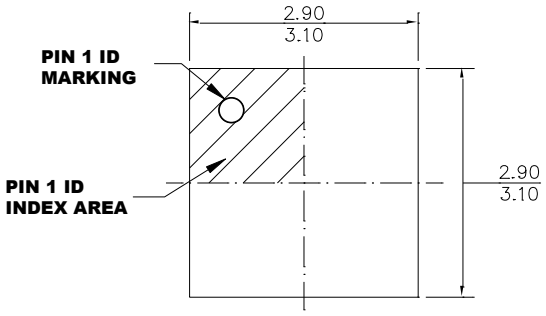
Note:

8) When VIN is low, see the Selecting the Input Capacitor Section on page 17.

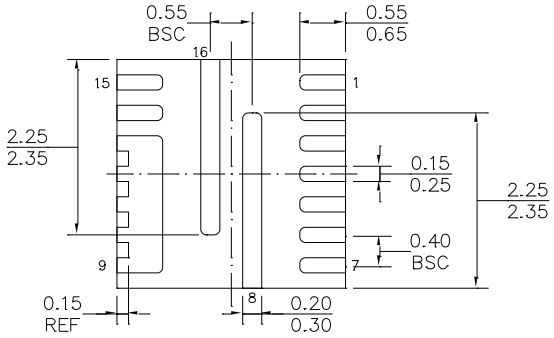
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PACKAGE INFORMATION

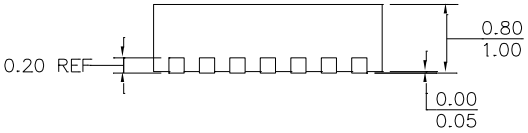
QFN-16 (3mmx3mm)



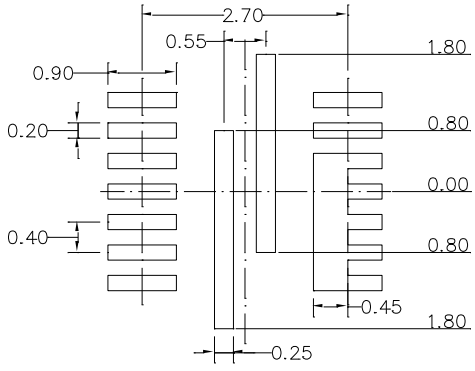
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

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3) JEDEC REFERENCE IS MO-220.
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