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High-Speed, Quad, Industrial Digital Input with Parallel Output

MAX22193

Product Highlights

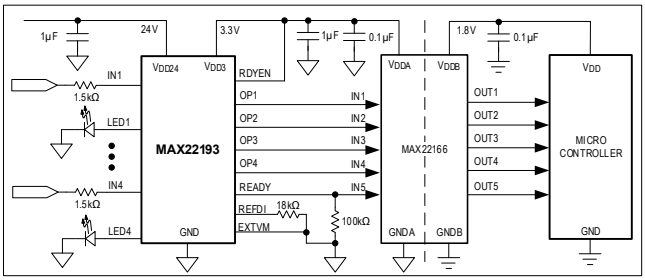
- High-Speed, Industrial Digital Inputs
  - 300ns Maximum Propagation Delay
  - 40ns Maximum Channel-to-Channel Skew
  - Parallel Output for Simultaneous Signal Delivery
- High Integration Reduces BOM and Space
  - Operates Directly from Field Supply (7V to 65V)
  - Compatible with 3.3V or 5V Logic
  - 4mm x 4mm, 20-TQFN Package
- Low Power and Low Heat Dissipation
  - 1.2mA (max) Quiescent Current with 3.3V Supply
  - Accurate Input Current-Limiters
  - Energyless Field-Side LED Drivers
- Fault Tolerant with Built-In Diagnostics
  - Integrated Field-Side Supply Monitor
  - Integrated Over-Temperature Monitor
  - Current-Setting Resistor Monitor
- Configurability Enables Wide Range of Applications
  - Configurable IEC 61131-2 Types 1, 2, 3 Inputs
  - Input Current Limiting from 1.18mA to 7.01mA
- Robust Design for Industrial Environments
  - ±2kV Surge Tolerant using 470Ω Resistor (min)
  - ±8kV Contact ESD and ±15kV Air Gap ESD Using 470Ω Resistor (min)
  - -40°C to +125°C Ambient Operating Temperature

Key Applications

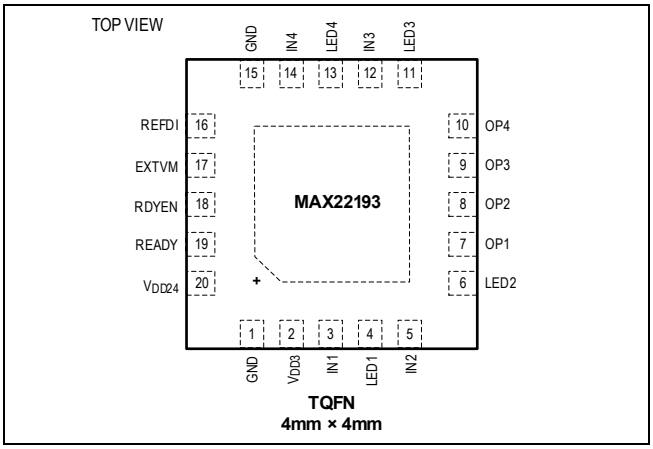
- Programmable Logic Controllers (PLC)
- Distributed Control System (DCS)
- Motor Control
- Industrial Automation
- Process Automation

The MAX22193 translates four 24V industrial digital inputs to four CMOS-logic-compatible, parallel outputs. Propagation delay from input-to-output is less than 300ns for all four channels. Current-limiter on each digital input greatly reduces power dissipation compared to traditional resistive input. The accuracy of these current-limiters minimizes power dissipation while ensures compliance with the IEC 61131-2 standard. A current-setting resistor allows the MAX22193 to be configured for Type 1, Type 2 or Type 3 digital inputs. Additionally, the MAX22193 has energyless field-side LED drivers to meet the indicator light requirement of IEC 61131-2 with no additional power dissipation.

Simplified Application Diagram



Pin Configuration



The MAX22193 provides a 3.3V integrated voltage regulator. The internal LDO accepts the field supply V_{DD24} from 7V to 65V. The internal LDO output can supply up to 25mA of current in addition to powering the basic MAX22193 requirements. This LDO can be used to power digital isolators and other field-side circuits. Alternatively, the MAX22193 can be powered from an external 3.0V to 5.5V supply at V_{DD3}.

The MAX22193 includes an open-drain READY output that asserts high to indicate the MAX22193 is functional. If the V_{DD24} field-side supply voltage is too low, or a fault in the current-setting resistor is detected, or the device reaches an over-temperature condition, the READY signal is set to high-impedance.

***Ordering Information* appears at end of data sheet.**

19-101349; Rev 0; 06/22

Absolute Maximum Ratings

V_{DD3} to GND ..... -0.3V to +6V

V_{DD24} to GND..... -0.3V to +70V

OP1-OP4 to GND..... -0.3V to (V_{DD3}+0.3)V

IN1-IN4 to GND..... -40V to +40V

REFDI to GND ..... -0.3V to (V_{DD3}+0.3)V

READY, RDYEN to GND ..... -0.3V to +6V

EXTVM to GND..... -0.3V to +6V

LED1-LED4 to GND..... -0.3V to +6V

Continuous Power Dissipation (T_A = +70°C)

Single-layer Board (derate 16.90mW/°C above T_A = +70°C) 1355.90mW

Multilayer Board (derate 25.60mW/°C above T_A = +70°C) 2051.30mW

Temperature Ratings

Operating Temperature Range..... -40°C to +125°C

Maximum Junction Temperature.....+150°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20-TQFN

Package Code	T2044+3C
Outline Number	*21-0139*
Land Pattern Number	*90-0037*
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient (θ_{JA})	59°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	39°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	6°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{DD3} = +3.0V to +5.5V, C_L on OP_ = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD24} = +24V, field inputs $V_{IN\_}$ = +24V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Supply Voltage	V_{DD24}	Normal Operation	7		65	V
	V_{DD3}	Powered from an external power supply	3.0		5.5	
Supply Current Powered from V_{DD24}	I_{DD24}	V_{DD24} = 24V, $V_{IN\_}$ = 0V, LED_ = GND, no load on OP_		0.6	1.2	mA
Supply Current Powered from V_{DD3}	I_{DD3}	V_{DD3} = 3.3V, V_{DD24} floating, $V_{IN\_}$ = 0V, LED_ = GND, no load on OP_		0.6	1.2	mA
V_{DD3} Undervoltage-Lockout Threshold	V_{UVLO3}	Powered from V_{DD3}, V_{DD3} rising, V_{DD24} floating	2.4		2.9	V
V_{DD3} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST3}$			0.07		V
V_{DD24} READY Threshold	V_{READY_24VR}	V_{DD24} rising, EXTVM = GND	13.8	14.6	15.4	V
	V_{READY_24VF}	V_{DD24} falling, EXTVM = GND	13.3	14.1	15.0	
V_{DD24} Undervoltage-Lockout Threshold	V_{UVLO24}	V_{DD24} rising	6.0		6.8	V
V_{DD24} Undervoltage-Lockout Threshold Hysteresis	$V_{UVHYST24}$			0.45		V
Regulator Output Voltage	V_{DD3}	I_{LOAD} = 1mA, V_{DD24} = 7V to 65V	3.0	3.3	3.6	V
Line Regulation	dV_{DDLINE}	I_{LOAD} = 1mA, V_{DD24} = 12V to 24V		0		mV
Load Regulation	dV_{DDLOAD}	I_{LOAD} = 1mA to 10mA, V_{DD24} = 12V		1		mV
Short-Circuit Current Limit	I_{DD24_SC}	I_{DD24} when V_{DD3} short to GND, V_{DD24} = 12V	28	37.5	50	mA
EXTVM MONITOR						
EXTVM Glitch Filter				3		µs
EXTVM Threshold Off-to-On	$V_{24TH\_OFF\_ON}$	V_{DD24} rising	0.77	0.81	0.84	V
EXTVM Threshold On-to-Off	$V_{24TH\_ON\_OFF}$	V_{DD24} falling	0.74	0.79	0.82	V
External EXTVM Selection Threshold	EXTVM_SEL			0.3		V
External EXTVM Selectable V_{DD24} Threshold	EXTVM_VDD24		10		30	V
EXTVM Leakage Current	I_{EXTVM_L}		-1		+1	µA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SHDN}	V_{DD3} internal regulator off		165		°C

(V_{DD3} = +3.0V to +5.5V, C_L on OP_ = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD24} = +24V, field inputs $V_{IN\_}$ = +24V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown Threshold Hysteresis	T_{SHDN_HYS}			10		°C
REFDI SETTINGS						
REFDI Voltage	V_{REFDI}			0.61		V
Current-Limit Setting Resistance	R_{REFDI}		6	18	36	kΩ
REFDI Pin Short	REFDI_S	Increasing current at REFDI pin		550		µA
		Decreasing current at REFDI pin		548		
IC INPUTS (TYPE 1, 2, 3)						
Negative Input Current		-40V < $V_{IN\_}$ < 0V, VIN_ at the pin		100		µA
LED On-State Current	I_{LED_ON}	R_{REFDI} = 18kΩ, V_{LED} = 3V	1.5			mA
DI Leakage, Current Sources Disabled	I_{DI_LEAK}	$V_{IN\_}$ = 28V, REFDI floating	40	58	84	µA
Input Threshold Low-to-High	V_{THP+}	$V_{IN\_}$ at the pin, R_{REFDI} = 18kΩ	5.2	5.6	6	V
Input Threshold High-to-Low	V_{THP-}	$V_{IN\_}$ at the pin, R_{REFDI} = 18kΩ	4.4	4.7	5.0	V
Input Threshold Hysteresis	$V_{INPHYST}$	$V_{IN\_}$ at the pin, R_{REFDI} = 18kΩ		0.9		V
FIELD INPUTS TYPE 1, 3: (EXTERNAL SERIES RESISOR R_{IN} = 1.5kΩ, R_{REFDI} = 18kΩ)						
Field Input Current Limit	I_{INLIM}	6V (V_{THP+} MAX) ≤ $V_{IN\_}$ at the pin ≤ 28V, LED on, R_{REFDI} = 18kΩ	2.05	2.39	2.75	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 18kΩ, 1.5kΩ external series resistor			10	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 18kΩ, 1.5kΩ external series resistor	8			V
FIELD INPUTS TYPE 2: (EXTERNAL SERIES RESISOR R_{IN} = 470Ω, R_{REFDI} = 6kΩ)						
Field Input Current Limit	I_{INLIM}	6V (V_{THP+} MAX) ≤ $V_{IN\_}$ at the pin ≤ 28V, LED on, R_{REFDI} = 6kΩ	6	7	8.9	mA
Field Input Threshold Low-to-High	V_{INF+}	R_{REFDI} = 6kΩ, 470Ω external series resistor			10.2	V
Field Input Threshold High-to-Low	V_{INF-}	R_{REFDI} = 6kΩ, 470Ω external series resistor	7.2			V
LOGIC INPUT (RDYEN)						
Input Logic-High Voltage	V_{IH}		0.7 x V_{DD3}			V
Input Logic-Low Voltage	V_{IL}				0.3 x V_{DD3}	V
Input Pulldown Resistance	R_{PD}			199		kΩ
LOGIC OUTPUTS (OP_, READY)						

(V_{DD3} = +3.0V to +5.5V, C_L on OP_ = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD24} = +24V, field inputs $V_{IN\_}$ = +24V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic-High Voltage	V_{OH}	I_{OUT} = -4mA Source	V_{DD3} – 0.4			V
Output Logic-Low Voltage	V_{OL}	I_{OUT} = 4mA Sink			0.4	V
Output Leakage Current	I_{OL}		-1		+1	µA
DYNAMIC CHARACTERISTICS (OP_)						
Propagation Delay Low-to-High (*Figure 1*)	t_{PDLH}	IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 11V (Note 2)		85	280	ns
		IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 36V (Note 2)		85	280	
Propagation Delay High-to-Low (*Figure 1*)	t_{PDHL}	IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 11V (Note 2)		150	235	ns
		IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 36V (Note 2)		150	235	
Propagation Delay Skew Channel-to-Channel (*Figure 1*)	t_{PDSKEW_CH}	IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 11V (Note 2)	-20		+20	ns
		IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 36V (Note 2)	-20		+20	
Propagation Delay Skew Part-to-Part (*Figure 1*)	t_{PDSKEW_PT}	IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 11V, all conditions are the same between parts (Note 2)	-200		+200	ns
		IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 36V, all conditions are the same between parts (Note 2)	-200		+200	
Detectable Pulse Width (*Figure 1*)	t_{PW}	IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 11V (Note 2)			200	ns
		IN_ to OP_, R_{IN} = 470Ω, $V_{INF\_}$ = 36V (Note 2)			200	
Pulse Width Distortion	PWD	$\lvert t_{PDLH} - t_{PDHL} \rvert$, $V_{INF\_}$ = 11V (Note 2)	0	65	180	ns
		$\lvert t_{PDLH} - t_{PDHL} \rvert$, $V_{INF\_}$ = 36V (Note 2)	0	65	180	

Note 1: All parts are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: $V_{INF\_}$ is the voltage measured at the field input; $V_{IN\_}$ is the voltage measured at the pin.

EMC Characteristics

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Surge		IEC 61000-4-5, 1.2/50µs pulse, 42Ω/0.5µF, minimum 470Ω resistor in series with IN1–IN4	Line-to-Line		±2		kV
			Line-to-Ground		±2		
			V_{DD24}		±1		
ESD		All pins	Human Body Model		±2		kV
		IEC 61000-4-2, minimum 470Ω resistor in series with IN1–IN4	Contact Discharge		±8		
			Air-Gap Discharge		±15		

Timing Diagram

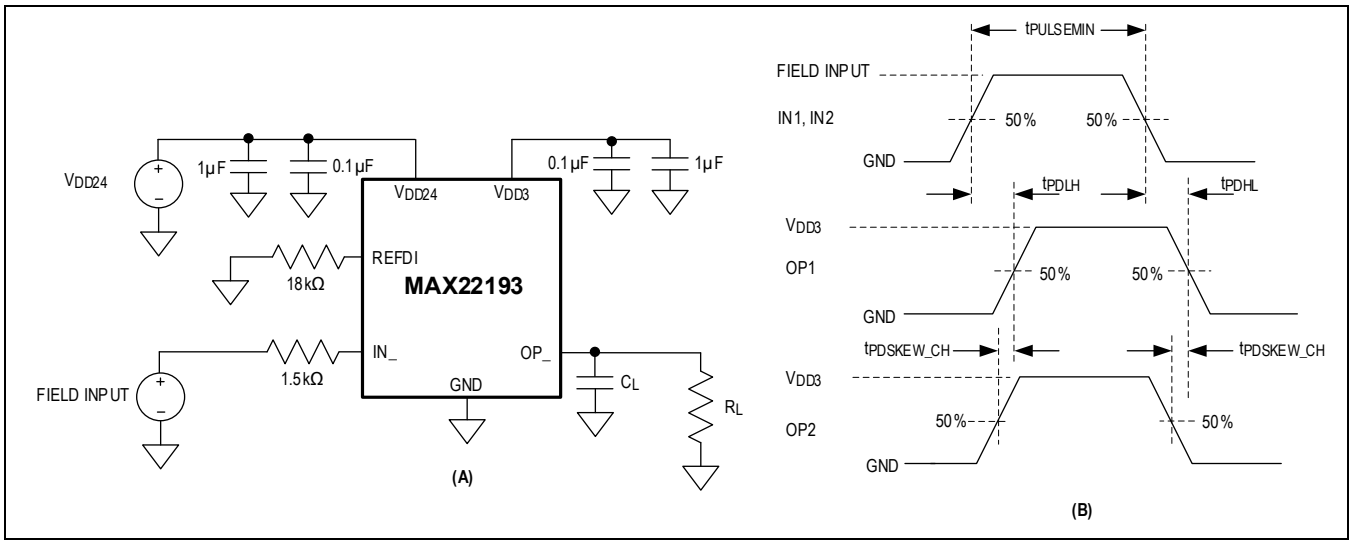
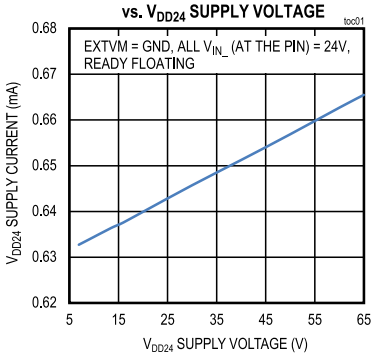


Figure 1. Test Circuit (A) and Timing Diagram (B)

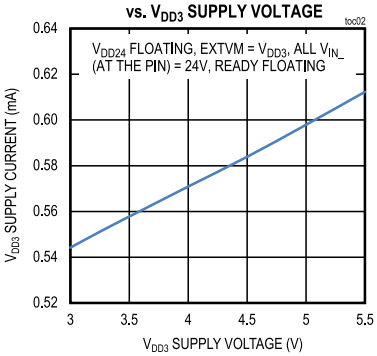
Typical Operating Characteristics

(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 18kΩ or 6kΩ, R_{IN} = 1.5k or 470Ω, unless otherwise noted.)

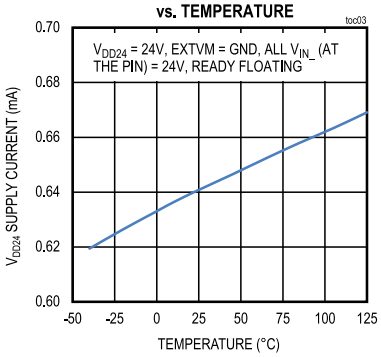
V_{DD24} SUPPLY CURRENT vs. V_{DD24} SUPPLY VOLTAGE



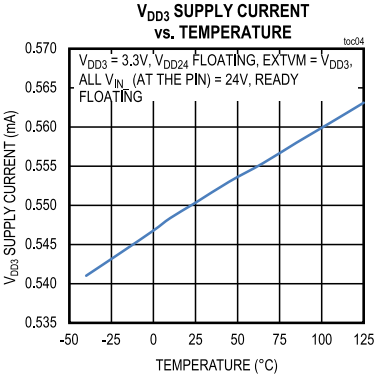
V_{DD3} SUPPLY CURRENT vs. V_{DD3} SUPPLY VOLTAGE



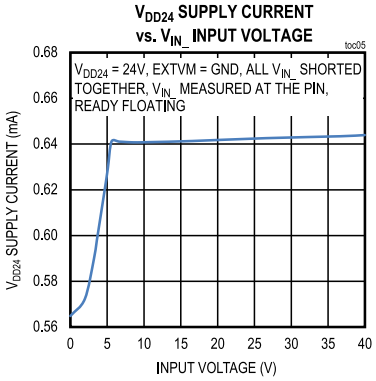
V_{DD24} SUPPLY CURRENT vs. TEMPERATURE



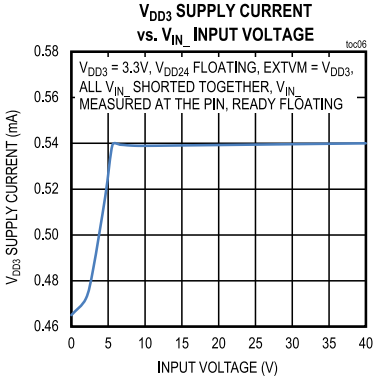
V_{DD3} SUPPLY CURRENT vs. TEMPERATURE



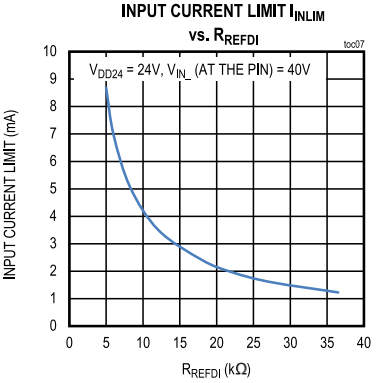
V_{DD24} SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE



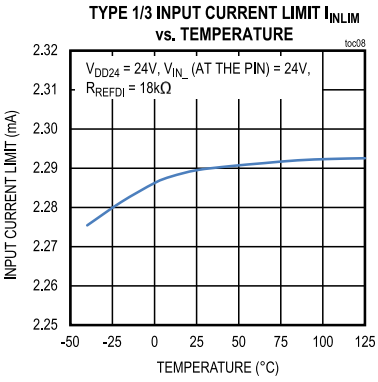
V_{DD3} SUPPLY CURRENT vs. $V_{IN\_}$ INPUT VOLTAGE



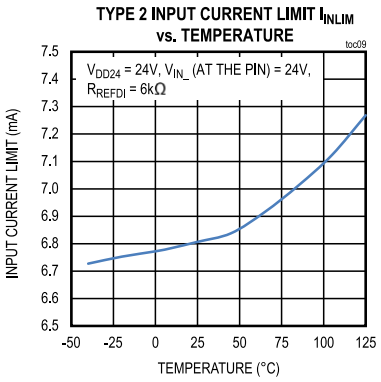
INPUT CURRENT LIMIT I_{INLIM} vs. R_{REFDI}



TYPE 1/3 INPUT CURRENT LIMIT I_{INLIM} vs. TEMPERATURE

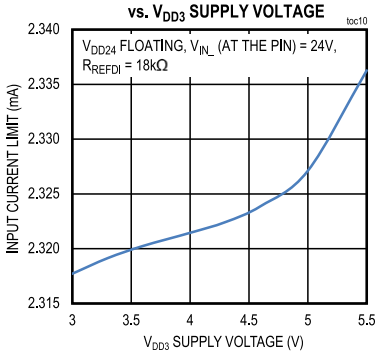


TYPE 2 INPUT CURRENT LIMIT I_{INLIM} vs. TEMPERATURE

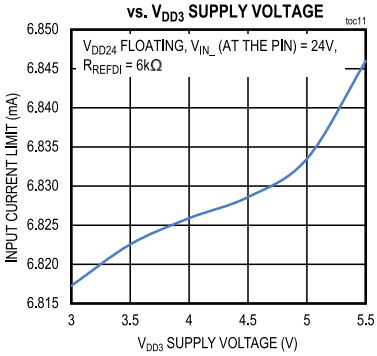


(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 18kΩ or 6kΩ, R_{IN} = 1.5k or 470Ω, unless otherwise noted.)

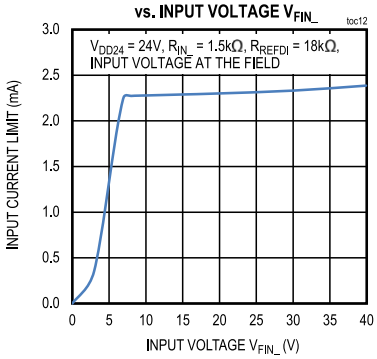
TYPE 1/3 INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3} SUPPLY VOLTAGE



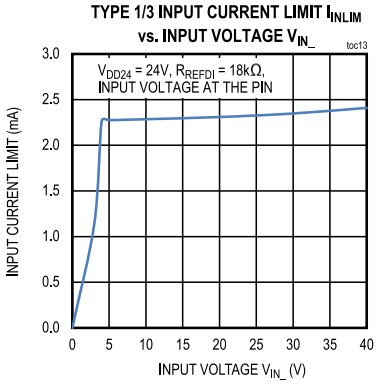
TYPE 2 INPUT CURRENT LIMIT I_{INLIM} vs. V_{DD3} SUPPLY VOLTAGE



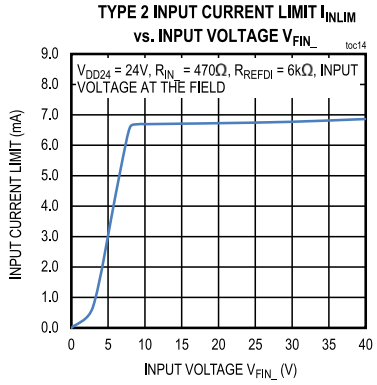
TYPE 1/3 INPUT CURRENT LIMIT I_{INLIM} vs. INPUT VOLTAGE $V_{FIN\_}$



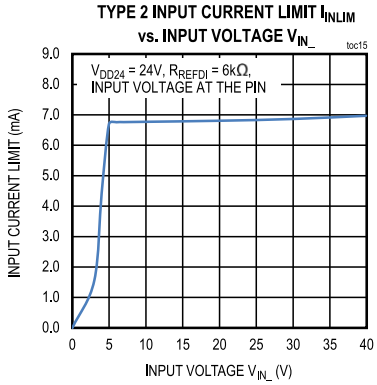
TYPE 1/3 INPUT CURRENT LIMIT I_{INLIM} vs. INPUT VOLTAGE $V_{IN\_}$



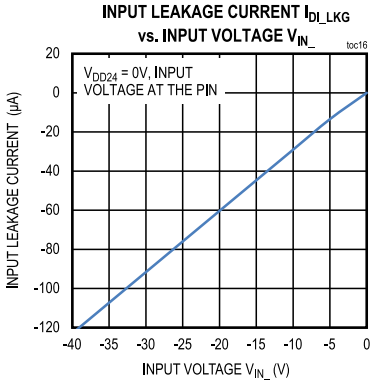
TYPE 2 INPUT CURRENT LIMIT I_{INLIM} vs. INPUT VOLTAGE $V_{FIN\_}$



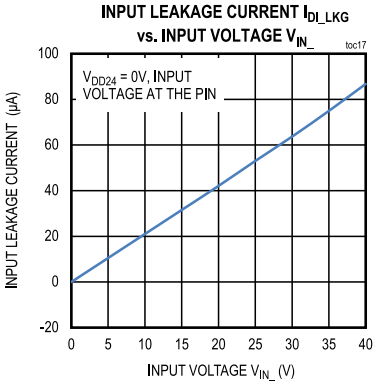
TYPE 2 INPUT CURRENT LIMIT I_{INLIM} vs. INPUT VOLTAGE $V_{IN\_}$



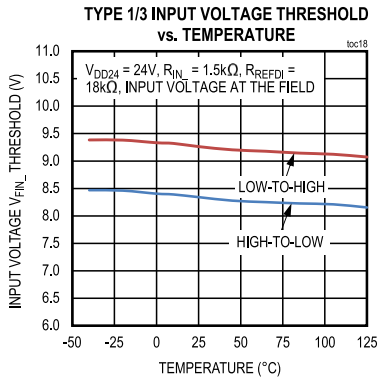
INPUT LEAKAGE CURRENT I_{DI_LKG} vs. INPUT VOLTAGE $V_{IN\_}$



INPUT LEAKAGE CURRENT I_{DI_LKG} vs. INPUT VOLTAGE $V_{IN\_}$

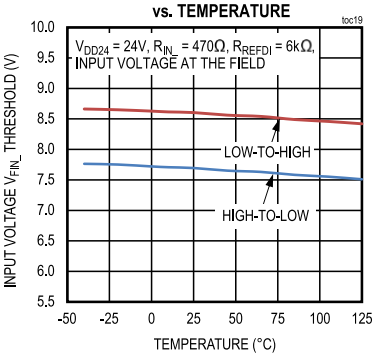


TYPE 1/3 INPUT VOLTAGE THRESHOLD vs. TEMPERATURE

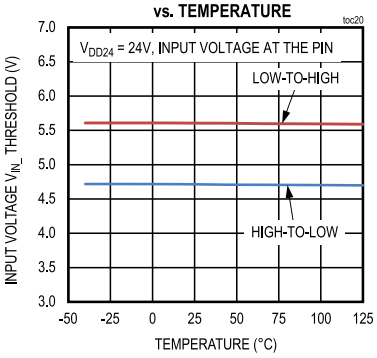


(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 18kΩ or 6kΩ, R_{IN} = 1.5k or 470Ω, unless otherwise noted.)

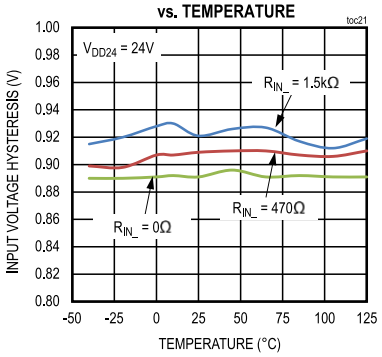
TYPE 2 INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



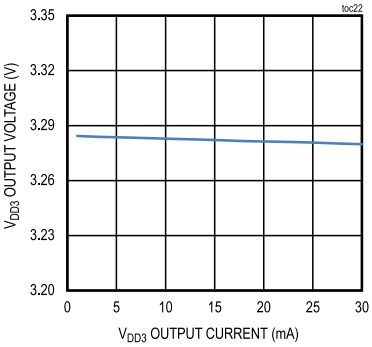
INPUT VOLTAGE THRESHOLD vs. TEMPERATURE



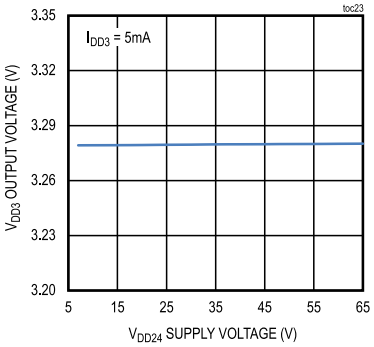
INPUT VOLTAGE HYSTERESIS vs. TEMPERATURE



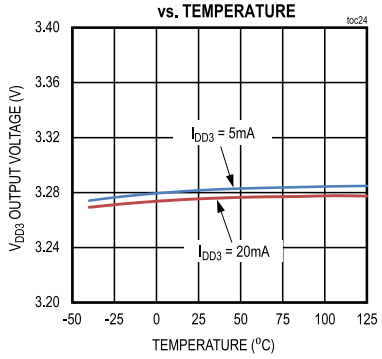
LDO LOAD REGULATION



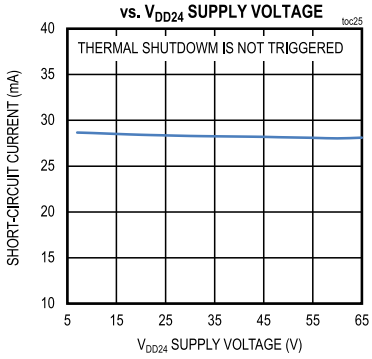
LDO LINE REGULATION



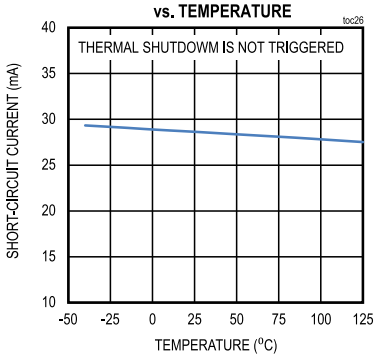
LDO OUTPUT VOLTAGE vs. TEMPERATURE



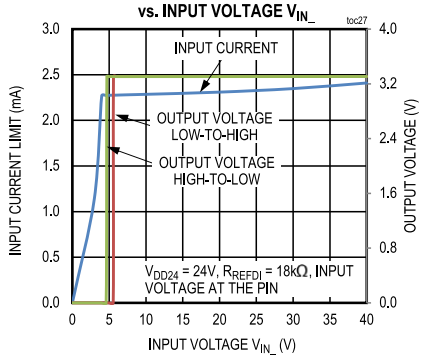
LDO SHORT-CIRCUIT CURRENT vs. V_{DD24} SUPPLY VOLTAGE



LDO SHORT-CIRCUIT CURRENT vs. TEMPERATURE

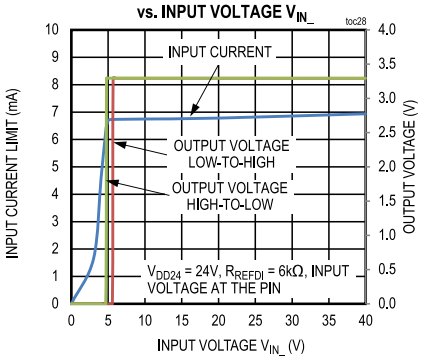


TYPE 1/3 INPUT CURRENT LIMIT I_{INLIM} AND OUTPUT VOLTAGE vs. INPUT VOLTAGE $V_{IN\_}$

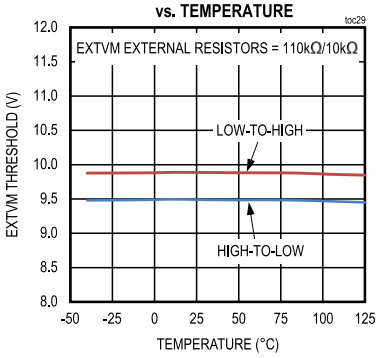


(V_{DD24} = 24V, V_{DD3} = 3.3V, T_A = +25°C, R_{REFDI} = 18kΩ or 6kΩ, R_{IN} = 1.5k or 470Ω, unless otherwise noted.)

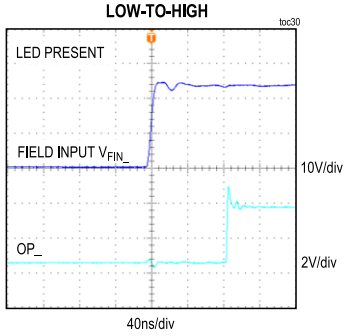
TYPE 2 INPUT CURRENT LIMIT I_{INLIM} AND OUTPUT VOLTAGE vs. INPUT VOLTAGE $V_{IN\_}$



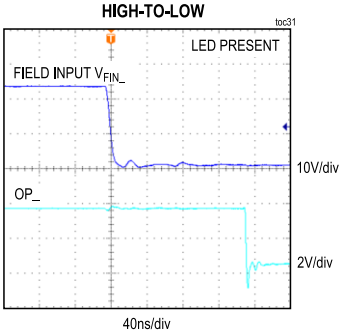
EXTVM THRESHOLD VOLTAGE vs. TEMPERATURE



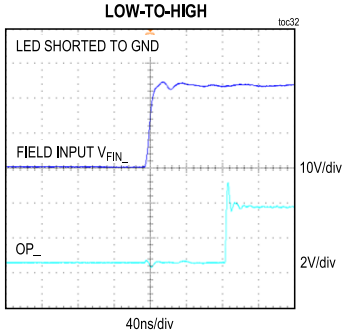
PROPAGATION DELAY LOW-TO-HIGH



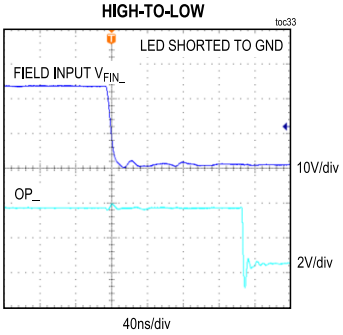
PROPAGATION DELAY HIGH-TO-LOW



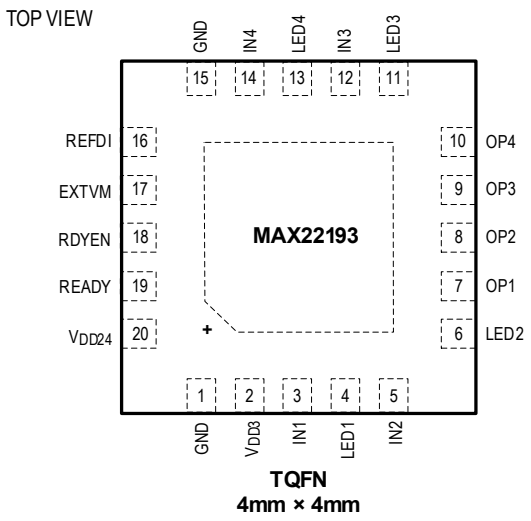
PROPAGATION DELAY LOW-TO-HIGH



PROPAGATION DELAY HIGH-TO-LOW



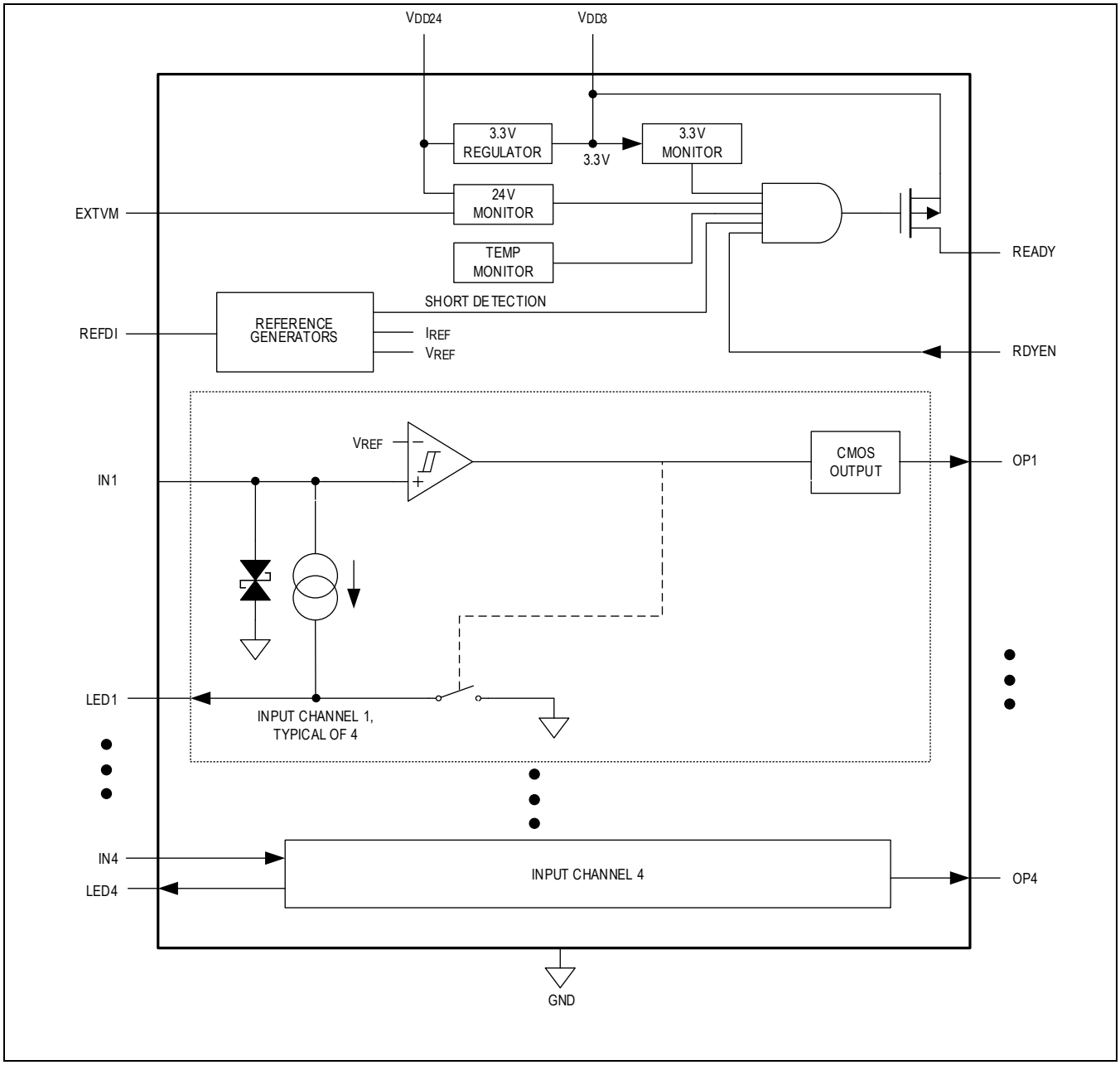
Pin Configuration



Pin Descriptions

PIN	NAME	FUNCTION
POWER SUPPLY		
20	V_{DD24}	24V Field Supply. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor. If powering V_{DD3} from an external supply, leave V_{DD24} floating.
2	V_{DD3}	3.3V output from integrated LDO when powered from V_{DD24}, or 3.0 - 5.5V supply input when V_{DD24} not driven. Bypass to GND with 0.1µF capacitor in parallel with 1µF capacitor. If powering V_{DD3} from an external supply, leave V_{DD24} floating. V_{DD3} output is turned off during thermal shutdown.
1, 15	GND	Ground Return for All Signals and the Power Supplies.
EP	-	Exposed Pad. Connect to GND. Solder entire exposed pad area to ground plane with multiple vias for best thermal performance.
ANALOG PINS		
17	EXTVM	Connect EXTVM to GND to use internal thresholds (14V, typ) for V_{DD24} voltage monitoring. Connect EXTVM to external resistive divider to set external thresholds for V_{DD24} voltage monitoring. Connect EXTVM to V_{DD3} to disable V_{DD24} voltage monitoring at READY pin if the device is powered by V_{DD3}.
16	REFDI	Digital Input Current Limiting Reference Resistor. For 24V type 1/3 inputs, place an 18kΩ resistor to GND. For type 2 inputs, place a 6kΩ resistor.
FIELD INPUT PINS		
3, 5, 12, 14	IN1 to IN4, respectively	Field Inputs. For 24V type 1/3 inputs, place a 1.5kΩ resistor between the field input and the IN_ pin. For type 2 inputs, place a 470Ω resistor. Capacitors for filtering should not be connected to the IN_ pins. See the *Surge Protection of Field Inputs section* for more information.
4, 6, 11, 13	LED1 to LED4, respectively	Energyless LED Driver Outputs. Connect to GND if LEDs are not used.
LOGIC PINS		
7, 8, 9, 10	OP1 to OP4, respectively	Logic Outputs. Indicate the state (high or low) of IN1 to IN4, respectively. High level is V_{DD3}. Low level is GND. If thermal shutdown is triggered, OP1 to OP4 are high-impedance.
18	RDYEN	Ready Enable. Has a weak internal pulldown. Assert high to enable the READY output. Cascade the READY signal of multiple devices through a single isolator or a microcontroller input pin by connecting the READY output of each device to the RDYEN input of the next device in the chain. READY from the last device in the chain drives the isolator input, or the microcontroller GPI.
19	READY	Open-drain Output. Connect a pulldown resistor between READY and GND pin. Assert high to indicate the device is functional and the outputs are valid. The following conditions must be met for READY to assert high: 1. V_{DD3} is above the UVLO threshold. 2. REFDI is not shorted to GND. 3. MAX22193 is not in thermal shutdown. 4. RDYEN is high. 5. V_{DD24} is valid if the device is powered by V_{DD24} and EXTVM is not connected to V_{DD3}.

Functional Diagram



Detailed Description

The MAX22193 senses the state (on, high or off, low) of each input (IN1 to IN4). The voltages at the IN_ input pins are compared against internal references to determine whether the sensor is on (logic 1) or off (logic 0). Placing an 18kΩ current-setting resistor between REFDI and GND, and a 1.5kΩ resistor in series with each input ensures that the current at the on and off trip points as well as the voltage at the trip points satisfy the requirements of IEC 61131-2 for Type 1/3 inputs (*Figure 2*). The current sunk by each input pin rises linearly with input voltage until the level set by the current-limiter is reached; any voltage increase beyond this point does not increase the input current. Limiting the input current ensures compliance with IEC 61131-2 while significantly reducing power dissipation compared to traditional resistive inputs.

The current-setting resistor R_{REFDI} can be calculated using this equation:

$$R_{REFDI}\ (k\Omega, typ) = 42 / (I_{INLIM}\ (mA) - V_{IN} / 517\ (V/k\Omega))$$

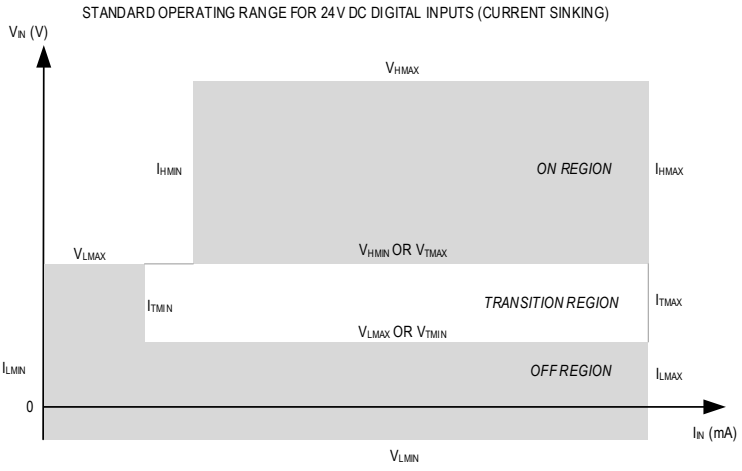
where V_{IN} is 5.6V at the input pin during production test for the typical value of Type 1/3, and Type 2 current limits.

RDYEN and READY Monitor

The READY output is used to signal a logic-side controller that the field-side circuit is working. This allows the controller to distinguish from a valid reading of four low inputs or an invalid reading caused by a field-side fault such as loss of power. The READY output is asserted high when the following five conditions are met: the UVLO voltage threshold for V_{DD3} is exceeded; the V_{DD24} field supply requirement is met as set by internal thresholds or EXTVM external thresholds if enabled; the device is not in thermal shutdown; the current through the REFDI pin is in a normal range; and the RDYEN is high.

Ready Enable RDYEN is used to cascade other READY signals through to a single digital isolation channel or a microcontroller GPI pin. Connect the READY output of one device to the RDYEN input of the next device in the chain. Connect the final READY output to a digital isolator or a microcontroller GPI pin. All READY signals must be high for the final READY signal to go high. READY is an open-drain output, driven to V_{DD3} for a high output and set at high-impedance for a low output. Refer to *Typical Application Circuits* section for details.

Outputs OP1 to OP4 are high-impedance only when thermal shutdown is triggered.



Type of Limit	Type 1 Limits						Type 2 Limits						Type 3 Limits					
	Off Region		Transition		On Region		Off Region		Transition		On Region		Off Region		Transition		On Region	
	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)	VL (V)	IL (mA)	VT (V)	IT (mA)	VH (V)	IH (mA)
Max	15/5	15	15	15	30	15	11/5	30	11	30	30	30	11/5	15	11	15	30	15
Min	-3	ND	5	0.5	15	2	-3	ND	5	2	11	6	-3	ND	5	1.5	11	2

ND = NOT DEFINED

Figure 2. Switching Characteristics for IEC 61131-2 Type 1, 2, and 3 24VDC Digital Inputs

External V_{DD24} Voltage Monitor

The EXTVM input controls how the V_{DD24} field supply affects the READY output. When EXTVM is connected to V_{DD3}, the status of the V_{DD24} field supply becomes a don't-care in the decision to assert READY. This is useful when the MAX22193 is being powered directly from a 3.3V supply on V_{DD3} and V_{DD24} is not in use. When EXTVM is connected to GND, the V_{DD24} must be above the nominal 14V threshold before READY asserted high. To use a user-defined V_{DD24} supply voltage threshold, use an external resistive divider to apply an analog voltage directly to EXTVM. The voltage at EXTVM must be greater than the threshold, 0.81V ($V_{24TH\_OFF\_ON}$) nominal, before READY asserted high. *Figure 3* shows an example of the V_{DD24} being monitored with the use of external resistive divider to set a nominal threshold before READY asserted high. Use the following equation to determine the threshold:

$$V_{DD24} = V_{REF} \times (1 + (R2/R1))$$

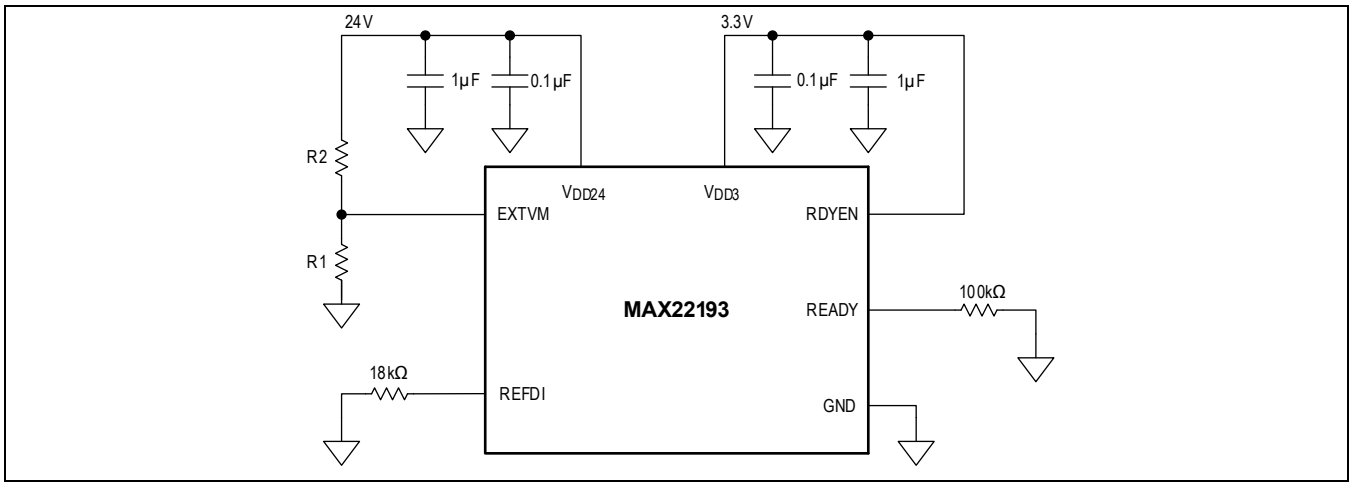


Figure 3. User-Defined V_{DD24} Threshold Set by EXTVM and External Resistive Divider

Short Detection at REFDI Pin

Short detection at REFDI pin is implemented by monitoring the current set by the resistor at the REFDI pin. When more than 550µA (typ) current is detected, meaning a short at REFDI, the 2mA minimum input current is not guaranteed; field input low-to-high and high-to-low thresholds are changed, and the READY pin is not asserted.

Energyless LED Drivers

When IN_ is determined to be on, its input current is diverted to the LED_ pin and flows from that pin to GND. Placing an LED between LED_ and GND provides an indication of the input state without increasing overall power dissipation. If the indicator LEDs are not used, connect LED_ to GND.

Type 2 Sensor Inputs

Each channel of the MAX22193 supports the higher current of Type 2 inputs (6mA, min) and the associated power dissipation. The current of the input channel is set to a nominal 7mA by placing a 6kΩ resistor from REFDI to GND. The proper voltage drop across the input resistor is maintained by reducing the resistance from 1.5kΩ to 470Ω (*Figure 4*).

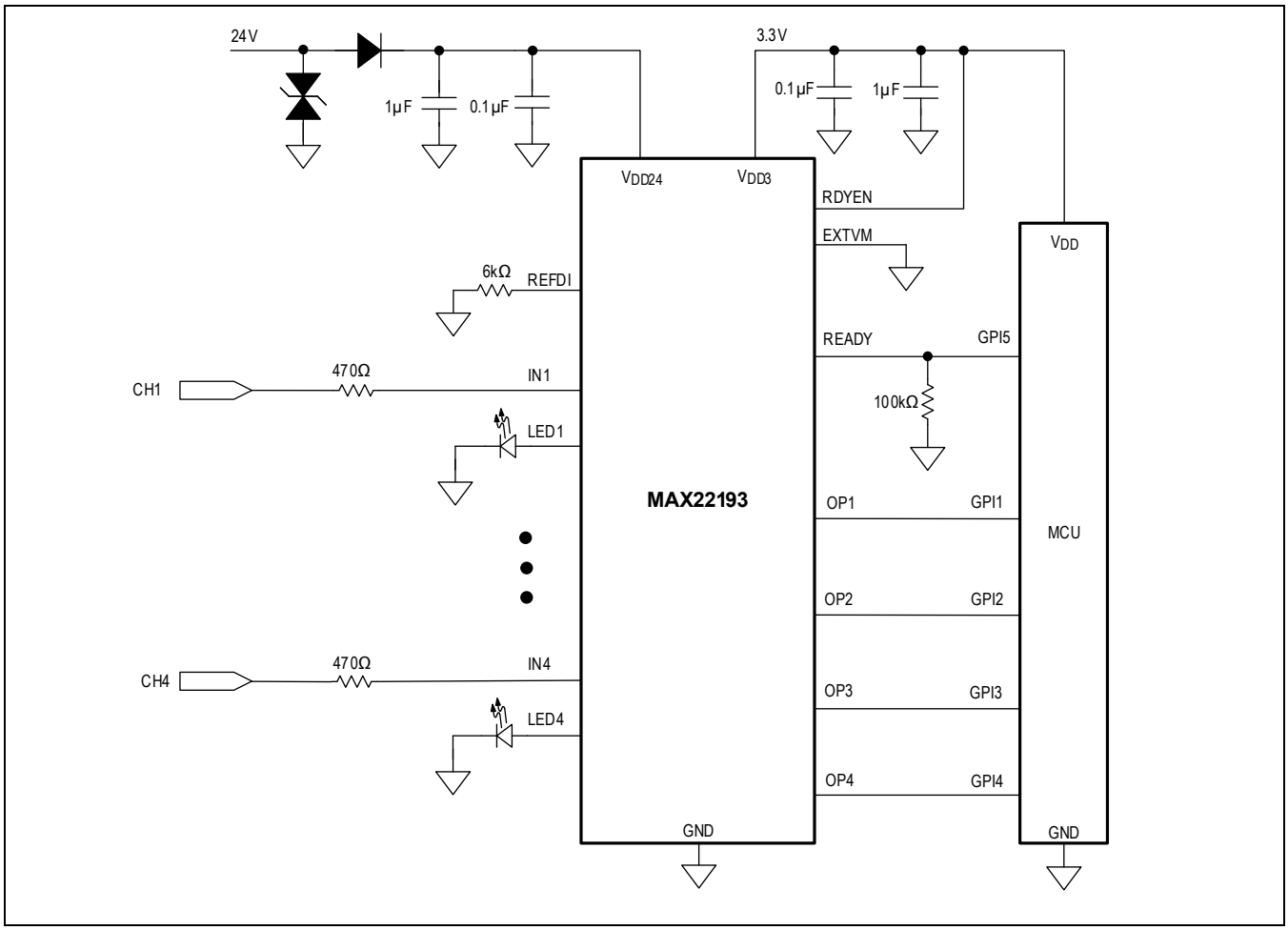


Figure 4. Implementing Type 2 Digital Inputs with MAX22193

Thermal Considerations

The MAX22193 will operate at an ambient temperature of 125°C on a properly designed multilayer PC board. Operating at higher voltages, or with heavy output loads such as optical isolators will increase power dissipation and reduce the maximum allowable operating temperature. See *Package Information* and *Absolute Maximum Ratings* for safety operation temperature and maximum power dissipation.

The MAX22193 is in thermal shutdown when the thermal shutdown temperature threshold is exceeded. During thermal shutdown, the internal voltage regulator, input channels, REFDI circuitry are all turned off, and outputs OP1 to OP4 are high-impedance.

Applications Information

Power Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DD24} and V_{DD3} with a 0.1µF low-ESR ceramic capacitor in parallel with 1µF ceramic capacitor to GND, respectively. Place the bypass capacitors as close as possible to the power supply input pins.

Powering MAX22193 with V_{DD3}

The MAX22193 can alternatively be powered using a 3.0–5.5V supply connected to the V_{DD3} pin. In this case, a 24V supply is no longer needed, the V_{DD24} pin must be left unconnected and EXTVM pin is connected to V_{DD3} to disable the V_{DD24} voltage monitoring, see *Typical Application Circuits* for details. This configuration has lower power consumption and heat dissipation since the on-chip LDO voltage regulator is disabled (the V_{DD24} undervoltage lockout is below threshold and automatically disables the LDO).

PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias on the signals to make low-inductance paths.
- Have a solid ground plane underneath the entire exposed pad (EP) area with multiple thermal vias for best thermal performance.
- In order to achieve the highest EFT performance, it is recommended to have the GND plane around the REFDI traces, and isolate the REFDI traces from all input traces, especially IN4, as much as possible. For example, route input traces and REFDI traces on two different layers and have a GND plane on the inner layers in between.

IEC 61131-2 EMC Requirements

The MAX22193 is required to operate reliably in harsh industrial environments. The device can meet the transient immunity requirements as specified in IEC 61131-2, including Electrostatic Discharge (ESD) per IEC 61000-4-2 and Surge Immunity per IEC 61000-4-5. Analog Devices' proprietary process technology provides robust input channels and field supply with internal ESD structures and high *Absolute Maximum Ratings*, but external components are also required to absorb excessive energy from ESD and surge transients. The circuit with external components shown in *Figure 5* allows the device to meet and exceed the transient immunity requirements as specified in IEC 61131-2 and related IEC 61000-4-x standards. The system shown in *Figure 5*, using the components shown in *Table 1*, is designed to be robust against ESD and Surge specifications as listed in *Table 2*. In all these tests, the part or DUT is soldered onto a properly designed application board (e.g., the MAX22193EVKIT#) with necessary external components.

Table 1. Recommended Components for EMC Compliance

COMPONENT	DESCRIPTION	REQUIRED/RECOMMENDED
C1	1µF, 100V ceramic capacitor	Required
C2	0.1µF, 100V low-ESR ceramic capacitor	Required
C3	1µF, 10V ceramic capacitor	Required
C4	0.1µF, 10V low-ESR ceramic capacitor	Required
C5	3.3nF, safety rated Y capacitor (2220)	Recommended
D1	Bi-directional TVS diode SMAJ33CA (42Ω) or SM30T39CAY (2Ω)	Recommended
D2	Bi-directional TVS diode SMAJ33CA (42Ω) or SM30T39CAY (2Ω)	Required to pair with R4
D3	Low forward voltage Schottky diode	Recommended
R1	Minimum 470Ω, 2512, 2W pulse withstanding resistor	Required
R2	Minimum 470Ω, 0603, 0.1W resistor	Required
All other resistors	0603, 0.1W resistors	Required
All LEDs	LEDs for visual input status indication	Recommended

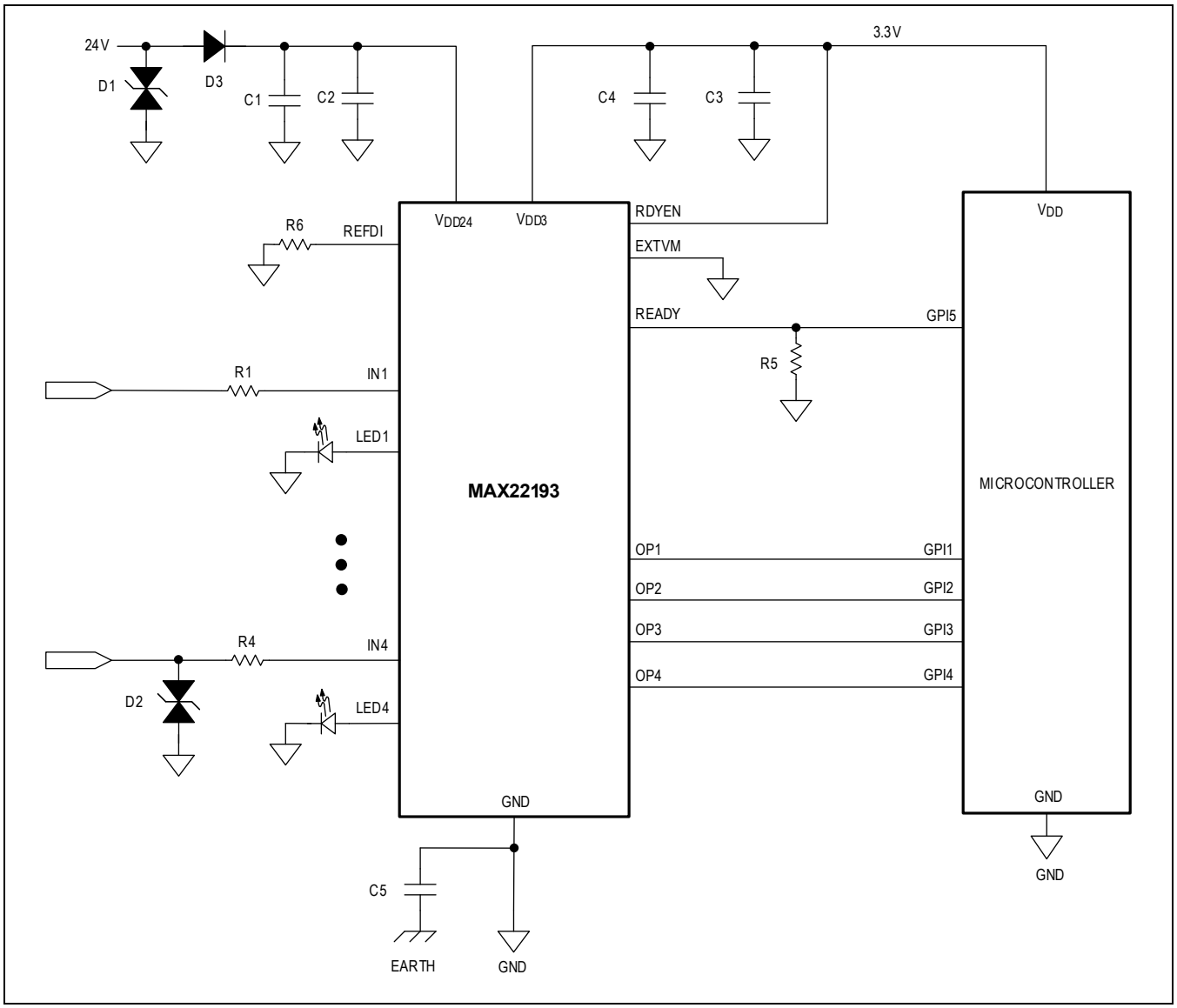


Figure 5. Typical EMC Protection Circuit for the MAX22193

ESD Protection of Field Inputs

The input resistor limits the energy into the MAX22193 IN_ pins and protects the internal ESD structure from excessive transient energy. An input series resistor is required and should be rated to withstand such ESD levels. The MAX22193 input channels can withstand up to ±8kV ESD contact discharge and ±15kV ESD air-gap discharge with an input series resistor of 470Ω or larger. The input resistor value shifts the field voltage switching threshold scaled by the input current; thus, it determines the input characteristics of the application. The package of the resistor should be large enough to prevent the arcing across the two resistor pads. Arcing depends on the ESD level applied to the field input and the application pollution degree.

Surge Protection of Field Inputs

In order to protect the IN_ pins against ±2kV/42Ω, 1.2/50µs surges (*Figure 6* and *Figure 7*), two options exist. The first option is to use a series pulse-withstanding resistor as shown in the various application diagrams in the data sheet. The pulse resistor should support dissipation of the surge energy. For Type 1/3 digital inputs with 1.5kΩ series resistors, it is recommended to use CRCW-IF or CRCW-HP thick film resistor, or similar, to protect against up to ±2kV surges. For Type 2 digital inputs with 470Ω series resistors, it is recommended to use CRCW-IF or CRCW-HP thick film resistor, or similar,

to protect against up to ±1kV surge. Use the CMB0207 MELF resistor for ±2kV surge protections. Capacitors for filtering should not be connected to the IN_ pins.

The second option, which can result in a smaller overall footprint, is to use a bidirectional TVS to GND at the field input with a low-power series resistor, greater or equal to 470Ω. The TVS must be able to absorb the surge energy and has the function of limiting the peak voltage so that the resistor only sees a low differential voltage. Suitable TVS with a small footprint are SMAJ33CA, offering protection against ±2kV /42Ω surges.

Surge Protection of 24V Supply

In order to protect the V_{DD24} pin against ±1kV/42Ω, 1.2/50µs surges (*Figure 6*), an SMAJ33CA TVS can be applied to the V_{DD24} pin, along with a series Schottky diode for reverse current protection. To protect against ±1kV/2Ω, 1.2µs/50µs surges, an SM30T39CAY TVS can be applied to the V_{DD24} pin.

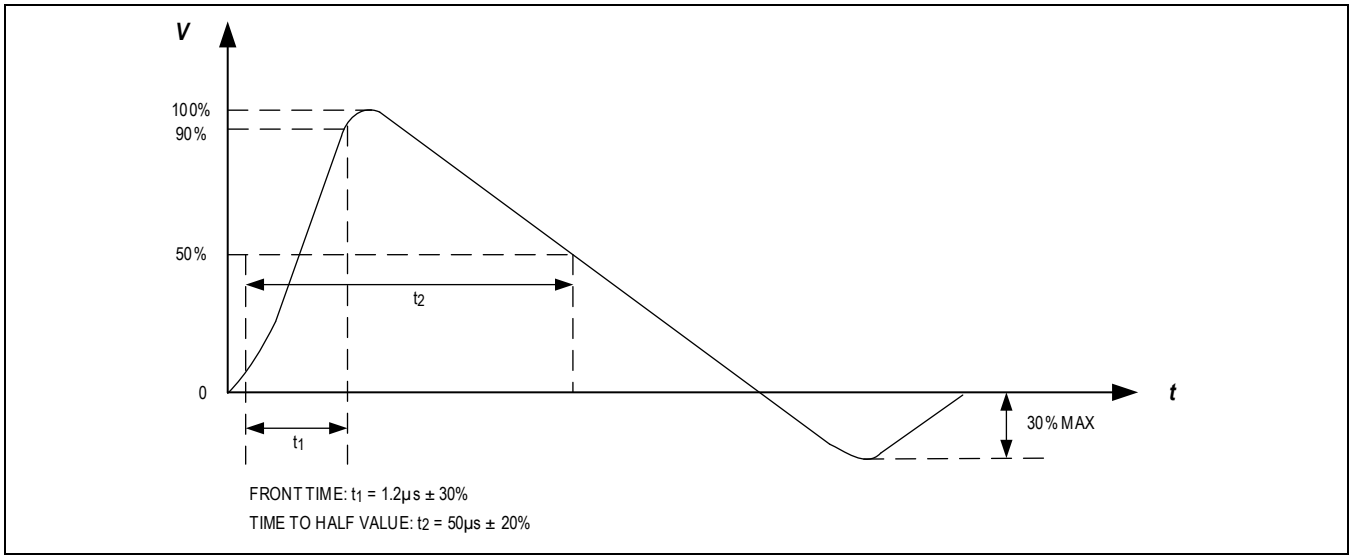


Figure 6. 1.2/50µs Surge Voltage Waveform

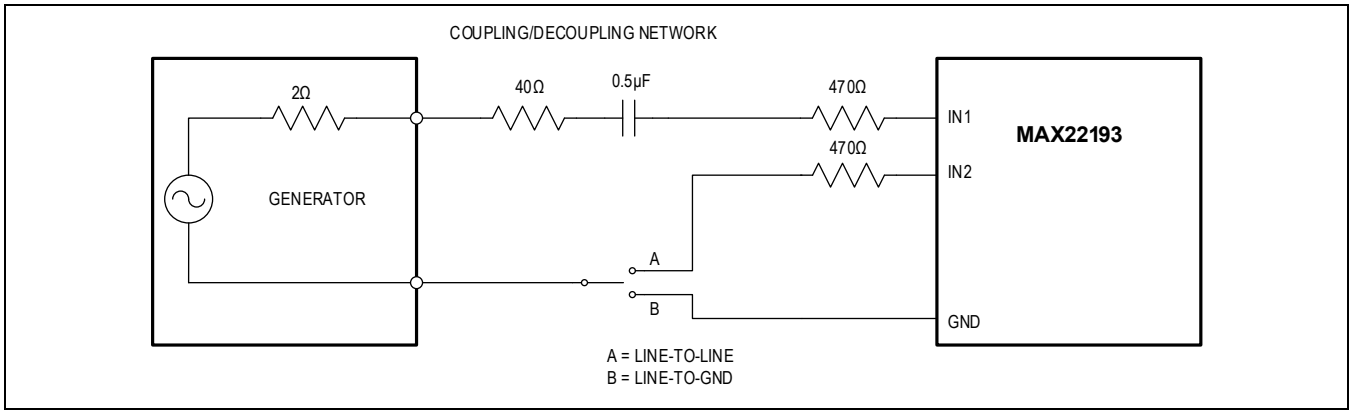
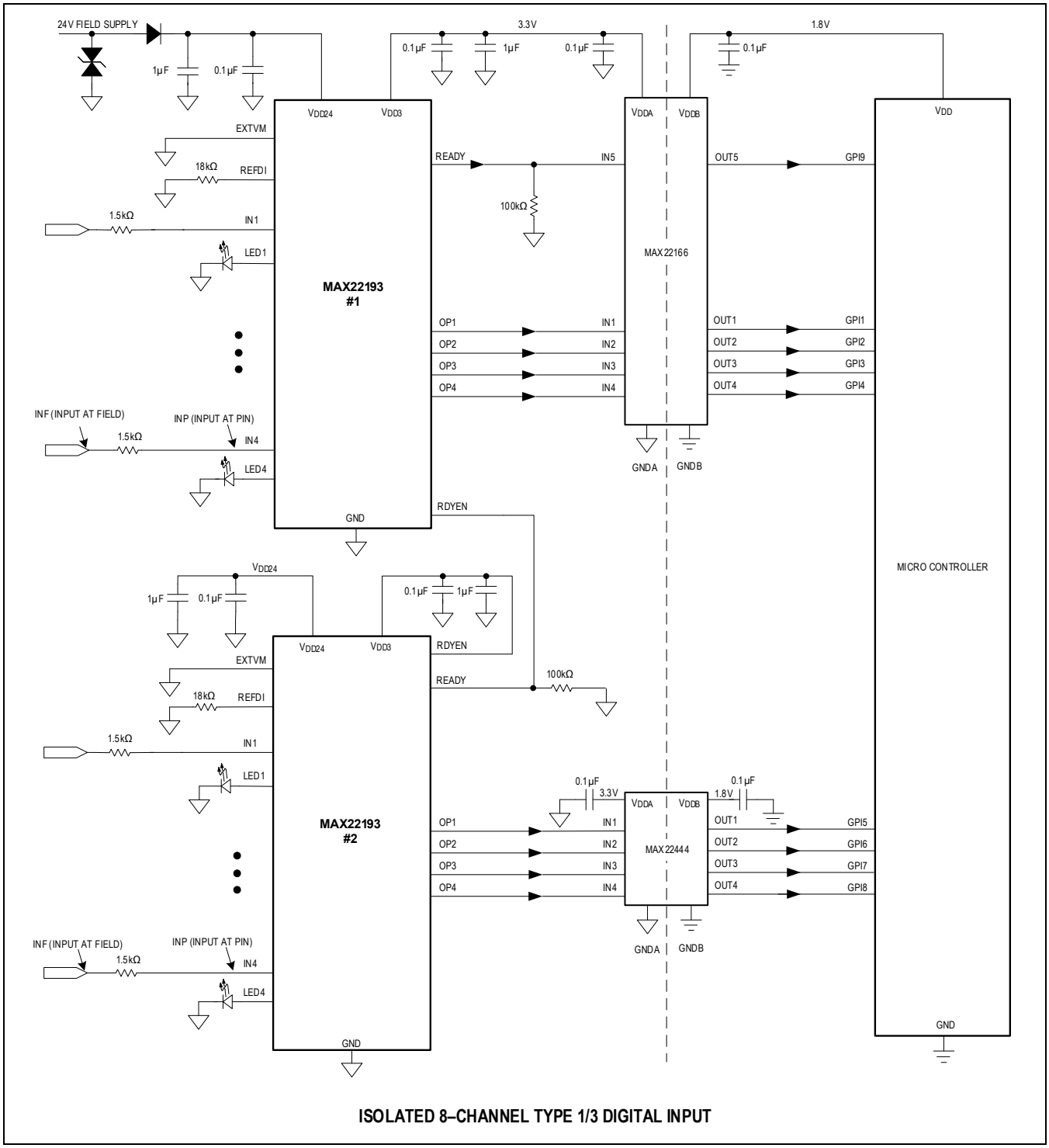


Figure 7. Surge Testing Method

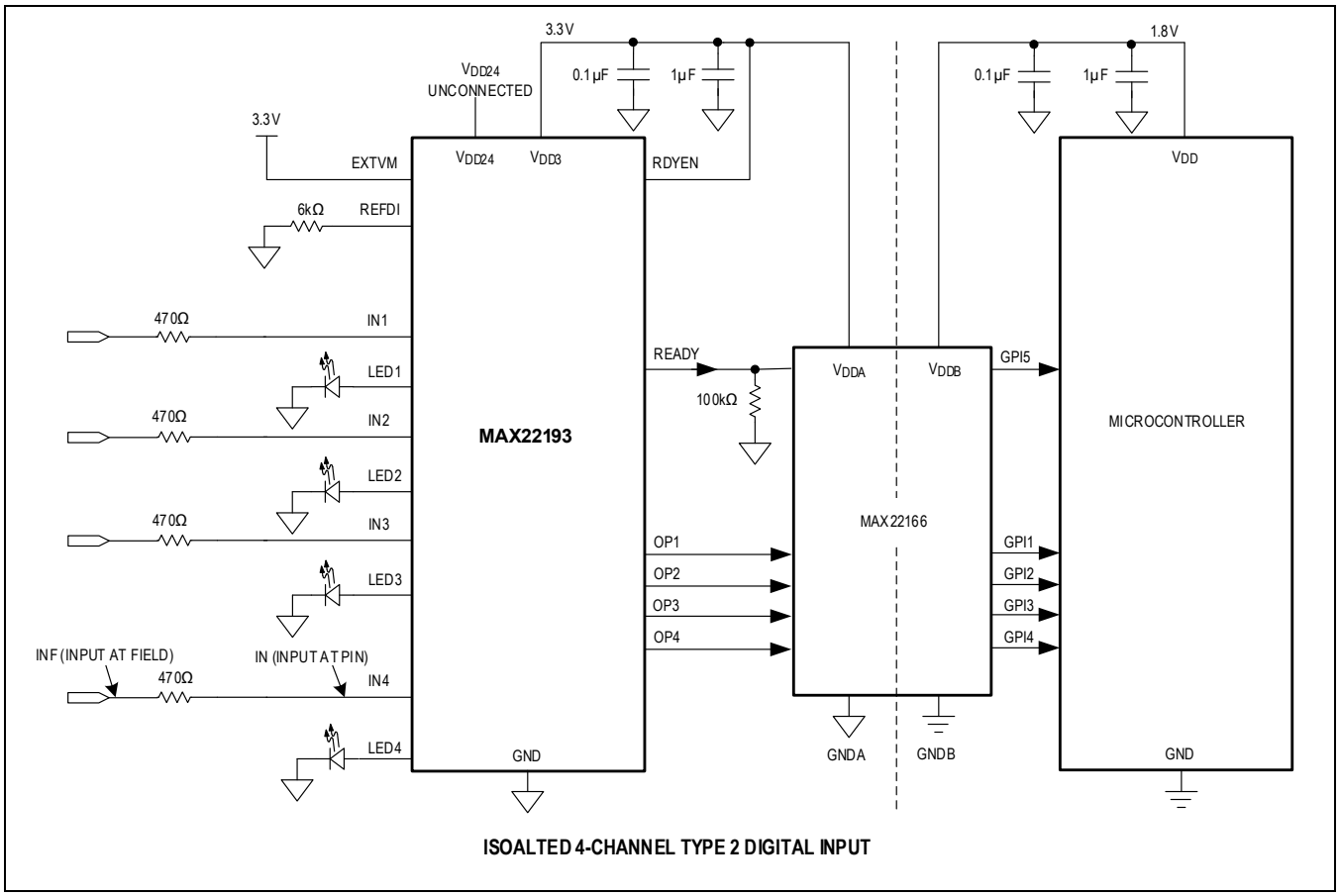
Table 2. Transient Immunity Test Results

TEST		RESULT
IEC 61000-4-2 Electrostatic Discharge (ESD)	Contact ESD	±8kV
	Air-Gap ESD	±15kV
IEC 61000-4-5 Surge Immunity	Line-to-Ground	±2kV
	Line-to-Line	±2kV
	Power Supply	±1kV

Typical Application Circuits



ISOLATED 8–CHANNEL TYPE 1/3 DIGITAL INPUT



ISOALTED 4-CHANNEL TYPE 2 DIGITAL INPUT

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22193ATP+	-40°C to +125°C	20-TQFN
MAX22193ATP+T	-40°C to +125°C	20-TQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and Read.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	06/22	Release for Market Intro	—