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NTE4514B & NTE4515B
Integrated Circuit
CMOS, 4–Bit Latch/4–to–16 Line Decoder

Description:

The NTE4514B (output active high option) and NTE4515B (output active low option) are two output options of a 4–to–16 line decoder with latched inputs. The NTE4514B presents a logical “1” at the selected output, whereas the NTE4515B presents a logical “0” at the selected output. The latches are R–S type flip–flops which hold the last input data presented prior to the strobe transition from “1” to “0”. These high and low options of a 4–bit latch/4–to–16 line decoder are constructed with N–channel and P–channel enhancement mode devices in a single monolithic structure. The latches are R–S type flip–flops and data admitted upon a signal incident at the strobe input, decoded, and presented at the output.

These complementary circuits find primary use in decoding applications where low power dissipation and/or high immunity is desired.

Features:

- Quiescent Current = 5nA/Package (Typ) at 5Vdc
- Noise Immunity = 45% of V_{DD} (Typ)
- Supply Voltage Range: 3Vdc to 18Vdc
- Capable of Driving Two Low–Power TTL Loads, One Low–Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Single Supply Operation – Positive or Negative
- Input Impedance = 10^{12} Ohms (Typ)

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (All Inputs), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I 10mA
Operating Temperature Range, T_A . . . . . –55° to +125°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. These devices contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 3)

Parameter	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage (Note 5) "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	−1.2	–	−1.0	−1.7	–	−0.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	mAdc
(V_{OH} = 9.5Vdc)		10	−0.62	–	−0.5	−0.9	–	−0.35	–	mAdc
(V_{OH} = 13.5Vdc)		15	−1.8	–	−1.5	−3.5	–	−1.1	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all outputs, all buffers switching, Note 4, Note 6)	I_T	5.0	I_T = (1.35µA/kHz) f + I_{DD}							µAdc
		10	I_T = (2.70µA/kHz) f + I_{DD}							µAdc
		15	I_T = (4.05µA/kHz) f + I_{DD}							µAdc

Note 3. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 4. The formulas given are for the typical characteristics only at +25°C.

Note 5. Noise immunity specified for worst−case input combination.
Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
2.0Vdc min @ V_{DD} = 10Vdc
2.5Vdc min @ V_{DD} = 15Vdc

Note 6. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + 2 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, f in kHz is input frequency.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 3)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					
t_{TLH} = (3.0ns/pf) C_L + 30ns		5.0	–	180	360	ns
t_{TLH} = (1.5ns/pf) C_L + 15ns		10	–	90	180	ns
t_{TLH} = (1.1ns/pf) C_L + 10ns		15	–	65	130	ns
Output Fall Time	t_{THL}					
t_{THL} = (1.5ns/pf) C_L + 25ns		5.0	–	100	200	ns
t_{THL} = (0.75ns/pf) C_L + 12.5ns		10	–	50	100	ns
t_{THL} = (0.55ns/pf) C_L + 9.5ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 465ns		5.0	–	550	1100	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 192ns		10	–	225	450	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 125ns		15	–	150	300	ns
Inhibit Propagation Delay Times	t_{PLH}, t_{PHL}					
t_{PLH}, t_{PHL} = (1.7ns/pf) C_L + 315ns		5.0	–	400	800	ns
t_{PLH}, t_{PHL} = (0.66ns/pf) C_L + 117ns		10	–	150	300	ns
t_{PLH}, t_{PHL} = (0.5ns/pf) C_L + 75ns		15	–	100	200	ns
Setup Time	t_{su}	5.0	250	125	–	ns
		10	100	50	–	ns
		15	75	38	–	ns
Strobe Pulse Width	t_{WH}	5.0	350	175	–	ns
		10	100	50	–	ns
		15	75	38	–	ns

Note 3. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

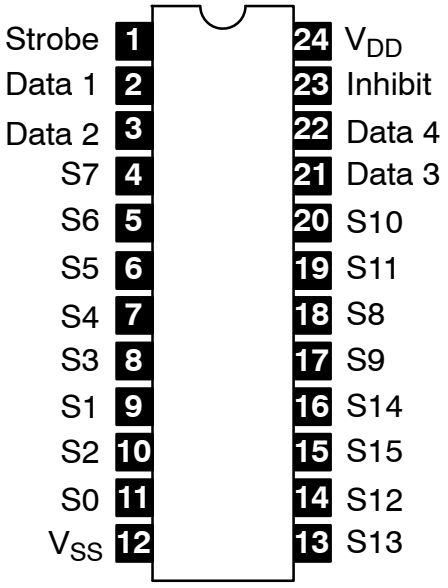
Note 4. The formulas given are for the typical characteristics only at +25°C.

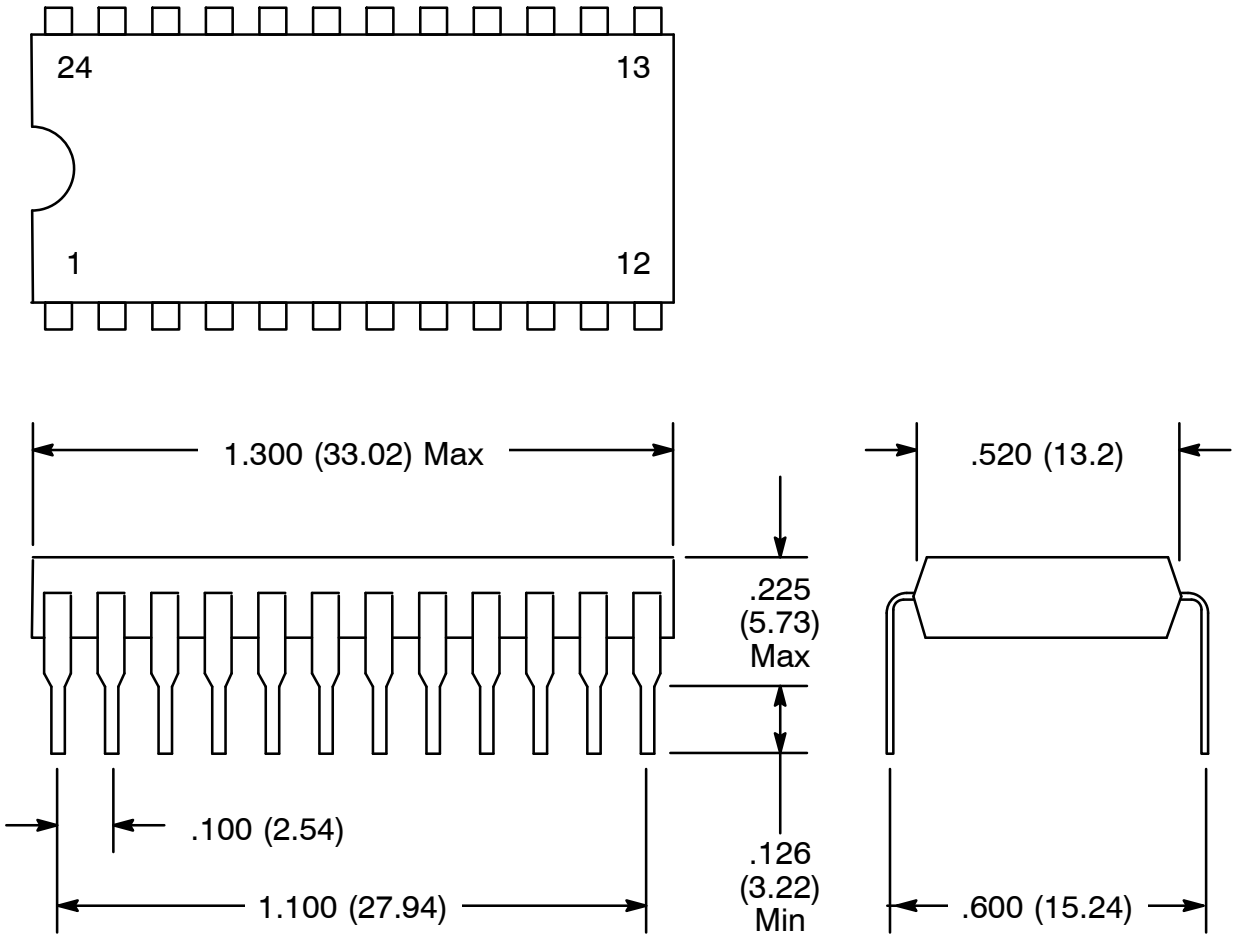
Truth Table

Inhibit	Data Inputs				Selected Output NTE4514B = Logic “1” NTE4515B = Logic “0”
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, NTE4514B All Output = 1, NTE4515B

X = Don’t Care

Pin Connection Diagram




24
13
1
12
1.300 (33.02) Max
.520 (13.2)
.225
(5.73)
Max
.100 (2.54)
1.100 (27.94)
.126
(3.22)
Min
.600 (15.24)