MPM3690-50A/B

16V, Dual 25A or Single 50A DC/DC Power Module

DESCRIPTION

The MPM3690-50 is a dual 25A or single 50A output power module that offers a complete power solution with excellent load and line regulation. The MPM3690-50 supports a 4V to 16V input voltage range and a 0.6V to 1.8V output voltage range. The voltages at the MPM3690-50's two outputs can be set separately by a single resistor per output.

The MPM3690-50 offers two configurations: the MPM3690-50A has a dual 25A output, and the MPM3690-50B has a single 50A output. The MPM3690-50 is also pin-compatible with the MPM3690-20A/B (dual 13A or single 26A) and the MPM3690-30A/B (dual 18A or single 36A) power modules.

The MPM3690-50 adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and minimizes the output capacitance.

The MPM3690-50 integrates a monolithic DC/DC converter, power inductor, and other passive components, and is available in a BGA (16mmx16mmx5.18mm) package,

FEATURES

- Pin-Compatible Dual 25A and Single 50A Output Power Modules
  - MPM3690-50A Dual 25A
  - MPM3690-50B Single 50A
- 4V to 16V Input Voltage Range
  - 3.2V to 16V Input Voltage Range with External 3.3V VCC Bias
- 0.6V to 1.8V Output Voltage Range
- Ultra-Fast Transient Enabled by COT Control
- Adjustable Switching Frequency
- Adjustable Soft-Start Time
- Over-Current and Over-Voltage Protection
- Differential Remote Sense for Both Output Channels
- Pin-Compatible with the MPM3690-20A/B and MPM3695-30A/B
- Available in a BGA Package (16mmx16mmx5.18mm)

APPLICATIONS

- Telecom and Networking Equipment
- Industrial Equipment
- FPGA and ASIC Power Systems

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TYPICAL APPLICATION

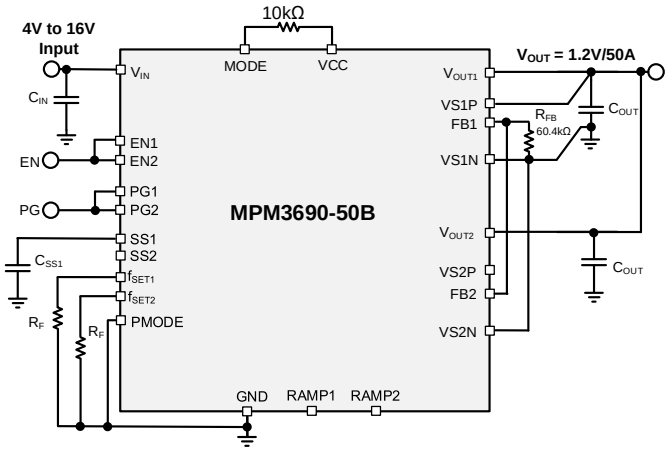
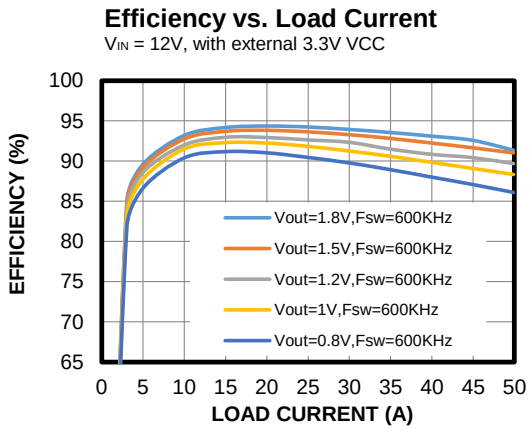


Figure 1: Interleaved Operation at 1.2V, 50A



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ORDERING INFORMATION

Part Number*	Configuration	Package	Top Marking	MSL Rating
MPM3690GBF-50A	Dual 25A Output	BGA (16mmx16mmx5.18mm)	*See Below*	3
MPM3690GBF-50B	Single 50A Output			

* For tray, add suffix -T (e.g. MPM3690GBF-50A-T).

TOP MARKING (MPM3690GBF-50A)

```
MPS   YYWW
M3690-50A
LLLLLLLLL
        M
```

MPS: MPS prefix
YY: Year code
WW: Week code
M3690-50A: Part number
LLLLLLLLL: Lot number
M: Module

TOP MARKING (MPM3690GBF-50B)

```
MPS   YYWW
M3690-50B
LLLLLLLLL
        M
```

MPS: MPS prefix
YY: Year code
WW: Week code
M3690-50B: Part number
LLLLLLLLL: Lot number
M: Module

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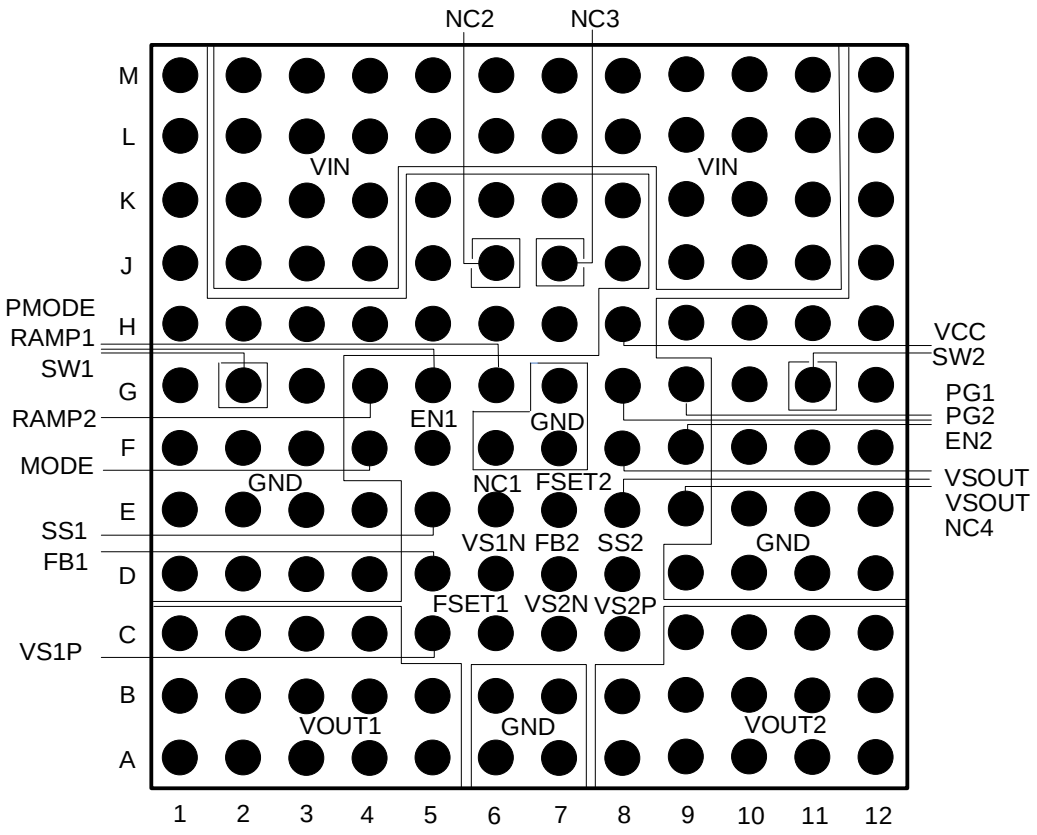
PIN-COMPATIBLE PARTS

Part Number	Output	Description
MPM3690GBF-20A	Dual 13A	4V to 16V input, 0.6V to 3.3V output, BGA (16mmx16mmx5.18mm) package
MPM3690GBF-20B	Single 26A	4V to 16V input, 0.6V to 3.3V output, BGA (16mmx16mmx5.18mm) package
MPM3690GBF-30A	Dual 18A	4V to 16V input, 0.6V to 3.3V output, BGA (16mmx16mmx5.18mm) package
MPM3690GBF-30B	Single 36A	4V to 16V input, 0.6V to 3.3V output, BGA (16mmx16mmx5.18mm) package
MPM3690GBF-50A	Dual 25A	4V to 16V input, 0.6V to 1.8V output, BGA (16mmx16mmx5.18mm) package
MPM3690GBF-50B	Single 50A	4V to 16V input, 0.6V to 1.8V output, BGA (16mmx16mmx5.18mm) package

Order directly from MonolithicPower.com or our distributors.

PACKAGE REFERENCE

TOP VIEW



BGA Package (16mmx16mmx5.18mm)

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PIN FUNCTIONS

Pin Number	Name	Description
A1–A5, B1–B5, C1–C4	VOUT1	**Power output 1.** Power output pins for channel 1.
A6, A7, B6, B7, D1–D4, D9–D12, E1–E4, E10, E11, E12, F1, F2, F3, F6, F7, F10, F11, F12, G1, G3, G7, G10, G12, H1–H7, H9–H12, J1, J5, J8, J12, K1, K5–K8, K12, L1, L12, M1, M12	GND	**Power ground.** GND is the ground of the regulated output voltage (V_{OUT}).
A8–A12, B8–B12, C9–C12	VOUT2	**Power output 2.** Power output pins for channel 2.
C5, C8	VS1P, VS2P	**Positive input of the remote-sense amplifier.** Connect these pins to the V_{OUT} remote sense point.
D6, C7	VS1N, VS2N	**Negative input of the remote-sense amplifier.** Connect these pins to the output GND remote sense point to enable remote sense. Connect directly to GND to disable the remote sense function.
C6, E7	FSET1, FSET2	**Frequency set.** Connect a resistor between these pins and AGND to configure the switching frequency (f_{SW}) between 400kHz to 1MHz. For the MPM3690-50B, the FSET1 and FSET2 resistors must be the same.
D5, D7	FB1, FB2	**Feedback voltage.** Connect a resistor to these pins between VS1N and VS2N to configure V_{OUT}. This pin is connected to VS1P and VS2P with a 60.4kΩ resistor.
E5, D8	SS1, SS2	**Soft-start time setting.** Connect a ceramic capacitor to set the soft-start time (t_{SS}).
G5, G4	RAMP1, RAMP2	**Ramp selection pin.** Float these pins to set the internal compensation ramp to high; pull these pins pin low to set the internal compensation ramp to low.
E8, F8	VSOUT	**Not connected (internally floated).** Float these pins**.**
F4	MODE	**Operation mode set.** Pull MODE up to VCC for forced continuous conduction mode (FCCM).
F5, F9	EN1, EN2	**Enable pins.** Drive EN pin high to turn the output on, drive it low to turn the output off. Do not float this pin.
G2, G11	SW1, SW2	**Switching nodes.** Float these pins.
G6	PMODE	**Protection mode selection.** Connect PMODE to GND for latch-off mode, pull PMODE up to VCC for hiccup mode.
G9, G8	PG1, PG2	**Power good outputs.** The output of the PG pins is an open drain. Pull the PG pins high with a pull-up resistor.
H8	VCC	**Output of the internal power supply.** Float this pin or connect it to an external 3.3V power supply to improve efficiency.
E6, J6, J7, E9	NC1, NC2, NC3, NC4	**Not connected (internally floated).** Float these pins.
M2–M11, L2–L11, J2, J3, J4, J9, J10, J11, K2, K3, K4, K9, K10, K11	VIN	**Supply voltage.** Connect input voltage between these pins and GND pins.

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PIN MAP

Table 1: Pins A1–F12

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
A1	VOUT1	B1	VOUT1	C1	VOUT1	D1	GND	E1	GND	F1	GND
A2	VOUT1	B2	VOUT1	C2	VOUT1	D2	GND	E2	GND	F2	GND
A3	VOUT1	B3	VOUT1	C3	VOUT1	D3	GND	E3	GND	F3	GND
A4	VOUT1	B4	VOUT1	C4	VOUT1	D4	GND	E4	GND	F4	MODE
A5	VOUT1	B5	VOUT1	C5	VS1P	D5	FB1	E5	SS1	F5	EN1
A6	GND	B6	GND	C6	FSET1	D6	VS1N	E6	NC1	F6	GND
A7	GND	B7	GND	C7	VS2N	D7	FB2	E7	FSET2	F7	GND
A8	VOUT2	B8	VOUT2	C8	VS2P	D8	SS2	E8	VSOUT	F8	VSOUT
A9	VOUT2	B9	VOUT2	C9	VOUT2	D9	GND	E9	NC4	F9	EN2
A10	VOUT2	B10	VOUT2	C10	VOUT2	D10	GND	E10	GND	F10	GND
A11	VOUT2	B11	VOUT2	C11	VOUT2	D11	GND	E11	GND	F11	GND
A12	VOUT2	B12	VOUT2	C12	VOUT2	D12	GND	E12	GND	F12	GND

Table 2: Pins G1–M12

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	VIN	K2	VIN	L2	VIN	M2	VIN
G3	GND	H3	GND	J3	VIN	K3	VIN	L3	VIN	M3	VIN
G4	RAMP2	H4	GND	J4	VIN	K4	VIN	L4	VIN	M4	VIN
G5	RAMP1	H5	GND	J5	GND	K5	GND	L5	VIN	M5	VIN
G6	PMODE	H6	GND	J6	NC2	K6	GND	L6	VIN	M6	VIN
G7	GND	H7	GND	J7	NC3	K7	GND	L7	VIN	M7	VIN
G8	PG2	H8	VCC	J8	GND	K8	GND	L8	VIN	M8	VIN
G9	PG1	H9	GND	J9	VIN	K9	VIN	L9	VIN	M9	VIN
G10	GND	H10	GND	J10	VIN	K10	VIN	L10	VIN	M10	VIN
G11	SW2	H11	GND	J11	VIN	K11	VIN	L11	VIN	M11	VIN
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
$V_{SW1/2}$ (DC) .....-0.3 V to +18.3V
V_{CC} 4.5V
V_{CC} (1s) (3)..... 6V
All other pins .....-0.3V to +4.3V
All other pins (1s) (3) 6V
Continuous power dissipation (T_A = 25°C) (2)
..... 18.59W
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....4V to 16V
Output voltage (V_{OUT}).....0.6V to 1.8V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
EVM3690-50B-BF-00A	7.8	4.1	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3690-50B-BF-00A, 4-layer PCB, 10cmx10cm.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
V_{IN} Supply Current						
Supply current (quiescent)	I_{IN}	EN = 0V, FB = 0.65V, R_{FREQ} = 30kΩ to GND		1.5	2	mA
Output Current Limit						
Output current limit (inductor valley)	I_{LIM_VALLEY}	Individual phase current limit, f_{SW} = 800kHz, V_{OUT} = 1.2V		24		A
Low-side negative current limit	I_{LIM_NEG}	Individual phase current limit		-13		A
Frequency and Timer						
Switching frequency	f_{SW}	R_{FREQ} = 30kΩ		800		kHz
Minimum on time (5)	t_{ON_MIN}	f_{SW} = 800kHz, V_{OUT} = 0.6V		50		ns
Minimum off time (5)	t_{OFF_MIN}			220		ns
Output Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		116%	120%	124%	V_{REF}
UVP threshold	V_{UVP}		70%	74%	79%	V_{REF}
EN						
Input high voltage	V_{IH_EN}		2.15			V
Input low voltage	V_{IL_EN}				1.20	V
Feedback Voltage						
Feedback accuracy			594	600	606	mV
Soft Start						
Soft-start current	I_{SS}		15	20	25	μA
Error Amplifier						
Feedback current	I_{FB}	V_{FB} = 0.65V		50	100	nA
Soft Shutdown						
Soft shutdown discharge FET	R_{ON_DISCH}	T_J = 25°C		60	120	Ω
UVLO						
VCC under-voltage lockout rising threshold	VCC_{VTH_RISE}		2.6	2.75	2.9	V
VCC under-voltage lockout falling threshold	VCC_{VTH_FALL}		2.3	2.45	2.6	V
VCC output voltage	V_{CC}		3.1	3.25	3.4	V
Power Good (PG)						
Power good high threshold	$PG_{VTH_HI_RISE}$	FB from low to high	88.5%	92.5%	96.5%	V_{REF}
Power good low threshold	$PG_{VTH_LO_RISE}$	FB from low to high	116%	120%	124%	V_{REF}
	$PG_{VTH_LO_FALL}$	FB from high to low	70%	74%	78%	V_{REF}
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3V, T_J = 25°C		1.5	2.5	μA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PG up to 3.3V through a 100kΩ resistor, T_J = 25°C		600	720	mV
	V_{OL_10}	V_{IN} = 0V, pull PG up to 3.3V through a 10kΩ resistor, T_J = 25°C		700	820	
Thermal Protection						
Thermal shutdown threshold (5)				160		°C
Thermal hysteresis threshold (5)				30		°C

Note:

5) Guaranteed by sample characterization. Not tested in production. The parameter is tested during parameters characterization.

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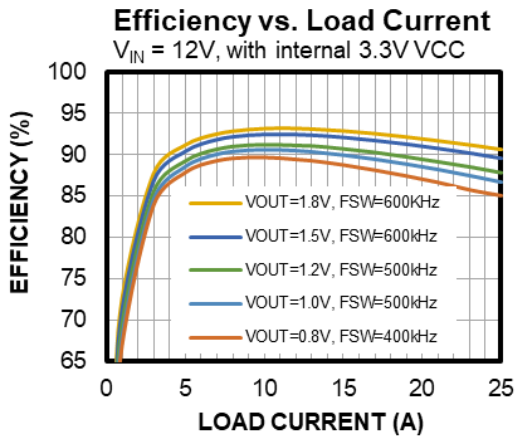
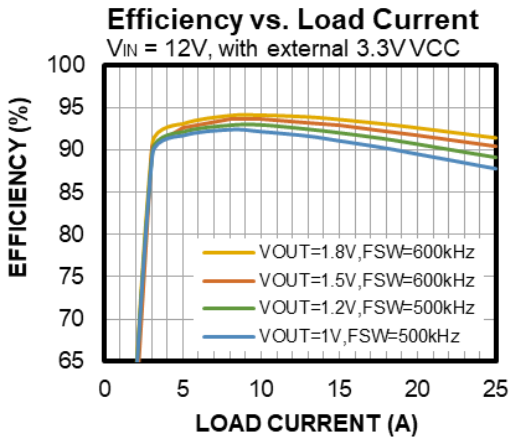
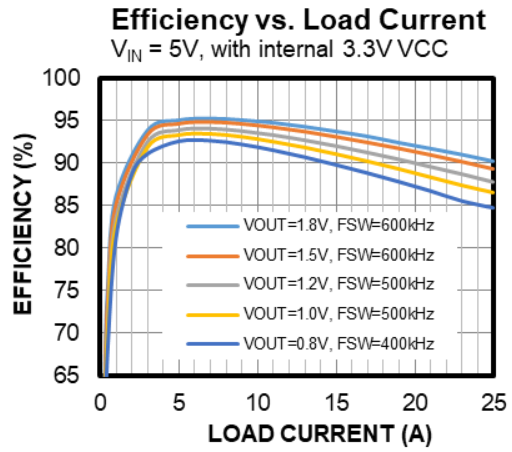
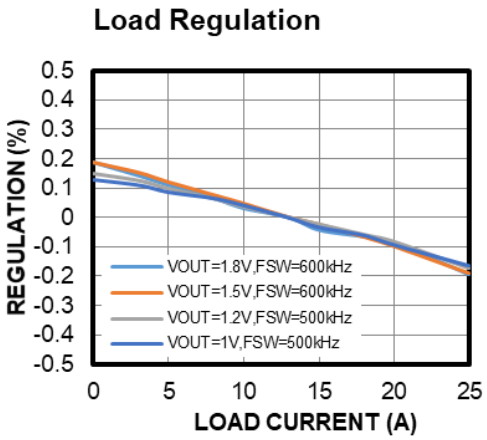
TYPICAL PERFORMANCE CHARACTERISTICS

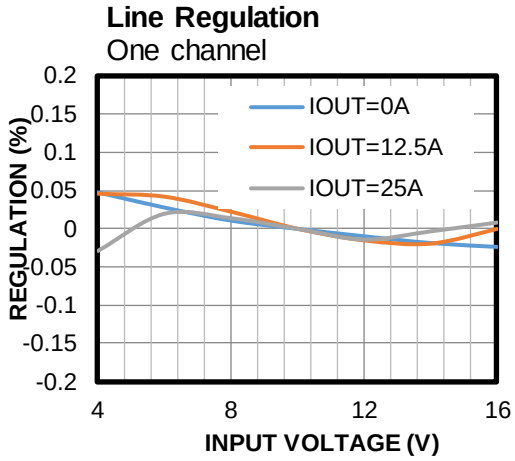
MPM3690-50A, V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 1.2V, C_{OUT1} = C_{OUT2} = 690µF, f_{SW1} = f_{SW2} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.











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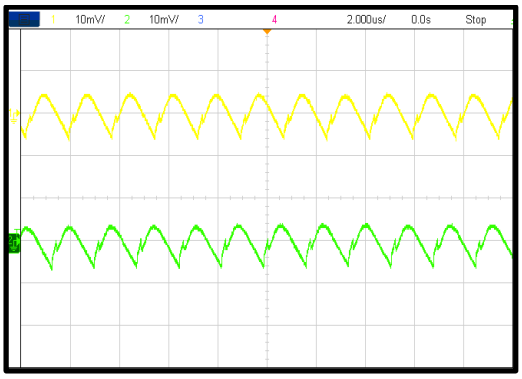
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50A, V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 1.2V, C_{OUT1} = C_{OUT2} = 690µF, f_{SW1} = f_{SW2} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

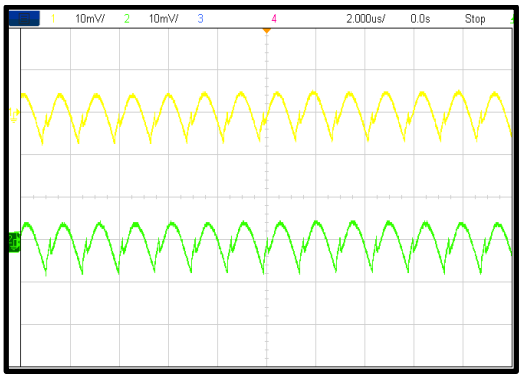
Ripple

I_{OUT1} = I_{OUT2} =0A



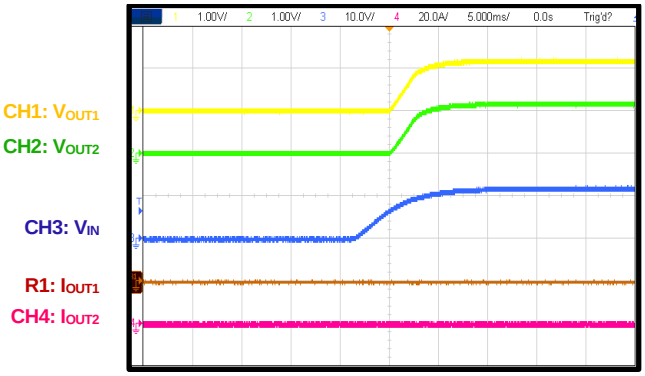
Ripple

I_{OUT1} = I_{OUT2} =25A



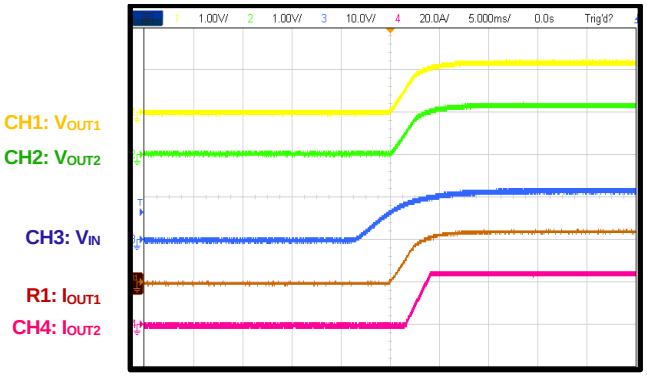
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 0A



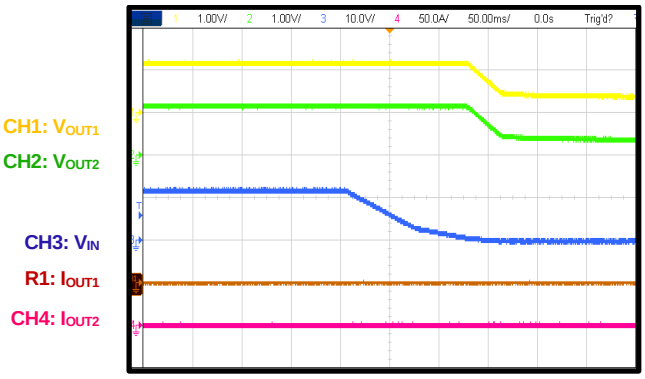
Start-Up through VIN

I_{OUT1} = I_{OUT2} = 25A



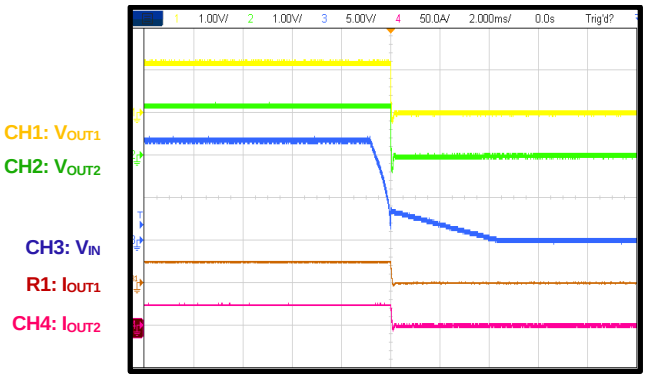
Shutdown through VIN

I_{OUT1} = I_{OUT2} = 0A



Shutdown through VIN

I_{OUT1} = I_{OUT2} = 25A



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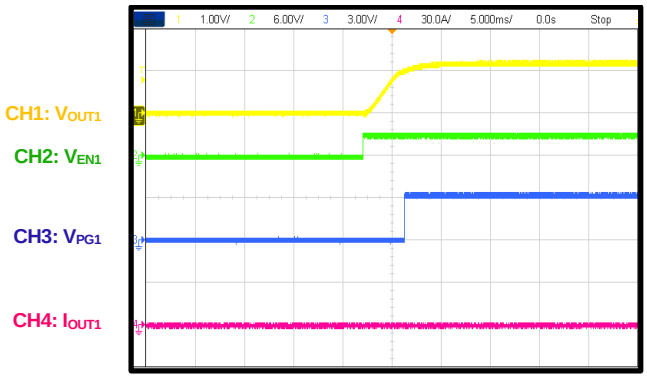
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50A, V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 1.2V, C_{OUT1} = C_{OUT2} = 690µF, f_{SW1} = f_{SW2} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

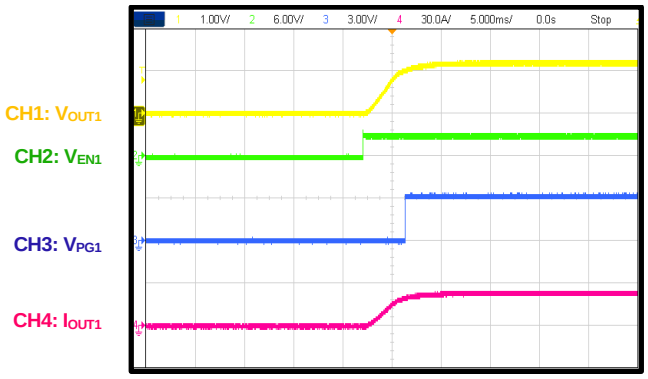
Start-Up through EN

I_{OUT1} = 0A



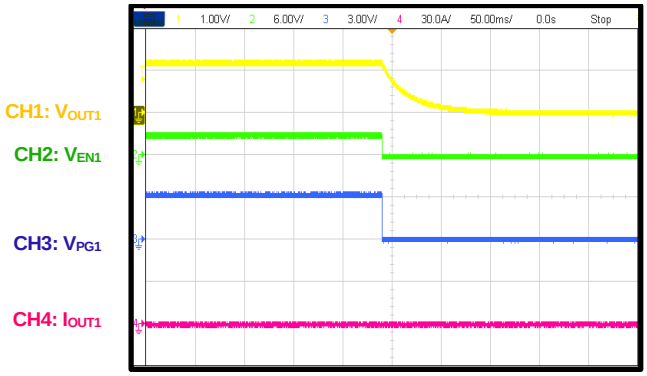
Start-Up through EN

I_{OUT1} = 25A



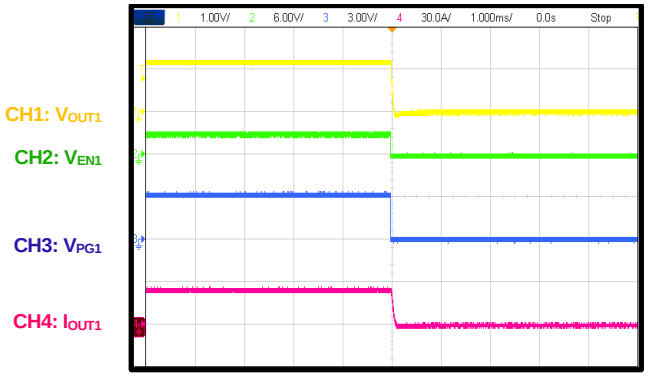
Shutdown through EN

I_{OUT1} = 0A



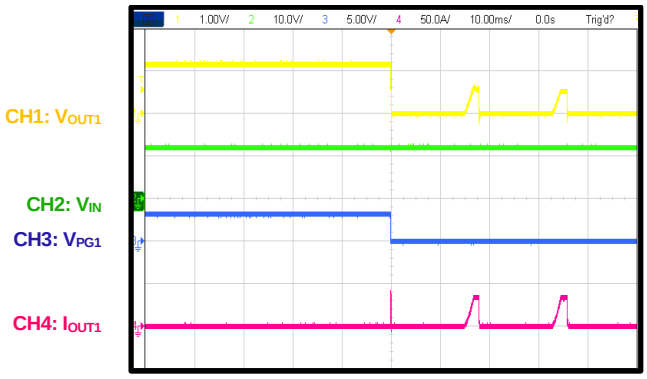
Shutdown through EN

I_{OUT1} = 25A



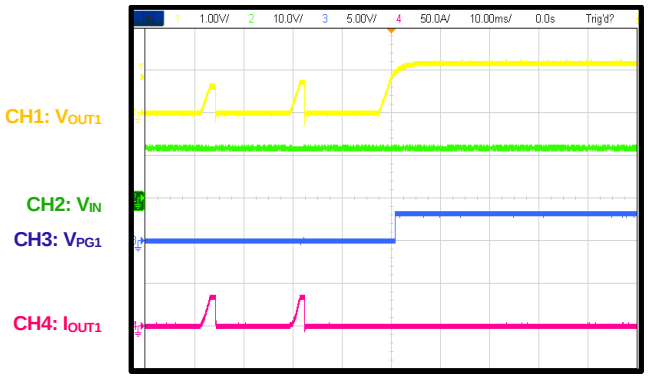
SCP Entry

I_{OUT1} = 0A



SCP Recovery

I_{OUT1} = 0A



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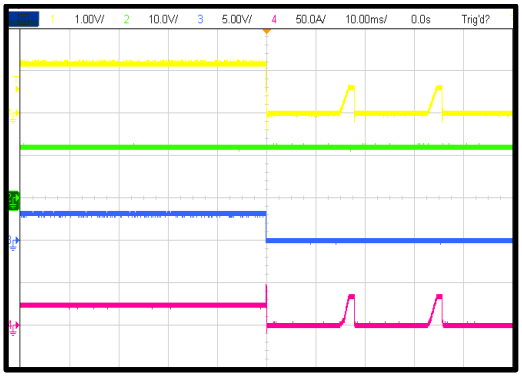
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50A, V_{IN} = 12V, V_{OUT1} = V_{OUT2} = 1.2V, C_{OUT1} = C_{OUT2} = 690µF, f_{SW1} = f_{SW2} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

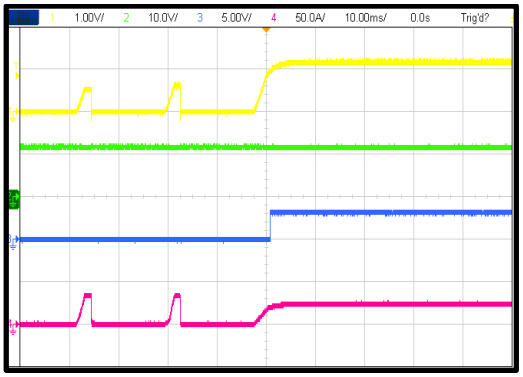
SCP Entry

I_{OUT1} = 25A

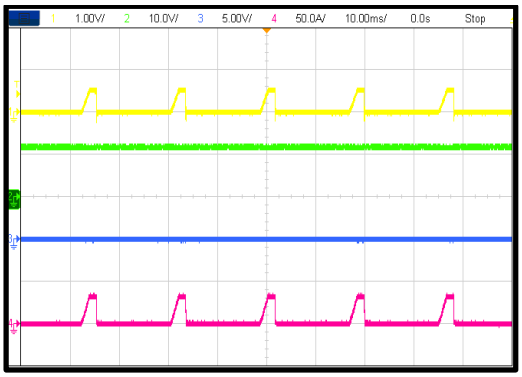


SCP Recovery

I_{OUT1} = 25A

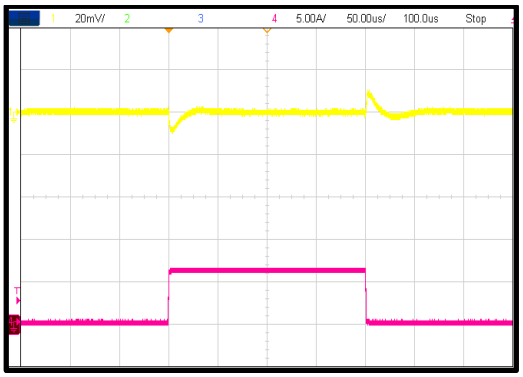


SCP Steady State



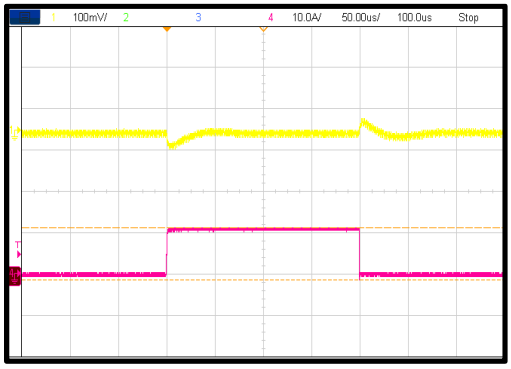
Load Transient

6.25A load step, 10A/µs, C_{OUT} = 10 x 47µF ceramic + 220µF POSCAP, C_{FF} = 33nF, low ramp



Load Transient

12.5A Load Step, 10A/µs, C_{OUT} = 10 x 47µF ceramic + 220µF POSCAP, C_{FF} = 33nF, high ramp



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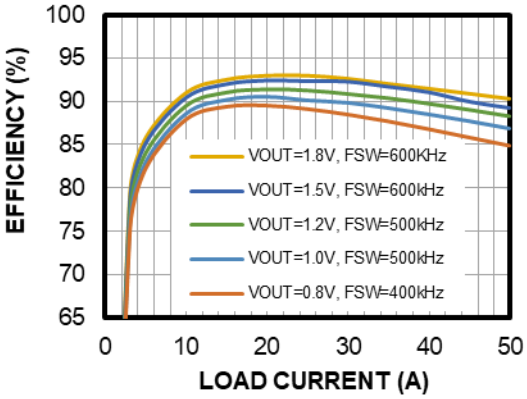
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50B, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1380µF, f_{SW} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

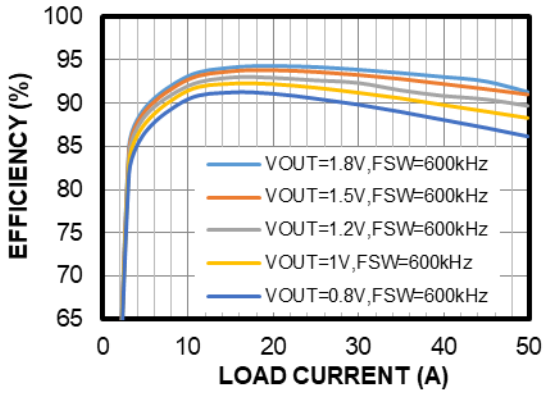
Efficiency vs. Load Current

V_{IN} = 12V,with internal 3.3V VCC

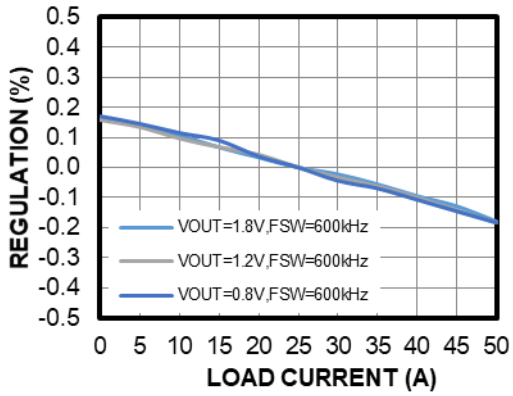


Efficiency vs. Load Current

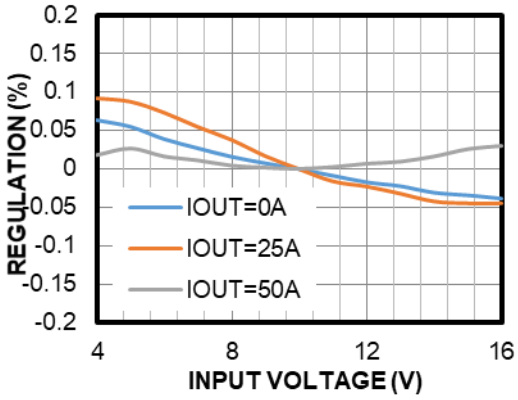
V_{IN} = 12V, with external 3.3V VCC



Load Regulation

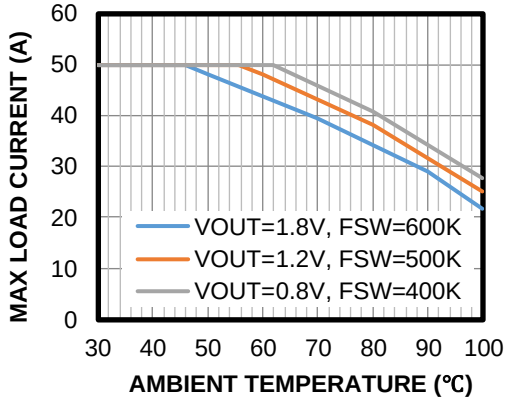


Line Regulation



Thermal Derating

V_{IN} = 12V, 1m/s with air flow



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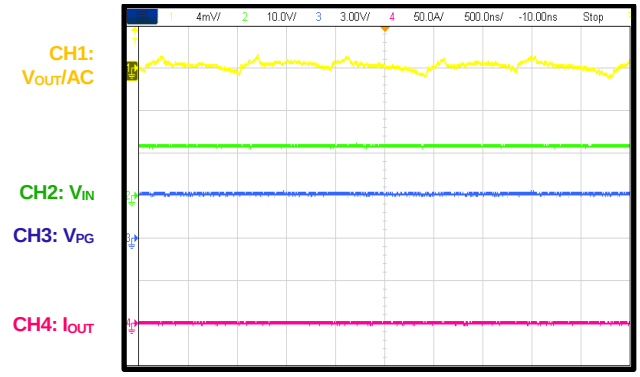
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50B, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1380µF, f_{SW} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

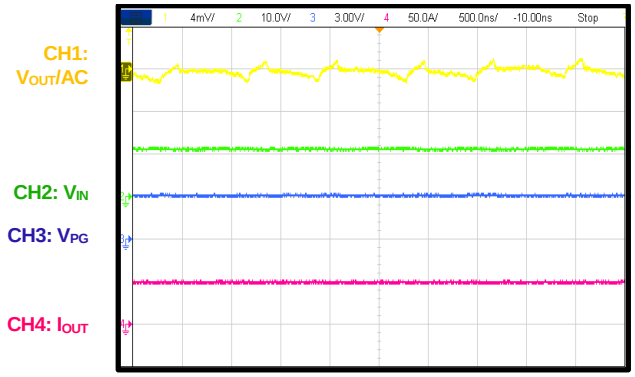
Ripple

I_{OUT} = 0A, C_{OUT} = 20 x 47µF ceramic + 2 x 220µF POSCAP



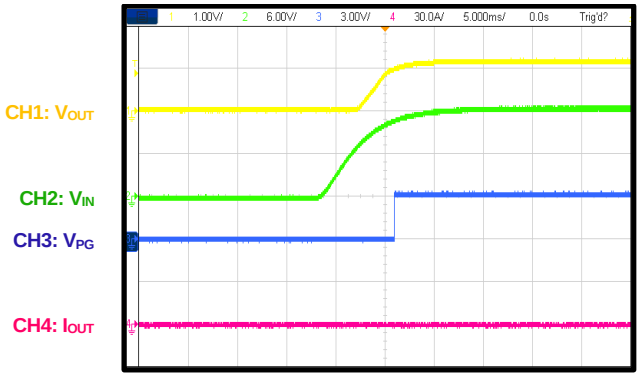
Ripple

I_{OUT} = 50A, C_{OUT} = 20 x 47µF ceramic + 2 x 220µF POSCAP



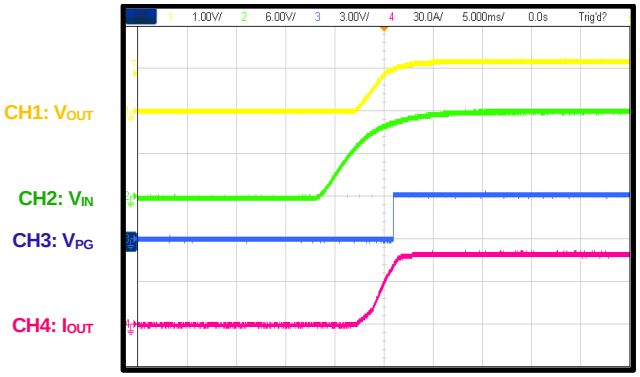
Start-Up through VIN

I_{OUT} = 0A



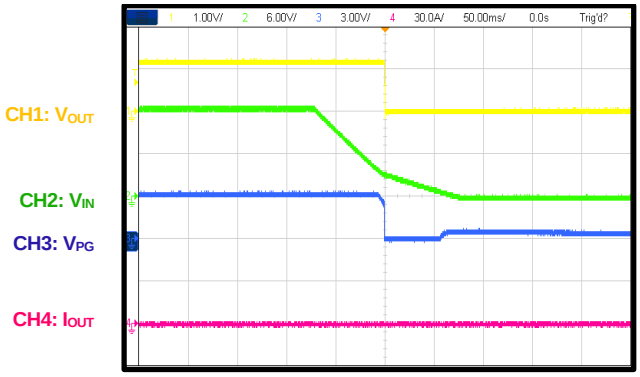
Start-Up through VIN

I_{OUT} = 50A



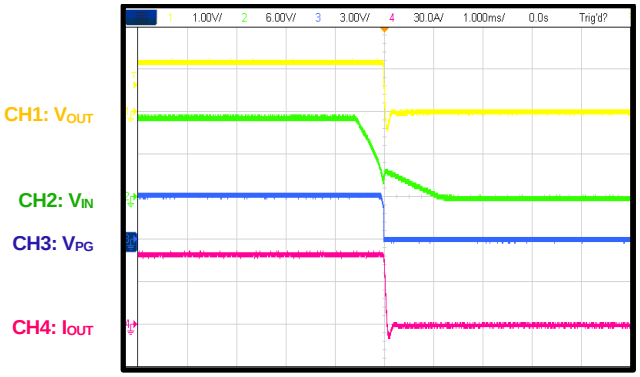
Shutdown through VIN

I_{OUT} = 0A



Shutdown through VIN

I_{OUT} = 50A



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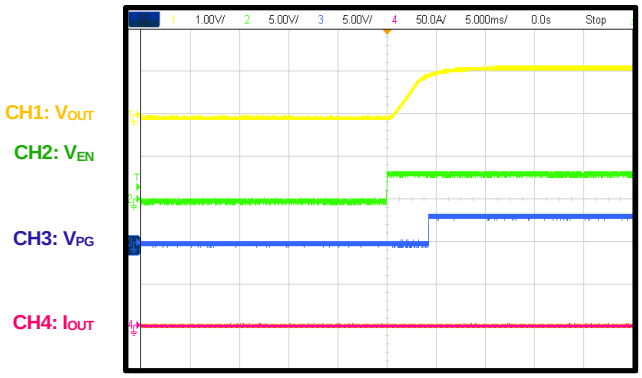
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50B, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1380µF, f_{SW} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

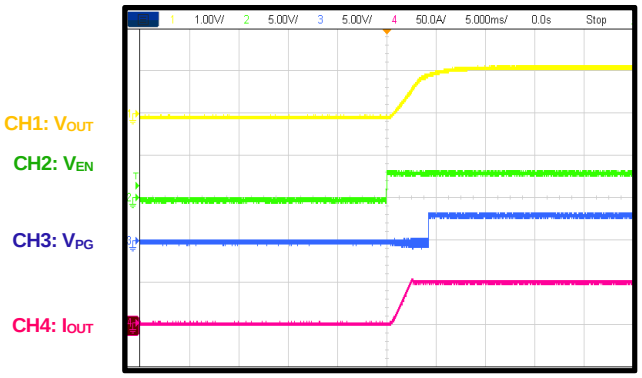
Start-Up through EN

I_{OUT} = 0A



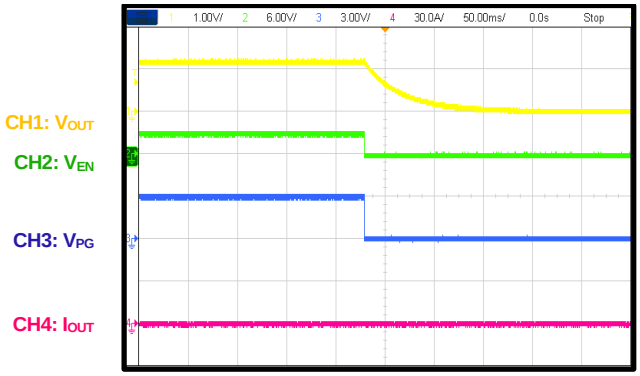
Start-Up through EN

I_{OUT} = 50A



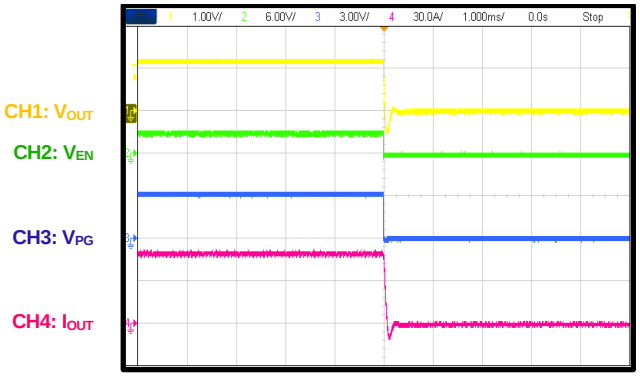
Shutdown through EN

I_{OUT} = 0A



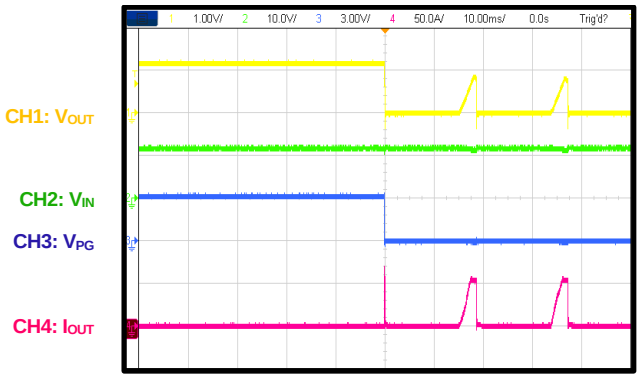
Shutdown through EN

I_{OUT} = 50A



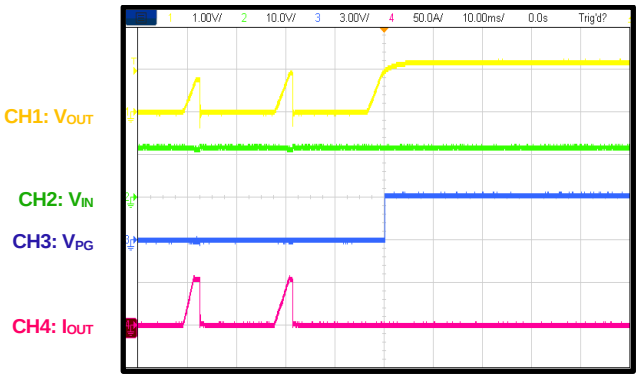
SCP Entry

I_{OUT} = 0A



SCP Recovery

I_{OUT} = 0A



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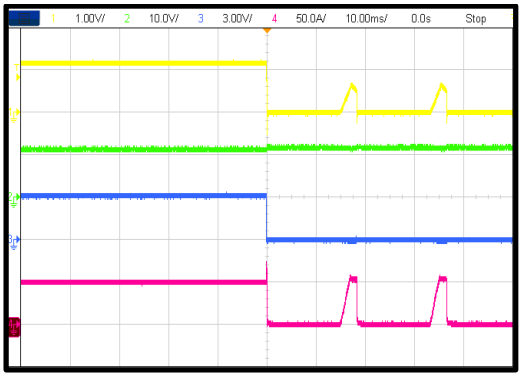
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

MPM3690-50B, V_{IN} = 12V, V_{OUT} = 1.2V, C_{OUT} = 1380µF, f_{SW} = 500kHz, FCCM, T_A = 25°C, unless otherwise noted.

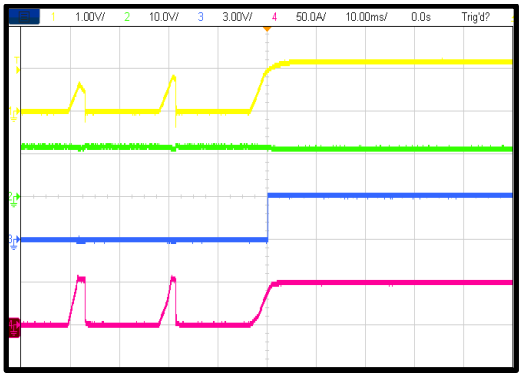
SCP Entry

I_{OUT} = 50A

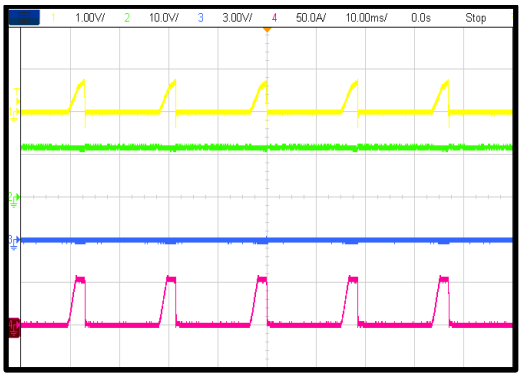


SCP Recovery

I_{OUT} = 50A

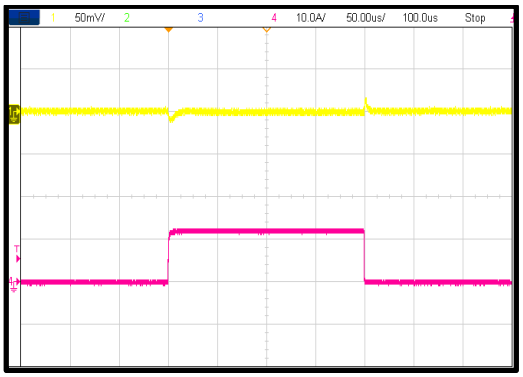


SCP Steady State



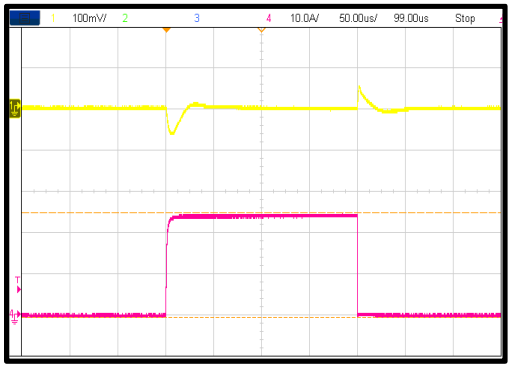
Load Transient

12.5A load step, 10A/µs, C_{OUT} = 20 x 47µF ceramic + 2 x 220µF POSCAP, C_{FF} = 33nF, low ramp



Load Transient

25A load step, 10A/µs, C_{OUT} = 20 x 47µF ceramic +2 x 220µF POSCAP, C_{FF} = 33nF, high ramp



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FUNCTIONAL BLOCK DIAGRAMS

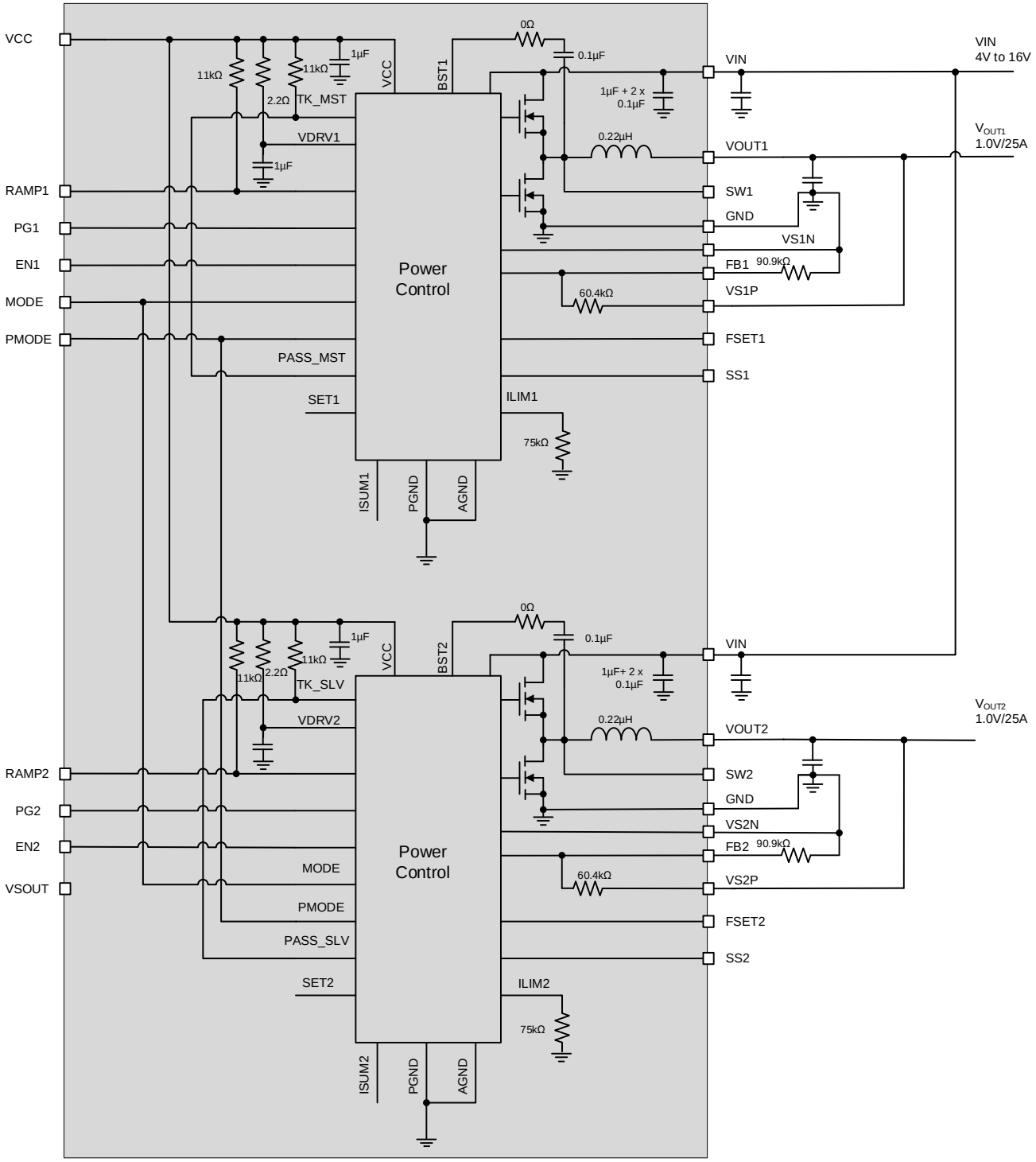

Figure 2: MPM3690-50A Functional Block Diagram

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FUNCTIONAL BLOCK DIAGRAMS *(continued)*

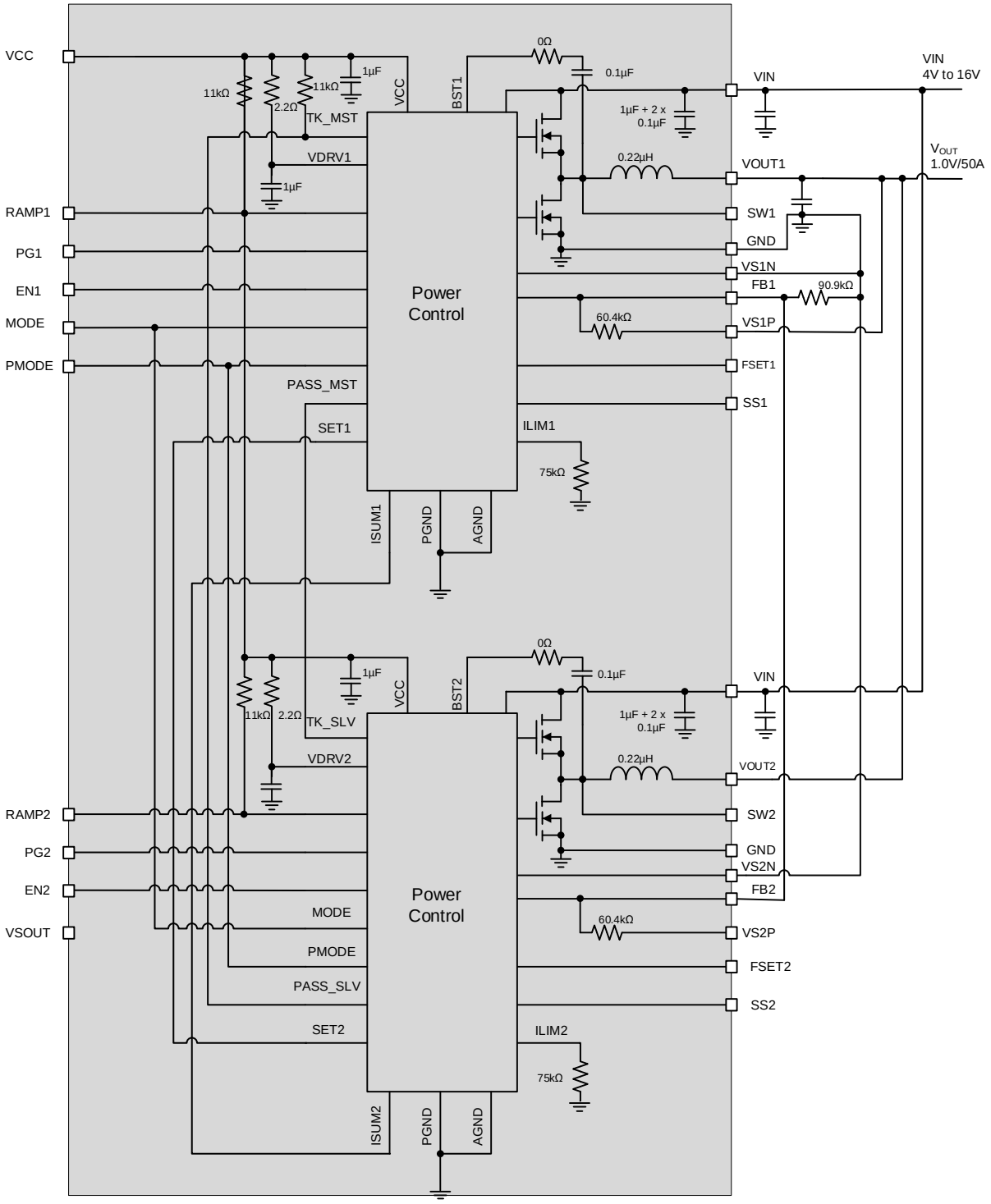

Figure 3: MPM3690-50B Functional Block Diagram

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OPERATION

Constant-On-Time (COT) Operation

The MPM3690-50 is a dual 25A or single 50A output power module that integrates two inductors and two monolithic power ICs. The MPM3690-50 utilizes constant-on-time (COT) control to provide a fast transient response.

Multi-Phase Operation

The MPM3690-50B adopts multi-phase constant-on-time (MCOT) control. MCOT control configures the two ICs for master and slave functionality. The slew rate of the supply voltage (VIN) during start-up must be greater than 2V/ms for MPM3690-50B.

MCOT Operation (Master)

The master phase performs the following functions:

- Generates the SET signals.
- Manages start-up, shutdown, and all protections.
- Monitors for any fault alerts from the slave phases through the PG pin.
- Starts the first on pulse.
- Starts the on pulse when receiving RUN and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.
- Sends the PASS/TAKE signal.

MCOT Operation (Slave)

The slave phase performs the following functions:

- Takes the SET signal from the master.
- Sends over-voltage (OV), under-voltage (UV), and over-temperature (OT) alerts to the master through the PG pin.
- Starts the on pulse when receiving RUN and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.
- Sends the PASS/TAKE signal.

MCOT control enables the MPM3690-50B to respond to a load step transient much faster than traditional current mode control schemes. When a load step occurs, the FB signal is below the internal reference; therefore, the SET signal is generated more frequently than it would be during steady state to respond to the load transient. Depending on the load transient step size and slew rate, the SET signal can be generated with a minimum 50ns interval (i.e., the next phase can be turned on as fast as 50ns after the previous phase to provide ultra-fast load transient response).

RAMP Compensation

The MPM3690-50 provides internal RAMP compensation to support various types of output capacitors. The ramp value is selected with the RAMP pin. Float the RAMP pin for large ramp compensation, or connect the RAMP pin to ground for small ramp compensation. The RAMP signal is superimposed onto the FB signal. When the superimposed RAMP + FB signal reaches the internal reference signal, the MPM3690-50 generates a new SET signal (which generates a PWM on pulse). A larger ramp value reduces system jitter, but slows the load transient response. The ramp value should be selected based on the application and design target.

Mode Selection

The MPM3690-50 only supports forced continuous conduction mode (FCCM) operation. FCCM can be enabled by setting the MODE pin to logic high.

Soft Start

The MPM3690-50A features an adjustable soft-start time (t_{SS}) for both output channels. The soft start time can be configured by connecting a soft-start capacitor (C_{SS}) between the SS pins and GND. The soft-start time can be calculated with Equation (1):

$$t_{ss}(ms) = 30 \times C_{SS}(\mu F) \quad (1)$$

Switching Frequency

The MPM3690-50A features an adjustable switching frequency (f_{SW}) for both output channels. For the MPM3690-50B, the frequency resistance (R_{FREQ}) for both channels must be the same.

The switching frequency (f_{SW}) can be configured by connecting a resistor between the FREQ pin and GND. f_{SW} can be calculated with Equation (2):

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$$f_{sw}(MHz) = \frac{24}{R_T(k\Omega)} \quad (2)$$

Output Voltage Discharge

When the MPM3690-50 is disabled through EN, it enables output voltage (V_{OUT}) discharge. Both the high-side MOSFET (HS-FET) and the low-side MOSFET (LS-FET) are latched off. A discharge MOSFET connected between SW and GND turns on to discharge V_{OUT}. The typical on resistance of this MOSFET is about 50Ω. Once the FB voltage (V_{FB}) drops below 10% of the reference voltage (V_{REF}), the discharge MOSFET turns off.

Protection MODE Selection

The MPM3690-50 includes a protection MODE selection function. If the PMODE pin is pulled high, then the MPM3690-50 enters hiccup mode when over-current protection (OCP), over-voltage protection (OVP), or over-temperature protection (OTP) is triggered. If PMODE is pulled down to GND, then the MPM3690-50 latches off when OCP, OVP, or OTP is triggered.

Inductor Valley Over-Current Protection (OCP)

The MPM3690-50 features on-die current sense. When the LS-FET is on, the switching current (inductor current) is sensed and monitored cycle by cycle. When V_{FB} drops below V_{REF}, the HS-FET can only turn on whenever there is no over-current (OC) condition detected during the LS-FET on period. This means that the inductor current is limited cycle by cycle. If an OC condition is detected for 31 consecutive cycles, OCP is triggered. If V_{OUT} drops below the under-voltage protection (UVP) threshold during an OC condition or output short-circuit condition, the part enters OCP immediately.

Once OCP is triggered, the MPM3690-50 either enters hiccup mode or latches off, depending on the PMODE pin setting. If the device latches off, cycle the power on VCC or VIN to enable the part again.

Negative Inductor Current Limit

If the LS-FET detects a negative current below -13A, the LS-FET turns off for a set time to limit the negative current.

Over-Temperature Protection (OTP)

The MPM3690-50 has over-temperature protection (OTP). The IC internally monitors the junction temperature. If the junction temperature exceeds 160°C, the converter shuts off.

After OTP is triggered, the MPM3690-50 either enters hiccup mode or latches off. If the device latches off, cycle the power on VCC or EN to enable the part again.

Feedback Circuit

Connect a resistor between FB1 and VS1N and another between FB2 and VS2N to set the output voltages for the MPM3690-50A. For the MPM3690-50B, connect a resistor between FB1 to VS1N to set the output voltage, and tie FB1 to FB2. Connect a 60.4kΩ resistor between FB1 and VS1P and another between FB2 and VS2P. Figure 4 shows the block diagram.

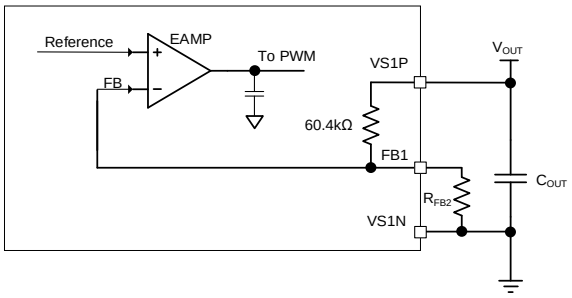

Figure 4: Feedback Circuit of MPM3690-50

V_{OUT} can be calculated with Equation (3):

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB1}}{R_{FB2}}) \quad (3)$$

Where V_{REF} is the reference voltage (0.6V), and R_{FB1} = 60.4kΩ.

Power Good (PG)

The MPM3690-50 has a power good (PG) output for each channel. The PG pin is the open drain of a MOSFET. Connect it to VCC or an external voltage source that is below 3.6V through a pull-up resistor (typically 100kΩ). After applying the input voltage (V_{IN}), the MOSFET turns on so that the PG pin is pulled to GND before soft start (SS) is ready. After V_{FB} reaches the threshold, the PG pin is pulled high after a delay.

When the converter encounters any fault (e.g. UV, OV, OT, or UVLO), the PG pin is latched low. After PG is latched low, it cannot be pulled high again until a new SS is initialized. If the input supply fails to power the MPM3690-50, PG is

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clamped low, even though it is tied to an external DC source through a pull-up resistor. Figure 5 shows the relationship between the PG voltage (V_{PG}) and the pull-up current (I_{PG}).

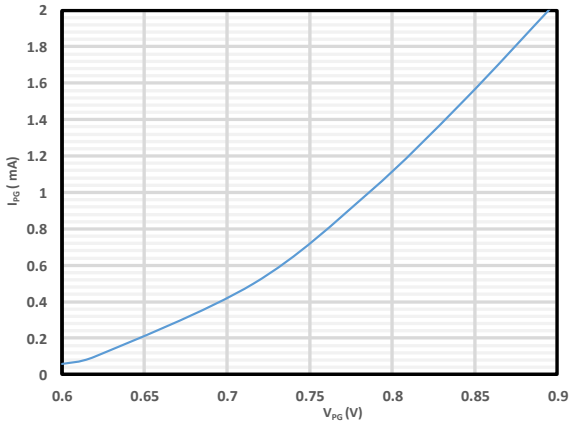

Figure 5: PG Current vs. PG Voltage

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APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for best performance. Place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable across a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance determines the converter input voltage ripple. Select a capacitor that meets any input voltage ripple requirements.

Estimate the input voltage ripple (ΔV_{IN}) with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation 7:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (7)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes majority of the output voltage. For simplification, calculate the output voltage ripple (ΔV_{OUT}) with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

When using capacitors with a larger ESR (e.g. POSCAP, OSCON), the ESR dominates the impedance at the switching frequency. The output voltage ripple is determined by the ESR. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

Low V_{IN} Applications

For low V_{IN} applications ($3V < V_{IN} < 4V$), an external VCC bias power supply is needed. The external bias VCC must be above 2.9V (the VCC UVLO rising threshold maximum value).

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PCB Layout Guidelines

VIN

Place sufficient decoupling capacitors as close as possible to the VIN and GND pins. Sufficient GND vias should be placed around the GND pad of the decoupling capacitors. Avoid placing sensitive signal traces close to the input copper plane and/or vias without sufficient ground shielding. A minimum of four 22µF/25V ceramic capacitors are recommended at the input channel to provide sufficient decoupling.

VOUTx

Each VOUTx pin should be connected together on a copper plane. Place sufficient vias near the VOUTx pads to provide a current path with minimal parasitic impedance. For the MPM3690-50B, combine all the corresponding VOUT copper planes.

GND

Connect all GND pins of the module on a copper plane. Place sufficient vias close to the GND pins to provide a current return path with minimal thermal resistance and parasitic impedance.

VSxP and VSxN

For the MPM3690-50A, route each pair of VSxP/N pins as differential signals. For the MPM3690-50B, connect FB1 to FB2, then connect all of the VSxN pins. Avoid routing VSxP/N traces close to the input plane and high-speed signals.

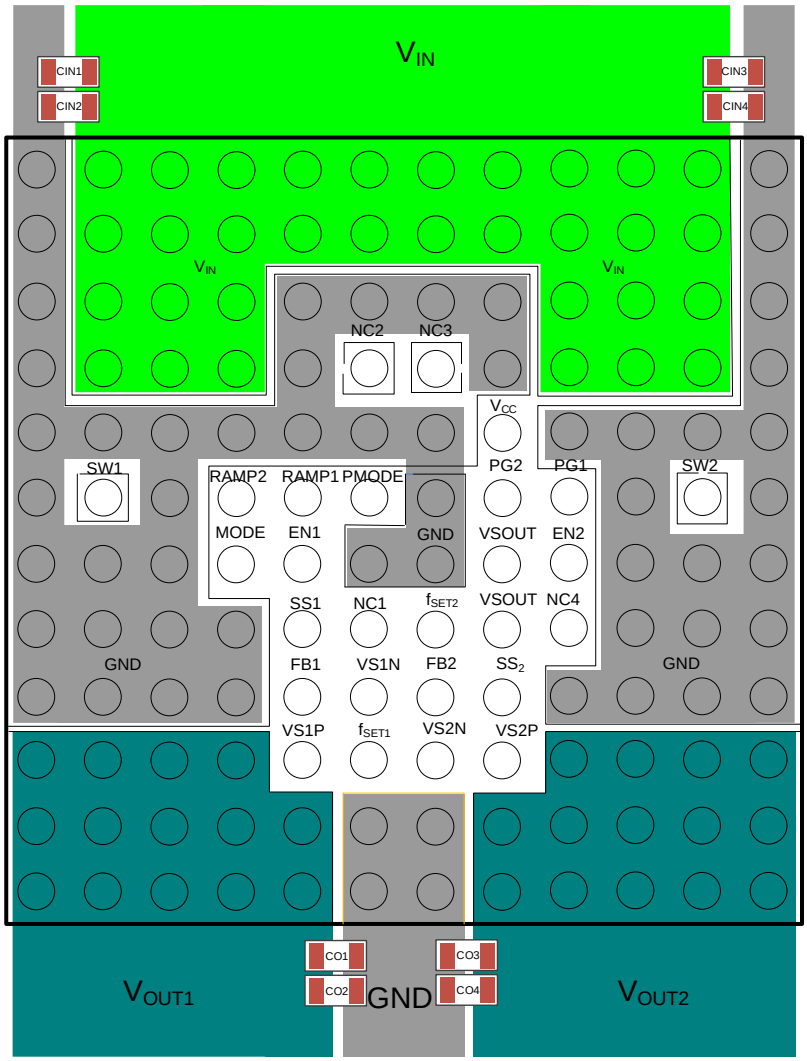

Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

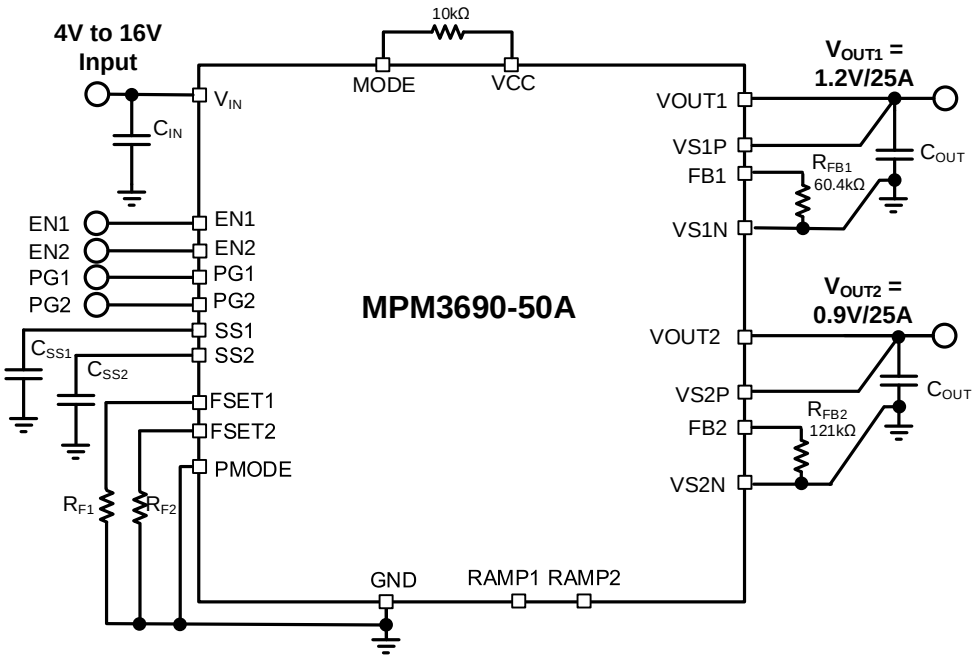

Figure 7: Typical Application Circuit (Dual-Output Operation, 1.2V and 0.9V at 25A with Remote Sense for Both Outputs)

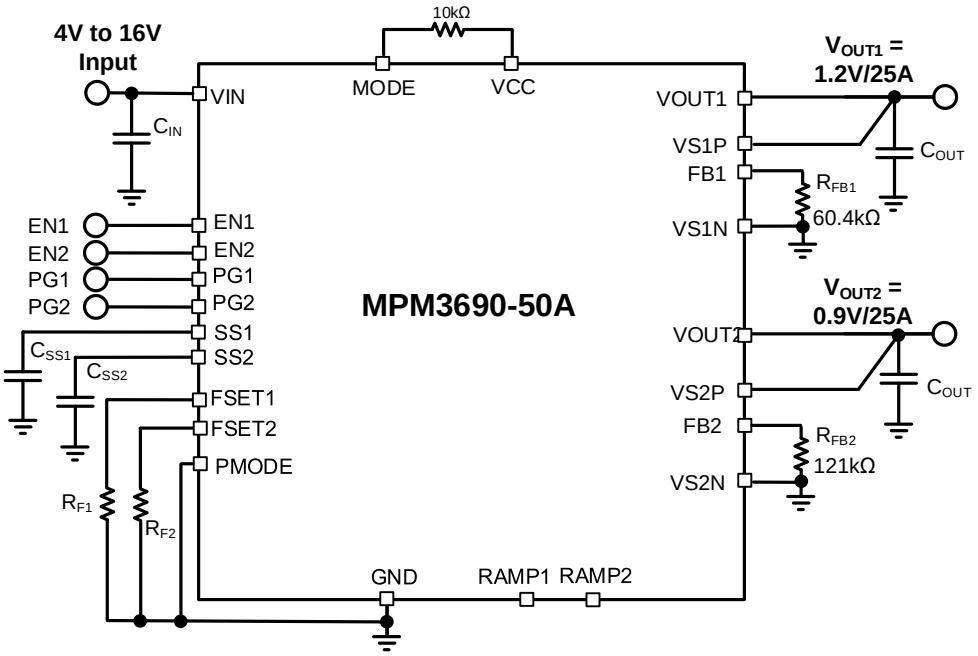

Figure 8: Typical Application Circuit (Dual-Output Operation, 1.2V and 0.9V at 25A with Remote Sense Disabled)

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TYPICAL APPLICATION CIRCUITS *(continued)*

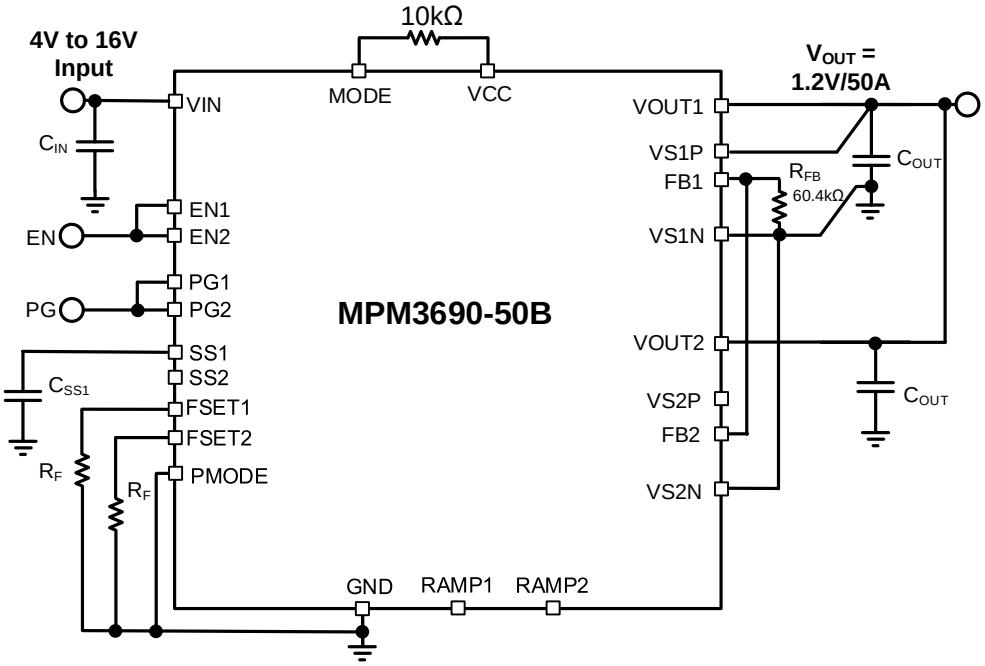

Figure 9: Typical Application Circuit (Interleaved Operation, 1.2V at 50A with Remote Sense)

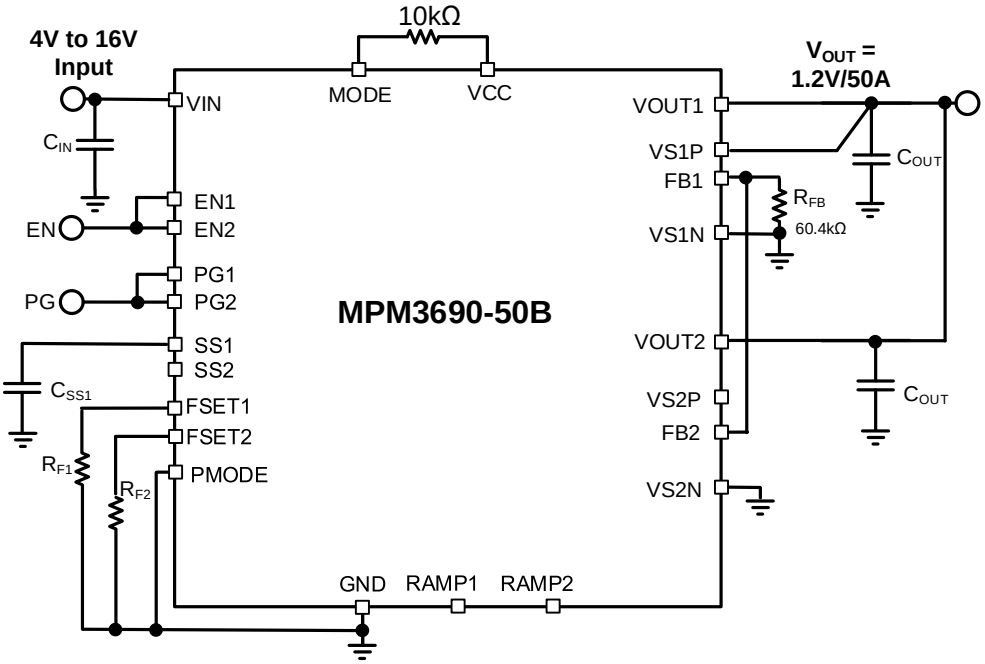

Figure 10: Typical Application Circuit (Interleaved Operation, 1.2V at 50A without Remote Sense)

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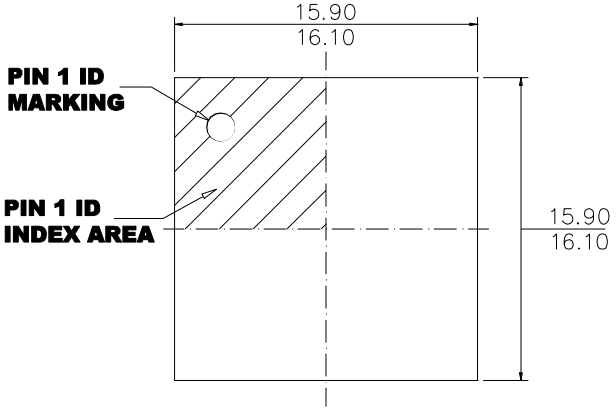
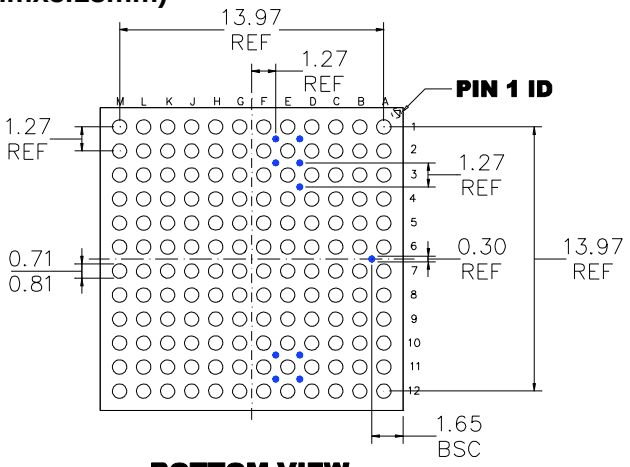
PACKAGE INFORMATION

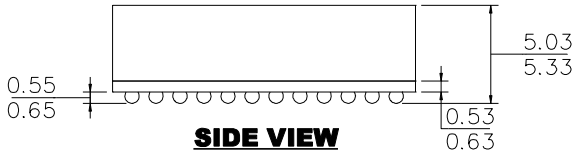
BGA (16mmx16mmx5.18mm)



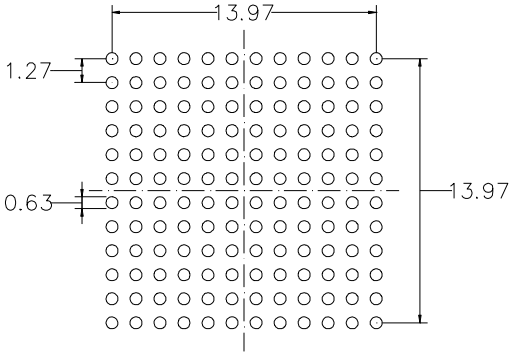
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE SOLID BLUE CIRCLES REPRESENT TEST PADS WITHOUT SOLDER BALL.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-275A.
5) DRAWING IS NOT TO SCALE.

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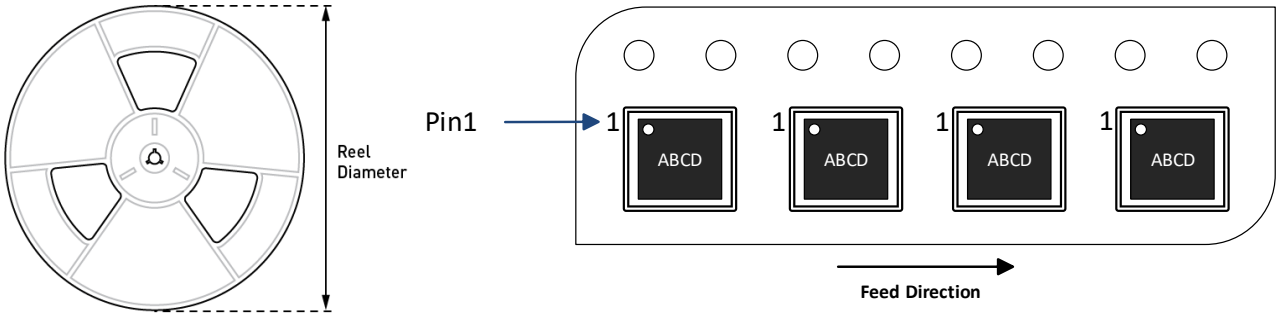
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tray	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3690GBF-50A	BGA (16mmx16mmx5.18mm)	N/A	90	N/A	N/A	N/A	N/A
MPM3690GBF-50B							

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/24/2021	Initial Release	-

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