MP4835A

32-Channel, High-Voltage Analog Switch with Output Bleed Resistors and 5.0V Bias

DESCRIPTION

The MP4835A is a 32-channel, high-voltage, single-pole/single-throw (SPST) analog switch with integrated output bleed resistors, designed for medical ultrasound imaging applications. It is designed to multiplex the transmission and can receive voltages to and from multiple piezoelectric transducers (PZTs).

The output switches are controlled by a 32-bit serial shift register, followed by a 32-bit data latch. A data out (DOUT) pin is provided to allow for multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high signal in the data latch turns the corresponding analog switch on, whereas a logic low signal turns it off.

The MP4835A does not require any high-voltage supplies. Only two low-voltage supplies are required (3.3V and 5.0V). The analog switch can block or pass analog voltages up to ±100V with peak currents of up to ±1.8A.

The MP4835A is available in a QFN-72 (10mmx10mm) package.

FEATURES

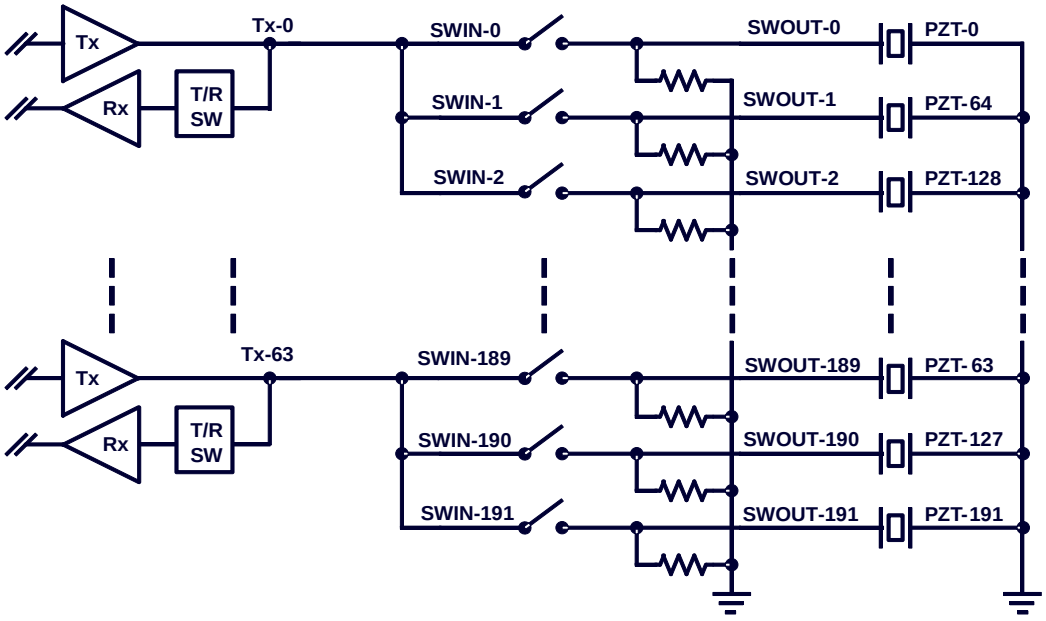
- No High-Voltage Supplies Required
- 32 Channels
- Up to ±100V Analog Signals
- 14Ω Typical Switch Resistance
- ±1.8A Typical Switch Peak Current
- Off-Isolation of -66dB at 5.0MHz
- Integrated Output Bleed Resistor
- 60MHz Clock Frequency
- 5.0V Bias Supply
- Available in a QFN-72 (10mmx10mm) Package

APPLICATIONS

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT)

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4835AGRD	QFN-72 (10mmx10mm)	*See Below*	3

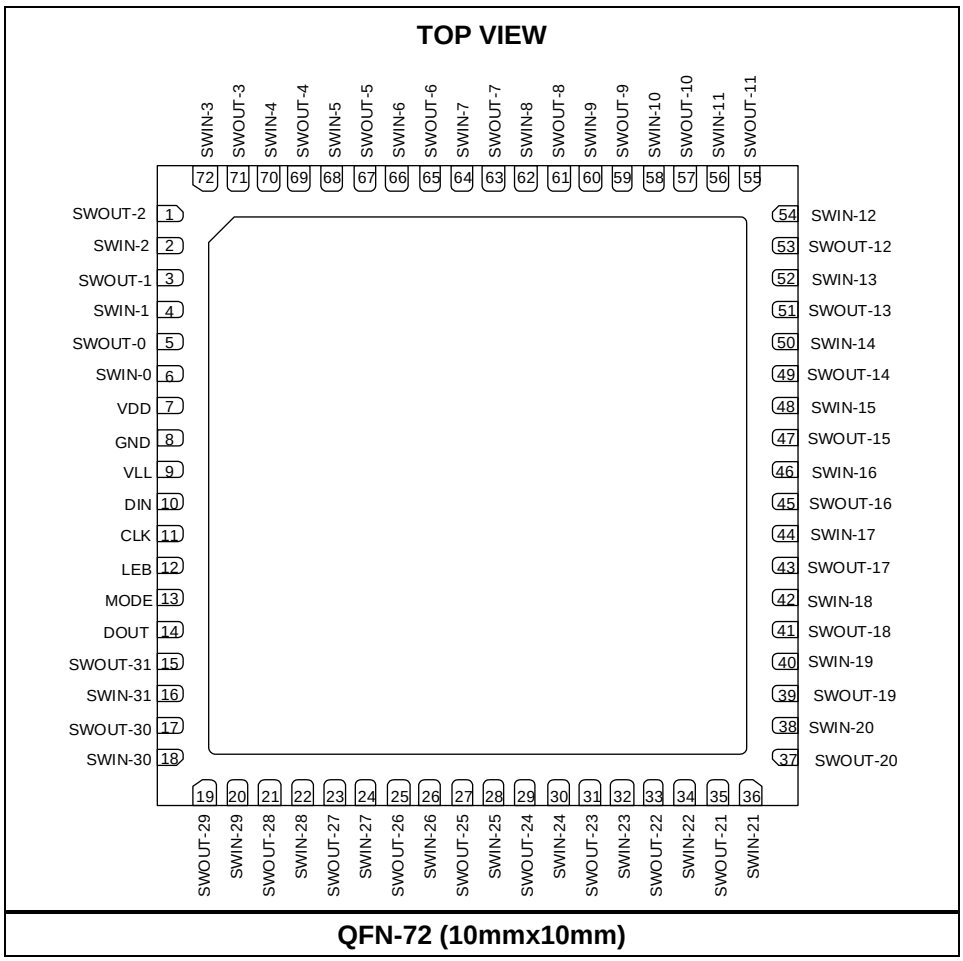
* For Tray, add suffix –T (e.g. MP4835AGRD–T).

TOP MARKING

MPSYYWW
MP4835A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4835A: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



QFN-72 (10mmx10mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SWOUT-2	**Analog switch output 2.** Connect this pin to the piezoelectric transducer.
2	SWIN-2	**Analog switch input 2.** Connect this pin to the high-voltage pulser/transmitter.
3	SWOUT-1	**Analog switch output 1.** Connect this pin to the piezoelectric transducer.
4	SWIN-1	**Analog switch input 1.** Connect this pin to the high-voltage pulser/transmitter.
5	SWOUT-0	**Analog switch output 0.** Connect this pin to the piezoelectric transducer.
6	SWIN-0	**Analog switch input 0.** Connect this pin to the high-voltage pulser/transmitter.
7	VDD	**Translators supply voltage.** 4.5V to 5.5V operating range.
8	GND	**Device ground.** Connect this pin to center DAP externally.
9	VLL	**Logic supply voltage.** This pin has a 2.7V to 5.5V operating range.
10	DIN	**Logic input.** When MODE is logic low, DIN is the data input for the 32-bit serial shift register. When MODE is logic high, DIN going logic low turns all 32 output switches off, while DIN going logic high turns all 32 output switches on.
11	CLK	**Logic input.** Clock input for the 32-bit serial shift register. Data is loaded in at the rising edge of the clock.
12	LEB	**Logic input.** Latch enable bar for the 32-bit latch. A logic low signal initiates a data transfer from the shift registers to the latches. A logic high signal means the data is held in the latches. See the Logic Truth Table on page 9 for more details.
13	MODE	**Logic input.** Sets the function of DIN. When MODE is logic low, DIN is the data input for the 32-bit serial shift register. When MODE is logic high, DIN is a single-pin control for all 32 output switches.
14	DOUT	**Logic output.** Data output for the 32-bit serial shift register.
15	SWOUT-31	**Analog switch output 31.** Connect this pin to the piezoelectric transducer.
16	SWIN-31	**Analog switch input 31.** Connect this pin to the high-voltage pulser/transmitter.
17	SWOUT-30	**Analog switch output 30.** Connect this pin to the piezoelectric transducer.
18	SWIN-30	**Analog switch input 30.** Connect this pin to the high-voltage pulser/transmitter.
19	SWOUT-29	**Analog switch output 29.** Connect this pin to the piezoelectric transducer.
20	SWIN-29	**Analog switch input 29.** Connect this pin to the high-voltage pulser/transmitter.
21	SWOUT-28	**Analog switch output 28.** Connect this pin to the piezoelectric transducer.
22	SWIN-28	**Analog switch input 28.** Connect this pin to the high-voltage pulser/transmitter.
23	SWOUT-27	**Analog switch output 27.** Connect this pin to the piezoelectric transducer.
24	SWIN-27	**Analog switch input 27.** Connect this pin to the high-voltage pulser/transmitter.
25	SWOUT-26	**Analog switch output 26.** Connect this pin to the piezoelectric transducer.
26	SWIN-26	**Analog switch input 26.** Connect this pin to the high-voltage pulser/transmitter.
27	SWOUT-25	**Analog switch output 25.** Connect this pin to the piezoelectric transducer.
28	SWIN-25	**Analog switch input 25.** Connect this pin to the high-voltage pulser/transmitter.
29	SWOUT-24	**Analog switch output 24.** Connect this pin to the piezoelectric transducer.
30	SWIN-24	**Analog switch input 24.** Connect this pin to the high-voltage pulser/transmitter.
31	SWOUT-23	**Analog switch output 23.** Connect this pin to the piezoelectric transducer.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
32	SWIN-23	**Analog switch input 23.** Connect this pin to the high-voltage pulser/transmitter.
33	SWOUT-22	**Analog switch output 22.** Connect this pin to the piezoelectric transducer.
34	SWIN-22	**Analog switch input 22.** Connect this pin to the high-voltage pulser/transmitter.
35	SWOUT-21	**Analog switch output 21.** Connect this pin to the piezoelectric transducer.
36	SWIN-21	**Analog switch input 21.** Connect this pin to the high-voltage pulser/transmitter.
37	SWOUT-20	**Analog switch output 20.** Connect this pin to the piezoelectric transducer.
38	SWIN-20	**Analog switch input 20.** Connect this pin to the high-voltage pulser/transmitter.
39	SWOUT-19	**Analog switch output 19.** Connect this pin to the piezoelectric transducer.
40	SWIN-19	**Analog switch input 19.** Connect this pin to the high-voltage pulser/transmitter.
41	SWOUT-18	**Analog switch output 18.** Connect this pin to the piezoelectric transducer.
42	SWIN-18	**Analog switch input 18.** Connect this pin to the high-voltage pulser/transmitter.
43	SWOUT-17	**Analog switch output 17.** Connect this pin to the piezoelectric transducer.
44	SWIN-17	**Analog switch input 17.** Connect this pin to the high-voltage pulser/transmitter.
45	SWOUT-16	**Analog switch output 16.** Connect this pin to the piezoelectric transducer.
46	SWIN-16	**Analog switch input 16.** Connect this pin to the high-voltage pulser/transmitter.
47	SWOUT-15	**Analog switch output 15.** Connect this pin to the piezoelectric transducer.
48	SWIN-15	**Analog switch input 15.** Connect this pin to the high-voltage pulser/transmitter.
49	SWOUT-14	**Analog switch output 14.** Connect this pin to the piezoelectric transducer.
50	SWIN-14	**Analog switch input 14.** Connect this pin to the high-voltage pulser/transmitter.
51	SWOUT-13	**Analog switch output 13.** Connect this pin to the piezoelectric transducer.
52	SWIN-13	**Analog switch input 13.** Connect this pin to the high-voltage pulser/transmitter.
53	SWOUT-12	**Analog switch output 12.** Connect this pin to the piezoelectric transducer.
54	SWIN-12	**Analog switch input 12.** Connect this pin to the high-voltage pulser/transmitter.
55	SWOUT-11	**Analog switch output 11.** Connect this pin to the piezoelectric transducer.
56	SWIN-11	**Analog switch input 11.** Connect this pin to the high-voltage pulser/transmitter.
57	SWOUT-10	**Analog switch output 10.** Connect this pin to the piezoelectric transducer.
58	SWIN-10	**Analog switch input 10.** Connect this pin to the high-voltage pulser/transmitter.
59	SWOUT-09	**Analog switch output 09.** Connect this pin to the piezoelectric transducer.
60	SWIN-09	**Analog switch input 09.** Connect this pin to the high-voltage pulser/transmitter.
61	SWOUT-08	**Analog switch output 08.** Connect this pin to the piezoelectric transducer.
62	SWIN-08	**Analog switch input 08.** Connect this pin to the high-voltage pulser/transmitter.
63	SWOUT-07	**Analog switch output 07.** Connect this pin to the piezoelectric transducer.
64	SWIN-07	**Analog switch input 07.** Connect this pin to the high-voltage pulser/transmitter.
65	SWOUT-06	**Analog switch output 06.** Connect this pin to the piezoelectric transducer.
66	SWIN-06	**Analog switch input 06.** Connect this pin to the high-voltage pulser/transmitter.
67	SWOUT-05	**Analog switch output 05.** Connect this pin to the piezoelectric transducer.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
68	SWIN-05	**Analog switch input 05.** Connect this pin to the high-voltage pulser/transmitter.
69	SWOUT-04	**Analog switch output 04.** Connect this pin to the piezoelectric transducer.
70	SWIN-04	**Analog switch input 04.** Connect this pin to the high-voltage pulser/transmitter.
71	SWOUT-03	**Analog switch output 03.** Connect this pin to the piezoelectric transducer.
72	SWIN-03	**Analog switch input 03.** Connect this pin to the high-voltage pulser/transmitter.
Center DAP		**Substrate.** Connect to GND externally.

ABSOLUTE MAXIMUM RATINGS (1)

Logic supply voltage (V_{LL}) ..... -0.5V to +6.6V
Translator supply voltage (V_{DD}) ... -0.5V to +6.6V
Analog signal range (V_{SIG}) ..... 0V to ±105V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation ..... T_A = 25°C (2)
..... 6.7W
Storage temperature ..... -55°C to +150°C

ESD Ratings

Human body model (HBM): JEDEC standard
SWOUTx..... Class 1B
SWINx..... Class 1C
Other pins..... Class 2

Charged device model (CDM): JEDEC standard

All pins..... Class 3

Recommended Operating Conditions (3)

Logic supply voltage (V_{LL}) ..... 2.7V to 5.5V
Translator supply voltage (V_{DD}) ..... 4.5V to 5.5V
Analog signal range (V_{SIG}) ..... 0 to ±100V
Junction temperature (T_J) ..... -25°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-72 (10mmx10mm) ..... 15 ..... 3 .... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0, V_{LL} = 5.0V, T_A = 25°C, unless otherwise noted. (5)

Parameter	Sym	Conditions	T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Analog signal range	V_{SIG}	Applied to any SWIN pin	0	±100	0		±100	0	±100	V
On resistance	R_{ON}	I_{SIG} = ±5.0mA, SW_{OUT} = 0V (see test circuit 1 on page 10)		20		14	24		30	Ω
		I_{SIG} = ±200mA, SW_{OUT} = 0V (see Figure 1 on page 10)		16		14	19		24	
Small signal on resistance matching	ΔR_{ON}	I_{SIG} = ±5.0mA, SW_{OUT} = 0V				5.0				%
Large signal on resistance (6)	R_{ONL}	I_{SIG} = ±1.0A, t_{PW} ≤ 500ns, duty cycle ≤ 1.0%, SW_{OUT} = 0V (see Figure 2 on page 10)				13				Ω
Switch output peak current	I_{SWPK}	t_{PW} ≤ 100ns, duty cycle ≤ 1.0%				±1.8				A
Output bleed resistor	R_{BLEED}	I_{SIG} = ±50µA			20	30	50			kΩ
Switch off DC offset	V_{DC-OFF}	No load, no V_{SIG} (see Figure 3 on page 10)		±50			±50		±50	mV
Switch on DC offset	V_{DC-ON}	No load, no V_{SIG} (see Figure 3 on page 10)		±50			±50		±50	mV
V_{LL} quiescent current	I_{LLQ}	All logic inputs are static		50			50		50	µA
V_{DD} quiescent current	I_{DDQ}	All switches on or off, SW_{IN} = SW_{OUT} = GND		1			1		1	µA
V_{LL} average dynamic current	I_{LL}	f_{CLK} = 30MHz, D_{IN} = 15MHz				4	8			mA
		f_{CLK} = 60MHz, D_{IN} = 30MHz				8.7				
V_{DD} average dynamic current	I_{DD}	All output switches turn on and off at 50kHz				3.2	4.5			mA
Input voltage logic low	V_{IL}		0	0.2V_{LL}	0		0.2V_{LL}	0	0.2V_{LL}	V
Input voltage logic high	V_{IH}		0.8V_{LL}	V_{LL}	0.8V_{LL}		V_{LL}	0.8V_{LL}	V_{LL}	V
Input current logic low	I_{IL}		-1.0		-1.0			-1.0		µA
Input current logic high	I_{IH}			1.0			1.0		1.0	µA
Data out logic low voltage	V_{OL}	I_{SINK} = 10mA		1.0			1.0		1.0	V
Data out logic high voltage	V_{OH}	I_{SOURCE} = 10mA	V_{LL}-1.0		V_{LL}-1.0			V_{LL}-1.0		V
Logic input capacitance (6)	C_{IN}			10			10		10	pF

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AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0, V_{LL} = 5.0V, T_A = 25°C, unless otherwise noted. (5)

Parameter	Sym	Conditions		T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
Clock frequency (6)	f_{CLK}	50% duty cycle	V_{LL} = 3.3V	0	30	0		30	0	30	MHz
			V_{LL} = 5.0V	0	60	0		60	0	60	
Clock rise time (6)	t_r				50			50		50	ns
Clock fall time (6)	t_f				50			50		50	ns
Set-up time from data to rising edge of clock (6)	t_{SU}			3.0		3.0			3.0		ns
Hold time from rising edge of clock to data (6)	t_H			3.0		3.0			3.0		ns
Set-up time before LE bar rises (6)	t_{SD}			6.0		6.0			6.0		ns
LE\ pulse width (6)	t_{WLE_BAR}			6.0		6.0			6.0		ns
Data out propagation delay time from rising edge of clock (6)	t_{DOHL}, t_{DOLH}	20pF on DOUT to GND		8.5	13	8.5	11	13	8.5	13	ns
Output switch turn on time	t_{ON}	SW_{IN} = 2.0V, SW_{OUT} = 50Ω to GND (see Figure 4 on page 11)			2.0			2.0		2.0	µs
Output switch turn off time	t_{OFF}				2.0			2.0		2.0	µs
Analog signal slew rate (6)	dV/dt				20			20		20	V/ns
Off-isolation (6)	K_O	Freq = 5.0MHz, R_{LOAD} = 50Ω (see Figure 5 on page 11)					-66				dB
Switch crosstalk (6)	K_{CR}	Freq = 5.0MHz, R_{LOAD} = 50Ω (see Figure 6 on page 11)					-60				dB
Switch off capacitance (6)	$C_{SWIN-OFF}$						10				pF
Switch on capacitance (6)	C_{SW-ON}						13				pF
Positive output voltage spike (6)	$+V_{SPK}$	SW_{IN} = 1kΩ to GND, SW_{OUT} = 50Ω to GND (see Figure 7 on page 12)					78				mV
Negative output voltage spike (6)	$-V_{SPK}$						-5				mV
Output charge injection (6)	Q_{INJ}	C_{LOAD} = 1000pF (see Figure 8 on page 12)					18				pC

Notes:

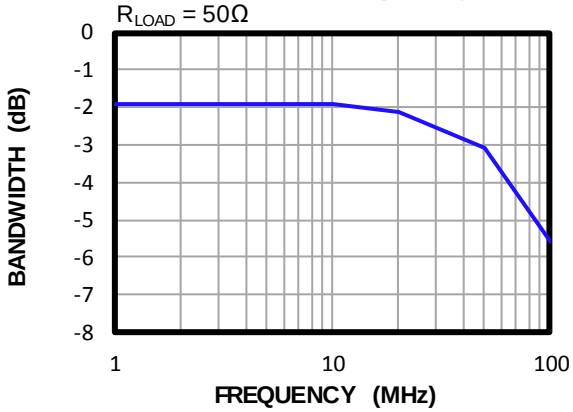
5) Production testing is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.
6) Parameters are not tested in mass production. Guaranteed by design or bench characterization.

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TYPICAL PERFORMANCE CHARACTERISTICS

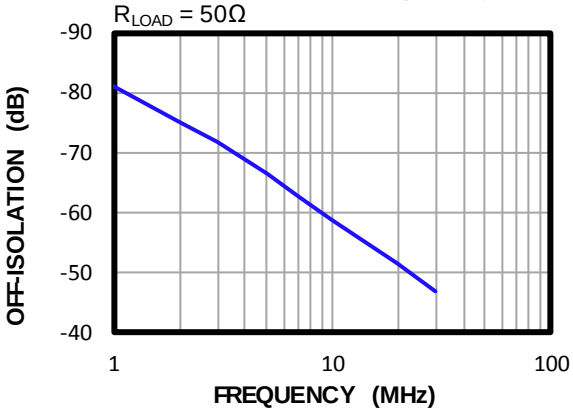
Bandwidth vs. Frequency

R_{LOAD} = 50Ω



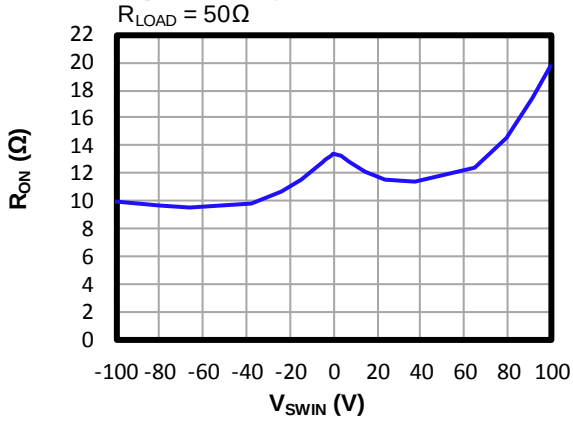
Off-Isolation vs. Frequency

R_{LOAD} = 50Ω



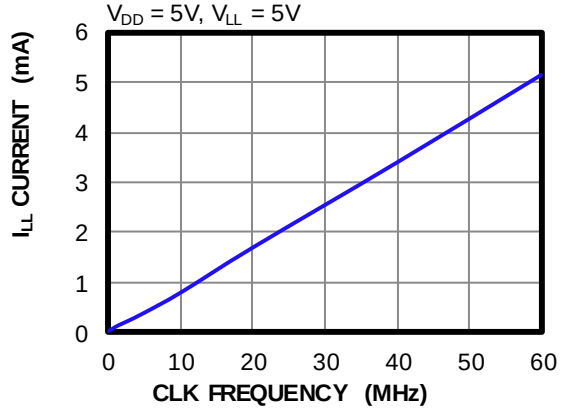
Switch Resistance vs. Switch Input Voltage

R_{LOAD} = 50Ω



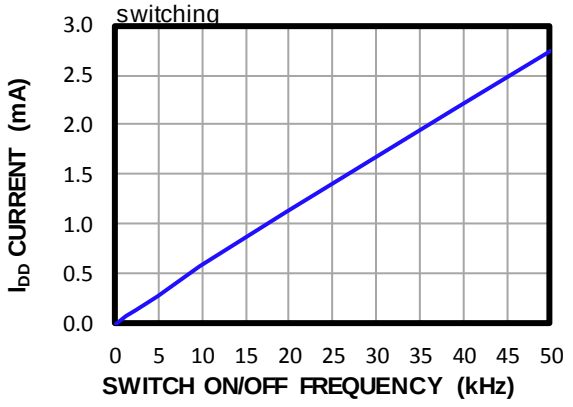
I_{LL} Current vs. CLK Frequency

V_{DD} = 5V, V_{LL} = 5V



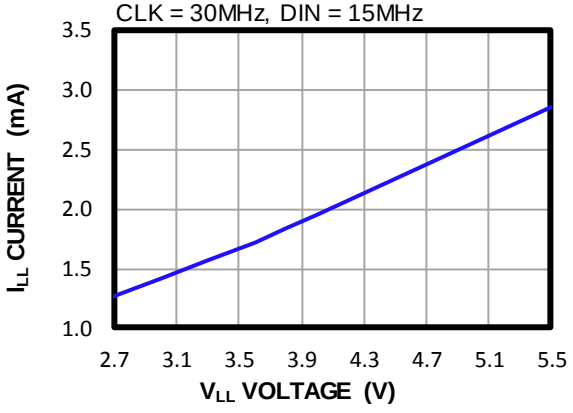
I_{DD} Current vs. Switch On/Off Frequency

V_{DD} = 5V, V_{LL} = 5V, all 32 channels switching



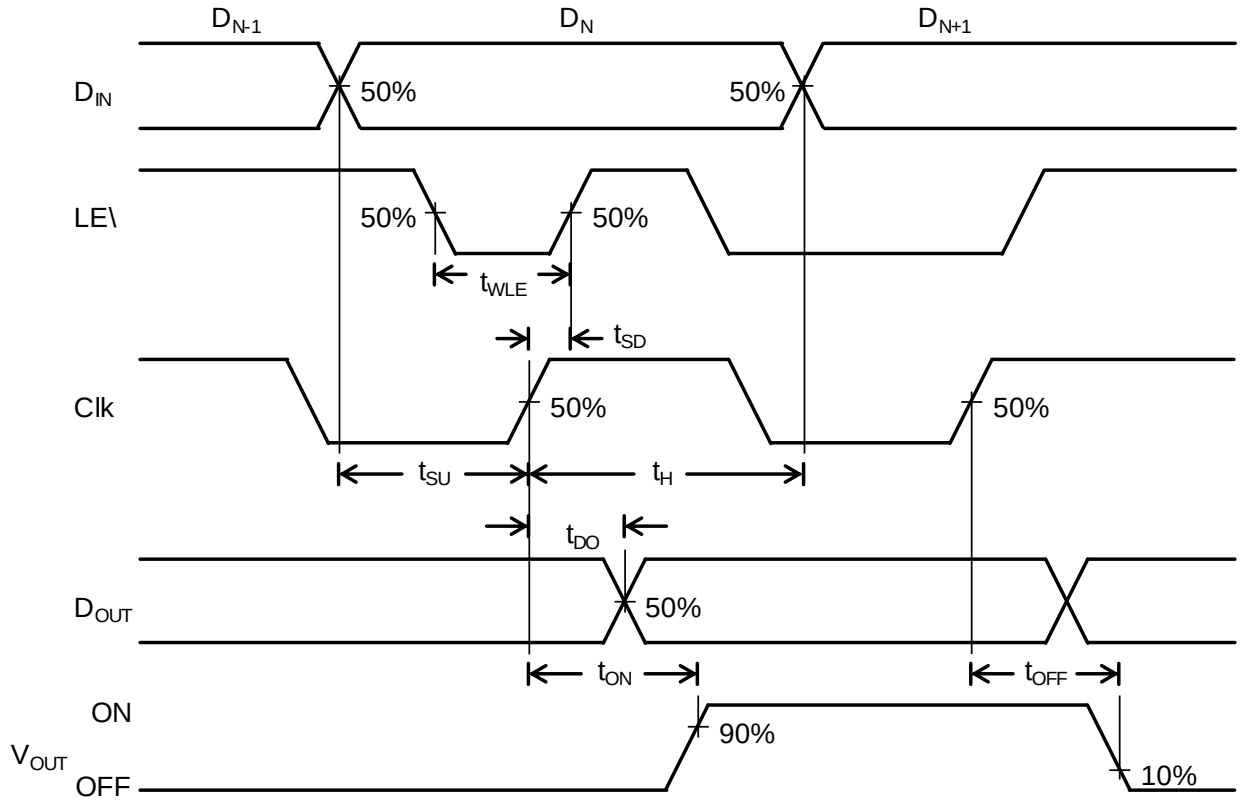
I_{LL} Current vs. V_{LL} Voltage

CLK = 30MHz, DIN = 15MHz



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TIMING DIAGRAM



LOGIC TRUTH TABLE (7)

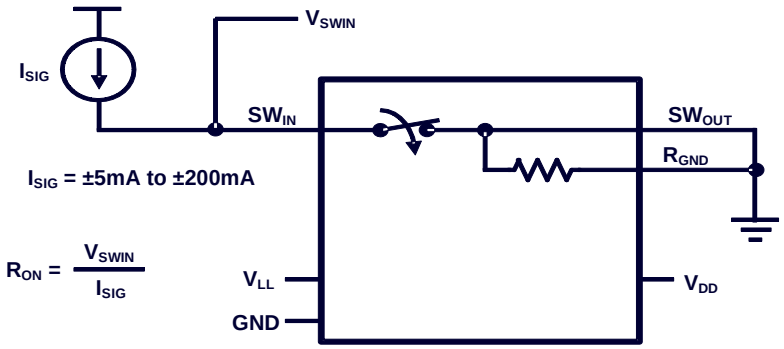
Logic Input								Switch State				
D0	**D1**	**D2**	**– – –**	**D31**	**Din**	**LE bar**	**Mode**	**SW0**	**SW1**	**SW2**	**– – –**	**SW31**
L	-	-		-	x	L	L	Off	-	-		-
H	-	-		-	x	L	L	On	-	-		-
-	L	-		-	x	L	L	-	Off	-		-
-	H	-		-	x	L	L	-	On	-		-
-	-	L		-	x	L	L	-	-	Off		-
-	-	H		-	x	L	L	-	-	On		-
⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮
-	-	-		L	x	L	L	-	-	-		Off
-	-	-		H	x	L	L	-	-	-		On
x	x	x		x	x	H	L	Hold previous state				
x	x	x		x	L	x	H	All switches off				
x	x	x		x	H	x	H	All switches on				

Note:

7) "L" denotes logic level low, "H" denotes logic level high, and "x" denotes not applicable.

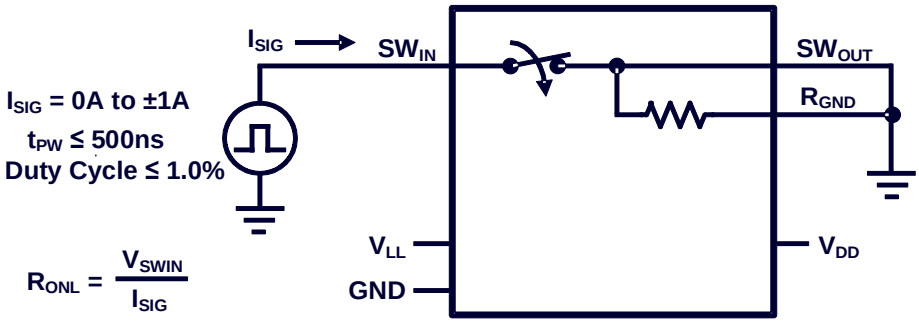
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TEST CIRCUITS



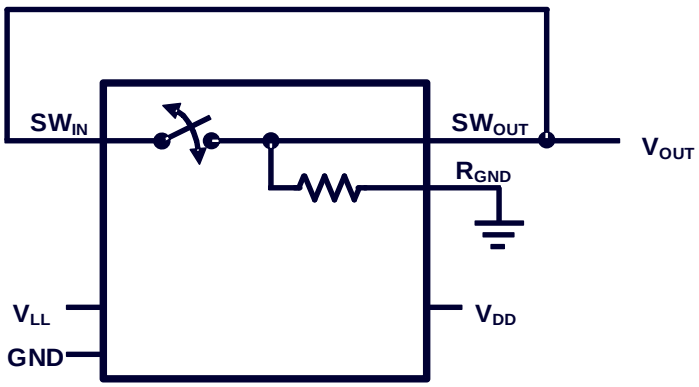
R_{ON}

Figure 1: Test Circuit 1



Large Signal R_{ON}

Figure 2: Test Circuit 2

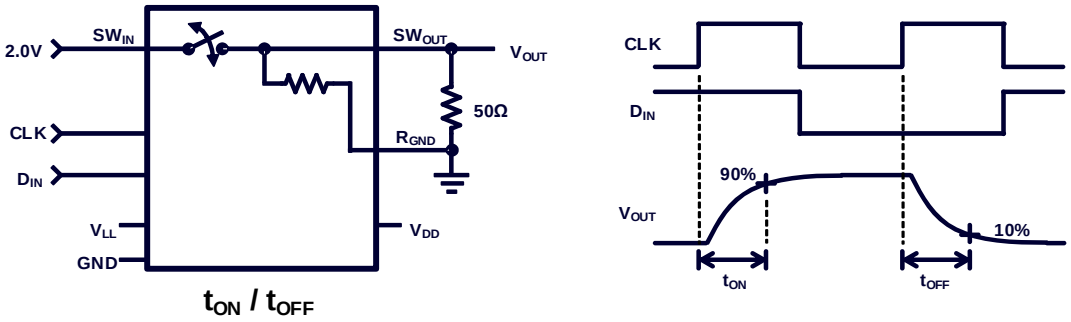


Switch On/Off DC Offset

Figure 3: Test Circuit 3

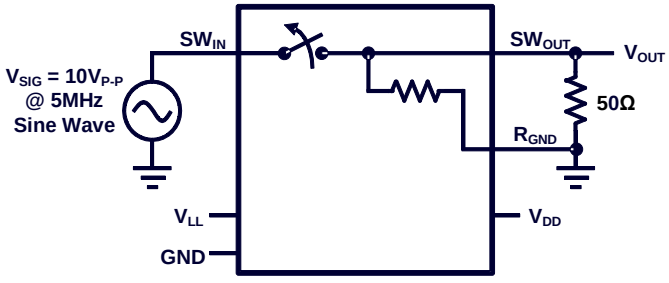
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TEST CIRCUITS *(continued)*



t_{ON} / t_{OFF}

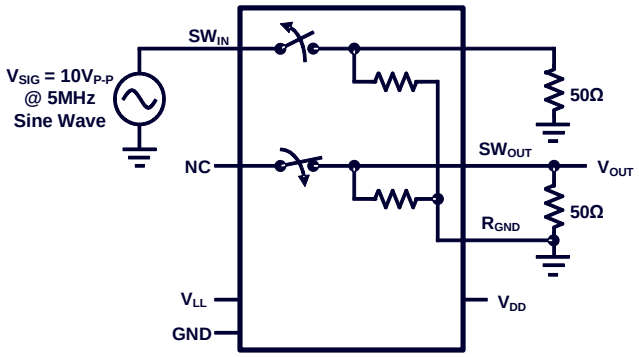
Figure 4: Test Circuit 4



$$K_O = 20Log \left| \frac{V_{OUT}}{V_{SIG}} \right|$$

Switch Off-Isolation

Figure 5: Test Circuit 5



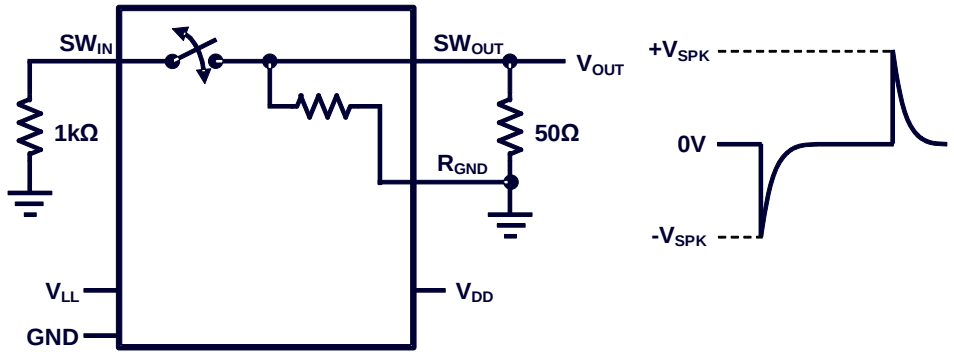
$$K_{CR} = 20Log \left| \frac{V_{OUT}}{V_{SIG}} \right|$$

Switch Crosstalk

Figure 6: Test Circuit 6

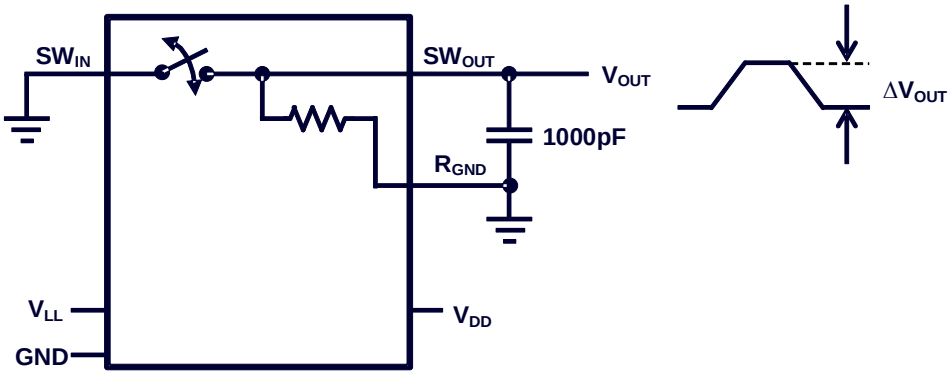
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TEST CIRCUITS *(continued)*



Output Voltage Spike

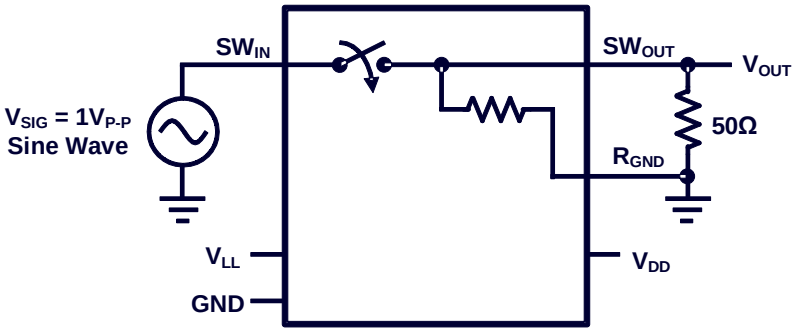
Figure 7: Test Circuit 7



$Q_{INJ} = 1000pF \times \Delta V_{OUT}$

Charge Injection

Figure 8: Test Circuit 8



Small Signal Bandwidth

Figure 9: Test Circuit 9

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FUNCTIONAL BLOCK DIAGRAM

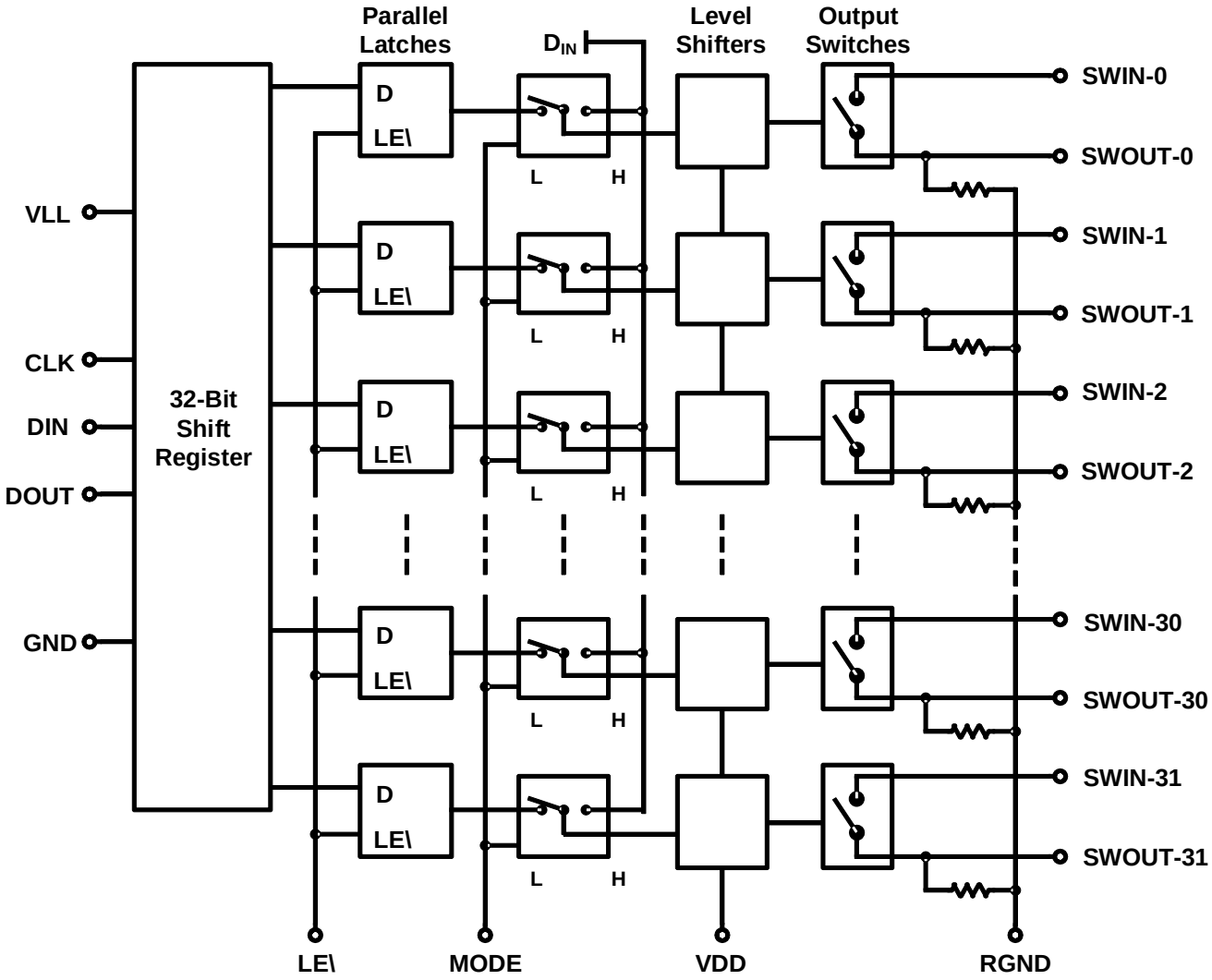


Figure 10: Functional Block Diagram

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APPLICATION INFORMATION

Detailed Description

The MP4835A is a 32-channel, high-voltage, single-pole/single-throw (SPST) analog switch with integrated output bleed resistors. It is designed for medical ultrasound imaging applications, and can also be used for non-destructive testing (NDT) applications. It can multiplex high transmission voltages to the selected piezoelectric transducer (PZT) and can multiplex the small analog echo signal to the selected receiver.

There are two modes to control the states of the output switches. When MODE is low, the output switches are controlled by a 32-bit serial shift register, followed by a 32-bit data latch. The data out (DOUT) pin allows multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high signal in the data latch turns the corresponding analog switch on, whereas a logic low signal turns it off. When MODE is high, the DIN pin acts as a global control for all 32 output switches. If DIN is high, all 32 output switches turn on; if DIN is low, all 32 output switches turn off.

The MP4835A has a unique patented design that does not require any high-voltage negative or positive supplies. This eliminates:

- The need to generate high-voltage positive and negative supplies
- The need for high-voltage bypass capacitors next to each device
- Safety concerns on high-voltage buses
- Start-up/shutdown fault condition concerns

Analog Switch

Analog switches have a typical switch resistance of 14Ω. When turned on, a switch can pass transmission voltages up to ±100V, with peak currents of up to ±1.8A. When turned off, it can block voltages up to ±100V.

Each switch has a dedicated input and output pin, SWIN-x and SWOUT-x. The transmission voltages must be connected to the SWIN pins and the PZT load to the SWOUT pins. The SWIN and SWOUT pins are not interchangeable.

Typical high-voltage transmission waves are short bursts of high-voltage pulses. The burst can consist of a single cycle or multiple cycles of 1.0MHz to 15MHz pulses, starting at 0V and ending at 0V (see Figure 11).

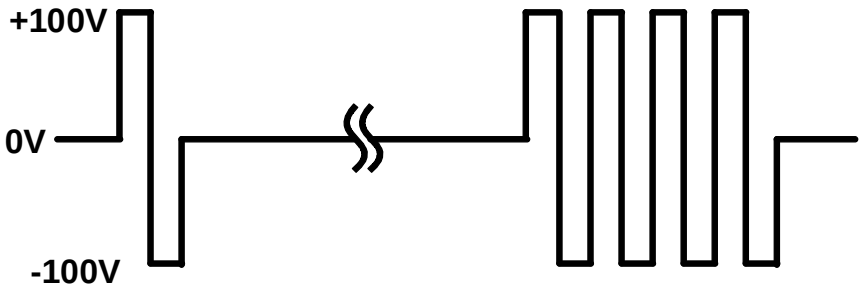


Figure 11: Typical Transmitter High-Voltage Burst

The SWIN pin must be close to ground before sending the high-voltage pulses. This allows the internal circuitry to properly drive the output switches.

Transmission voltages above ±5V must have frequencies above 500kHz. When receiving the echo signals where the voltages are below ±0.5V, there is no restriction. The switch can pass low-voltage DC signals.

Logic Interface, MODE = Low

The MP4835A is controlled by a 32-bit serial shift register, followed by a 32-bit latch. Data is loaded into the shift register at the rising edge of the clock. No data is transferred during the falling edge. Data is shifted into register 0 and is shifted out from register 31.

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Figure 12 shows the logic interface details. On the first clock cycle, the first data bit enters into shift register 0. After 31 more clocked cycles, the first bit will be in register 31.

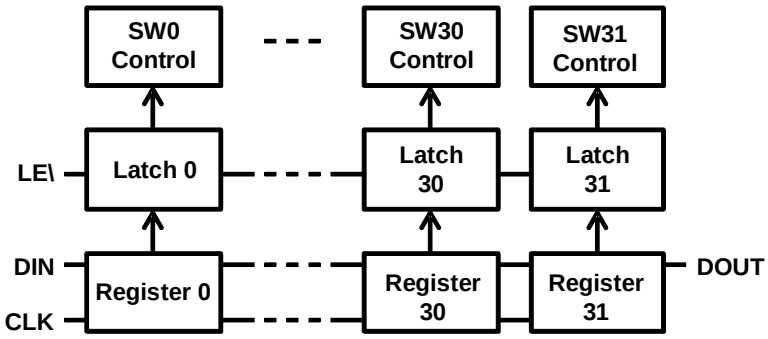


Figure 12: Logic Interface Details

When the latch enable bar (LE\) is low, the data in the shift registers is transferred to the 32-bit latch. When LE\ is high, the data in the latches is held. With LE\ high, new data can be shifted to the 32-bit serial shift register without affecting the data in the 32-bit latch. The output switch states follows the data in the 32-bit latch.

The maximum clock frequency for the MP4835A is 60MHz. The front-end logic control is designed to minimize the number of input and output (I/O) control lines. A system requiring 192 channels will need 192 / 32 = 6 devices. Figure 13 shows six MP4835A devices in a single daisy chain configuration.

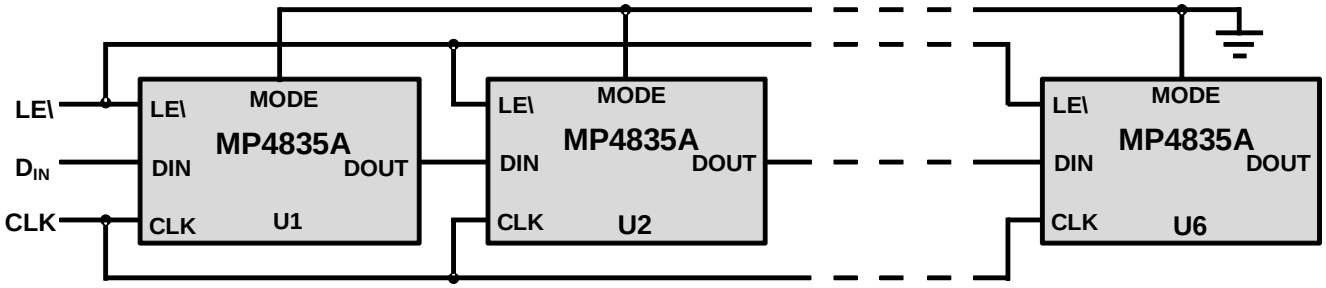


Figure 13: Daisy Chaining 6 MP4835A Devices with a Single Data Input Line

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With a 60MHz clock, all six devices can be updated in 3.2µs. Only three control lines are required: clock (CLK), data in (D_{IN}), and a latch enable bar (LE\). For systems requiring a faster update, multiple D_{IN} lines can be used (see Figure 14).

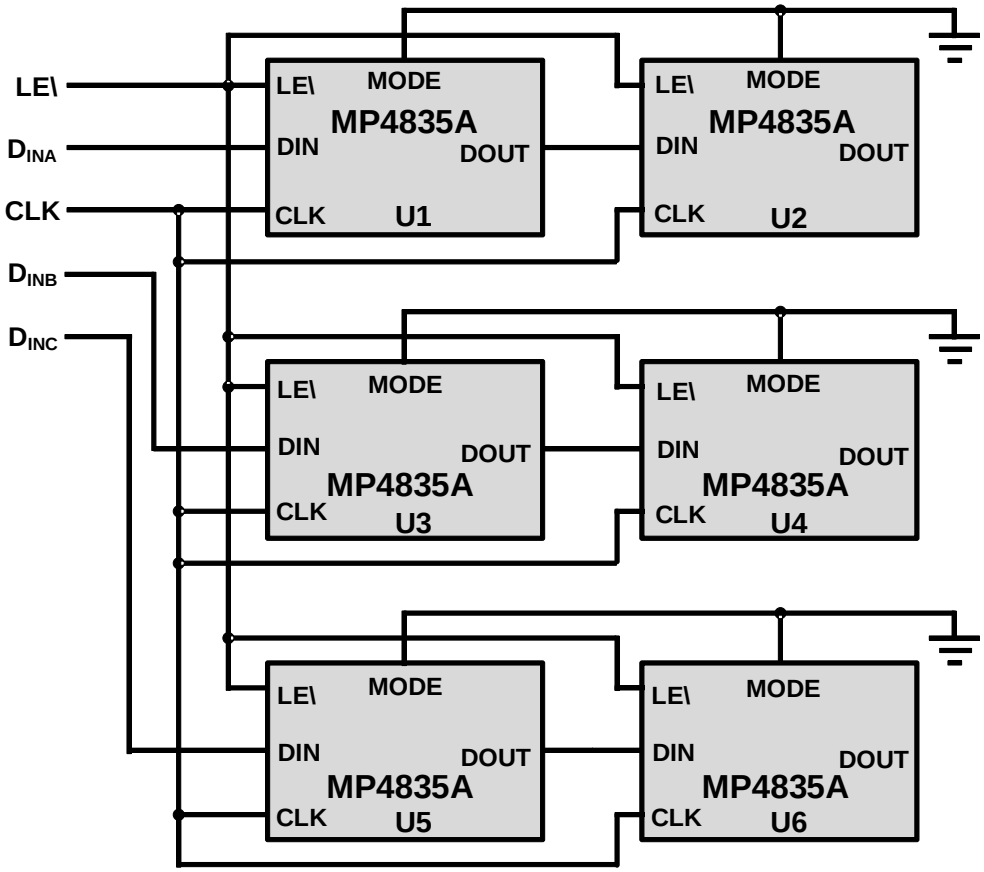


Figure 14: Daisy Chaining MP4835A Devices with Multiple D_{IN} Lines

Figure 14 shows a 192-channel system incorporating three data input lines: D_{INA}, D_{INB}, and D_{INC}. Each data input lines are for two MP4835A devices daisy chained together. This creates five control lines. With a 60MHz clock, all 192 channels can be updated in 1.07µs.

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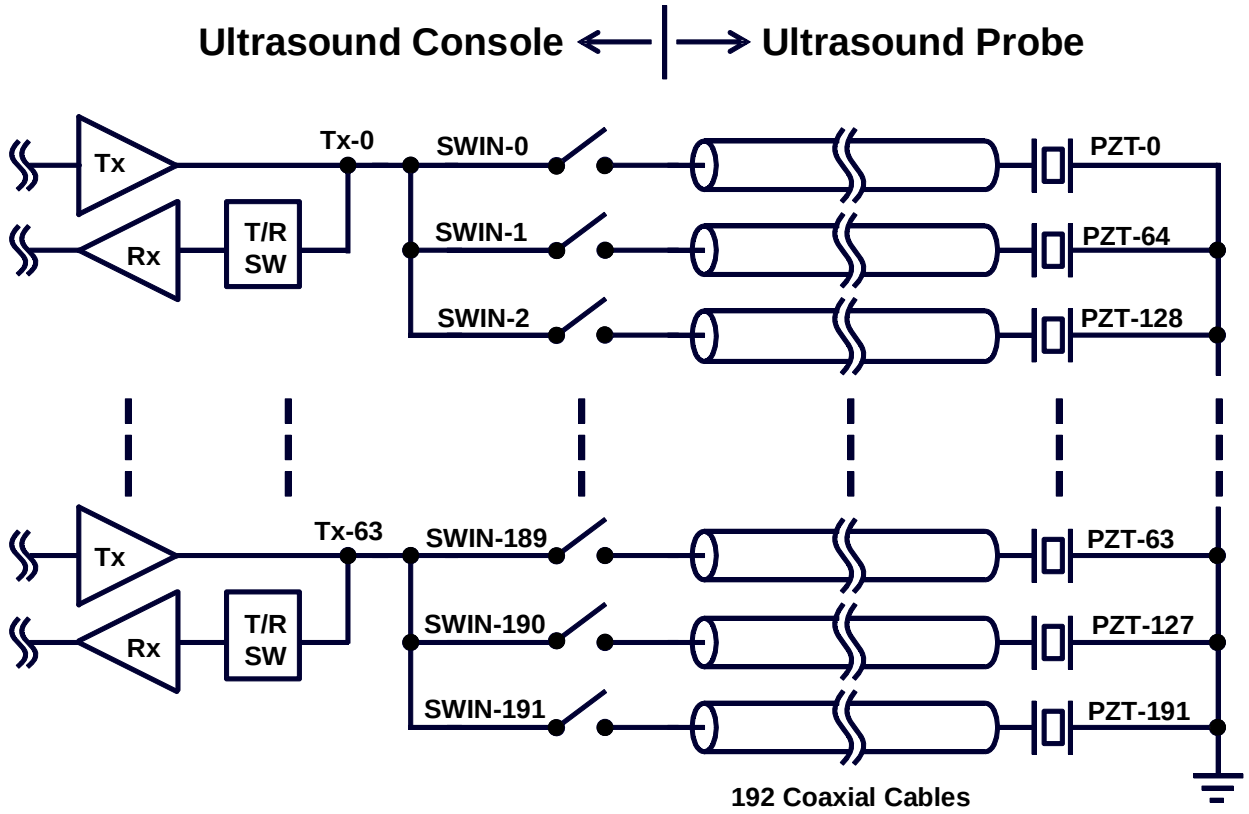


Figure 15: MP4835A in the Console

Figure 15 shows where the MP4835A analog switches reside in an ultrasound system. A 1:3 multiplexing configuration is shown as an example. Multiplexing configurations typically range from 1:2 to 1:8, and can be even higher. 1:8 or higher ratios have slower image frame rates and/or lower quality images, which are typically employed for lower-end, lower-cost ultrasound markets. The MP4835A can be used in any ratio.

The main advantage of using the MP4835A is to reduce the number of transmitter and receiver circuits. Without any analog switches, an ultrasound console requires 192 transmitters and receivers to drive an ultrasound probe with 192 PZT elements (see Figure 15). With analog switches, only 64 transmitters and receivers are needed. This reduction saves board space, power, and cost given that the transmitter and receiver circuitry can be quite complex. These benefits are especially important for portable ultrasound systems, in which space, battery life, and weight are all at a premium.

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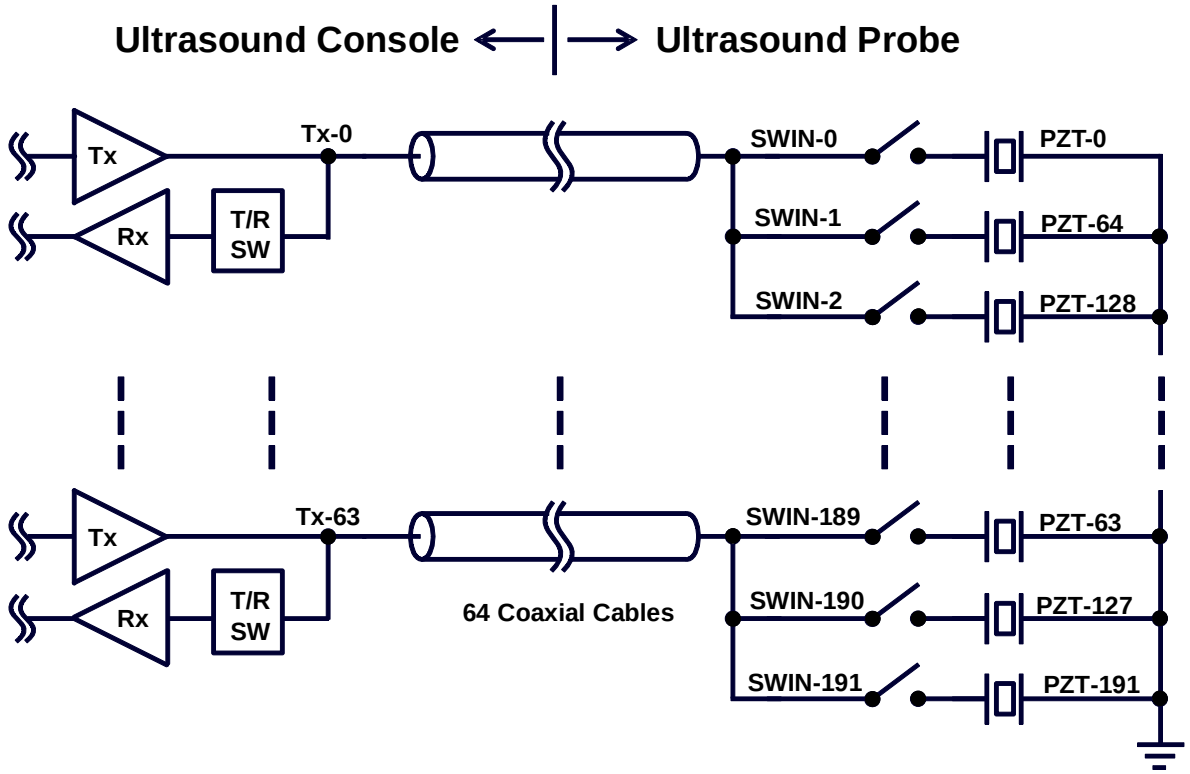


Figure 16: The MP4835A Inside the Ultrasound Probe Head

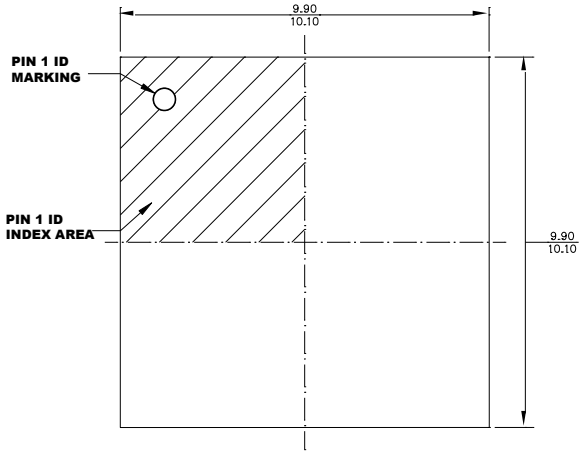
Figure 16 shows the advantages of putting analog switches inside the probe head, which may be referred to as an active probe. The probe head is often severely space-limited and thermally limited. The housing is waterproof, as it needs to be submersed in alcohol for sterilization. By employing analog switches inside the probe head, the number of coaxial cables can be reduced. Instead of 192 coaxial cables, only 64 coaxial cables are needed for the PZT, plus 10 or fewer additional coaxial cables for the supply lines and logic interface.

The reduction in the number of coaxial cables offers a significant cost reduction for the probe head, given that the coaxial cable is by far the most expensive component. Aside from the material costs, the labor to connect the coaxial cables can also be quite costly. An added user benefit is that the probe head becomes more maneuverable. The sonographer will be less fatigued over time when using an active probe. The MP4835A not requiring high-voltage supplies eliminates concerns with running high-voltage DC lines on the coaxial cables, the minimal power dissipation design eliminates the concern for thermal constraints inside the probe head, and the higher clock speed reduces the number of necessary data lines.

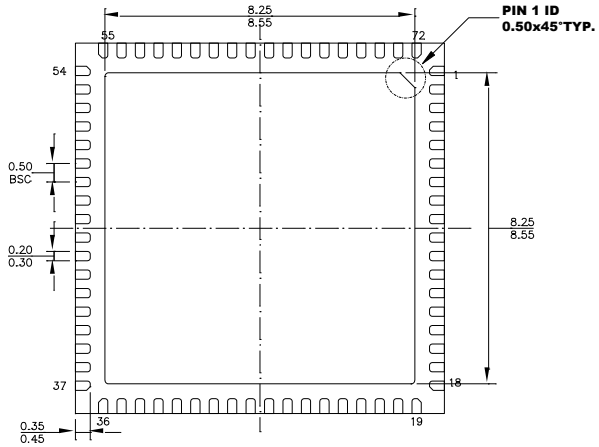
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PACKAGE INFORMATION

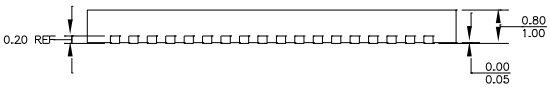
QFN-72 (10mmx10mm)



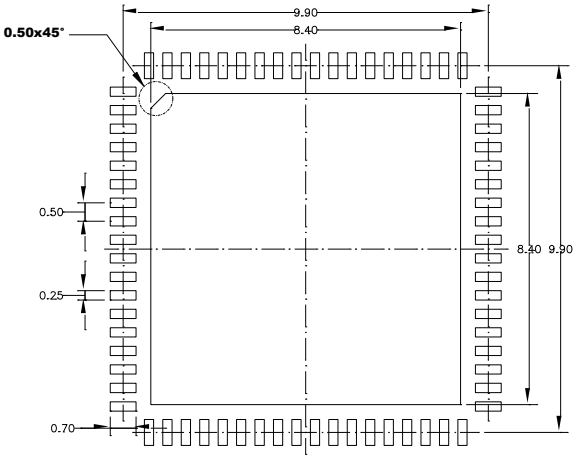
TOP VIEW



BOTTOM VIEW



SIDE VIEW



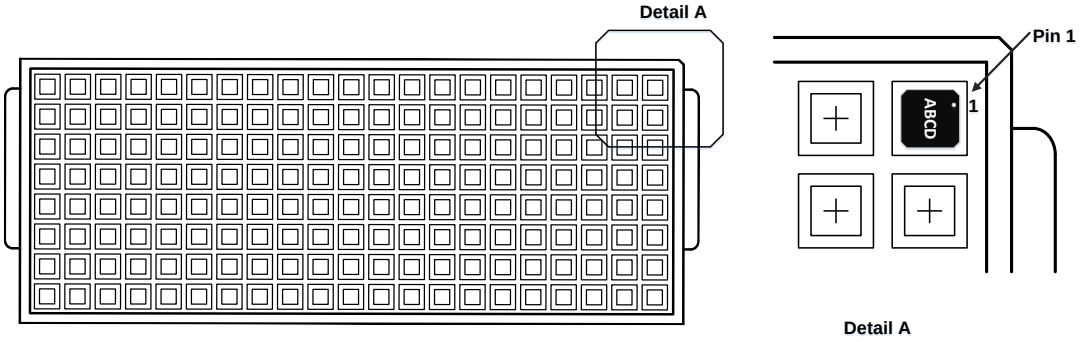
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION (8)



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4835AGRD–T	QFN-72 (10mmx10mm)	N/A	N/A	240	N/A	N/A	N/A

Note:

8) This is a schematic diagram of the tray. Different packages correspond to different trays with different lengths, widths, and heights.

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	12/8/2020	Initial Release	-
1.01	8/5/2021	Updated Figure Numbers	Page 14 to 17

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