# MP3910A

**Peak Current Mode Boost PWM Controller with Programmable Frequency, External Soft Start Light Load Operation, and SOIC8 Package**

The Future of Analog IC Technology

## DESCRIPTION

The MP3910A is a Peak Current Mode PWM controller that can drive an external MOSFET capable of handling more than 10A current. It has a typical operational current of 400μA and can accommodate flyback, boost for non-isolated and isolated applications.

Current mode control provides inherently simple loop compensation and cycle-by-cycle current limit. Under-voltage lockout, soft-start and slope compensation are all provided to minimize the external component count.

While designed for Flyback applications, the MP3910A can also be used for other topologies including Boost, Forward and Sepic. The 1A gate driver minimizes the power loss of the external MOSFET while allowing the use of a wide variety of standard threshold devices. Additionally, MP3910A has pulse skipping mode function that improves the efficiency with light load or no load. It also provides hiccup protection for OLP, OVP and SCP condition.

The MP3910A is available in SOIC8 package.

## FEATURES

- 9V to 14V Supply Voltage Range
- 1A MOSFET Gate Driver
- External Soft-Start
- Pulse Skipping Operation with Light Load
- Programmable Switching Frequency (30kHz-to-400kHz)
- Cycle-by-Cycle Current Limit
- Over Voltage Protection
- Short Circuit Protection
- Over Temperature Protection
- Available in SOIC8 Package

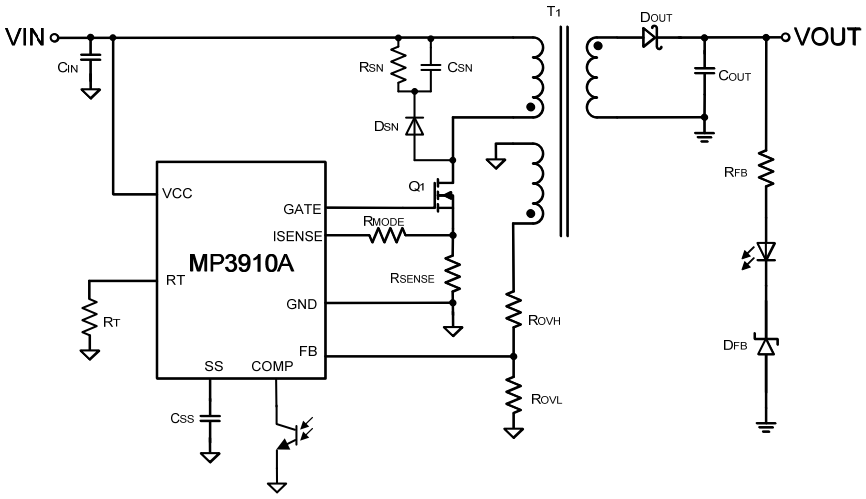
## APPLICATIONS

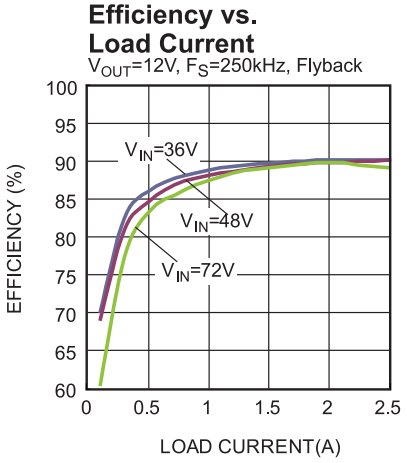
- Telecom Isolated Power Supplies
- Brick Modules
- Off-line Controller
- General Step Up Applications
- PoE Powered Devices

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## TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP3910AGS | SOIC-8 | *See Below* |

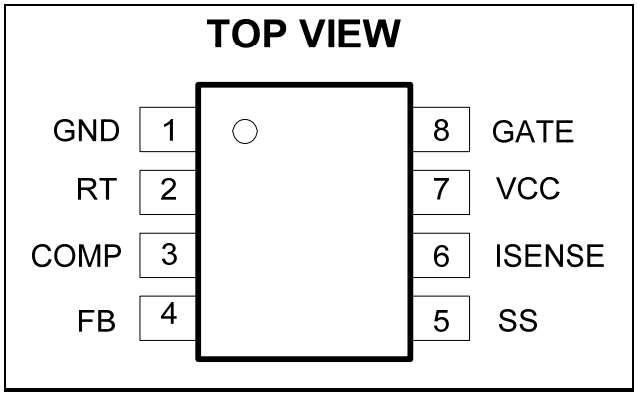
* For Tape & Reel, add suffix –Z (e.g. MP3910AGS–Z);

## TOP MARKING

MP3910A
LLLLLLLL
MPSYWW

MP3910A: product code of MP3910AGS;
LLLLLLLL: lot number;
MPS: MPS prefix;
Y: year code;
WW: week code:

## PACKAGE REFERENCE





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## ABSOLUTE MAXIMUM RATINGS (1)

VCC, GATE to GND.....–0.3V to 16V
All Other Pins.....–0.3V to 6V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
..... 1.38W
Maximum Operating Frequency..... 500kHz
Storage Temperature..... -55°C to +150°C
Junction Temperature.....150°C
Lead Temperature .....260°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{CC}$ .....9V to 14V
Operating Junction Temp. ($T_J$). -40°C to +125°C

| *Thermal Resistance* (4) | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| SOIC-8 | 90 | 45 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 12V, $T_J$ = -40°C to125°C (typical values are tested at 25°C), unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Supply Management** | | | | | | |
| VCC UVLO Threshold | $V_{UVLO}$ | Rising edge | 7.4 | 8 | 8.7 | V |
| VCC UVLO Hysteresis | $V_{UVLO_HYS}$ | | | 650 | | mV |
| Quiescent Current | $I_Q$ | $V_{FB}$=1.35V | | 400 | 520 | µA |
| **Driving Signal** | | | | | | |
| Gate Driver Impedance (Sourcing) | | $I_{GATE}$=-20mA | | 4.1 | | Ω |
| Gate Driver Impedance (Sinking) | | $I_{GATE}$=20mA | | 2 | | Ω |
| **Error Amplifier** | | | | | | |
| Error Amplifier Transconductance | $G_{EA}$ | $V_{FB}$ is +-50mV from FB Reference, $V_{COMP}$=1.5V | | 0.56 | | mA/V |
| Maximum Amplifier Output Current | | Sourcing or Sinking | | 75 | | µA |
| COMP High Voltage | | $I_{SENSE}$=0V, $V_{FB}$ =1V | | 2.4 | | V |
| | | $I_{SENSE}$=1V, Floating COMP | | | | |
| **Current Sense** | | | | | | |
| Current Comparator Leading Edge Blanking (7) | $T_{LEB}$ | | | 214 | 398 | ns |
| ISENSE Limit | Vlimit | $T_J$=25°C | 163 | 185 | 206 | mV |
| SCP Limit(5) | $V_{SCP}$ | | | 350 | | mV |
| Current Sense Amplifier Gain | $G_{SENSE}$ | $\Delta V_{COMP}/\Delta V_{ISENSE}$ | | 2.7 | | V/V |
| ISENSE Bias Current | $I_{SENSE}$ | $T_J$=25°C | | 0.01 | 0.15 | µA |
| **PWM** | | | | | | |
| $V_{COMP}$ (Skipping Mode) (5) | | Pulse skipping mode operation threshold, V(comp) | | 0.95 | | V |
| Switching Frequency | $F_{SW}$ | $R_T$=6.81kΩ | 308 | 337 | 363 | kHz |
| | | $R_T$ =80.6kΩ | 25 | 30 | 35 | kHz |
| Minimum ON Time | $T_{ON-MIN}$ | | | 214 | 398 | ns |
| Maximum Duty Cycle | $D_{MAX}$ | $R_T$=6.81kΩ | 93 | 95 | | % |
| **Soft-start (6)** | | | | | | |
| Charge Current | $I_{SS}$ | | | 54 | | µA |
| Over Load Detection Discharge Current | | | | 17.8 | | µA |
| Discharge Current During Protection | | | | 1.66 | | µA |
| Charged Threshold Voltage | | | | 3.65 | | V |
| Over Load Shutdown Threshold Voltage | | | | 2.9 | | V |
| Protection Reset Threshold Voltage | | | | 0.2 | | V |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{CC}$ = 12V, $T_J$= -40°C to125°C(typical at a temperature range of 25°C), unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Voltage Feedback Management** | | | | | | |
| Mode Detection Voltage(5) | | | | 185 | | mV |
| Mode Detection Current(5) | | | | 55 | | μA |
| Mode Detection Time(5) | | | | 180 | | μs |
| FB Reference Voltage | $V_{FB}$ | $T_J$=25°C | 1.222 | 1.237 | 1.252 | V |
| | | $T_J$=-40°C to 125°C | 1.211 | 1.237 | 1.258 | V |
| FB Bias Current | $I_{FB}$ | $V_{FB}$=1.237V, $T_J$= 25°C | | 0.01 | 0.15 | μA |
| OVP Reference Level | $V_{OVP}$ | | 1.391 | 1.438 | 1.479 | V |
| COMP Pull up Resistor | | | | 14.4 | | kΩ |
| COMP Pull up Voltage(5) | | | | 3.6 | | V |
| **Thermal Protection** | | | | | | |
| Thermal Shutdown(5) | $T_{SD}$ | | | 160 | | ºC |
| Thermal Hysteresis(5) | | | | 20 | | ºC |

**Notes:**

5) Guaranteed by engineering sample characterization.
6) Refer to “soft-start section” for detail function of discharge current and threshold voltage.
7) It is same as Minimum on Time.


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## PIN FUNCTIONS

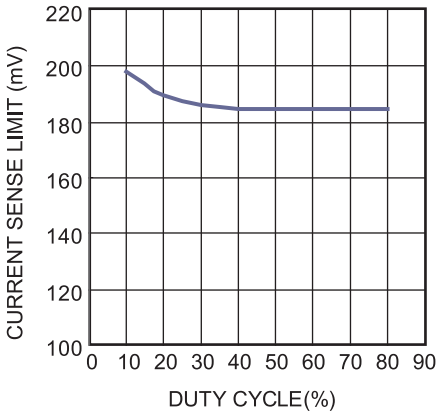
| Pin # | Name | Description |
|---|---|---|
| 1 | GND | Power ground pin which is gate driver return. |
| 2 | RT | Switching frequency set pin. Connect a resistor from this pin to GND to set the switching frequency (30kHz~400kHz). |
| 3 | COMP | Feedback pin for isolated solution. Error amplifier output pin for un-isolated solution. |
| 4 | FB | Feedback and OVP monitor pin with respective internal reference voltage for un-isolated solution. OVP monitor pin for isolated solution. Connected to GND if not used in isolated solution. |
| 5 | SS | Soft-start pin. Connect one capacitor between this pin and GND to control the duration of COMP voltage rising. It determines both the soft-start current, and hiccup protection delay. |
| 6 | ISENSE | Current Sense and application mode (isolated/un-isolated) setting pin. At start-up, this pin will output one current signal and sense the voltage for mode setting detection. During normal operation, this pin will sense the voltage across sense resistor for current mode control, as well as cycle-by-cycle current limit, over load and short circuit protection. |
| 7 | VCC | IC Input supply. Connect a bypass capacitor from this pin to GND. VCC voltage should be lower than 14V in application. |
| 8 | GATE | This pin drives the external N-channel power MOSFET device. |


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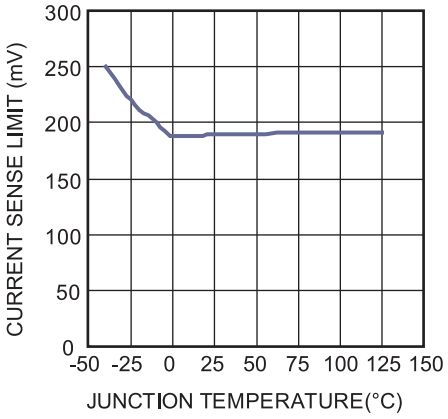
## TYPICAL CHARACTERISTICS

**$V_{CC}$ = 12V, $T_A$ = 25°C, unless otherwise noted.**

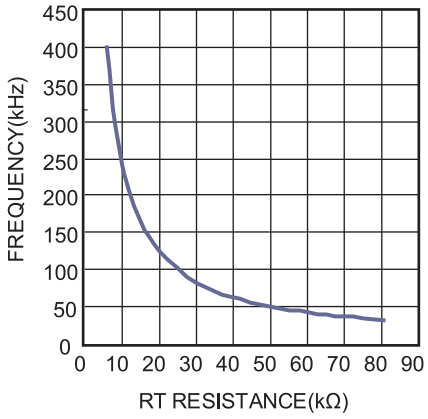
### Current Sense Limit vs. Duty Cycle




### Current Sense Limit vs. Temperature

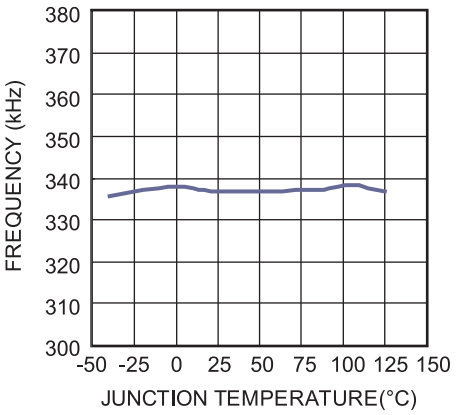



### Frequency vs. RT Resistance



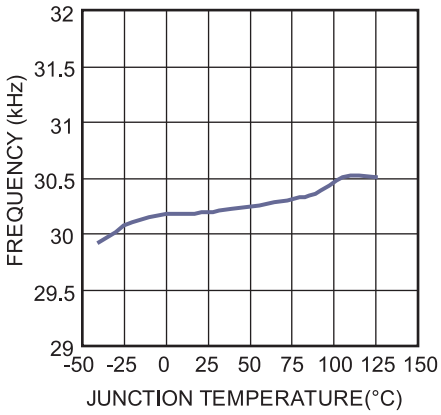

### Frequency vs. Temperature

$R_T$=6.81kΩ

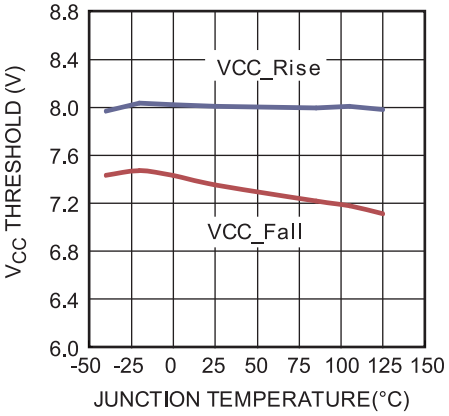



### Frequency vs. Temperature

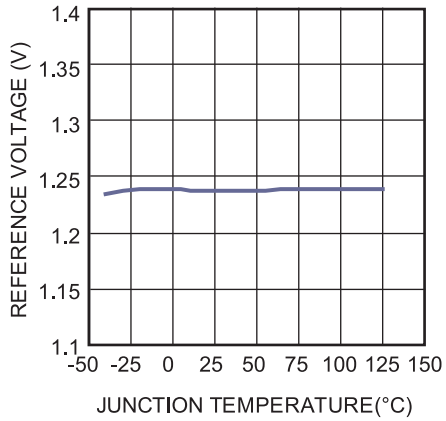
$R_T$=80.6kΩ



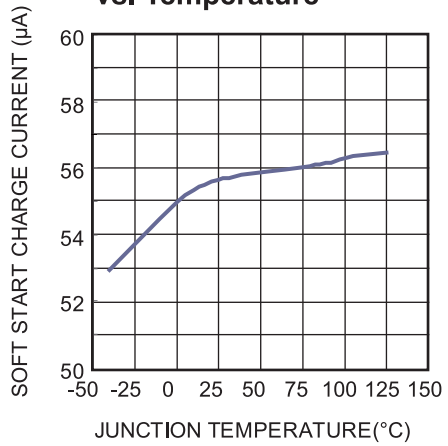

### Vcc Threshold vs. Temperature




### $V_{REF}$ vs. Temperature




### SS Charge Current vs. Temperature





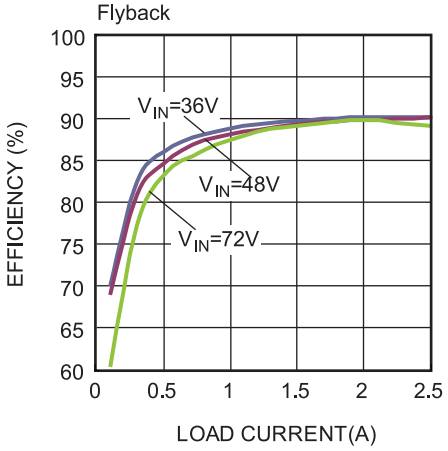
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## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $F_{SW}$=250kHz, Fly-back Mode, $T_A$ = 25°C, unless otherwise noted.**

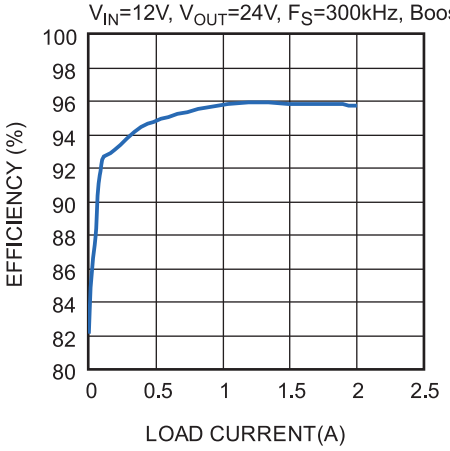
**Efficiency vs. Load Current**

Flyback

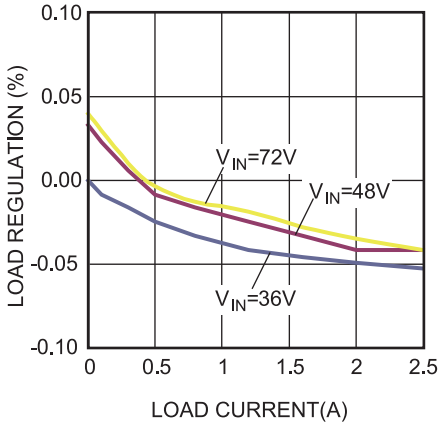



**Efficiency vs. Load Current**

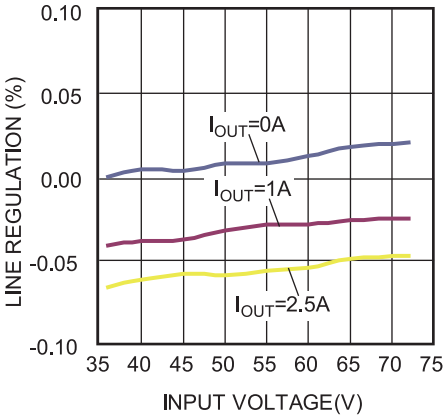
$V_{IN}$=12V, $V_{OUT}$=24V, $F_S$=300kHz, Boost




**Load Regulation vs. Load Current**

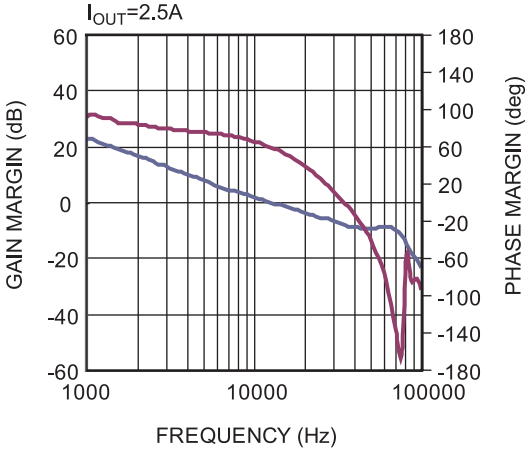



**Line Regulation vs. Input Voltage**




**Gain and Phase vs. Frequency**

$I_{OUT}$=2.5A





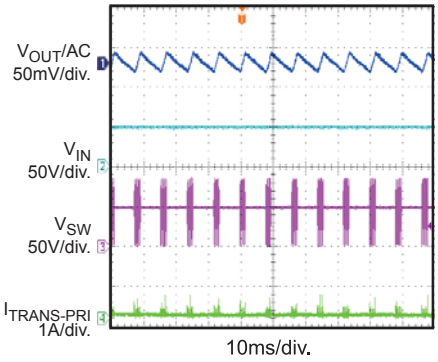
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## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $F_{SW}$=250kHz, Fly-back Mode, $T_A$ = 25°C, unless otherwise noted.**

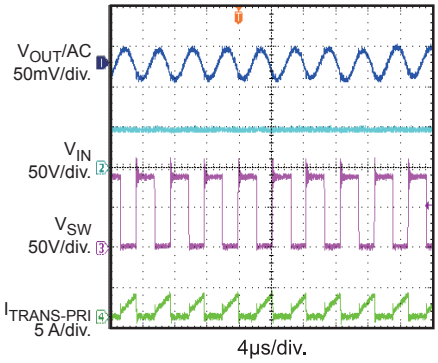
### Steady State

$I_{OUT}$=0A



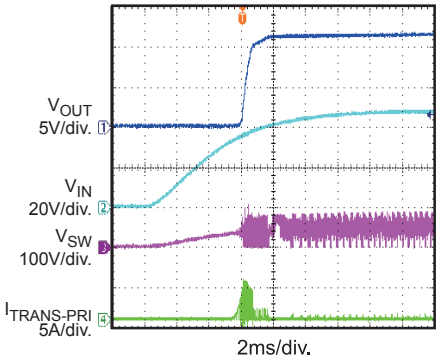

### Steady State

$I_{OUT}$=2.5A



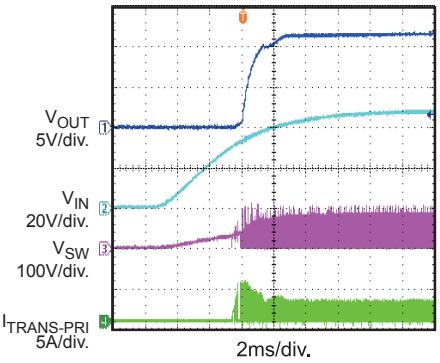

### Startup Through $V_{IN}$

$I_{OUT}$=0A



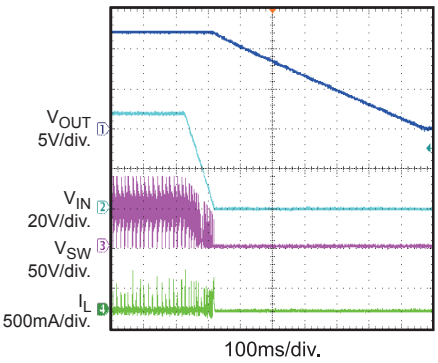

### Startup Through $V_{IN}$

$I_{OUT}$=2.5A



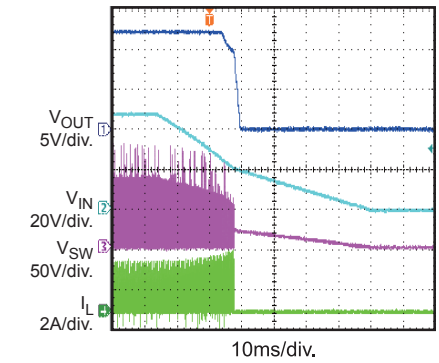

### Shutdown Through $V_{IN}$

$I_{OUT}$=0.01A



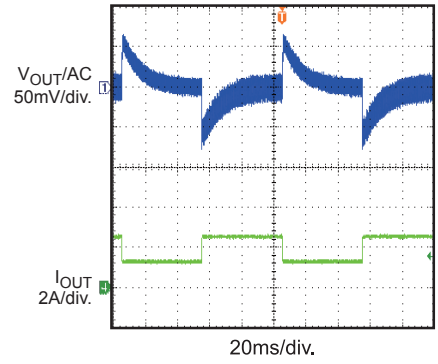

### Shutdown Through $V_{IN}$

$I_{OUT}$=2.5A



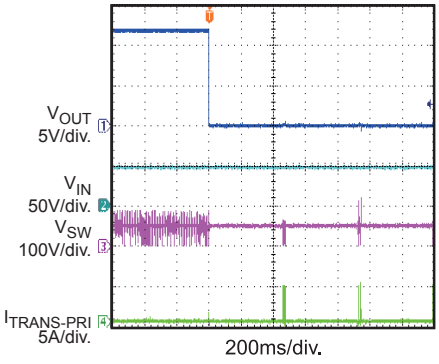

### Load Transient

$I_{OUT}$=1.25A->2.5A, $I_{RAMP}$=800mA/µs



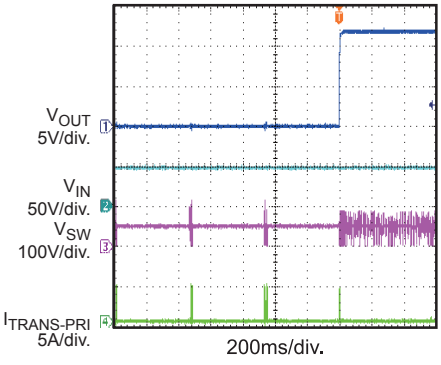

### SCP Entry

$I_{OUT}$=0A->short




### SCP Recovery

$I_{OUT}$=short->0A





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## FUNCTION BLOCK DIAGRAM

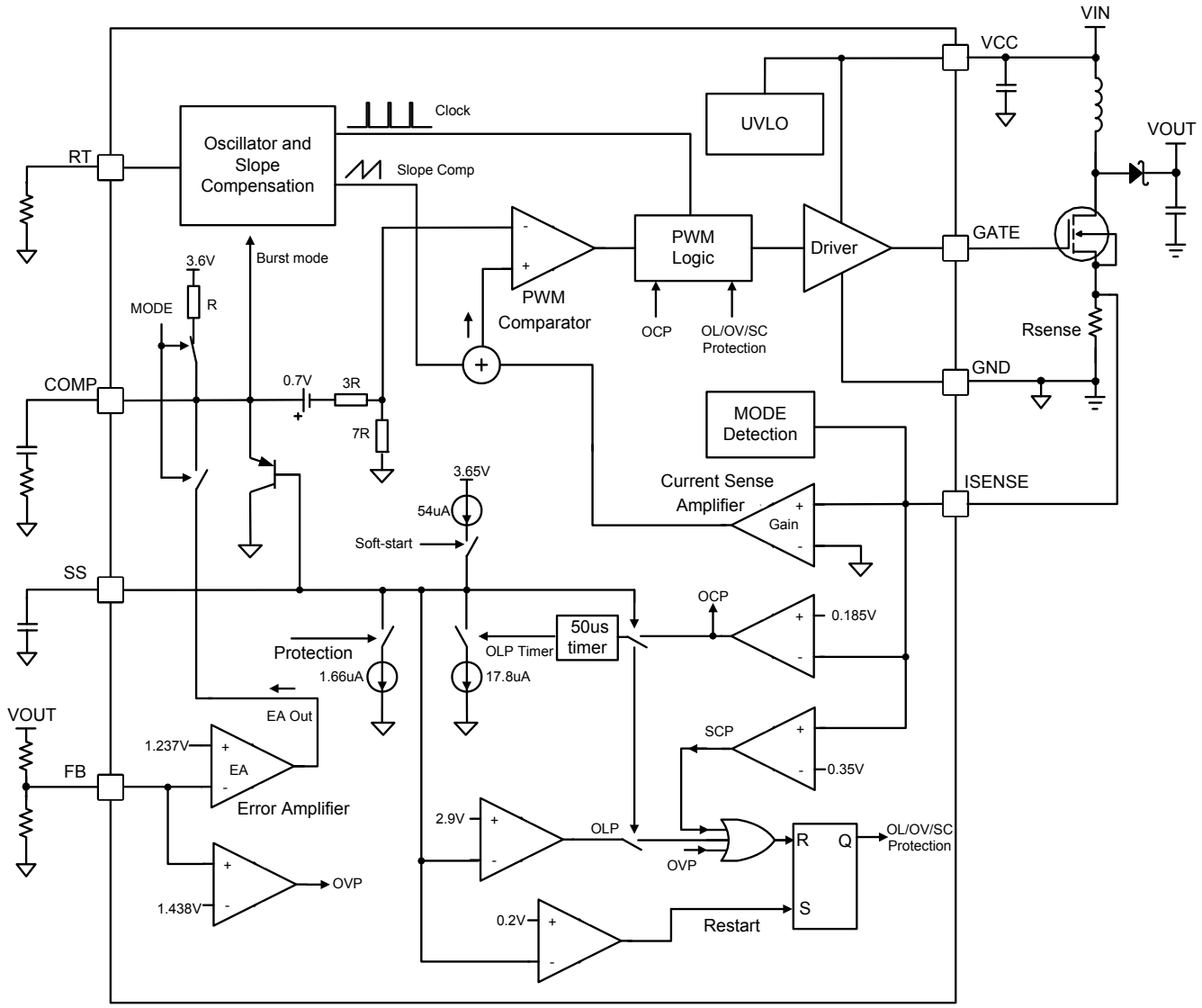



**Figure 1: Functional Block Diagram**


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## OPERATION

The MP3910A uses a programmable frequency, peak current mode architecture to regulate the feedback voltage. The operation of the MP3910A can be understood with the block diagram of Figure 1.

### PWM Operation

At the beginning of each cycle the external N-channel MOSFET is turned on, forcing the current in the inductor to increase. The current through the FET can be sensed and when the sum voltage of amplified ISENSE signal and slope signal rises above the voltage set by the COMP pin, the external FET is turned off. The inductor current then flows to the output capacitor through the schottky diode. The inductor current is controlled by the COMP voltage, which itself is controlled by the output voltage. Thus the output voltage controls the inductor current to satisfy the load. This current mode architecture improves transient response and control loop stability over voltage mode architecture.

### Pulse Skipping Mode

At light load condition, the MP3910A goes into pulse skipping mode to improve light load efficiency. Pulse skipping decision is based on its internal COMP voltage. If COMP is lower than the internal sleep threshold with typical 0.95V, a PAUSE command is generated to block the turn-on clock pulse so the power MOSFET is turned off immediately, saving gate driving and switching losses. This PAUSE command also puts the whole chip into sleep mode, consuming very low quiescent current to further improve the light load efficiency. The gate driver output remains low until COMP voltage is higher than the sleep threshold, then PAUSE signal is reset so the chip is back into normal PWM operation.

### VCC Power Supply

MP3910A operates with supply voltage from 9V to 14V on VCC pin. VCC UVLO's rising threshold is 8V with a hysteresis of 650mV. When the voltage at VCC pin crosses the VCC UVLO, the controller is enabled and all the internal circuitry is powered by VCC source. VCC voltage should be lower than 14V. For high input voltage application, one external voltage clamp circuit is needed to regulate VCC voltage in appropriate range.

### Feedback Loop Setting

To be coincident for different design in isolated and un-isolated application, MP3910A can feedback the output signal through either of FB pin or COMP pin by different setting on ISENSE pin.

For un-isolated application such as boost mode, MP3910A integrates one error amplifier which can amplify the output error signal from FB pin, COMP pin needs one RC network for compensation. For isolated application such as fly-back mode, the feedback signal from opto-coupler has been amplified by secondary circuitry, directly connect the signal to COMP pin will make loop compensation much easier by eliminating the primary side amplifier.

The different feedback loop can be set by different ISENSE pin connection. At the beginning of part enabled, ISENSE pin will output 180us current pulse with typical value of 55uA, as showed in Figure 2, if the reflected voltage on ISENSE pin is higher than 185mV, MP3910A will disable the internal error amplifier between FB and COMP pins and pull up COMP pin to 3.6V source with 14.4kΩ resistor, the feedback signal can be connected to COMP pin directly. If the detected voltage is lower than 185mV, MP3910A will enable the internal error amplifier but turn off the pull up resistor. Then COMP pin is just one output pin of error amplifier and the feedback signal should be connected to FB pin.

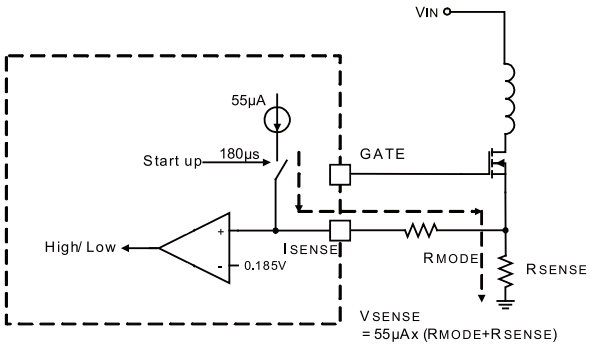



**Figure 2: Feedback Mode Setting**


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Generally, it is recommended to place one resistor with 5Kohm~10Kohm between ISENSE pin and current sense resistor for the feedback mode through COMP pin, and connect ISENSE pin to current sense resistor directly for feedback mode through FB pin.

**Soft-Start**

MP3910A uses one external capacitor on SS pin to control COMP voltage rising for soft-start. When the chip starts, the capacitor on SS pin is charged by one 54uA current source at a slow pace set by the capacitance. When the SS voltage is lower than the external COMP voltage, SS overrides the COMP signal so the PWM comparator uses SS instead of COMP as the PWM turn off reference. When SS is higher than COMP voltage, COMP gains the control back and the soft start finishes. The soft-start can reduce voltage stresses and surge currents during start up, also prevent the converter output voltage from overshooting during startup. Soft start occurs during the start up time and protection recovery time after OLP, SCP and OVP. During normal condition, the SS voltage is clamped at 3.65V.

**Programmable Oscillator**

The MP3910A oscillating frequency is set by an external resistor from the RT pin to ground. The value of $R_T$ can be estimated from:

$$R_T = \frac{2.35 \times 10^3}{f_{SW}}$$

$R_T$ is in kΩ and $f_{SW}$ is in kHz.

The frequency setting resistor value shouldn't be too large for noise immunity consideration. It is recommended to set the frequency within 30kHz to 400kHz.

**Current Sense and Over Current Protection**

The MP3910A is peak current mode controller. The current through the external FET can be sensed through a sensing resistor used in series with the source terminal of FET. The sensed voltage on ISENSE pin is then amplified and fed to the high speed current comparator for the current mode control purpose. The current comparator takes this sensed voltage (plus slope compensation) as one of its inputs, then compares the power switch current with the COMP voltage. When the amplified current signal is higher than the COMP voltage, the comparator output is low, turning off the power MOSFET.

If the voltage on the ISENSE pin exceeds the current-limit threshold voltage with typical value of 185mV, MP3910A will turn off the GATE output for that cycle, until the internal oscillator starts the next cycle, and sense current again. MP3910A limits the current of MOSFET cycle-by-cycle.

**Over Load Protection (OLP)**

The peak current is limited cycle-by-cycle, if the load continues increasing after triggering OCP protection, the output voltage will decrease and the peak current will trigger OCP every cycle. MP3910A set the over load detection by continue monitoring the ISENSE pin voltage.

Once the SS voltage is charged to 3.65V after start up, the OLP protection is enabled. If an OCP signal is detected, the soft-start charging current is disabled and one over current discharge source is enabled, the SS voltage drops with the rate of 17.8uA current. At the same time, one 50us one-shot timer is activated and it remains active for 50μs after the OCP condition stops. The 17.8uA discharge source cannot be turn off until the one-shot timer becomes inactive. If the OCP disappears before at least 50us prior than the SS capacitor discharging to 2.9V, MP3910A will run back to normal work condition and the SS capacitor will be re-charged to 3.65V with 54uA rate. If the SS capacitor is discharged to 2.9V, MP3910A will register it as over load condition and turn off the gate output until next re-start cycle. At the same time, 17.8uA discharge current is disabled and the 1.66uA over load discharge source is enabled. After the SS voltage is discharged to 0.2V, MP3910A will re-start up with new soft-start cycle. This is hiccup mode protection.

The OLP detection function is disabled after the SS voltage is discharged to be lower than 2.9V and it will be re-enabled after SS voltage is re-charged to 3.65V. So the OLP only occurs after the soft-start is completed.


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**Short Circuit Protection**

When the output is shorted to the ground, the part works in OCP mode and current is limited cycle-by-cycle, the part may run into OLP protection.

But if the peak current cannot be limited by 185mV ISENSE voltage in every cycle due to leading edge blanking (LEB) time, the current may run out of control and transformer may run into saturation. If the monitored ISENSE voltage reaches 0.35V, the part will turn off the GATE out and run into hiccup mode by discharge SS capacitor with 1.66uA current. It will also re-start up if SS voltage is discharged to 0.2V.

In case the short circuit is removed, the output voltage will recover only after the next new restart cycle.

For boost converter, it has no method to limit current from the input to the output in the condition of output short circuit. If protection from this type condition is desired, it is necessary to add some secondary protection circuit.

**Over Voltage Protection**

For isolated-flyback application, the positive plateau of auxiliary winding voltage is proportional to the output voltage, MP3910A features the over voltage protection by using the auxiliary winding voltage instead of directly monitoring the output voltage. The auxiliary voltage can be monitored by FB pin through resistor divider, once the voltage is higher than OVP reference voltage, MP3910A turns off the GATE output and discharge SS voltage with 1.66uA current until SS voltage is lower than 0.2V, then the part will initial one new re-start cycle.

To avoid the mis-trigger due to the oscillation of the leakage inductance and the parasitic capacitance, the OVP sampling has a $T_{OVPS}$ blanking with 500ns typical value. For some oscillation condition, one external filter is necessary to work together with the 500ns LEB time.

For un-isolated solution, the DC output voltage is applied to FB pin and it can easily detect the OVP condition.

**Thermal Shutdown**

Thermal shutdown is implemented to prevent the chip from thermally running away. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its low threshold, thermal shutdown is gone so the chip is enabled again with a new start-cycle.


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# APPLICATION INFORMATION

## COMPONENT SELECTION

MP3910A can be used for topologies including Flyback, Boost and Sepic. Refer to figure 5 and below introduction for typical external component selection of boost converter.

### Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. If we use 10kΩ for the low-side resistor ($R_{FBL}$) of the voltage divider, we can determine the high-side resistor ($R_{FBH}$) by the equation:

$$R_{FBH} = \frac{R_{FBL} \times (V_{OUT} - V_{REF})}{V_{REF}}$$

Where $V_{OUT}$ is the output voltage

For $R_{FBL}$=10kΩ, $V_{OUT}$=24V and $V_{REF}$=1.237V, then $R_{FBH}$=182kΩ.

### Selecting the Soft-start Capacitor

MP3910A ramps external capacitor voltage on SS pin to control COMP voltage, which determines inductor peak current. The SS pin voltage can be estimated from below equation:

$$Vss = \frac{54\mu A}{C_{ss}} \times T_{ss}$$

When OLP, SCP, OVP occurs, the SS acts as a timer. Once the protection occurs, the 1.66uA current discharges SS cap for hiccup protection.

### Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a small high quality ceramic capacitor, i.e. 1uF, should be place close to IC. The capacitance for boost input can be calculated as:

$$C_{IN} \approx \frac{\Delta I}{8 \times \Delta V_{IN} \times F_{SW}}$$

Where ΔI is the peak-to-peak inductor ripple current and $\Delta V_{IN}$ is the input voltage ripple.

### Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. For best results, use low-ESR capacitors to minimize the output voltage ripple.

The output capacitor's characteristics also affect system stability. For best results, use ceramic, tantalum, or low-ESR electrolytic capacitors. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is estimated as:

$$\Delta V_{OUT} \approx I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times F_{SW}}$$

Where $\Delta V_{OUT}$ is the output ripple voltage, $V_{IN}$ and $V_{OUT}$ are the DC input and output voltage, respectively, $I_{LOAD}$ is the load current, $F_{SW}$ is the switching frequency, and $C_{OUT}$ is the value of the output capacitor.

For tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, so the output ripple is estimated as:

$$\Delta V_{OUT} \approx I_{LOAD} \times \frac{1 - \frac{V_{IN}}{V_{OUT}}}{C_{OUT} \times F_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}}$$

Where $R_{ESR}$ is the equivalent series resistance of the output capacitors. Choose an output capacitor that satisfies the output ripple and load transient requirements of the design.

### Selecting the Inductor and Current Sensing Resistor

The inductor is required to transfer the energy between the input source and the output capacitors. A larger value inductor results in less ripple current that results in lower peak inductor current, and therefore reduces the stress on the power MOSFET. However, the larger value inductor has a larger physical size, higher series resistance, and lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Make sure that the peak inductor current is below 80% of the IC's maximum current limit at the operating duty cycle to prevent loss of regulation. Make sure that the inductor does not saturate under the worst-case load transient and startup


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conditions. The required inductance value can be calculated by:

$$L \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times F_{SW} \times \Delta I}$$

$$I_{IN} = \frac{V_{OUT} \times I_{LOAD}}{V_{IN} \times \eta}$$

$$\Delta I = (30\% - 50\%) \times I_{IN}$$

Where $I_{LOAD}$ is the load current, ΔI is the peak-to-peak inductor ripple current and η is the efficiency. For a typical design, boost converter efficiency can reach 85%~95%.

The switch current is usually used for the peak current mode control. In order to avoid hitting the current limit, the voltage across the sensing resistor $R_{SENSE}$ should be less than 80% of the worst case current limit voltage, 185mV.

$$R_{SENSE} = \frac{0.8 \times 0.185}{I_{L(PEAK)}}$$

Where $I_{L(PEAK)}$ is the peak value of the inductor current.

**Selecting the Power MOSFET**

The MP3910A is capable of driving a wide variety of N-Channel power MOSFETS. The critical parameters of selecting a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$
2. Maximum current, $I_{D(MAX)}$
3. On-resistance, $R_{DS(ON)}$
4. Gate source charge $Q_{GS}$ and gate drain charge $Q_{GD}$
5. Total gate charge, $Q_G$

Ideally, the off-state voltage across the MOSFET is equal to boost output voltage. Considering the voltage spike when it turns off, $V_{DS(MAX)}$ should be greater than 1.5 times of the output voltage.

The maximum current through the power MOSFET happens when the input voltage is minimum and the output power is maximum. The maximum RMS current through the MOSFET is given by:

$$I_{RMS} = I_{IN} \times \sqrt{\frac{V_{OUT} - V_{IN}}{V_{OUT}}}$$

The current rating of the MOSFET should be greater than 1.5 times $I_{RMS}$,

The on resistance of the MOSFET determines the conduction loss, which is given by:

$$P_{LOSS} = I_{RMS}^2 \times R_{DS(ON)} \times K$$

Where K is the on-resistance temperature coefficient of the MOSFET. So it is smaller, it is better.

The switching loss is related to $Q_{GD}$ and $Q_{GS1}$ which determine the commutation time. $Q_{GS1}$ is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the chart of $V_{GS}$ vs. $Q_G$ of the MOSFET datasheet. $Q_{GD}$ is the charge during the plateau voltage. These two parameters are needed to estimate the turn on and turn off loss.

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times F_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times F_{SW}$$

Where $V_{TH}$ is the threshold voltage, $V_{PLT}$ is the plateau voltage, $R_G$ is the gate resistance, $V_{DS}$ is the drain-source voltage. Please note that the switching loss is the most difficult part in the loss estimation. The formula above provides a simple physical expression.

On the other hand, small $Q_G$ will cause fast turn on/off speed which determines the spike and kick.

**Selecting the Diode**

The boost output rectifier diode supplies current to the inductor when the MOSFET is off. Use a Schottky diode to reduce losses due to the diode forward voltage and recovery time. The diode should be rated for a reverse voltage greater than the expected output voltage. The average current rating must exceed the maximum expected load current, and the peak current rating must exceed the peak inductor current.

**Boost Converter Compensation Design**

The output of the transconductance error amplifier (COMP) is used to compensate the regulation control system. The system uses two poles and one zero to stabilize the control loop. The poles are $F_{P1}$, which is set by the output capacitor ($C_{OUT}$) and load resistance, and $F_{P2}$ which starts from origin. The zero ($F_{Z1}$) is set by the compensation capacitor ($C_{COMP}$) and the compensation resistor ($R_{COMP}$). These parameters are determined by the equations:


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$$F_{P1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}}$$

$$F_{Z1} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}}$$

Where $R_{LOAD}$ is the load resistance.

The DC mid-band loop gain is:

$$A_{VDC} = \frac{0.5 \times G_{EA} \times V_{IN} \times R_{LOAD} \times V_{REF} \times R_{COMP}}{V_{OUT}^2 \times R_{SENSE} \times G_{SENSE}}$$

Where $V_{REF}$ is the voltage reference, 1.237V. $G_{SENSE}$ is the current sense amplifier gain and $G_{EA}$ is the error amplifier transconductance.

The ESR zero in this example locates at very high frequency. Therefore, it is not taken into design consideration.

There is also a right-half-plane zero ($F_{RHPZ}$) that exists in continuous conduction mode (inductor current does not drop to zero on each cycle) step-up converters. The frequency of the right half plane zero is:

$$F_{RHPZ} = \frac{V_{IN}^2 \times R_{LOAD}}{2 \times \pi \times L \times V_{OUT}^2}$$

The right-half-plane zero increases the gain and reduces the phase simultaneously, which results in smaller phase margin and gain margin. The worst case happens at the condition of minimum input voltage and maximum output power.

In order to achieve system stability, $F_{z1}$ is placed close to $F_{P1}$ to cancel the pole. $R_{COMP}$ is adjusted to change the voltage gain. Make sure the bandwidth $F_C$ is about 1/10 of the lower one of the ESR zero and the right-half-plane zero.

$$\frac{1}{2 \times \pi \times C_{OUT} \times R_{LOAD}} = \frac{1}{2 \times \pi \times C_{COMP} \times R_{COMP}}$$

$$R_{COMP} = \frac{V_{OUT}^2 \times 2 \times \pi \times C_{OUT} \times F_C \times R_{SENSE} \times G_{SENSE}}{G_{EA} \times V_{REF} \times V_{IN}}$$

Based on these equations, $R_{COMP}$ and $C_{COMP}$ can be solved.

In cases where the ESR zero is in a relatively low frequency region and results in insufficient gain margin, an optional capacitor ($C_{POLE}$) should be added between COMP pin and GND. Then a pole, formed by $C_{POLE}$ and $R_{COMP}$, should be placed at the ESR zero to cancel the adverse effect.

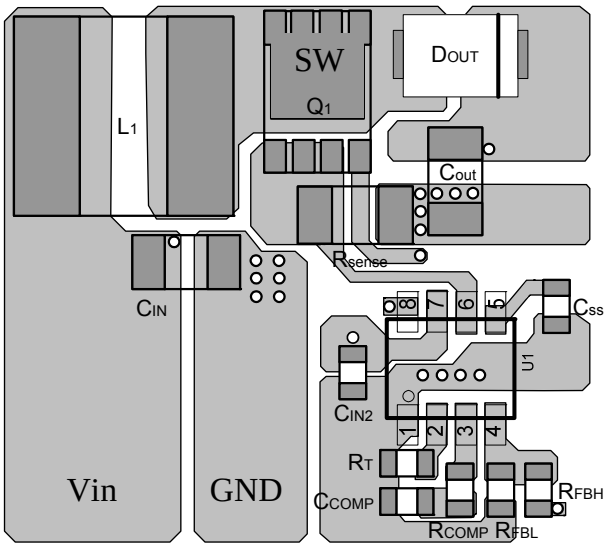
$$C_{POLE} = \frac{1}{2 \times \pi \times R_{COMP} \times F_{ESRZ}}$$

**PCB Layout Guide**

High frequency switching regulators require very careful layout for stable operation and low noise. For boost topology layout:

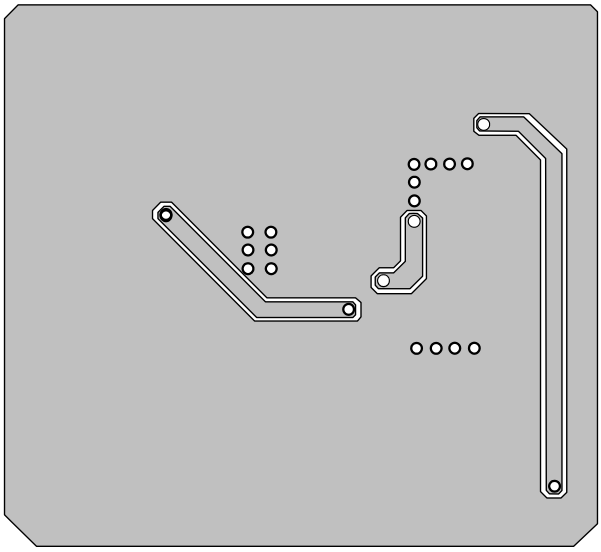
1. Keep the high current path as short as possible between the MOSFET drain, output diode, output capacitor and current sense resistor for minimal noise and ringing.
2. The VCC capacitor must be placed close to the VCC pin for best decoupling.
3. All feedback components must be kept close to the FB pin to prevent noise injection on the FB pin trace.
4. The ground return of the input and output capacitors should be tied to the GND pin with single point connection.

Refer to Figure 3 for boost layout, which is referenced to schematic in Figure 5




Top Layer


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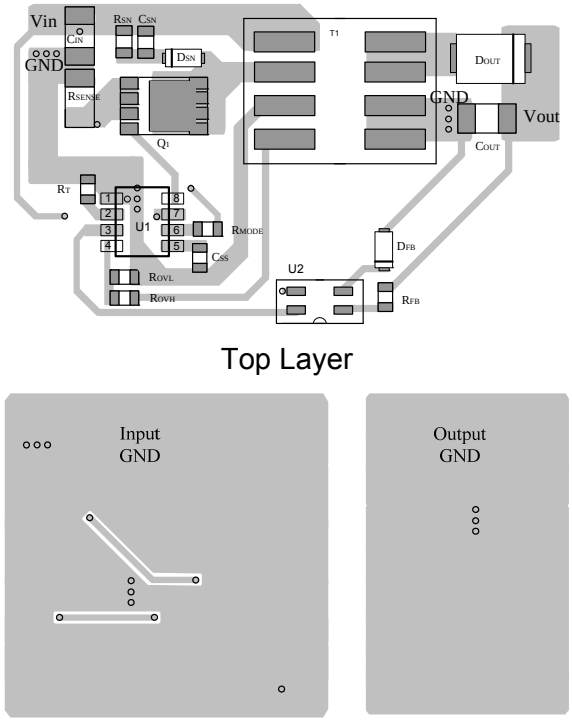
Bottom Layer

**Figure 3: Boost PCB Layout**

For flyback topology PCB layout:

1. Keep the input loop as short as possible between input cap, transformer, MOSFET, current sense resistor and GND plane for minimal noise and ringing.
2. Keep the output loop between rectifier diode, output cap and transformer as short as possible.
3. The clamp loop circuit between $D_{SN}$, $C_{SN}$ and transformer should be as small as possible
4. The VCC capacitor must be placed close to the VCC pin for best decoupling.
5. The feedback trace should be far away from noise source such as drain of power FET.
6. Use single point connection between power GND and signal GND.

Refer to Figure 4 for flyback layout, which is referenced to schematic on page 1 (excluding the snubber). For more detail information, refer to flyback EVB datasheet.




Top Layer

Bottom Layer

**Figure 4: Fly-back PCB Layout**

## Design Example

Below is a design example following the application guidelines for the specifications:

**Table 1: Boost Design Example**

| | |
|---|---|
| $V_{IN}$ | 9-14V |
| $V_{OUT}$ | 24V |
| $f_{SW}$ | 300kHz |

The detailed application schematic is shown in Figure 6. And there is another design example for fly-back application in Figure 7.

**Table 2: Fly-back Design Example**

| | |
|---|---|
| $V_{IN}$ | 36-72V |
| $V_{OUT}$ | 12V |
| $f_{SW}$ | 250kHz |

The typical performance and circuit waveforms of flyback have been shown in the Typical Performance Characteristics section.


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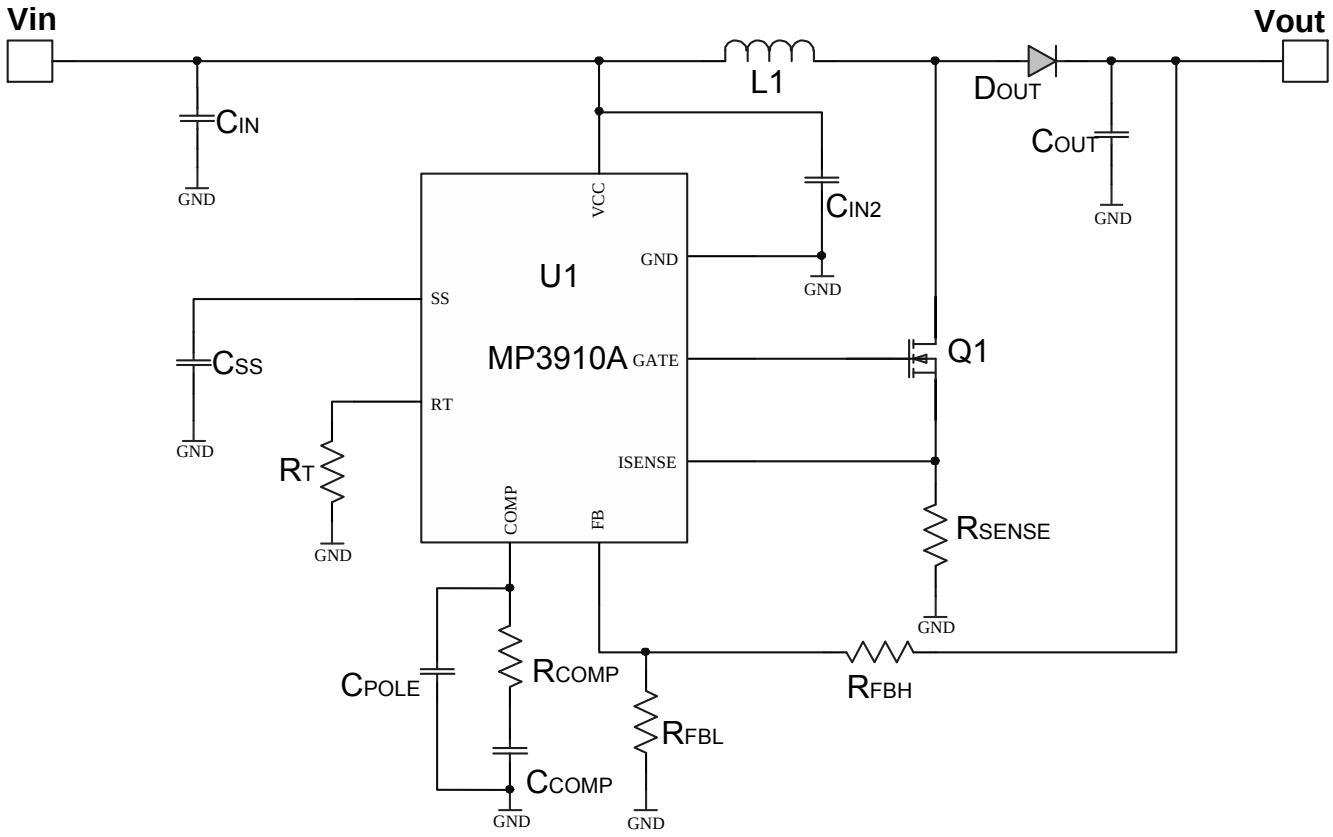



**Figure 5: Boost Design Reference Schematic**


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## TYPICAL APPLICATION CIRCUITS

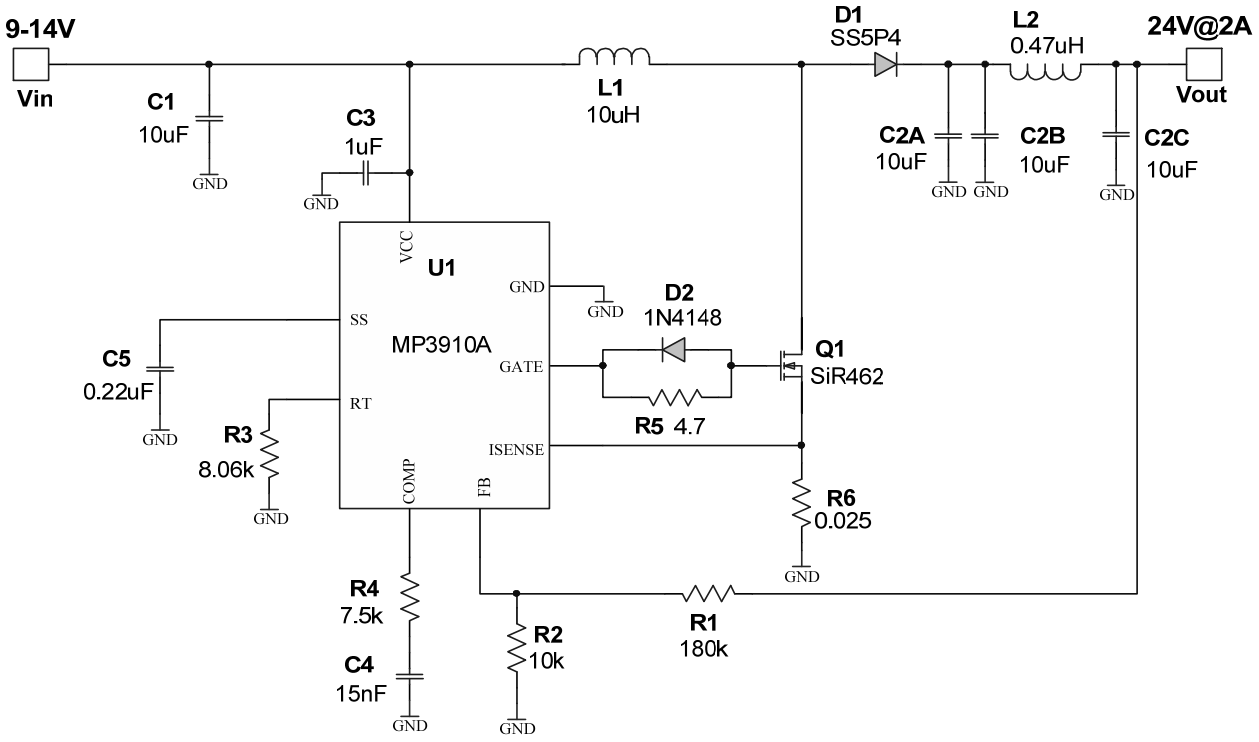



**Figure 6: Typical Boost Converter Application Schematic**

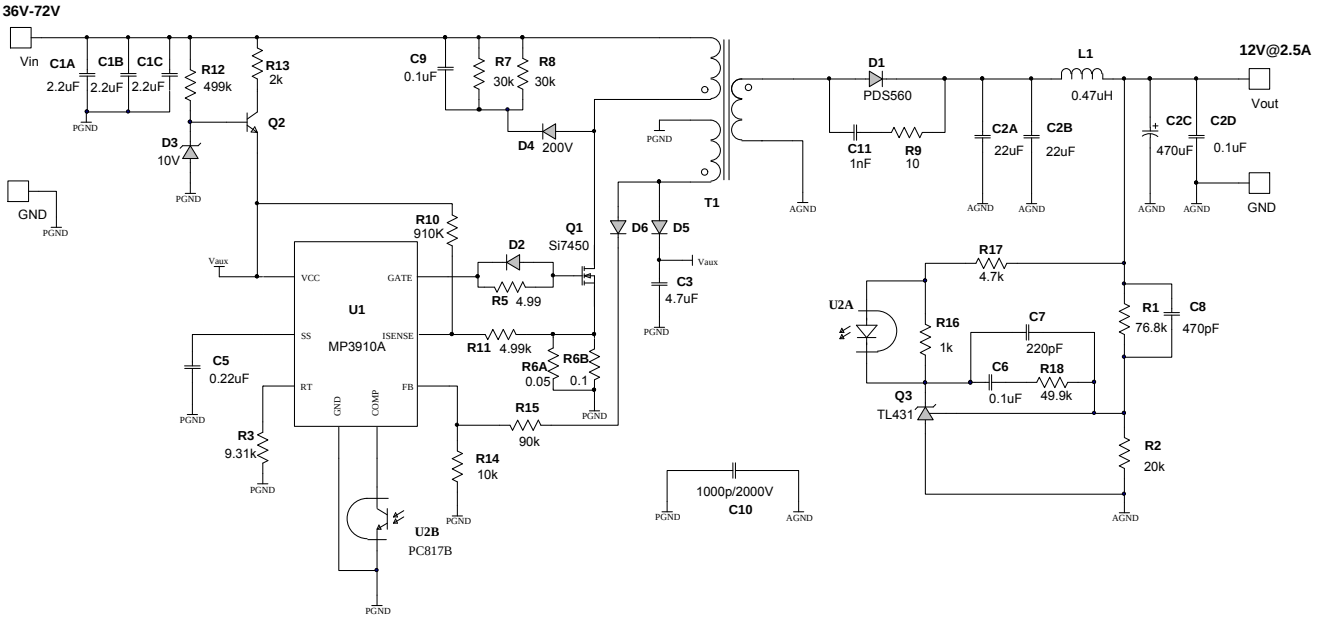



**Figure 7: Typical Fly-back Converter Application Schematic**


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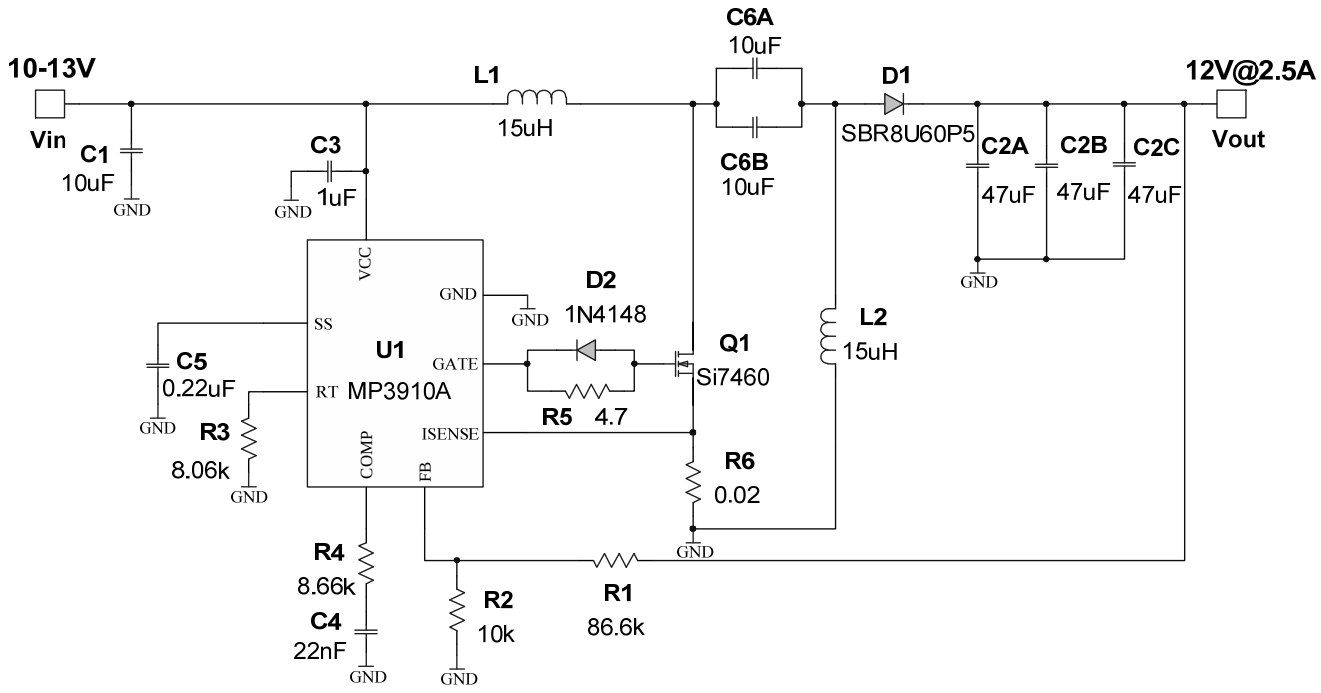



**Figure 8: Typical Sepic Converter Application Schematic**

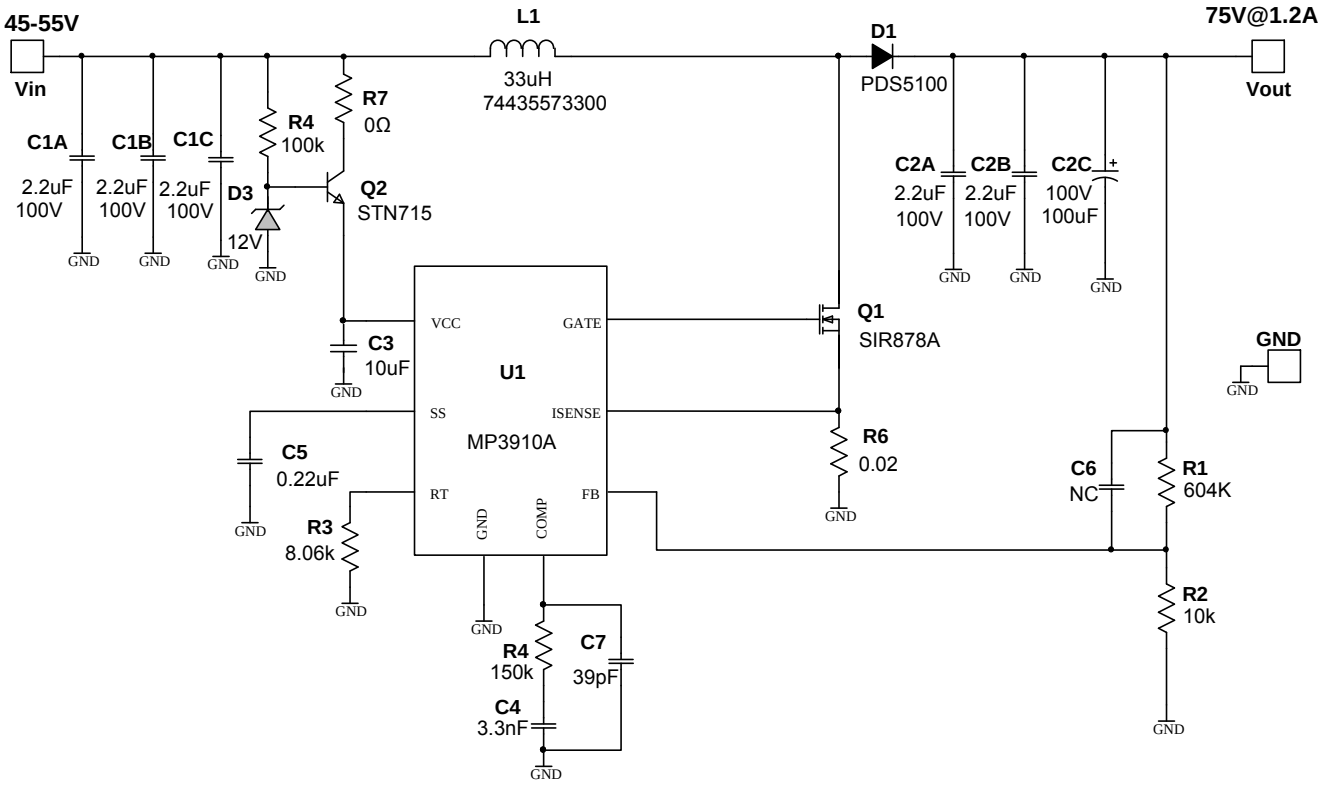
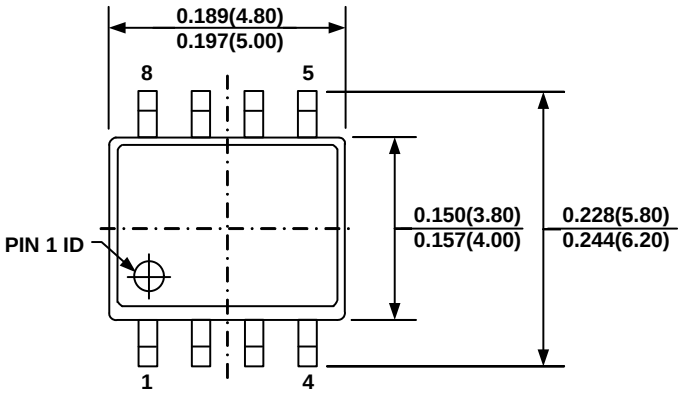



**Figure 9: High-voltage Input Boost Application Schematic**

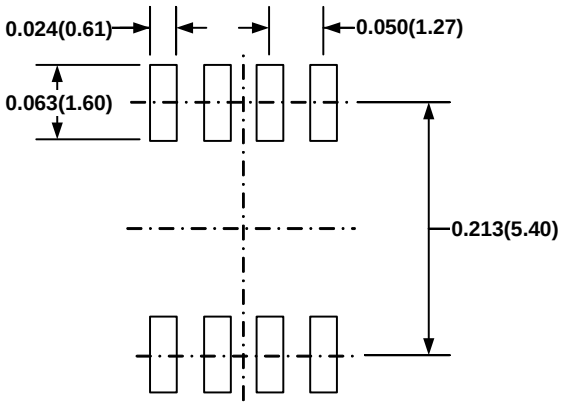

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## PACKAGE INFORMATION

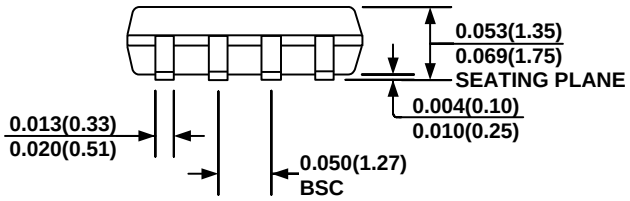
### SOIC-8



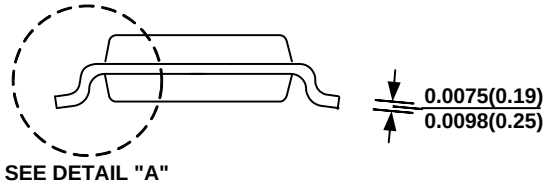

TOP VIEW



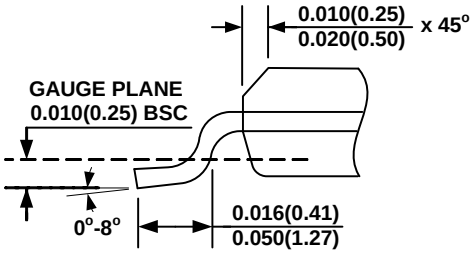

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW




DETAIL "A"

**NOTE:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
6) DRAWING IS NOT TO SCALE.

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