

ECOSPARK[®] Ignition IGBT

500 mJ, 360 V, N-Channel Ignition IGBT

**ISL9V5036S3ST,
ISL9V5036P3-F085,
ISL9V5036S3ST-F085C**

General Description

The ISL9V5036S3ST, ISL9V5036S3ST-F085C and ISL9V5036P3-F085 are the next generation IGBTs that offer outstanding SCIS capability in the D²-Pak (TO-263) and TO-220 plastic package. These devices are intended for use in automotive ignition circuits, specifically as coil drivers. Internal diodes provide voltage clamping without the need for external components.

ECOSPARK devices can be custom made to specific clamp voltages. Contact your nearest onsemi sales office for more information.

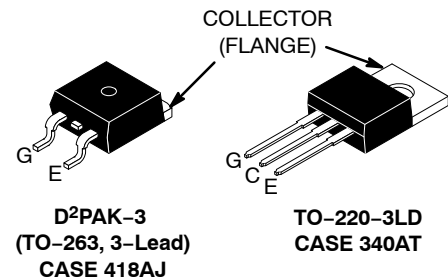
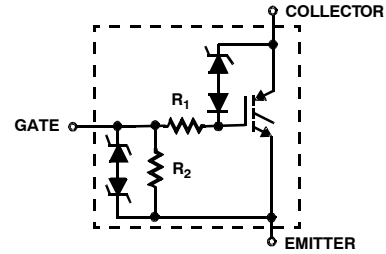
Formerly Developmental Type 49443.

Features

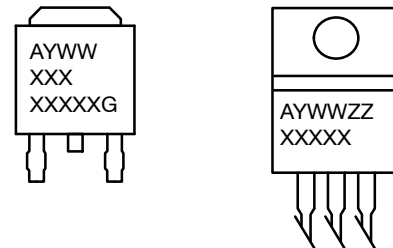
- Industry Standard D²-Pak package
- SCIS Energy = 500 mJ at T_J = 25°C
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Ignition Coil Driver Circuits
- Coil-On Plug Applications



MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
XXXX	= Device Code
ZZ	= Assembly Lot Number
G	= Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

ISL9V5036S3ST, ISL9V5036P3–F085, ISL9V5036S3ST–F085C

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Collector to Emitter Breakdown Voltage (I _C = 1 mA)	BV _{CER}	390	V
Emitter to Collector Voltage – Reverse Battery Condition (I _C = 10 mA)	BV _{ECS}	24	V
At Starting T _J = 25°C, I _{SCIS} = 38.5A, L = 670 µHy	E _{SCIS25}	500	mJ
At Starting T _J = 150°C, I _{SCIS} = 30A, L = 670 µHy	E _{SCIS150}	300	mJ
Collector Current Continuous, at T _C = 25°C, See Figure 9	I _{C25}	46	A
Collector Current Continuous, at T _C = 110°C, See Figure 9	I _{C110}	31	A
Gate to Emitter Voltage Continuous	V _{GEM}	±10	V
Power Dissipation Total T _C = 25°C	P _D	250	W
Power Dissipation Derating T _C > 25°C		1.67	W/°C
Operating Junction Temperature Range	T _J	–40 to 175	°C
Storage Junction Temperature Range	T _{STG}	–40 to 175	°C
Max Lead Temp for Soldering (Leads at 1.6 mm from Case for 10 s)	T _L	300	°C
Max Lead Temp for Soldering (Package Body for 10s)	T _{pkg}	260	°C
Electrostatic Discharge Voltage at 100 pF, 1500 Ω	ESD	4	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction–Case	R _{θJC}	0.6	°C/W

ISL9V5036S3ST, ISL9V5036P3–F085, ISL9V5036S3ST–F085C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
OFF STATE CHARACTERISTICS							
Collector to Emitter Breakdown Voltage	BV _{CER}	I _C = 2 mA, V _{GE} = 0 V, R _G = 1 kΩ, See Figure 15 T _J = −40 to 150°C	330	360	390	V	
Collector to Emitter Breakdown Voltage	BV _{CES}	I _C = 10 mA, V _{GE} = 0 V, R _G = 0, See Figure 15 T _J = −40 to 150°C	360	390	420	V	
Emitter to Collector Breakdown Voltage	BV _{ECS}	I _C = −75 mA, V _{GE} = 0 V, T _J = 25°C	30	–	–	V	
Gate to Emitter Breakdown Voltage	BV _{GES}	I _{GES} = ±2 mA	±12	±14	–	V	
Collector to Emitter Leakage Current	I _{CER}	V _{CER} = 250 V, R _G = 1 kΩ, See Figure 11	T _C = 25°C	–	–	25	μA
			T _C = 150°C	–	–	1	mA
Emitter to Collector Leakage Current	I _{ECS}	V _{EC} = 24 V, See Figure 11	T _C = 25°C	–	–	1	mA
			T _C = 150°C	–	–	40	
Series Gate Resistance	R ₁		–	75	–	Ω	
Gate to Emitter Resistance	R ₂		10	–	30	kΩ	

ON STATE CHARACTERISTICS

Collector to Emitter Saturation Voltage	V _{CE(SAT)}	I _C = 10 A, V _{GE} = 4.0 V	T _C = 25°C See Figure 4	–	1.17	1.60	V
Collector to Emitter Saturation Voltage	V _{CE(SAT)}	I _C = 15 A, V _{GE} = 4.5 V	T _C = 150°C	–	1.50	1.80	V

DYNAMIC CHARACTERISTICS

Gate Charge	Q _{G(ON)}	I _C = 10 A, V _{CE} = 12 V, V _{GE} = 5 V, See Figure 14		–	32	–	nC
Gate to Emitter Threshold Voltage	V _{GE(TH)}	I _{CE} = 1.0 mA, V _{CE} = V _{GE} , See Figure 10	T _C = 25°C	1.3	–	2.2	V
			T _C = 150°C	0.75	–	1.8	
Gate to Emitter Plateau Voltage	V _{GEP}	I _C = 10 A, V _{CE} = 12 V		–	3.0	–	V

SWITCHING CHARACTERISTICS

Current Turn–On Delay Time–Resistive	t _{d(ON)R}	V _{CE} = 14 V, R _L = 1 Ω V _{GE} = 5 V, R _G = 1 kΩ T _J = 25°C, See Figure 12	–	0.7	4	μs
Current Rise Time–Resistive	t _{rR}		–	2.1	7	
Current Turn–Off Delay Time–Inductive	t _{d(OFF)L}	V _{CE} = 300 V, L = 2 mH, V _{GE} = 5 V, R _G = 1 kΩ T _J = 25°C, See Figure 12	–	10.8	15	
Current Fall Time–Inductive	t _{fL}		–	2.8	15	
Self Clamped Inductive Switching	SCIS	T _J = 25°C, L = 670 μH, R _G = 1 kΩ, V _{GE} = 5 V, See Figures 1, 2	–	–	500	mJ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

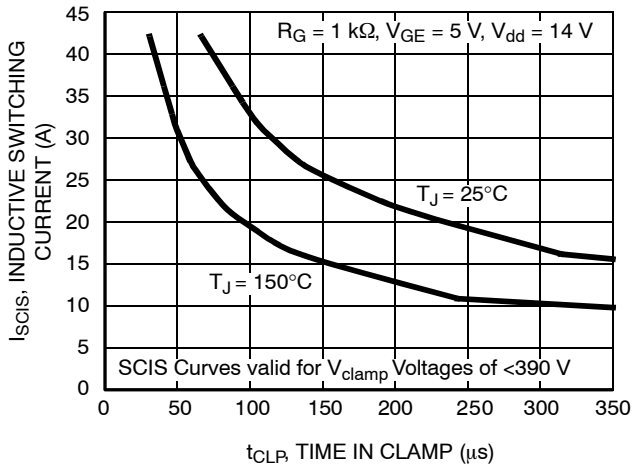


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

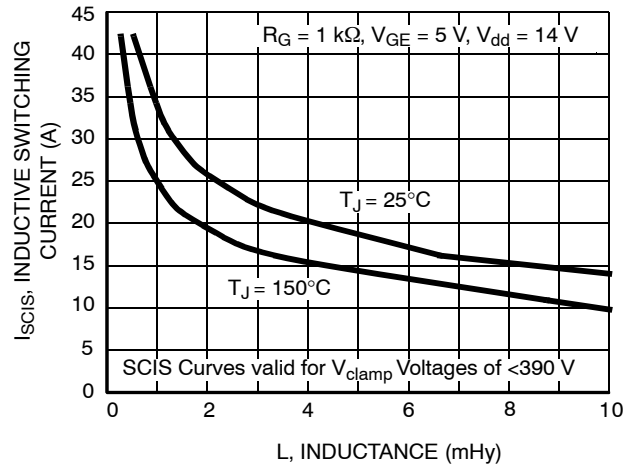


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

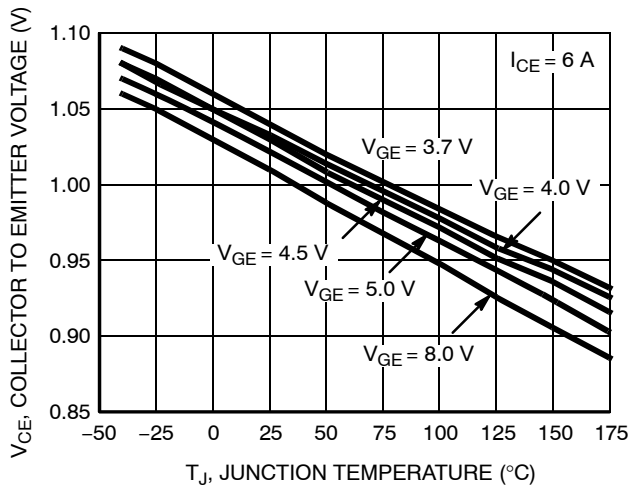


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

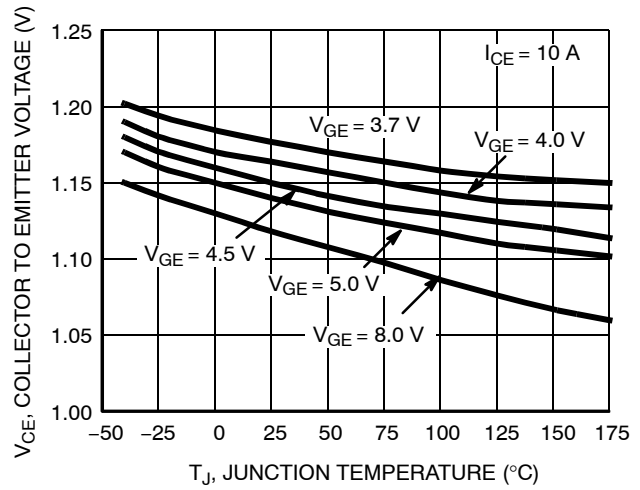


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

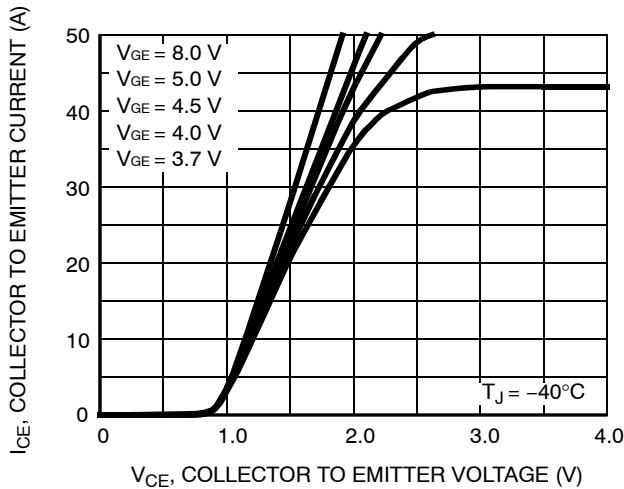


Figure 5. Collector Current vs. Collector to Emitter On-State Voltage

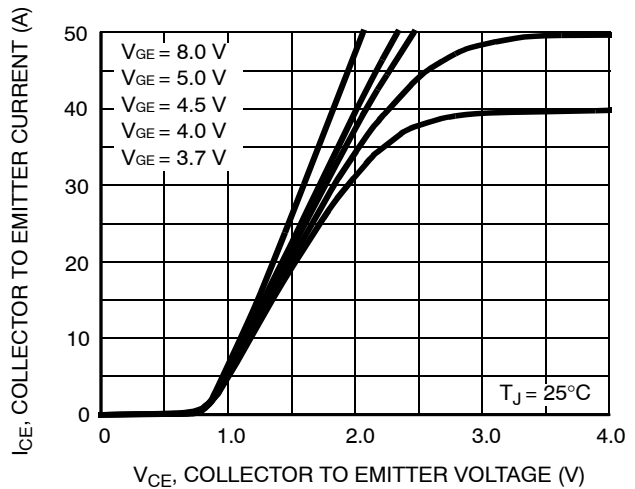


Figure 6. Collector Current vs. Collector to Emitter On-State Voltage

TYPICAL CHARACTERISTICS (continued)

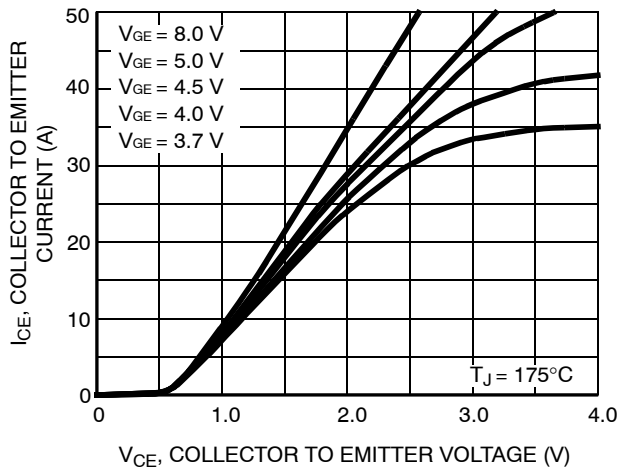


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

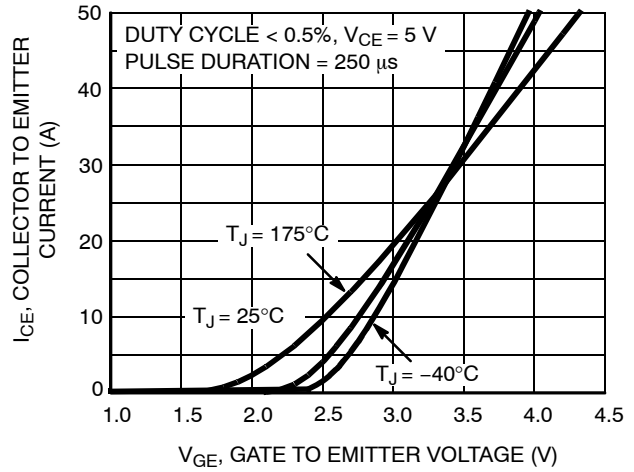


Figure 8. Transfer Characteristics

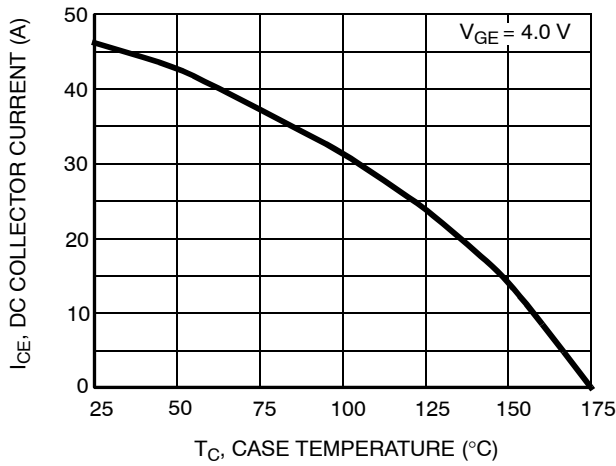


Figure 9. DC Collector Current vs. Case Temperature

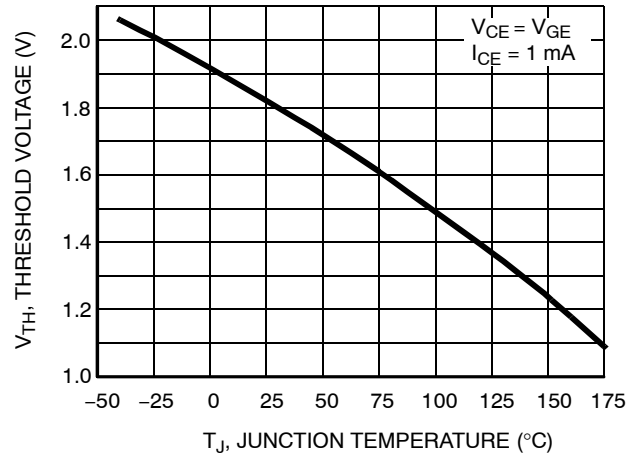


Figure 10. Threshold Voltage vs. Junction Temperature

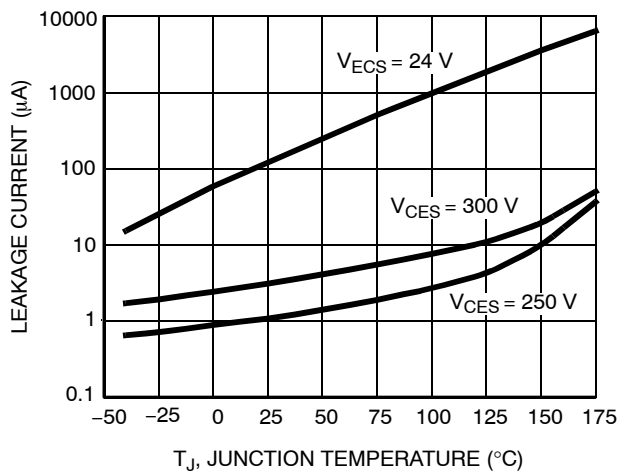


Figure 11. Leakage Current vs. Junction Temperature

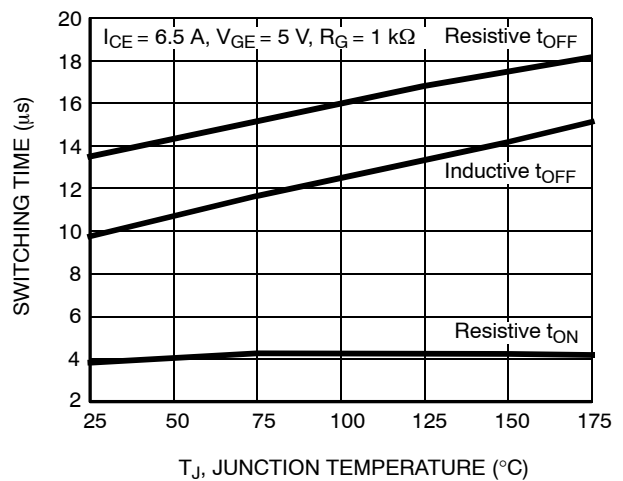


Figure 12. Switching Time vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

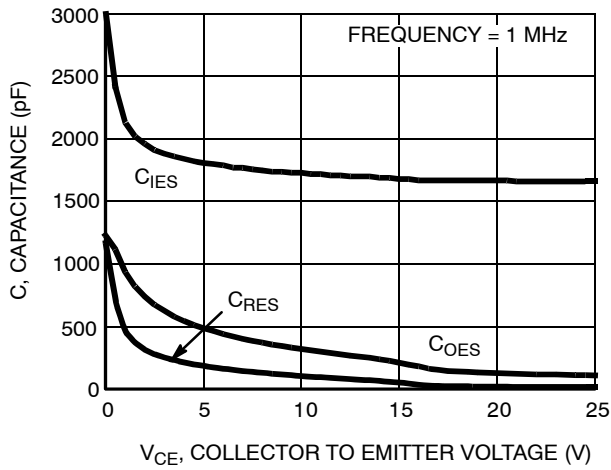


Figure 13. Capacitance vs. Collector to Emitter Voltage

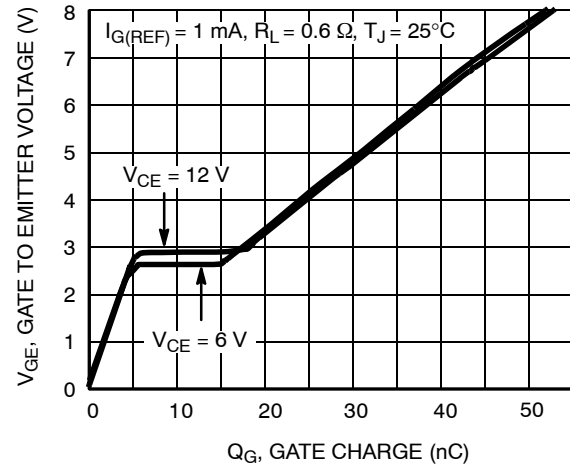


Figure 14. Gate Charge

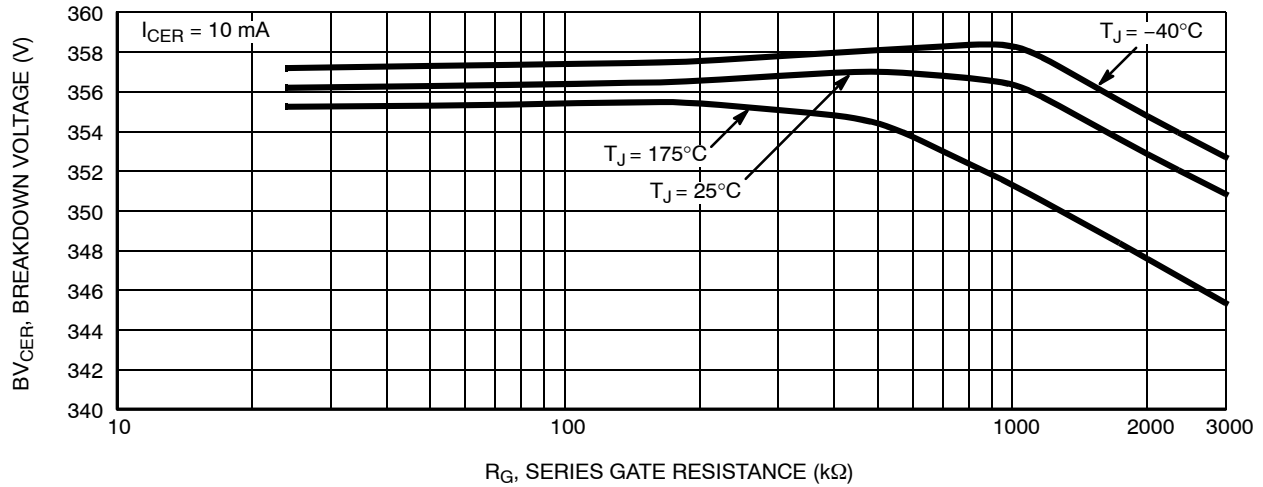


Figure 15. Breakdown Voltage vs. Series Gate Resistance

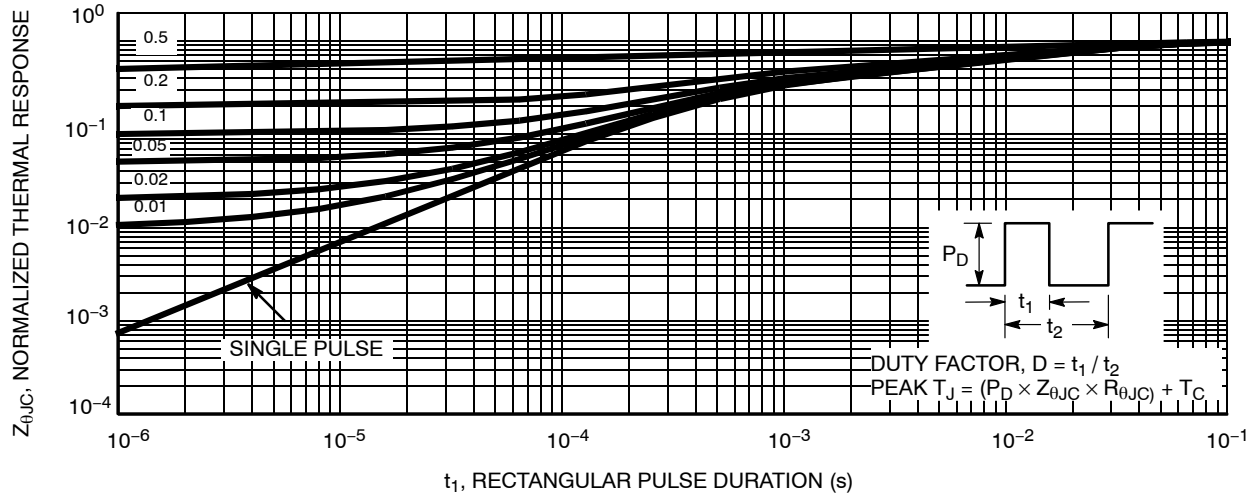


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TEST CIRCUITS AND WAVEFORMS

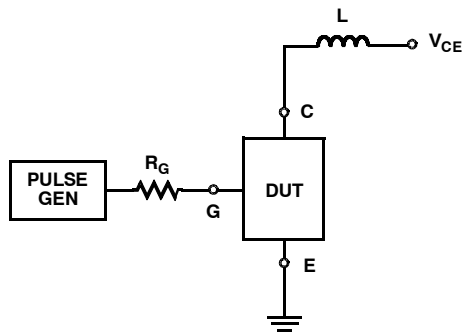


Figure 17. Inductive Switching Test Circuit

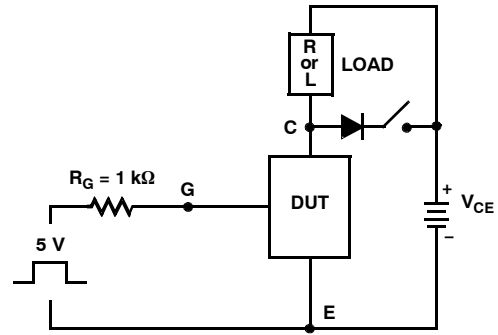


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

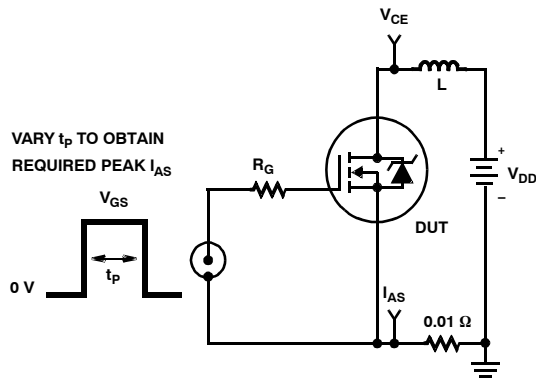


Figure 19. Energy Test Circuit

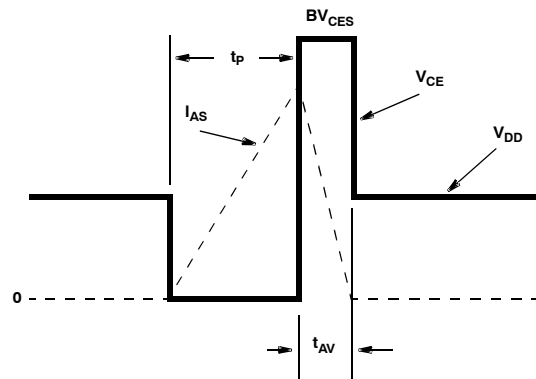


Figure 20. Energy Waveforms

ISL9V5036S3ST, ISL9V5036P3–F085, ISL9V5036S3ST–F085C

SPICE THERMAL MODEL

ISL9V5036S3ST / ISL9V5036P3–F085 / ISL9V5036S3ST–F085C

```
CTHERM1 th 6 4.0e2
CTHERM2 6 5 3.6e-3
CTHERM3 5 4 4.9e-2
CTHERM4 4 3 3.2e-1
CTHERM5 3 2 3.0e-1
CTHERM6 2 tl 1.6e-2
```

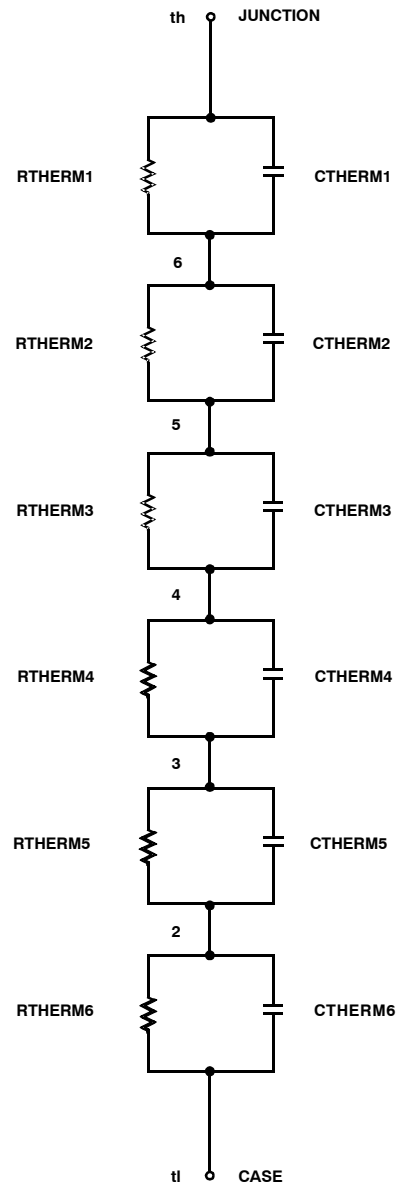
```
RTHERM1 th 6 1.0e-2
RTHERM2 6 5 1.4e-1
RTHERM3 5 4 1.0e-1
RTHERM4 4 3 9.0e-2
RTHERM5 3 2 9.4e-2
RTHERM6 2 tl 1.9e-2
```

SABER THERMAL MODEL

SABER thermal model

ISL9V5036S3ST / ISL9V5036P3–F085 / ISL9V5036S3ST–F085C

```
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 = 4.0e2
  ctherm.ctherm2 6 5 = 3.6e-3
  ctherm.ctherm3 5 4 = 4.9e-2
  ctherm.ctherm4 4 3 = 3.2e-1
  ctherm.ctherm5 3 2 = 3.0e-1
  ctherm.ctherm6 2 tl = 1.6e-2
  rtherm.rtherm1 th 6 = 1.0e-2
  rtherm.rtherm2 6 5 = 1.4e-1
  rtherm.rtherm3 5 4 = 1.0e-1
  rtherm.rtherm4 4 3 = 9.0e-2
  rtherm.rtherm5 3 2 = 9.4e-2
  rtherm.rtherm6 2 tl = 1.9e-2
}
```



PACKAGE MARKING AND ORDERING INFORMATION

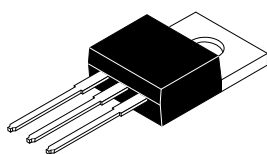
Device	Device Marking	Package	Shipping†
ISL9V5036S3ST	V5036S	D2PAK–3 (TO–263, 3–Lead) (Pb–Free)	800 / Tape & Reel
ISL9V5036S3ST–F085C	V5036SC	D2PAK–3 (TO–263, 3–Lead) (Pb–Free)	800 / Tape & Reel
ISL9V5036P3–F085	V5036P	TO–220–3LD (Pb–Free)	50 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

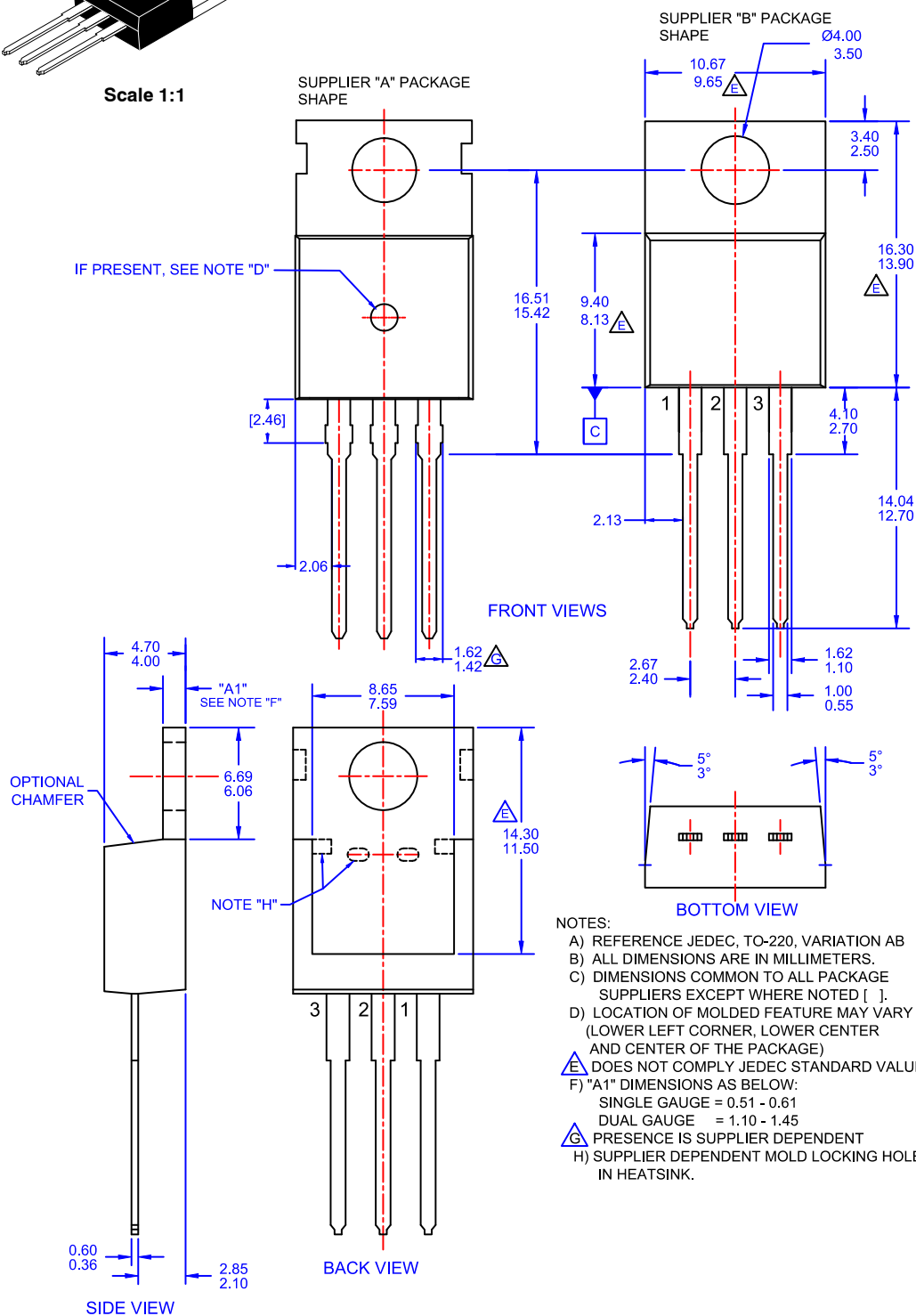
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Scale 1:1

TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017



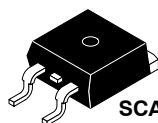
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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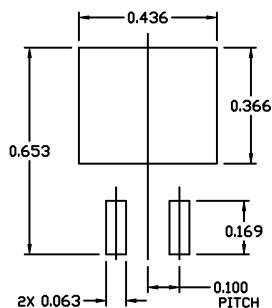
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D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

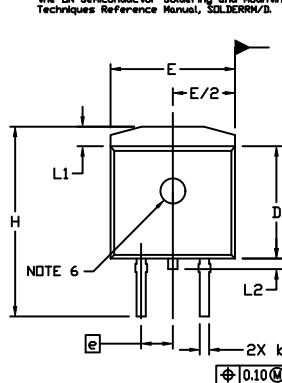
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

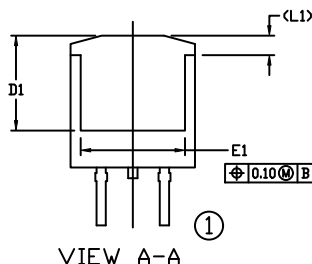
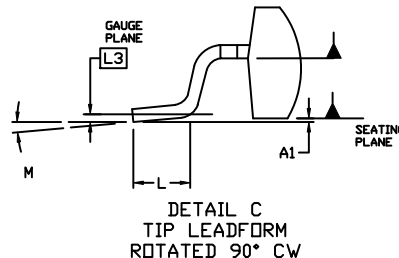
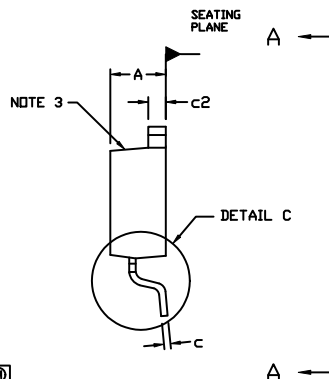
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



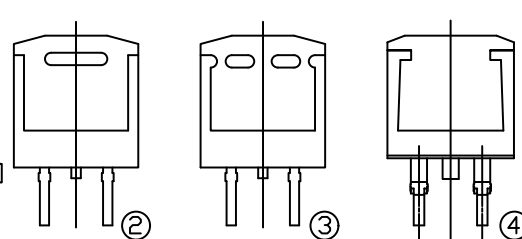
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

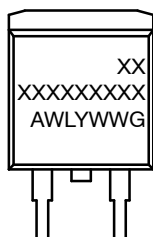


VIEW A-A

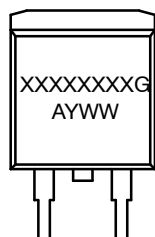


VIEW A-A
OPTIONAL CONSTRUCTIONS

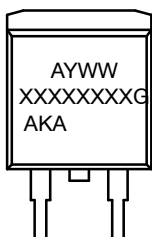
GENERIC MARKING DIAGRAMS*



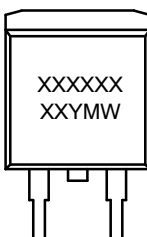
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot
 Y = Year
 WW = Work Week
 W = Week Code (SSG)
 M = Month Code (SSG)
 G = Pb-Free Package
 AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D ² PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

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