MP1477

17V, 3A, 800kHz, High-Efficiency, Synchronous, Step-Down Converter with COT Control in SOT563 Package

DESCRIPTION

The MP1477 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP1477 offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range. The MP1477 uses synchronous mode operation for higher efficiency over the output current-load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1477 requires a minimal number of readily available, standard, external components and is available in a space-saving SOT563 (1.6mmx1.6mm) package.

FEATURES

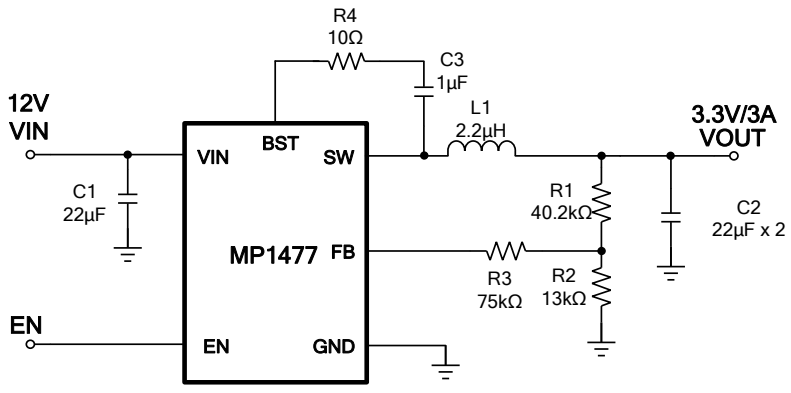
- Wide 4.2V to 17V Operating Input Range
- 58mΩ/27mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 200μA Low I_Q Current
- High-Efficiency Synchronous Mode Operation
- Power Save Mode (PSM) at Light Load
- Fast Load Transient Response
- 800kHz Switching Frequency
- Internal Soft Start (SS)
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a SOT563 (1.6mmx1.6mm) Package

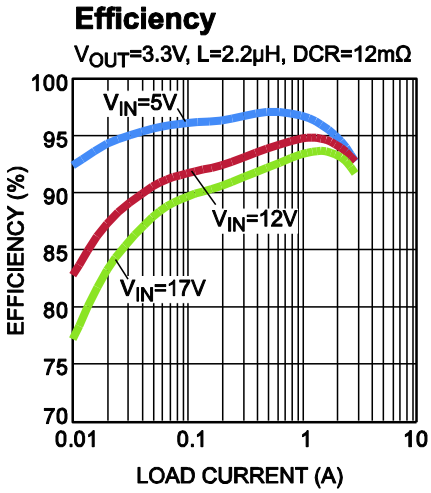
APPLICATIONS

- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1477GTF	SOT563 (1.6mmx1.6mm)	*See Below*

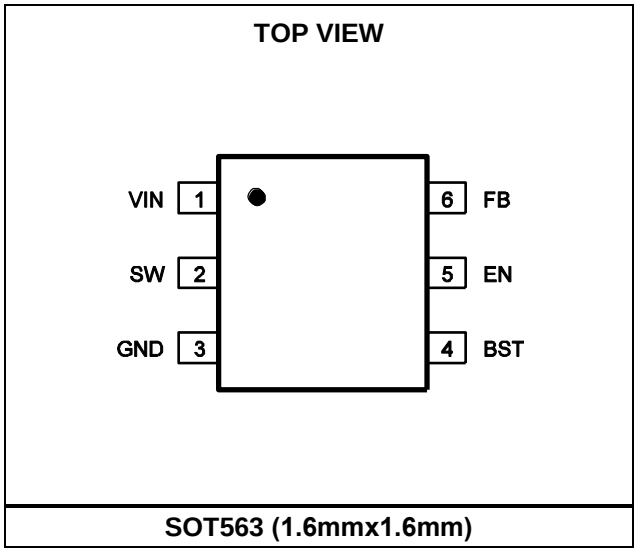
* For Tape & Reel, add suffix –Z (e.g. MP1477GTF–Z)

TOP MARKING

AUCY
LLL

AUC: Product code of MP1477GTF
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



SOT563 (1.6mmx1.6mm)

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ABSOLUTE MAXIMUM RATINGS (1)

VIN ..... -0.3V to 18V
V_{SW} ..... -0.6V (-6.5V for <10ns) to VIN + 0.3V (19V for <10ns)
V_{BST} ..... V_{SW} + 5V
V_{EN} ..... -0.3V to 5V (2)
All other pins..... -0.3V to 5V
Continuous power dissipation (T_A = +25°C) (3)(5) 2.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (VIN)..... 4.2V to 17V
Output voltage (V_{OUT})..... 0.8V to V_{IN} x D_{MAX} or 10V max
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance

SOT563	θ_{JA}	θ_{JC}	
EV1477-TF-00A (5)	55	21	°C/W
JESD51-7 (6)	130	60	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, please refer to the EN Control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV1477-TF-00A, 2-layer PCB.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to +125°C [7], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.85V	170	200	240	μA
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		58		mΩ
LS switch on resistance	$LS_{RDS(ON)}$			27		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			10	μA
Valley current limit	I_{LIMIT}	V_{OUT} = 0V	2.7	4	5.8	A
ZCD	I_{ZCD}	V_{OUT} = 3.3V, Lo = 2.2μH, I_{OUT} = 0A	-250	20	250	mA
Oscillator frequency	f_{SW}	V_{FB} = 0.75V	600	800	1000	kHz
Minimum on time [8]	T_{ON_MIN}			45		ns
Minimum off time [8]	T_{OFF_MIN}			180		ns
Feedback voltage	V_{REF}	T_J = +25°C	793	805	817	mV
		T_J = -40°C to 125°C	789	805	821	mV
Feedback current	I_{FB}			10	100	nA
FB UV threshold (H to L)	V_{UV_th}	Hiccup entry		75%		V_{REF}
Hiccup duty cycle [8]	D_{Hiccup}			25		%
EN rising threshold	V_{EN_RISING}		1.14	1.2	1.26	V
EN hysteresis	V_{EN_HYS}			100		mV
EN input current	I_{EN}	V_{EN} = 2V		2		μA
VIN under-voltage lockout threshold rising	$INUV_{Vth}$		3.7	4	4.18	V
VIN under-voltage lockout threshold hysteresis	$INUV_{HYS}$			330		mV
Soft-start period	T_{SS}		1.6	2.5	3	ms
Thermal shutdown [8]	TSD			150		°C
Thermal hysteresis [8]	TSD_{HYS}			20		°C

NOTES:

7) Guaranteed by over-temperature correlation, not tested in production.
8) Guaranteed by design and engineering sample characterization.

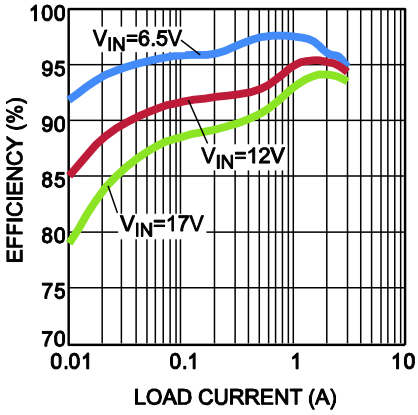
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TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

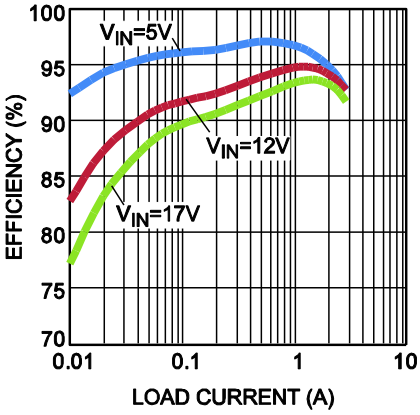
Efficiency

V_{OUT}=5V, L=3.3µH, DCR=9mΩ



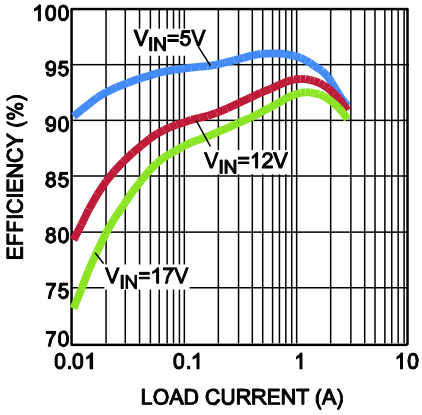
Efficiency

V_{OUT}=3.3V, L=2.2µH, DCR=12mΩ



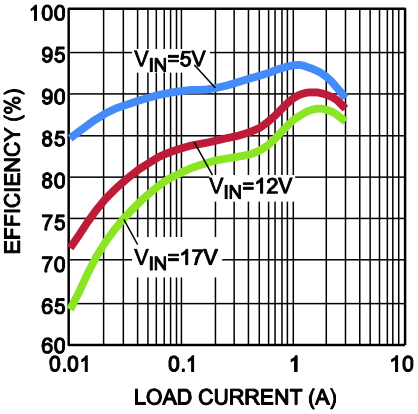
Efficiency

V_{OUT}=2.5V, L=2.2µH, DCR=12mΩ



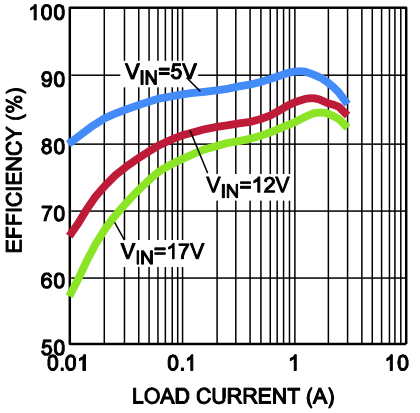
Efficiency

V_{OUT}=1.8V, L=1.5µH, DCR=4.3mΩ



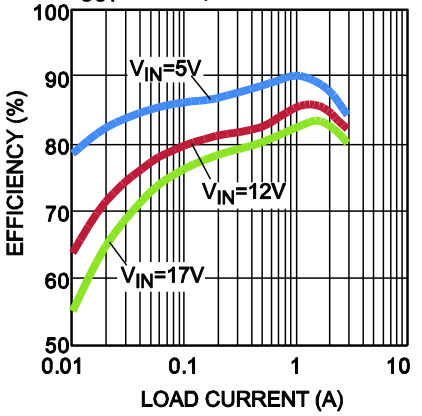
Efficiency

V_{OUT}=1.2V, L=1µH, DCR=4.6mΩ

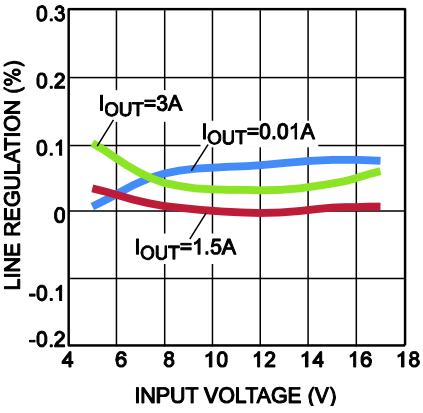


Efficiency

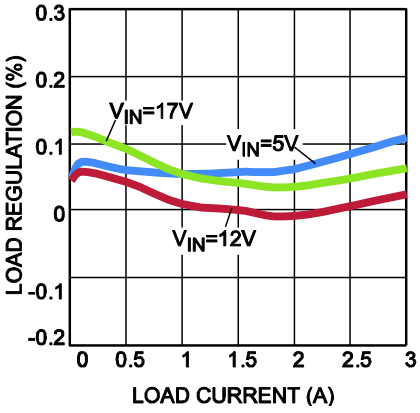
V_{OUT}=1V, L=1µH, DCR=4.6mΩ



Line Regulation

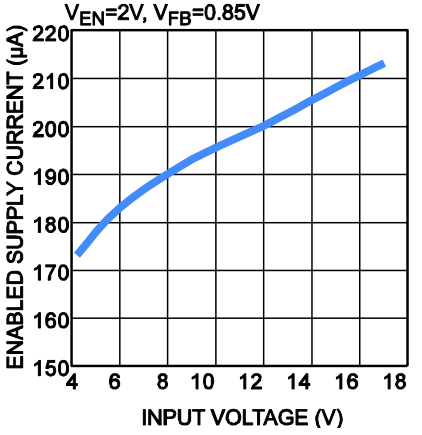


Load Regulation



Enabled Supply Current vs. Input Voltage

V_{EN}=2V, V_{FB}=0.85V



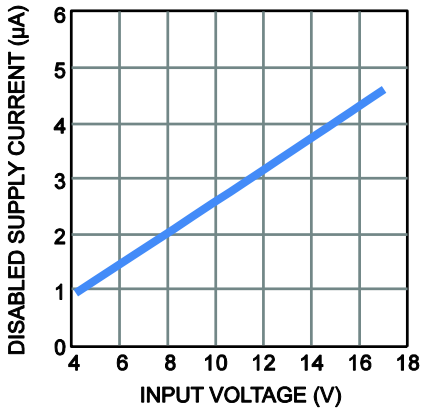
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 3.3V, L = 2.2µH, T_A = +25°C, unless otherwise noted.

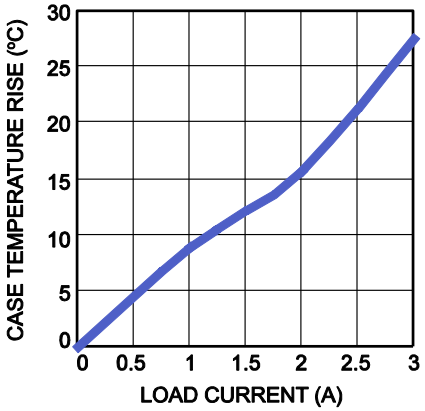
Disabled Supply Current vs. Input Voltage

V_{EN}=0V



Case Temperature Rise vs. Load Current

T_A=25°C, Board Size: 6.3cm x 4.7cm

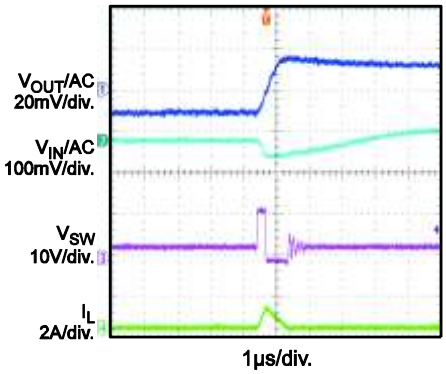


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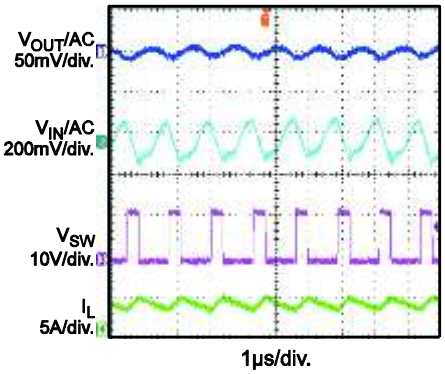
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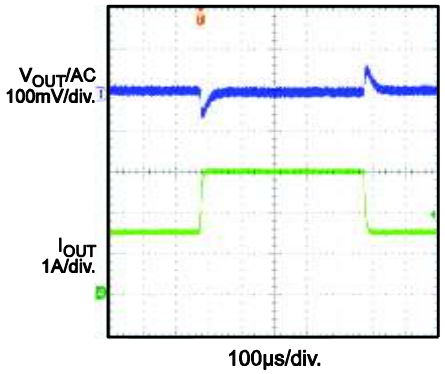
Input/Output Ripple
I_{OUT} = 0A



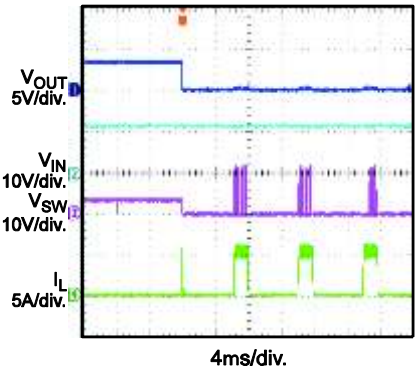
Input/Output Ripple
I_{OUT} = 3A



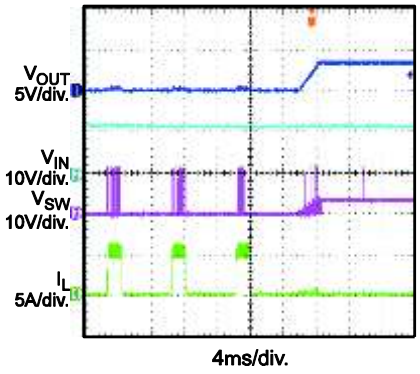
Transient Response
I_{OUT} = 1.5A to 3A, 2.5A/µs



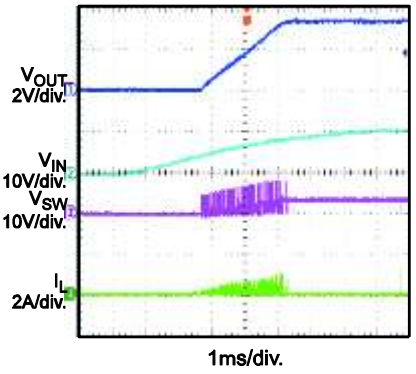
Short-Circuit Entry
I_{OUT} = 0A



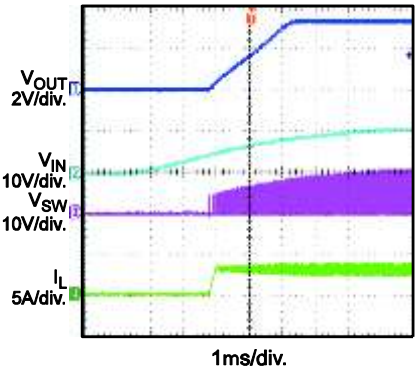
Short-Circuit Recovery
I_{OUT} = 0A



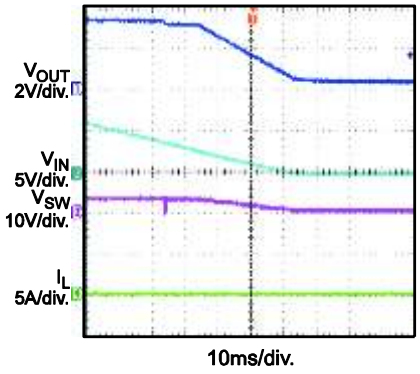
Start-Up through Input Voltage
I_{OUT} = 0A



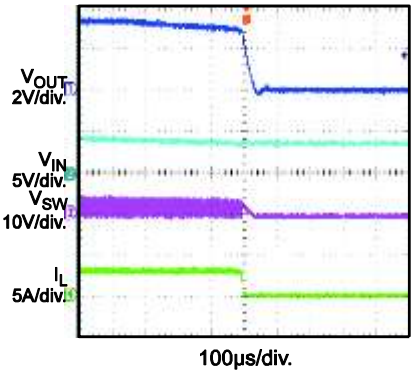
Start-Up through Input Voltage
I_{OUT} = 3A



Shutdown through Input Voltage
I_{OUT} = 0A



Shutdown through Input Voltage
I_{OUT} = 3A



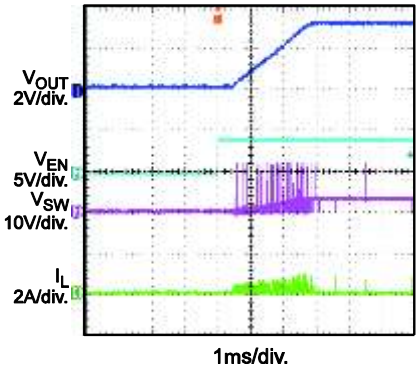
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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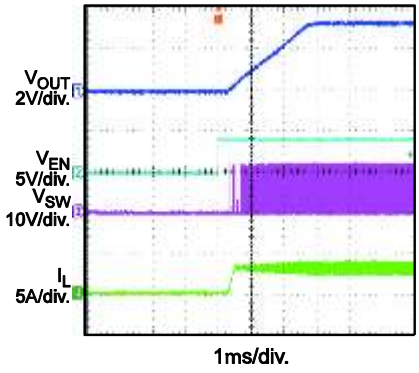
Start-Up through Enable

I_{OUT} = 0A



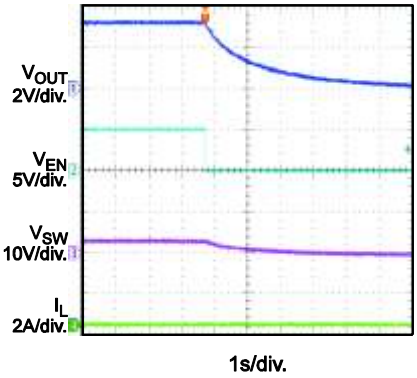
Start-Up through Enable

I_{OUT} = 3A



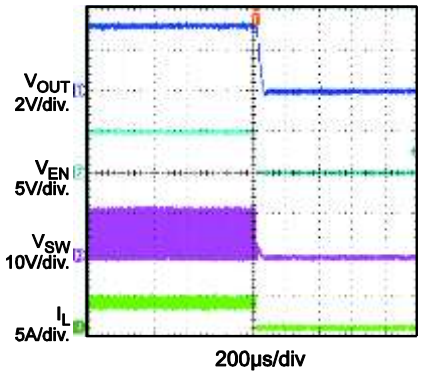
Shutdown through Enable

I_{OUT} = 0A



Shutdown through Enable

I_{OUT} = 3A



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PIN FUNCTIONS

Package Pin #	Name	Description
1	VIN	**Supply voltage.** The MP1477 operates from a 4.2V to 17V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	**Switch output.** Connect SW using a wide PCB trace.
3	GND	**System ground.** GND is the reference ground of the regulated output voltage and requires extra care during the PCB layout. Connect GND with copper traces and vias.
4	BST	**Bootstrap.** Connect a 1µF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	**Enable.** Drive EN high to enable the MP1477. For automatic start-up, connect EN to VIN with a 100kΩ pull-up resistor.
6	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current-limit runaway during a short-circuit fault.

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BLOCK DIAGRAM

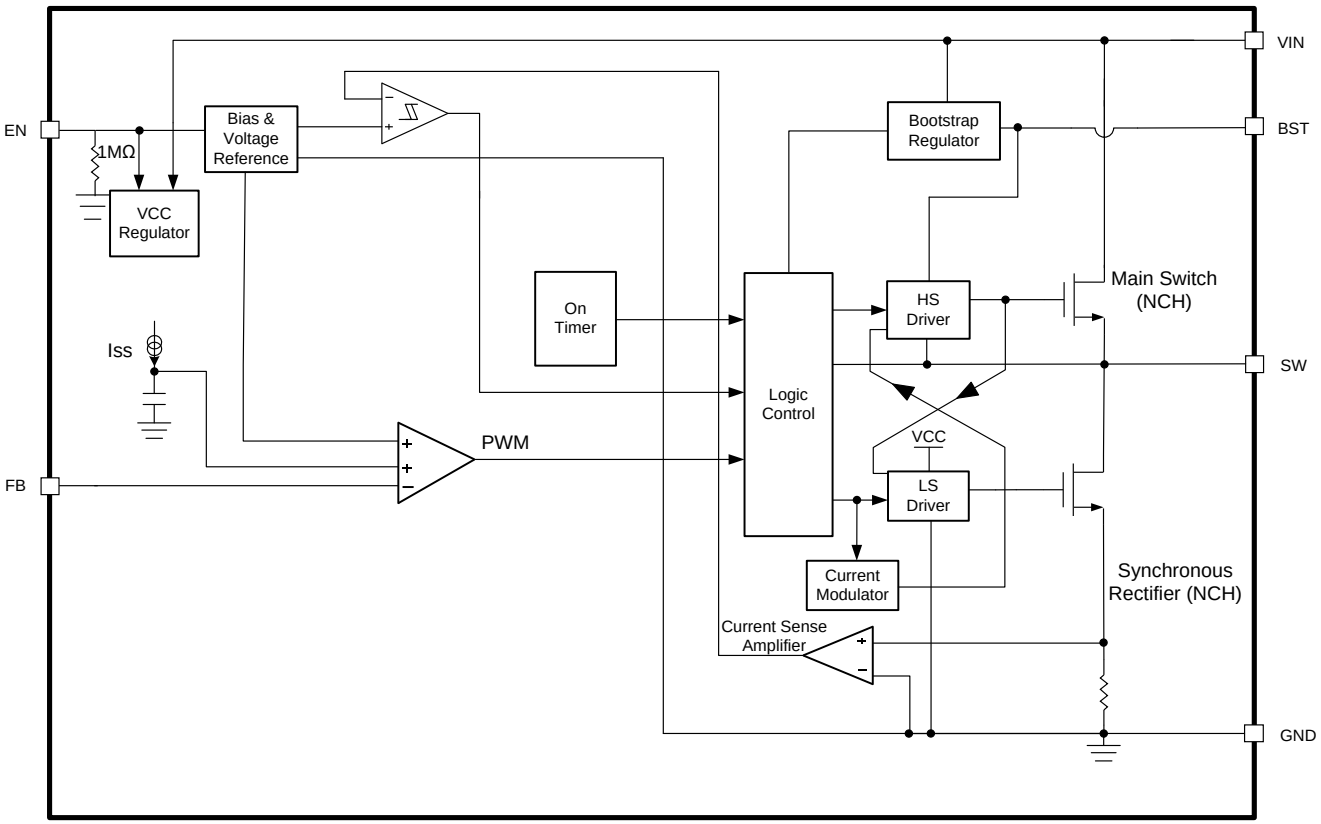


Figure 1: Functional Block Diagram

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OPERATION

The MP1477 is fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off until the next period. By repeating operation this way, the converter regulates the output voltage.

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps. The low-side MOSFET (LS-FET) is turned on when the HS-FET is off to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To prevent shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

When the MP1477 works in pulse-frequency modulation (PFM) mode during light-load operation, the MP1477 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver goes into tri-state (Hi-Z). Therefore, the output capacitors discharge slowly to GND through R1 and R2. When V_{FB} drops below V_{REF}, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to pulse-width modulation (PWM) mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

EN is clamped internally using a 2.8V series Zener diode (see Figure 2). Connecting the EN input through a pull-up resistor to VIN limits the EN input current to less than 100μA, preventing damage to the Zener diode.

For example, when connecting 12V to VIN, $R_{PULLUP} \geq$ (12V - 2.8V) / (100kΩ + 35kΩ) = 68μA.

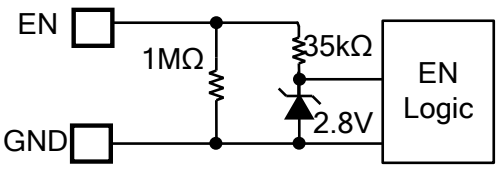


Figure 2: Zener Diode between EN and GND

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP1477 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V, while its falling threshold is 3.67V consistently.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, SS overrides REF so the error amplifier

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uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. The SS time is set to 2.5ms internally.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP1477 has a valley current-limit control. During the LS-FET on state, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the low-side limit comparator turns over, and the MP1477 enters over-current protection (OCP) mode. The HS-FET waits until the valley current limit disappears before turning on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 75% below the reference). Once UV is triggered, the MP1477 enters hiccup mode to restart the part periodically.

During OCP, the device tries to recover from the over-current fault with hiccup mode. During hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still remains after the soft start ends, the device repeats this operation cycle until the over-current condition disappears and the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Bias Start-Up

The MP1477 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start voltage exceeds the sensed output voltage at FB, the MP1477 starts working normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 2.2V and a hysteresis of 150mV. VIN regulates the bootstrap capacitor voltage internally through D1, M1, C3, L1, and C2 (see Figure 3). If VIN - V_{SW} exceeds 3.3V, U2 regulates M1 to maintain a 3.3V BST voltage across C3.

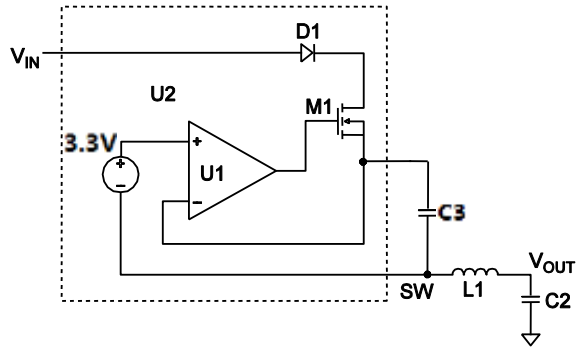


Figure 3: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both VIN and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 value leads to considerable quiescent current loss, but a large R2 value makes FB noise-sensitive. R2 is recommended to be within 5 - 100kΩ. Typically, an R2 value between 5 - 30μA provides a good balance between system stability and no-load loss. R1 can then be determined with Equation (2):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (2)$$

The feedback circuit is shown in Figure 4.

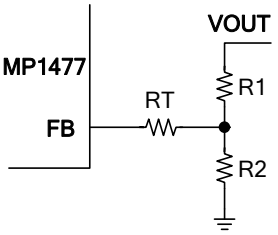


Figure 4: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages, C_{OUT} = 22μF*2 (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)	L (μH)
5	40.2	7.68	75	3.3
3.3	40.2	13	75	2.2
2.5	40.2	19.1	100	2.2
1.8	40.2	32.4	110	1.5
1.5	40.2	45.3	147	1.5
1.2	40.2	82	147	1
1	20.5	84.5	249	1

NOTE:

9) For a detail design circuit, please refer to the Typical Application Circuits on page 16 to page 18.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% to 60% of the maximum output current and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, place ceramic capacitors as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the

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system, choose an input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The output voltage ripple caused by the ESR is very small. In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Selecting a larger output capacitor can also achieve a better load transient response, but the maximum output capacitor limitation should be also considered in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and will fail to regulate.

The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (12):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (12)$$

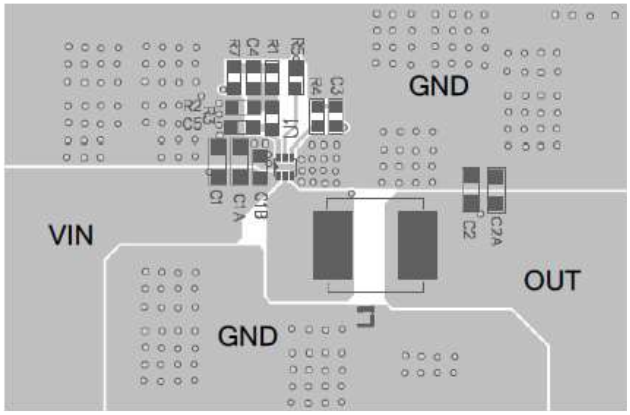
Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PCB Layout Guidelines

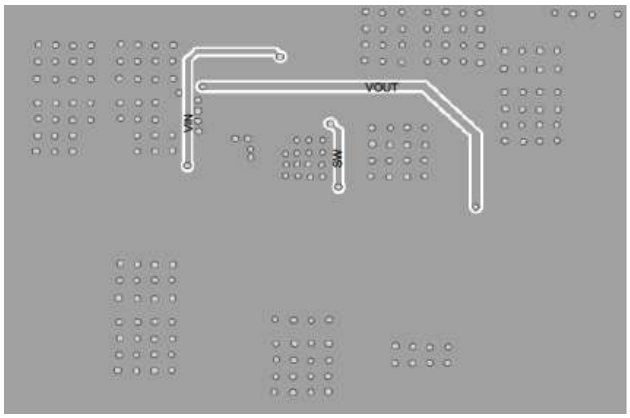
Efficient layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 5 and follow the guidelines below.

1) Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2) Place the input capacitor as close to VIN and GND as possible (recommended within 1mm).
3) Place the external feedback resistors next to FB.
4) Keep the switching node SW short and away from the feedback network.

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Top Layer



Bottom Layer

Figure 5: Recommended Layout

Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	3A

Detailed application schematics are shown in Figure 6 through Figure 12. The typical performance and waveforms are shown in the Typical Performance Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

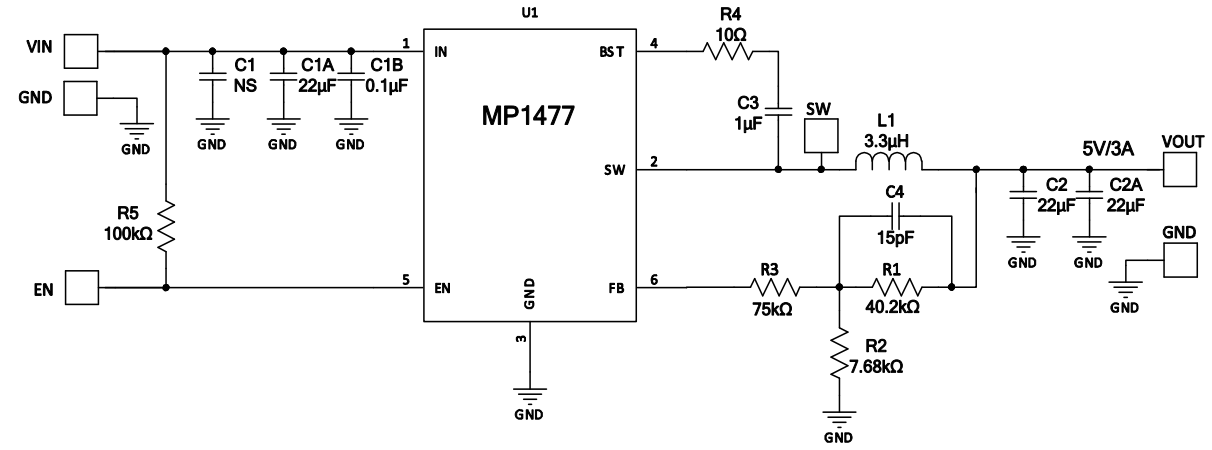


Figure 6: V_{IN} = 12V, V_{OUT} = 5V/3A

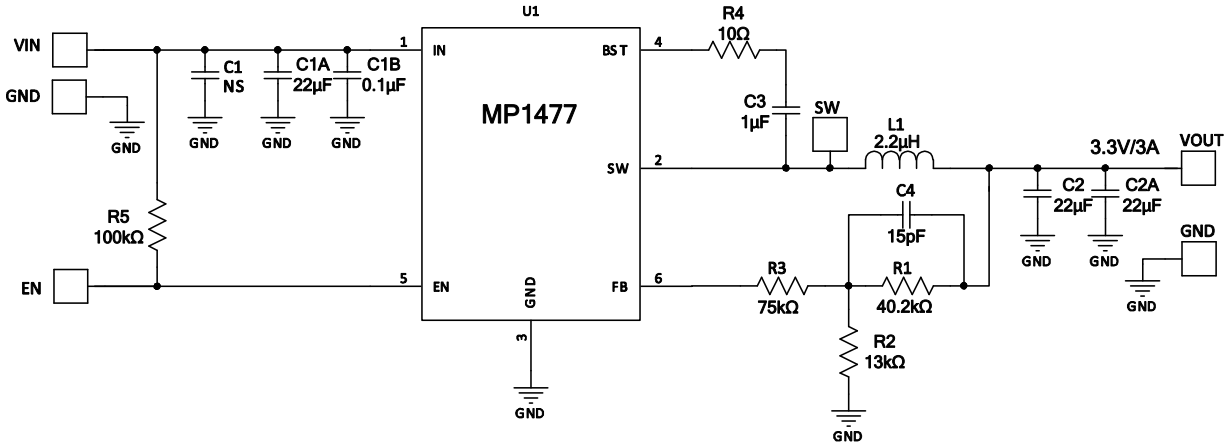


Figure 7: V_{IN} = 12V, V_{OUT} = 3.3V/3A

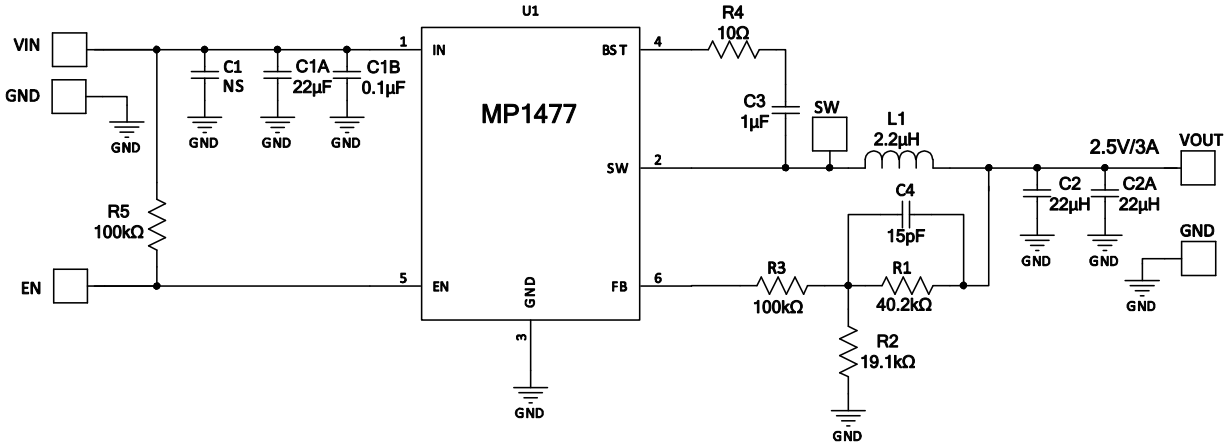


Figure 8: V_{IN} = 12V, V_{OUT} = 2.5V/3A

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TYPICAL APPLICATION CIRCUITS *(continued)*

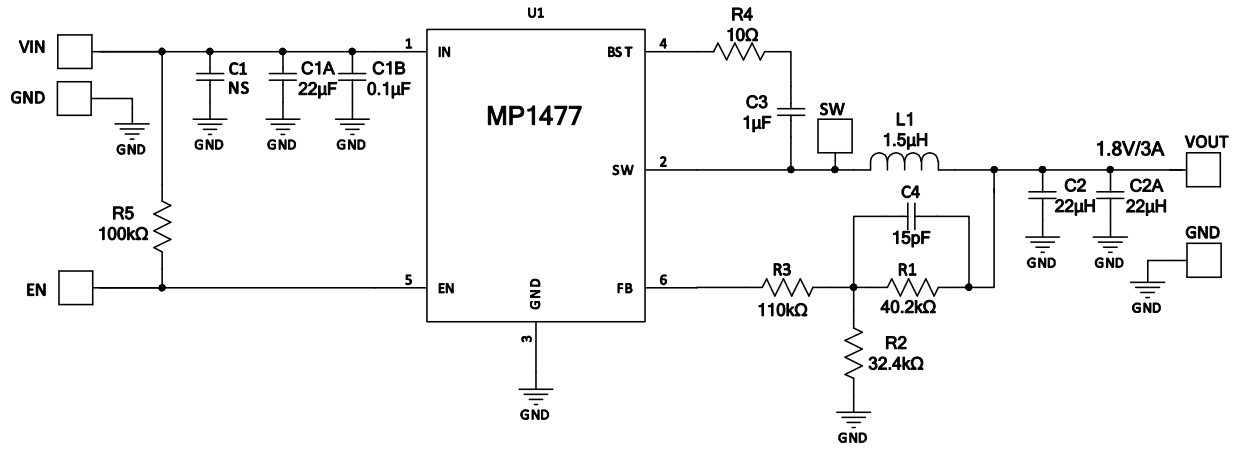


Figure 9: V_{IN} = 12V, V_{OUT} = 1.8V/3A

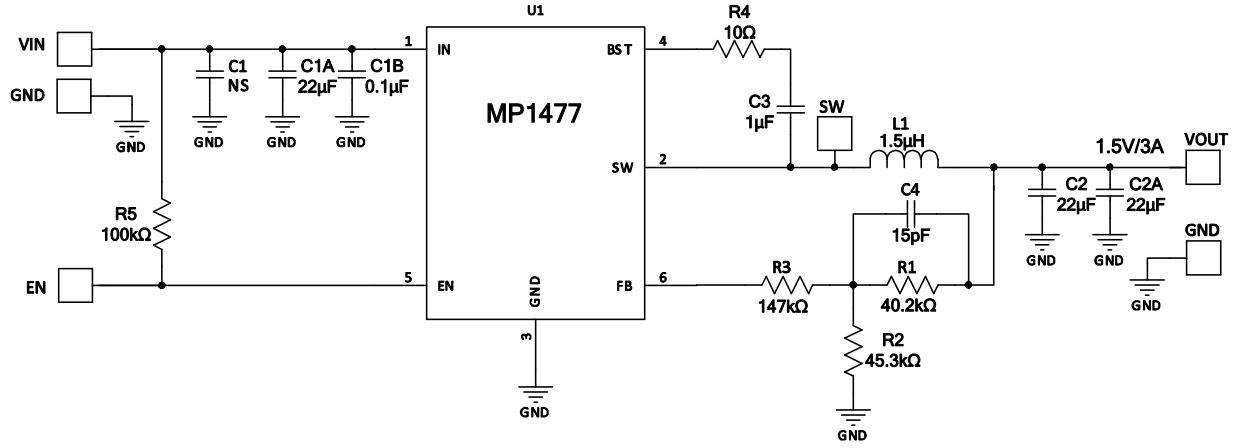


Figure 10: V_{IN} = 12V, V_{OUT} = 1.5V/3A

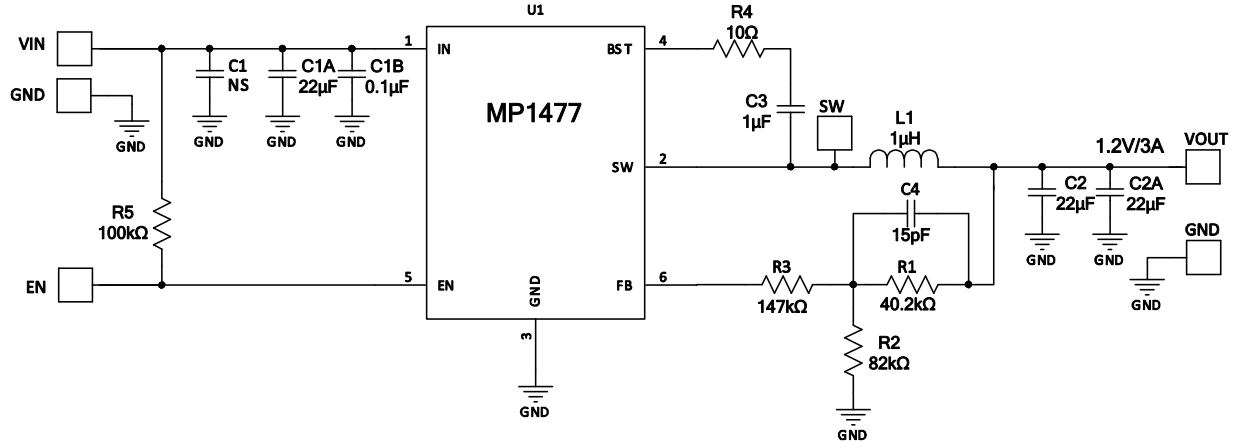


Figure 11: V_{IN} = 12V, V_{OUT} = 1.2V/3A

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TYPICAL APPLICATION CIRCUITS *(continued)*

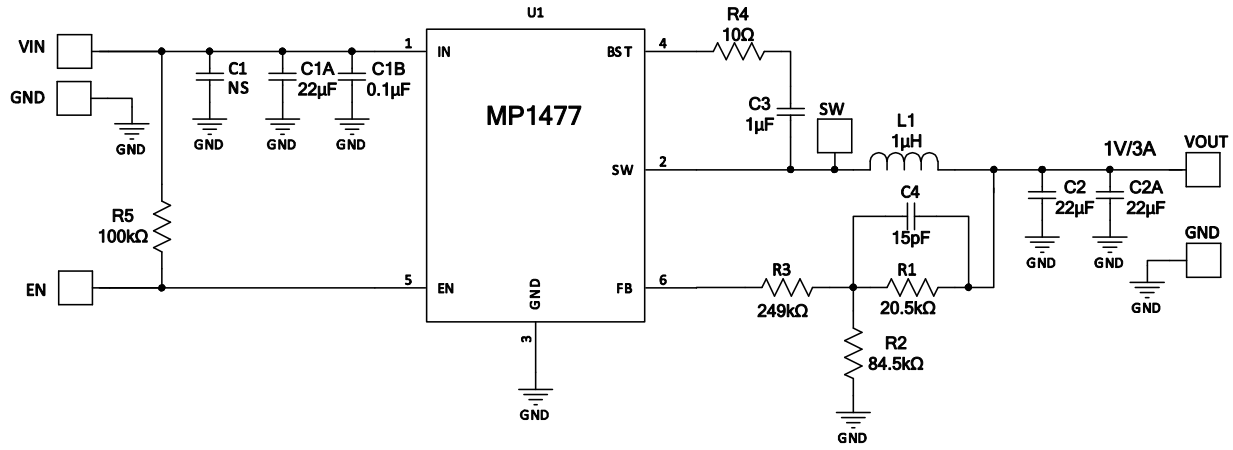
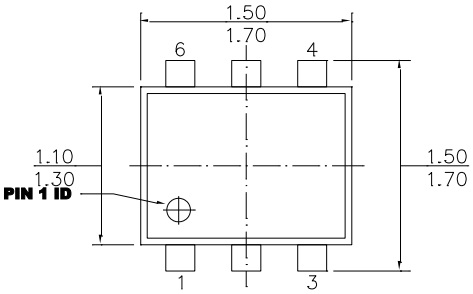


Figure 12: V_{IN} = 12V, V_{OUT} = 1V/3A

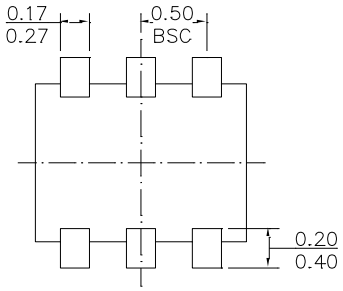
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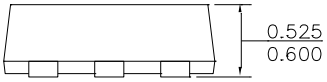
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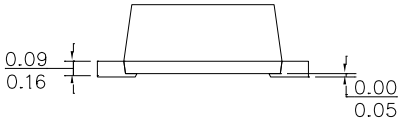
TOP VIEW



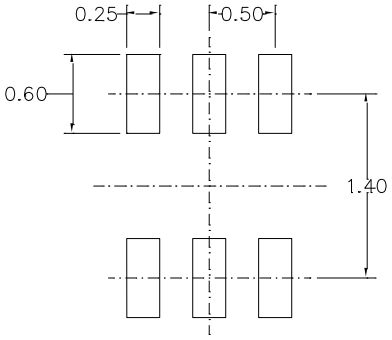
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



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