NCV7547

FLEXMOS™ 7x Half-bridge MOSFET Pre-driver

The NCV7547 programmable seven channel half−bridge MOSFET pre−driver is one of a family of FLEXMOS automotive grade products for driving logic−level NMOS FETs. The product is controllable by a combination of serial SPI and CMOS−compatible parallel inputs. An internal power−on reset provides controlled power up. A reset input allows external re−initialization and a failsafe input allows the device to be safely disabled in the event of system upset.

Each channel independently monitors its external MOSFETs' drain−source voltages for fault conditions. Overload detection thresholds are SPI−selectable and the product allows different detection thresholds for each channel.

The FLEXMOS family of products offers application scalability through choice of external MOSFETs.

Features

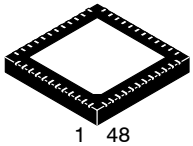
- Supports Functional Safety Compliance
- 7 Half−bridge Pre−drivers for External Logic−level NMOS FETs
  - One Channel with Separated High−side & Low−side Pre−drivers Configurable as a Half−bridge or as Independent Pre−drivers
- Integrated Charge Pump for:
  - High−side Gate Drive
  - Switched Reverse Battery Protection
- 5 V CMOS Compatible I/O:
  - 16−bit SPI Interface for Control and Diagnosis
  - Reset and Failsafe Inputs
  - 4 PWM Control Inputs
- Programmable:
  - Slew Rate Control
  - Overload Protection Thresholds
- Low Quiescent Current
- Wettable Flanks Pb−free Packaging
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

Benefits

- Scalable to Load by Choice of External MOSFET

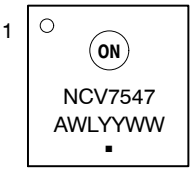
ON Semiconductor®

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QFNW48
7x7, 0.5P
CASE 484AJ

MARKING DIAGRAM



NCV7547	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCV7547MWTXG	QFN−48 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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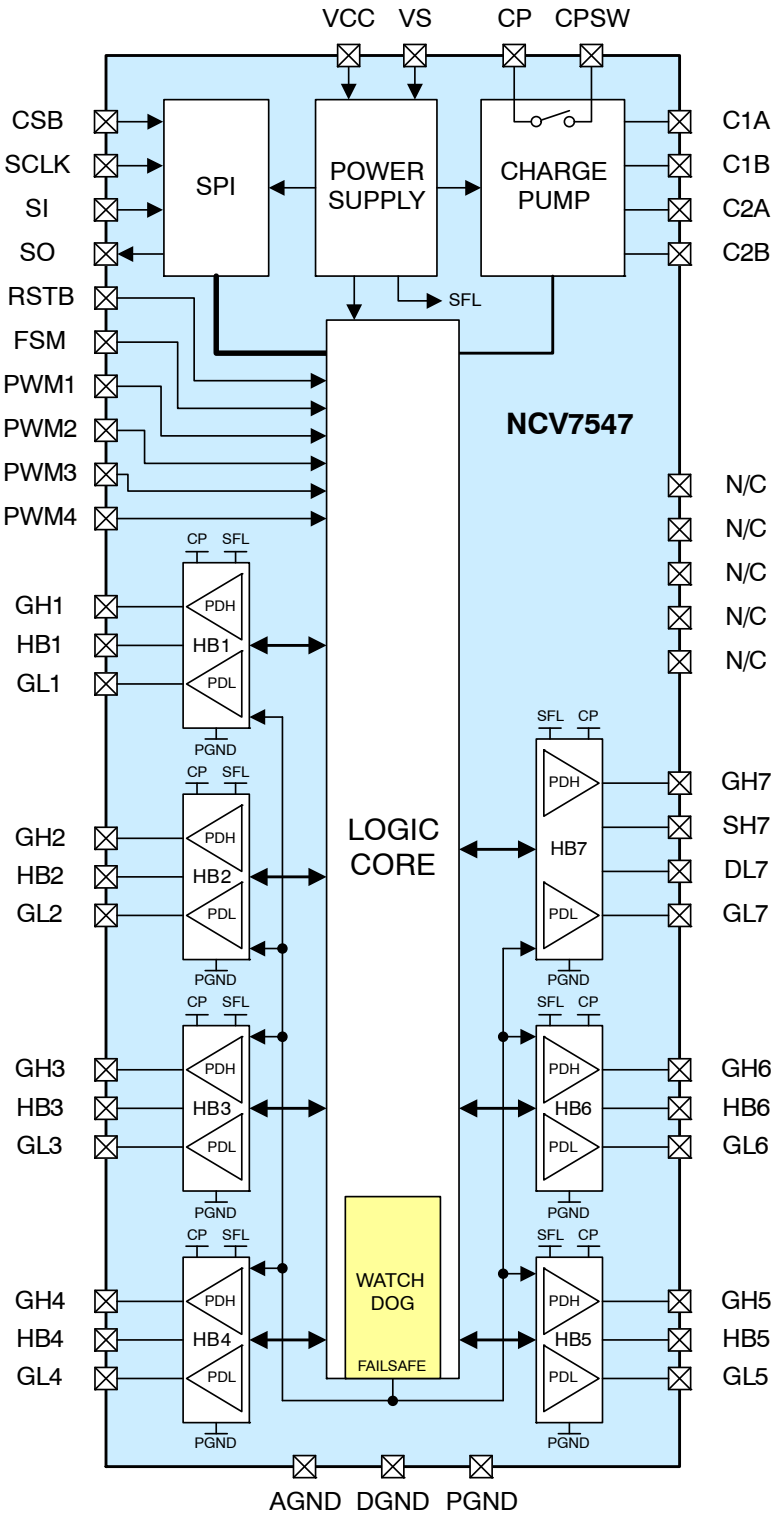


Figure 1. Block Diagram

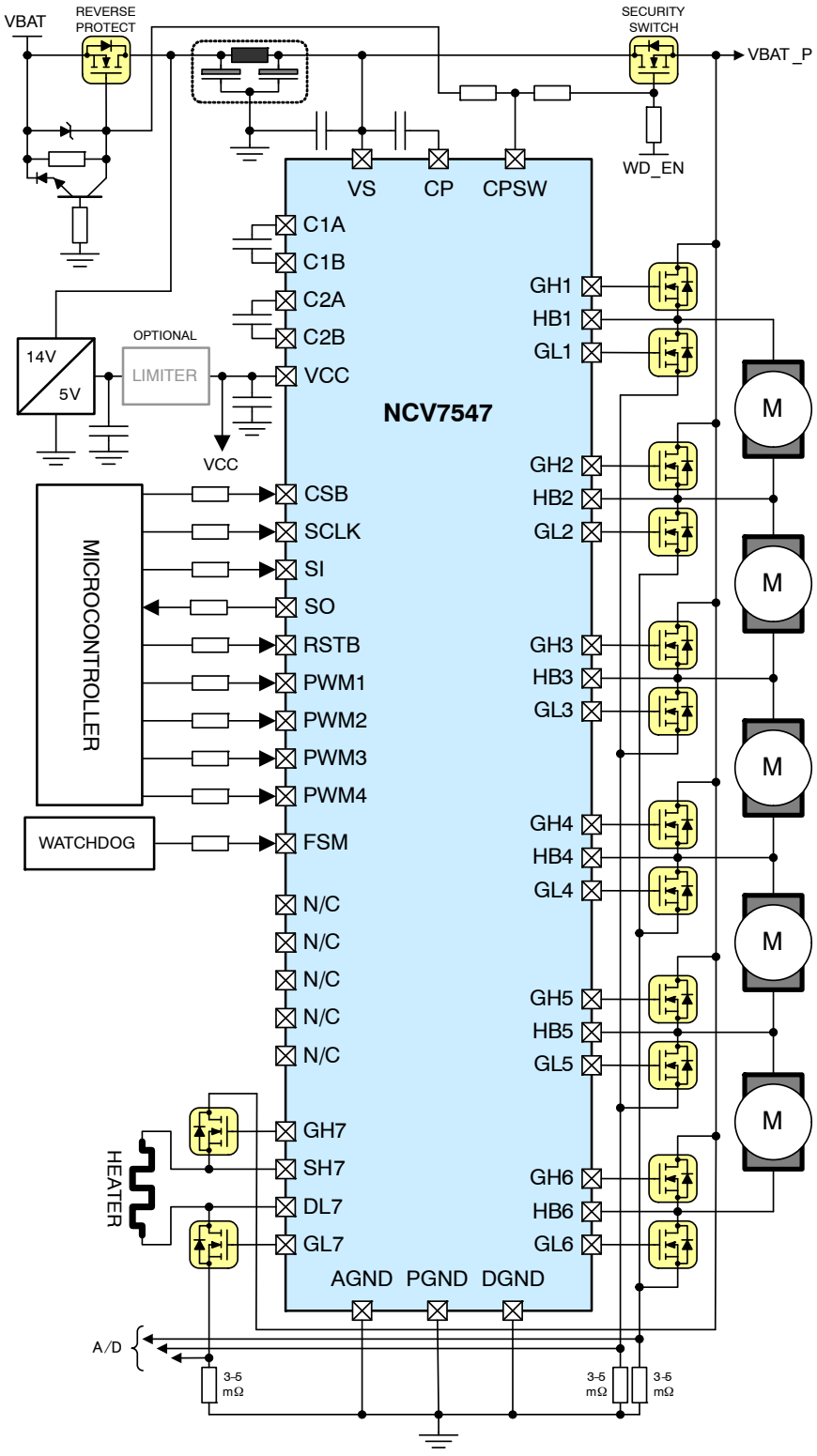


Figure 2. Application Diagram

PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description
48 PIN QFN EXPOSED PAD PACKAGE			
42	VS	Main Power Supply	Main high−power device supply (battery) input; VDS sense reference node for the half−bridge high−side drivers. An external ceramic bypass capacitor shall be connected between VS and GND close to the pin.
36	VCC	Logic Supply	SPI block and internal logic and low power (analog) supply input. An external ceramic bypass capacitor shall be connected between VCC and GND close to the pin.
24	AGND	Signal Ground	Low power return path; reference for the analog circuitry.
25	DGND	Digital Ground	Low power return path; reference for the digital circuitry.
13	PGND	Power Ground	High power return path; reference for the half−bridge drivers; VDS sense reference node for the half−bridge low−side drivers.
45	C1A	Charge Pump Switch Node	Switching nodes for external ceramic charge pumping capacitors 1 & 2.
46	C1B		
47	C2A		
48	C2B		
43	CP	Charge Pump Output	Charge pump output; an external ceramic buffer capacitor shall be connected between CP and VS to provide stable output voltage during transient noise on VS.
44	CPSW	Charge Pump Switched Output	Switched charge pump output; activates external reverse battery and security power MOSFET switches via SPI.
29	RSTB	Wake Input	Digital input with falling edge digital de−glitch and pull−down resistor; active low master reset; the device is in wake state when the pin is high.
34	FSM	Fail−safe Input	Digital input with symmetrical digital de−glitch and pull−down resistor; active high fail−safe mode (can be set via an external watchdog circuit).
33	PWM1	PWM Inputs	Digital inputs with symmetrical adaptive digital de−glitch and pull−down resistor; provide PWM signals to the half−bridge pre−drivers.
32	PWM2		
31	PWM3		
30	PWM4		
26	CSB	SPI Chip Select	Digital input with pull−up resistor; active low chip select.
27	SCLK	SPI Clock	Digital input with pull−down resistor.
28	SI	SPI Serial Input	Digital input with pull−down resistor.
35	SO	SPI Serial Output	Digital tri−state output with high−side path protection to prevent VCC back−bias in the event of an external voltage regulator failure or short to VS.
2	GH1	High−side Pre−driver Output	High−side pre−drivers with pull−down resistor to HBx switch nodes; gate drive for external logic−level N−MOS FETs.
5	GH2		
8	GH3		
11	GH4		
15	GH5		
18	GH6		
3	HB1	Half−bridge Switch Node	Monitoring inputs for external half−bridge switches 1:6 with pull−down resistor to AGND; high−side MOSFET source node; low−side MOSFET drain node.
6	HB2		
9	HB3		
12	HB4		
16	HB5		
19	HB6		

PACKAGE PIN DESCRIPTION

Pin	Label	Function	Description
48 PIN QFN EXPOSED PAD PACKAGE			
1	GL1	Low−side Pre−driver Output	Low−side pre−drivers with pull−down resistor to PGND; gate drive for external logic−level N−MOS FETs.
4	GL2		
7	GL3		
10	GL4		
14	GL5		
17	GL6		
22	GH7	High−side Pre−driver Output	High−side pre−driver with pull−down resistor to SH7 input; gate drive for external logic−level N−MOS FETs.
23	SH7	High−side Source Node	Monitoring input for external high−side switch 7 with pull−down resistor to AGND; high−side MOSFET source node.
21	DL7	Low−side Drain Node	Monitoring input for external low−side switch 7 with pull−down resistor to AGND; low−side MOSFET drain node.
20	GL7	Low−side Pre−driver Output	Low−side pre−driver with pull−down resistor to PGND; gate drive for external logic−level N−MOS FETs.
41	N/C	−	No internal connection.
40	N/C		
39	N/C		
38	N/C		
37	N/C		
	EP	Exposed Pad	Connect to GND.

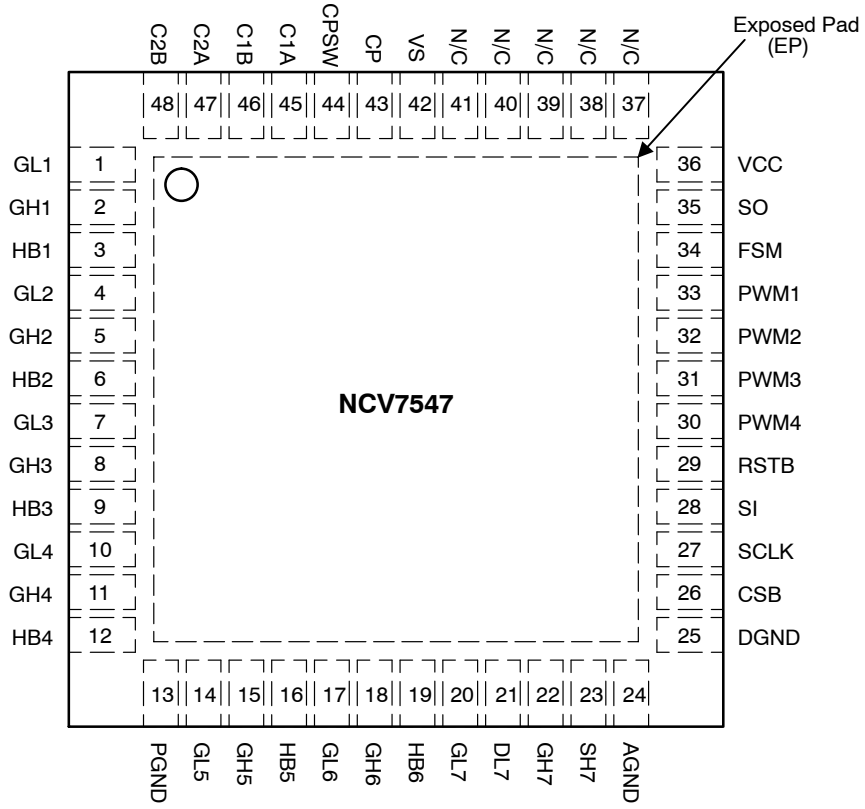


Figure 3. 32 Pin 5 x 5 mm Exposed Pad Pin−out (Top View)

MAXIMUM RATINGS (Except as noted, voltages are with respect to AGND = DGND = PGND = GND.)

Rating	Symbol	Value	Unit
VS Supply DC: 2 min @ 25°C AC: ISO7637 Pulse 5b, 400 ms @ 25°C	VS_{MAX}	−0.3 to 28 40	V
VCC Supply	VCC_{MAX}	−0.3 to 7.0	V
Output Voltage: CP, CPSW SO	V_OUT_{MAX} V_SO_{MAX}	−0.3 to 40 −0.3 to 20	V
Input Voltage: FSM, C1A, C1B, C2A, C2B	V_IN_{MAX1}	−0.3 to 40	V
Input Voltage (Clamped): HBx, SH7, DL7	V_IN_{MAX2}	−1.0 to 40	V
Input Voltage: CSB, SCLK, SI, RSTB, PWMx	V_IN_{MAX3}	−0.3 to 20	V
Input Current (Clamped): CSB, SCLK, SI, RSTB, FSM, PWMx, GHx, GLx	I_IN_{MAX}	± 5.0	mA
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−55 to 150	°C
Peak Reflow Soldering Temperature: Lead−free 60 to 150 seconds at 217°C (Note 1)	T_{PK}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. See or download ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

ATTRIBUTES

Characteristic	Symbol	Value	Unit
ESD Capability:	V_{ESD_HBM}		
Human Body Model per AEC−Q100−002			
All pins		≥ ± 2.0	kV
VS, HBx, SH7, DL7		≥ ± 4.0	kV
Charged Device Model per AEC−Q100−011	V_{ESD_CDM}		
All Pins		≥ ± 500	V
Corner Pins		≥ ± 750	V
Moisture Sensitivity (Note 1)	MSL	1	−
Package Thermal Resistance − Still−air, P_{IN} = 1 W (Uniform Power Density)			°C/W
Junction−to−Ambient, $R\theta_{JA}$ (Note 2)	$R\theta_{JA}$	61.7	
(Note 3)	$R\theta_{JA}$	37.5	
Junction−to−Exposed Pad, $R\Psi_{JPAD}$	$R\Psi_{JPAD}$	10.8	

2. Based on JESD51−3, 1.2 mm thick FR4, 2S0P PCB, 1 oz. signal, 4 thermal vias to 28 x 28 mm 1 oz. spreader on bottom layer.
3. Based on JESD51−7, 1.2 mm thick FR4, 1S2P PCB, 1 oz. signal, 4 thermal vias to 76 x 76 mm 1 oz. internal spreader planes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Main Power Supply Voltage	VS_{OP}	7.0	18.0	V
Logic Power Supply Voltage	VCC_{OP}	4.5	5.5	V
Logic High Input Voltage	V_{IN_HIGH}	3.5	VCC_{OP}	V
Logic Low Input Voltage	V_{IN_LOW}	0	1.5	V
Half−bridge Output PWM Rate	f_{PWM}	−	25	kHz
Charge Pump Capacitors (C1, C2, CCP)	−	220	4700	nF
SPI Clock Frequency	f_{SCLK}	0.1	2.5	MHz
Startup Delay at VCC Power−On Reset (POR) (Note 4)	t_{RESET}	−	200	μs
Ambient Still−Air Operating Temperature	T_A	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Minimum wait time until device is ready to accept serial input data.

PARAMETRIC TABLES

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
VS SUPPLY						
Standby Current	I_{VS_SBY}	VS = 12.0V, 0 ≤ VCC ≤ 5.5 V, RSTB = 0, T_A = 25°C	–	–	5.0	μA
Operating Current	I_{VS_OP0}	VCC = 5.0 V , RSTB = 1, T_A = 25°C Default Settings at POR, SPI Inactive CR1.D[10]=0	–	1.6	5.0	mA
	I_{VS_OP1}	CR1.D[10]=1	–	20.3	25.0	mA
Under−voltage Lockout	VS_{UVLO}	VS decreasing, SR0.D[5] → 1	4.5	5.0	5.5	V
Under−voltage Hysteresis	VS_{UVHY}	SR0.D[5] → 0 (after read status if VS > $VS_{UVLO+UVHY}$)	100	200	–	mV
Under−voltage Filter Time	t_{UVDGL}	VS decreasing	4.0	5.0	6.0	μs
Over−voltage Shutdown	VS_{OVSDR}	VS increasing, SR0.D[4] → 1	19.0	20.0	21.0	V
	VS_{OVSDF}	VS decreasing, SR0.D[4] → 0	18.0	19.0	20.0	V
Over−voltage Hysteresis	VS_{OVHY}	SR0.D[4] → 0 (after read status if VS < VS_{OV_OVHY})	–	0.9	–	V
Over−voltage Filter Time	t_{OVDGL}	VS increasing	4.0	5.0	6.0	μs
VS PWM Threshold	VS_{PWM}	VS decreasing, SR0.D[7] → 1	8.90	9.45	10.0	V
VS PWM Hysteresis	VS_{PWM_HY}	SR0.D[7] → 0 and/or SR0.D[6] → 0 (after read status if VS > $VS_{PWM+PWM_HY}$)	–	100	–	mV
VCC SUPPLY						
Standby Current	I_{VCC_SBY}	VS = 12.0V, VCC = 5.5 V , RSTB = 0, T_A = 25°C Default Settings at POR, SPI Inactive	–	–	5.0	μA
Operating Current	I_{VCC_OP}	VS = 12.0V, RSTB = 1, T_A = 25°C	–	8.0	12.0	mA
Power−On Reset Threshold	VCC_{PORR}	VCC Increasing	3.71	4.10	4.49	V
	VCC_{PORF}	VCC Decreasing	3.50	3.85	4.20	V
CHARGE PUMP						
C1 = C2 = 470 nF; CCP = 1000 nF						
Switching Frequency	f_{CP}	Single−stage, complementary−phase topology	0.75	1.10	1.45	MHz
Spread Spectrum Modulation Depth Modulation Rate	 CP_{MOD} f_{CPMOD}	(Note 6)	 – –	 ±15.0 45.6	 – –	 % kHz
Regulation Voltage	CP_{REG}	V(CP, VS), VS > VS_{PWM}, 0 ≤ I(CP) ≤ 15 mA	8.3	8.9	9.5	V
Startup Delay	CP_{DLY}	VS = 13V, I(CP) = no load (Note 6) C1 = C2 = 470 nF, CCP = 1000 nF	–	–	500	μs
Dropout Voltage	CP_{DROP0}	V(VS) − V(CP, VS), I(CP) = 10 mA, VS=9.4	–	–	1.50	V
	CP_{DROP1}	V(VS) − V(CP, VS), I(CP) = 15 mA, VS=10V and SR0.D[7] = 0 T_J ≥ 125°C	–	–	1.75	
			–	–	1.90	
Charge Pump Low Detection	CP_{LOW0}	V(CP, VS) decreasing, VS > VS_{PWM}, SR0.D[7] → 1	7.3	8.0	8.8	V
	CP_{LOW1}	Detection margin, CP_{LOW1} = CP_{REG} − CP_{LOW0}	300	–	–	mV
Charge Pump Low Detection Filter Time	t_{CPL_DGL}		120	150	180	μs
Charge Pump Low Hysteresis	CP_{LOW_HY}	SR0.D[7] → 0 (after read status if V(CP,VS) > $CP_{LOW+LOW_HY}$)	–	100	–	mV

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
CHARGE PUMP						
Charge Pump Fail Detection	CP_{FAIL}	V(CP, VS) decreasing, SR0.D[6] → 1	4.925	5.375	5.750	V
Charge Pump Fail Detection Filter Time	t_{CPF_DGL}		120	150	180	μs
Charge Pump Fail Hysteresis	CP_{FAIL_HY}	SR0.D[6] → 0 (after read status if V(CP,VS) > $CP_{FAIL+FAIL_HY}$)	–	100	–	mV
Charge Pump Over−voltage Detection	CP_{OV}	VS increasing	28.0	30.25	32.5	V
Charge Pump Over−voltage Hysteresis	CP_{OV_HYS}		0.5	1.0	2.0	V
CP Switch Resistance	R_{CPTOT}	*Guaranteed by Simulation* 8x CP switches in parallel, T_A = 25°C	–	1.5	–	Ω
Switched CP Output Resistance	R_{CPSW_ON}	CR1.D[9] = 1, I(CPSW) = 5 mA	–	–	100	Ω
Switched CP Output Leakage	CP_{SW_LKG}	CR1.D[9] = 0	−1.0	0	1.0	uA
DIGITAL I/O						
V_{IN_X} High	V_{INHX}	CSB, SCLK, SI, RSTB, FSM, PWMx	3.5	–	–	V
V_{IN_X} Low	V_{INLX}	CSB, SCLK, SI, RSTB, FSM, PWMx	–	–	1.5	V
Input Pull−down Resistance	R_{PDX}	SCLK, SI, RSTB, FSM, PWMx, V_{INX} = VCC	70	100	130	kΩ
Input Pull−up Resistance	R_{PU}	CSB, V_{IN} = 0V	70	100	130	kΩ
Input Current	I_{INX}	V_{INX} = 5.5V: SCLK, SI, RSTB, FSM, PWMx V_{INX} = 0V: CSB	– −80	0	80 –	μA
Input Leakage	I_{IN_LKG}	V_{INX} = 0V: SCLK, SI, RSTB, FSM, PWMx V_{INX} = VCC: CSB	−1.0	0	1.0	μA
Input Filter Time	t_{IN_DGL}	FSM input	8.0	10	12	μs
Reset De−glitch Time	t_{RST_DGL}	Minimum RSTB pulse (H → L → H) detected	8.0	–	–	μs
Reset Assert Time	t_{WRST}	Minimum RSTB hold after H → L transition	–	11	15	μs
SO Low Voltage	V_{SOL}	I_{SINK} = 1.0 mA	–	–	0.4	V
SO High Voltage	V_{SOH}	I_{SOURCE} = 1.0 mA	VCC − 0.4	–	–	V
SO Tri−State Leakage Current	SO_{LKG}	CSB = VCC, SO = VCC/2	−1.0	–	1.0	μA
SERIAL PERIPHERAL INTERFACE (See Figure 4)						
VCC = 5.0V, FSCLK = 2.5 MHz, CLOAD = 80 pF, all timing is at 30% and 70% VCC unless otherwise specified.						
SCLK Clock Period	t_{SCLK}		400	–	–	ns
SCLK High Time	t_{CLKH}	SCLK = 70% VCC to 70% VCC	200	–	–	ns
SCLK Low Time	t_{CLKL}	SCLK = 30% VCC to 30% VCC	200	–	–	ns
Maximum Input Capacitance	C_{INX}	SCLK, SI (Note 6)	–	–	15	pF
SI Setup Time	t_{SISU}	SI = 30%|70% to SCLK = 70% VCC (Note 6)	25	–	–	ns
SI Hold Time	t_{SIHD}	SCLK = 30% to SI = 30%|70% VCC (Note 6)	25	–	–	ns
SO Rise Time	t_{SOR}	(20% V_{SO} to 80% VCC) (Note 6)	–	25	50	ns
SO Fall Time	t_{SOF}	(80% V_{SO} to 20% VCC) (Note 6)	–	–	50	ns
CSB Setup Time	t_{CSBSU}	CSB = 30% to SCLK = 30% VCC (Note 6)	60	–	–	ns
CSB Hold Time	t_{CSBHD}	SCLK = 30% to CSB = 70% VCC (Note 6)	75	–	–	ns

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
SERIAL PERIPHERAL INTERFACE (See Figure 4)						
CSB to SO Assert Time	t_{SO_A}	CSB = 30% VCC to SO = 30%|70% VCC RLOAD = 5 kΩ (Note 6)	–	65	125	ns
CSB to SO Release Time	t_{SO_R}	CSB = 70% VCC to SO = 20%|80% VCC/2 RLOAD = 5 kΩ (Note 6)	–	–	350	ns
SO Delay Time	SO_{DLY}	SCLK = 70% VCC to SO = 30%|70% (Note 6)	–	65	125	ns
Transfer Delay Time	CS_{DLY}	CSB rising edge to next falling edge. (Note 6)	–	–	1.0	μs
HALF−BRIDGE PRE−DRIVER OUTPUTS						
VS > VS_{PWM}						
On−state Drive Voltage	V_{PDHX}	High−side, V_{PDHX} = H = V(GHx, HBx) or V(GHX, SH7), No External Load	8.3	–	9.5	V
	V_{PDLX}	Low−side, V_{PDLX} = H =V(GLx, PGND), No External Load	8.1	–	9.8	V
High−side driver Gate−source Clamp Positive Voltage	V_{GSX_CLPH}	V(GHx, HBx), V(GH7, SH7), I_{CLMP} = 3.0 mA	14.0	–	18.0	V
High−side driver Source−gate Clamp Negative Voltage	V_{SGX_CLPH}	V(HBx, GHx), V(SH7, GH7), I_{CLMP} = −2.0 mA	−20.0	–	−16.0	V
Low−side driver Gate−source Clamp Positive Voltage	V_{GSX_CLPL}	V(GLx, PGND), I_{CLMP} = 10 mA	11.5	–	15.0	V
Low−side driver Gate−source Clamp Negative Voltage	V_{GSX_CLN}	V(GLx, PGND), I_{CLMP} = −1.0 mA	−1.0	–	–	V
Gate Drive Timeout	$t_{TIMEOUT}$	I_{GHx} ≤ I_{GHx_SS}	16	20	24	μs
Gate Drive Timeout Current	I_{GHx_SS}	V(GHx, HBx) or V(GHx, SH7) = 0 V, t > $t_{TIMEOUT}$	−1.2	−1.0	−0.8	mA
Gate−source Pull−down Resistor	R_{GSX}	R(GHx, HBx), R(GHx, SH7), R(GLx, PGND)	70	–	130	kΩ
Cross Conduction Blank Time GHx, GLx	t_{BLANKX}	BLANKx[1:0] = 0x00	0.8	1.0	1.2	μs
		BLANKx[1:0] = 0x01	1.6	2.0	2.4	
		BLANKx[1:0] = 0x02	2.4	3.0	3.6	
		BLANKx[1:0] = 0x03	3.2	4.0	4.8	
PRE−DRIVER SLOPE CONTROL						
VS > VS_{PWM}						
High−side Pre−charge Time GHx Rising and Falling Slope	t_{PRCX}	T_PCx[1:0] = 0x00	80	100	120	ns
		T_PCx[1:0] = 0x01	160	200	240	
		T_PCx[1:0] = 0x02	240	300	360	
		T_PCx[1:0] = 0x03	320	400	480	
High−side Pre−charge Current GHx Rising Slope V(GHx) = 3.5 V	I_{PRCX_R}	I_PCRx[2:0] = 0x00	1.23	1.50	1.77	mA
		I_PCRx[2:0] = 0x01	4.52	5.25	5.99	
		I_PCRx[2:0] = 0x02	7.42	8.63	9.84	
		I_PCRx[2:0] = 0x03	10.65	12.38	14.11	
		I_PCRx[2:0] = 0x04	14.19	16.50	18.81	
		I_PCRx[2:0] = 0x05	17.42	20.25	23.09	
		I_PCRx[2:0] = 0x06	20.64	24.00	27.36	
		I_PCRx[2:0] = 0x07	24.19	28.13	32.07	

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
PRE−DRIVER SLOPE CONTROL						
High−side Pre−charge Current GHx Falling Slope V(GHx) = (VS + 3.5) V	I_{PRCX_F}	I_PCFx[2:0] = 0x00	24.84	28.88	32.92	mA
		I_PCFx[2:0] = 0x01	30.64	35.63	40.62	
		I_PCFx[2:0] = 0x02	36.12	42.00	47.88	
		I_PCFx[2:0] = 0x03	41.61	48.38	55.15	
		I_PCFx[2:0] = 0x04	47.41	55.13	62.85	
		I_PCFx[2:0] = 0x05	52.89	61.50	70.11	
		I_PCFx[2:0] = 0x06	58.38	67.88	77.38	
		I_PCFx[2:0] = 0x07	64.18	74.63	85.08	
High−side Slew Current GHx Rising and Falling Slope Rising: V(GHx) = (VS + 3.5) V Falling: V(GHx) = 3.5 V	I_{SRX}	SR_CTRLx[2:0] = 0x00	1.23	1.50	1.77	mA
		SR_CTRLx[2:0] = 0x01	1.94	2.25	2.57	
		SR_CTRLx[2:0] = 0x02	2.91	3.38	3.85	
		SR_CTRLx[2:0] = 0x03	4.52	5.25	5.99	
		SR_CTRLx[2:0] = 0x04	6.78	7.88	8.98	
		SR_CTRLx[2:0] = 0x05	10.00	11.63	13.26	
		SR_CTRLx[2:0] = 0x06	14.84	17.25	19.67	
		SR_CTRLx[2:0] = 0x07	21.93	25.50	29.07	
Low−side Drive Current GLx Rising and Falling slope V(GLx) = 3.5 V	I_{LSX}	SR_CTRLx[2:0] = 0x00	5.16	6.00	6.84	mA
		SR_CTRLx[2:0] = 0x01	7.74	9.00	10.26	
		SR_CTRLx[2:0] = 0x02	11.63	13.52	15.41	
		SR_CTRLx[2:0] = 0x03	18.06	21.00	23.94	
		SR_CTRLx[2:0] = 0x04	27.11	31.52	35.93	
		SR_CTRLx[2:0] = 0x05	40.01	46.52	53.03	
		SR_CTRLx[2:0] = 0x06	59.34	69.00	78.66	
		SR_CTRLx[2:0] = 0x07	87.72	102.00	116.28	
SLOPE CONTROL CALIBRATION UNIT						
Slope Calibration Comparator Window Thresholds	V_{CALF_L}	Falling slope window lower threshold	3.0	5.0	7.0	% VS
	V_{CALF_U}	Falling slope window upper threshold	13	15	17	
	V_{CALR_L}	Rising slope window lower threshold	82	85	88	
	V_{CALR_U}	Rising slope window upper threshold	92	95	98	
Comparator Propagation Delay	t_{CAL_PD}		–	62	100	ns
Sample Synchronization Delay	t_{SYNC}	$t_{SYNC} = 2/f_{CORE}$	–	50	–	ns
Calibration Pre−charge Time HBx Rising & Falling Slope	t_{CAL_PCx}	CAL_PC[3:0] = 0x00	(Note 7)	50	(Note 7)	ns
		CAL_PC[3:0] = 0x01		150		
		CAL_PC[3:0] = 0x02		250		
		CAL_PC[3:0] = 0x03		350		
		CAL_PC[3:0] = 0x04		450		
		CAL_PC[3:0] = 0x05		550		

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
SLOPE CONTROL CALIBRATION UNIT						
Calibration Pre−charge Time HBx Rising & Falling Slope	t_{CAL_PCx}	CAL_PC[3:0] = 0x06	(Note 7)	650	(Note 7)	ns
		CAL_PC[3:0] = 0x07		750		
		CAL_PC[3:0] = 0x08		850		
		CAL_PC[3:0] = 0x09		950		
		CAL_PC[3:0] = 0x0A		1050		
		CAL_PC[3:0] = 0x0B		1150		
		CAL_PC[3:0] = 0x0C		1250		
		CAL_PC[3:0] = 0x0D		1350		
		CAL_PC[3:0] = 0x0E		1450		
		CAL_PC[3:0] = 0x0F		1550		
Calibration Delay Time HBx Rising & Falling Slope	t_{CAL_DLYx}	CAL_DLY[3:0] = 0x00	(Note 7)	0.35	(Note 7)	μs
		CAL_DLY[3:0] = 0x01		0.55		
		CAL_DLY[3:0] = 0x02		0.75		
		CAL_DLY[3:0] = 0x03		0.95		
		CAL_DLY[3:0] = 0x04		1.15		
		CAL_DLY[3:0] = 0x05		1.35		
		CAL_DLY[3:0] = 0x06		1.55		
		CAL_DLY[3:0] = 0x07		1.75		
		CAL_DLY[3:0] = 0x08		1.95		
		CAL_DLY[3:0] = 0x09		2.15		
		CAL_DLY[3:0] = 0x0A		2.35		
		CAL_DLY[3:0] = 0x0B		2.55		
		CAL_DLY[3:0] = 0x0C		2.75		
		CAL_DLY[3:0] = 0x0D		2.95		
		CAL_DLY[3:0] = 0x0E		3.15		
		CAL_DLY[3:0] = 0x0F		3.35		
HALF−BRIDGE DIAGNOSTICS						
VDS Monitor Thresholds VDS = V(VS, HBx) − or− VDS = V(HBx, GND)	VDS_{THRX}	VDSx[2:0] = 0x00	263	300	337	mV
		VDSx[2:0] = 0x01	356	400	444	
		VDSx[2:0] = 0x02	445	500	555	
		VDSx[2:0] = 0x03	534	600	666	
		VDSx[2:0] = 0x04	623	700	777	
		VDSx[2:0] = 0x05	712	800	888	
		VDSx[2:0] = 0x06	801	900	999	
		VDSx[2:0] = 0x07	890	1000	1110	
VDS Monitor Filter Time	t_{DGL_STAT}		0.92	1.15	1.38	μs
VDS Monitor Propagation Delay	t_{VDSS_PD}		−	550	750	ns

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

ELECTRICAL CHARACTERISTICS

(4.5 V ≤ VCC ≤ 5.5 V, 7.0 V ≤ VS ≤ 18 V, RSTB = VCC, CR1.D[10] = 1, −40°C ≤ T_J ≤ 150°C, unless otherwise specified.) (Note 5)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
HALF−BRIDGE DIAGNOSTICS						
VDS Overload Detection Delay Time Rising or Falling Slope	t_{DLYX}	T_DLYX[3:0] = 0x00	(Note 7)	1.05	(Note 7)	µs
		T_DLYX[3:0] = 0x01		1.65		
		T_DLYX[3:0] = 0x02		2.25		
		T_DLYX[3:0] = 0x03		2.85		
		T_DLYX[3:0] = 0x04		3.45		
		T_DLYX[3:0] = 0x05		4.05		
		T_DLYX[3:0] = 0x06		4.65		
		T_DLYX[3:0] = 0x07		5.25		
		T_DLYX[3:0] = 0x08		5.85		
		T_DLYX[3:0] = 0x09		6.45		
		T_DLYX[3:0] = 0x0A		7.05		
		T_DLYX[3:0] = 0x0B		7.65		
		T_DLYX[3:0] = 0x0C		8.25		
		T_DLYX[3:0] = 0x0D		8.85		
		T_DLYX[3:0] = 0x0E		9.45		
		T_DLYX[3:0] = 0x0F		10.05		
HBx Input Resistance	R_{HBX}	HBx, SH7, DL7 − Pull−down to AGND	−	26	−	kΩ
HBx Monitor Threshold	VHB_{THR}		45	50	55	% VS
HBx Monitor Propagation Delay	t_{HBX_PD}		−	1.0	2.0	µs
HBx Monitor Test Currents	I_{TST}	CR0.HB_ENx = 0, HB1, HB3 source or sink, 10V ≤ VS ≤ 16V	± 6.0	± 7.5	± 9.0	mA
WATCHDOG TIMER						
Watchdog Timeout	t_{WD}	CR1.D[8] = 0 CR1.D[8] = 1	20 400	25 500	30 600	ms
Core Clock Oscillator	f_{CORE}		−	40	−	MHz
THERMAL OVERLOAD (Note 6)						
Warning Threshold	T_{OTW}	T_J increasing, SR0.D[3] → 1	110	125	140	°C
Warning Hysteresis	T_{OTW_HY}	SR0.D[3] → 0 (after read status if $T_J < T_{OTW - OTW_HY}$)	−	20	−	°C
Shutdown Threshold	T_{OTS}	T_J increasing, SR0.D[2] → 1, all outputs → OFF	150	170	190	°C
Shutdown Hysteresis	T_{OTS_HY}	SR0.D[2] → 0 (after read status if $T_J < T_{OTS - OTS_HY}$)	−	20	−	°C
Shutdown Filter Time	t_{OTDGL}		−	11.9	−	µs

5. Min/Max values are valid for the stated temperature range unless noted otherwise. Min/Max values are guaranteed by test, design or statistical correlation
6. No production test
7. These values, measured in production via test mode, result in values that are t_{SYNC} longer than the stated values. The specification limits shall therefore be: (t_{CAL_PCx} Typ + t_{SYNC} Typ) ±20%, (t_{CAL_DLYx} Typ + t_{SYNC} Typ) ±20%, and (t_{DLYX} Typ + t_{SYNC} Typ) ±20%.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

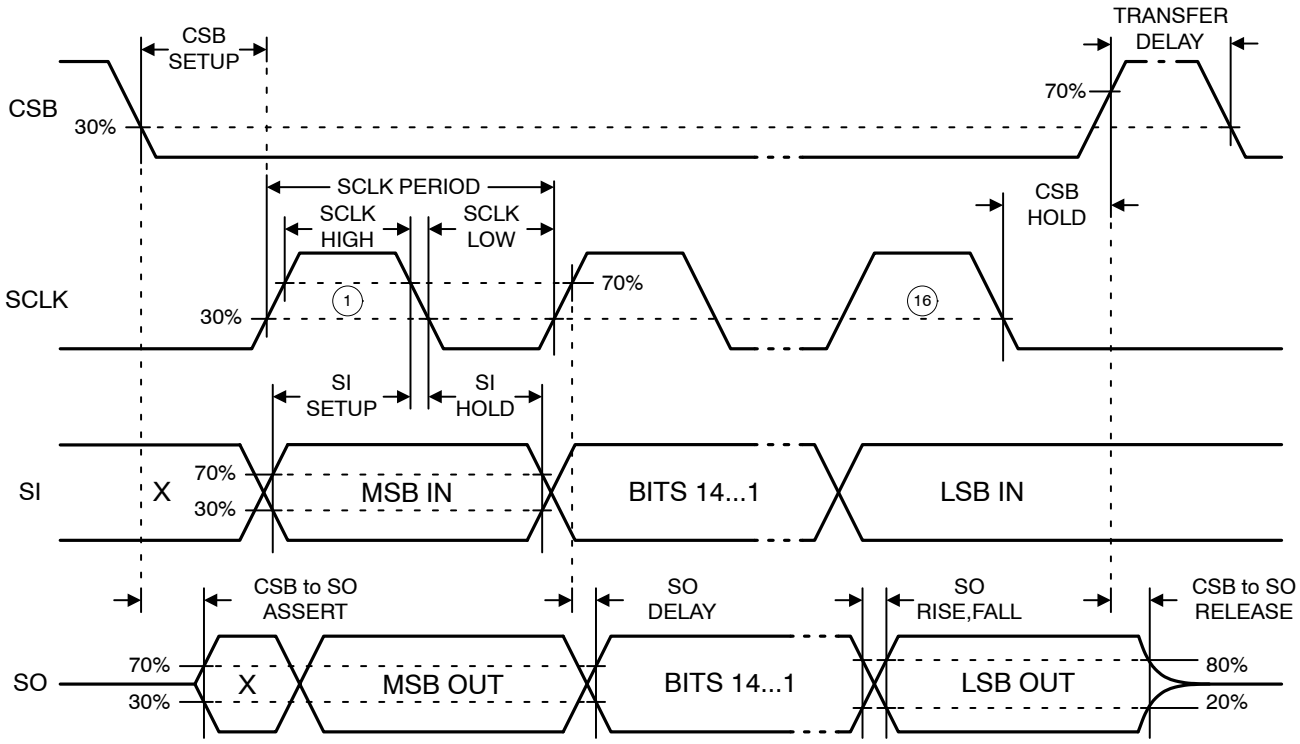


Figure 4. SPI Timing

DETAILED OPERATING DESCRIPTION

Power Supply

The power supply block provides:

- all internal supply and reference voltages;
- all internal bias and reference currents;
- VCC power−on reset (POR) and VS under/over−voltage lockout signals.

The analog and power portions of the device (reference voltages/currents, charge pump, low−side gate drivers, etc.) are supplied from the VS terminal. Each of the low−side gate driver outputs (GLx) is supplied from VS via an individual buffer (source follower) with voltage limit functionality. The high−side gate driver outputs (GHx) are supplied from a regulated charge pump.

The logic core and the SPI communication interface are supplied from the VCC terminal in order to achieve a high frequency operation by use of external bypass capacitors. In case of breakdown of the external voltage regulator, the device can be protected by use of an external voltage limiter, which must limit the maximum voltage at the VCC terminal to VCC_{MAX} (see § *MAXIMUM RATINGS*).

The outputs are disabled during device initialization at power−up via an interlock between VS and VCC and such that no control is available until after VCC > VCC_{PORR} (see § *Electrical Characteristics: VCC Supply*). Reverse battery protection for VS and the VCC regulator is provided externally by the application (see Figure 2).

The device is initialized at power−up into a reduced power state (CR1.DRV_EN = 0, see § *SPI Control Set*):

- the charge pump is disabled;
- all gate drive currents are disabled;
- gate pull−down structures are enabled;
- HBx diagnostic test currents are available (see § *OFF−state Monitoring of Half−bridge Drivers*).

The device is placed into a full power state when CR1.DRV_EN = 1.

Multiple GND pins are used in order to avoid loss of GND due to a single−point failure, to improve ESD capability, and to improve the VDS overload protection performance of the device.

Charge Pump

A regulated charge pump circuit in single−stage / complementary−phase configuration is implemented. The charge pump is sized to drive up 2 high−side drivers in PWM operation ($f_{PWM} \leq 25$ kHz).

The topology utilizes 2 external pump capacitors and an external buffer capacitor (see Figure 2) to supply:

- the high−side gate driver outputs (GHx);
- an optional external reverse protection power MOSFET;
- an optional external security switch power MOSFET.

Table 1 gives suggested values for the external pump and buffer capacitors to support the charge pump DC loading while maintaining good transient response and regulation stability.

Table 1. SUGGESTED CHARGE PUMP CAPACITORS

DC Load (mA)	Pump Capacitors C1, C2 (nF)	Buffer Capacitor CCP (nF)
1.0	100	220
7.5	220	470
15.0	470	1000

The device is initialized at power−up into a reduced power state and the charge pump disabled. The charge pump is controlled by SPI command via the CR1.DRV_EN bit (see Table 7) and the charge pump is:

- disabled when CR1.DRV_EN=0;
- enabled when CR1.DRV_EN=1.

The optional external reverse protection and security switches are connected to the charge pump buffer capacitor through the switched charge pump (CPSW) output. The output is controlled by SPI command via the CR1.CP_SW bit (see Table 7). The CPSW output is:

- disabled (the reverse and security MOSFETs are turned OFF) when CR1.CP_SW=0;
- enabled (the reverse and security MOSFETs are turned ON) when CR1.CP_SW=1.

The charge pump is internally monitored to ensure safe operation of the charge pump circuit and the high−side driver outputs (see § *Protection and Diagnosis − Charge Pump Monitoring*). Due to the single stage configuration the charge pump provides the following output characteristics (see Figure 5, Figure 6, § *SPI Diagnosis Set* and § *Electrical Characteristics: Charge Pump*):

- $V(CP, VS) < CP_{FAIL}$
  SR0.CPF $\rightarrow$ 1
  the GHx and GLx outputs are shut down to prevent damage to the external power MOSFETs;
- $VS < VS_{PWM}$
  SR0.CPL $\rightarrow$ 1
  the CP output voltage follows the VS voltage (the regulation saturates) with a maximum drop voltage per the equation $V(CP, VS) = VS - CP_{DROP}$;
- $CP_{FAIL} < V(CP, VS) < CP_{LOW}$
  SR0.CPL $\rightarrow$ 1
- $VS_{PWM} \leq VS \leq VS_{OVSDR}$
  the charge pump delivers a regulated output voltage $V(CP, VS) = CP_{REG}$ and PWM operation of the GHx outputs is allowed;

- VS_{OVSDF} < VS < VS(CP_{OV})
  the charge pump including the CPSW output is functional, but the GHx outputs are shut down;
- VS > VS(CP_{OV})
  the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

In the case of VS overvoltage, the charge pump automatically resumes normal operation when the VS voltage returns to below $CP_{OV} - CP_{OV_HYS}$. In the case of VS < VS_{PWM} or V(CP, VS) < CP_{LOW} it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.

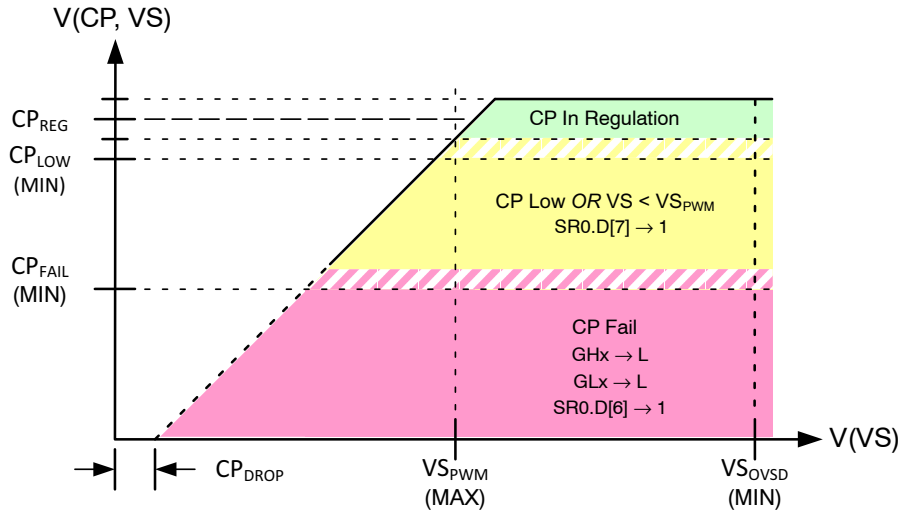


Figure 5. Charge Pump Characteristics

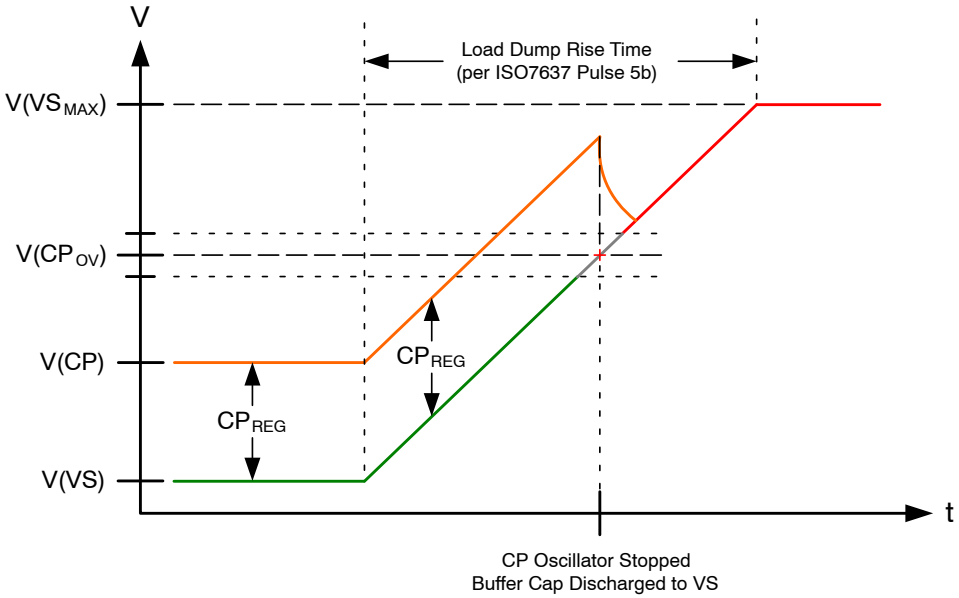


Figure 6. Charge Pump Overvoltage Behavior

SPI Interface

A full−duplex synchronous serial data transfer interface (SPI) is used to control the device and provide diagnosis during normal operation. Daisy chain capability of the interface is implemented in order to minimize circuit expenditure and communication efforts. The SPI protocol utilizes 16−bit data words (B15 = MSB). The idle state of SCLK is low and the SI data must be stable before the falling edge of SCLK (“legacy mode 1”: CPOL=0, CPHA=1).

The interface consists of 4 I/O lines with 5V CMOS logic levels and termination resistors (see Figure 7, Figure 2):

- the active−low CSB enables the SPI interface;
- the SCLK pin clocks the internal shift registers of the device;
- the SI pin receives data of the input shift registers MSB first;
- the SO pin sends data of the output shift registers MSB first.

The device offers the following SPI communication error checks in order to protect the application from unintended motor activation:

- protocol length error (modulo 16);
- no edges on SCLK during a CSB period;
- an undefined SPI command (not used bits must be set to logic 0);
- watchdog (WD) toggle (the internal watchdog bit (CRx.WD) must be toggled with each SPI message);
- WD timeout (the WD bit must be toggled before the internal watchdog timeout is reached).

An SI pin stuck−at condition during a CSB period is detected by a WD toggle error. A VCC under−voltage condition is directly blocking the complete SPI functionality via the VCC_{PORF} signal.

The length of the watchdog timeout is SPI programmable (see § *SPI Control Set* and § *Electrical Characteristics: Watchdog Timer*) in order to facilitate module boot loader programming. The timeout setting is controlled by the CR1.WD_CFG bit:

- when CR1.WD_CFG=0 (default setting) the WD timeout is t_{WD} = 25 ms;
- when CR1.WD_CFG=1 the WD timeout is t_{WD} = 500 ms.

The first WD bit value sent after VCC POR or wake−up must be WD = 0 in the first frame, then WD = 1 in the next.

A correct communication is reported when bit SR0.SPIF = 0 and the device is in **NORMAL MODE** (NM) when bit SRx.NM = 1. The device enters **FAILSAFE MODE** immediately in the event of an SPI communication error (see § *Operating Modes*).

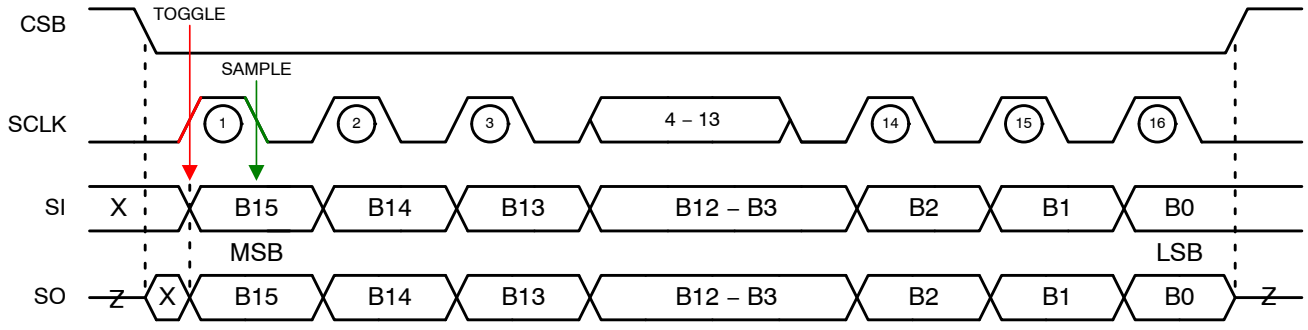
Serial Data and SPI Register Structures

The input and output message formats of the implemented SPI protocol are as shown in the following tables. In the descriptions in the following sections, it is implied that the frame length is correct and that the WD bit has been properly toggled when sending and receiving SPI messages. Please also note that the SPI hardware protocol is a “frame−behind” response type, i.e. the requested data is delivered in the next frame.

SPI Control Set

The first 4 bits (D15 ... D12) serve as address bits, while 12 bits (D11 ... D0) are used as data bits. The D11 bit is the WD toggle bit: A SPI fail is detected if the bit is not toggled within the WD timeout. The D10 bit may be used as an extended address in some messages.

All Control Register (CRx) bits are initialized to logic 0 after a reset. The predefined value is off / inactive unless otherwise noted. The SPI control set (input data map) and input data structure prototype are shown in the following tables.



Note: SPI Legacy Mode 1; X=Don’t Care, Z=Tri−State

Figure 7. SPI Communication Frame Format

Table 2. SPI INPUT DATA FORMAT

Command Input Message Format															
MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A3	A2	A1	A0	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4−bit REGISTER ADDRESS				WATCH DOG	11−bit INPUT DATA										

Table 3. INPUT DATA STRUCTURE PROTOTYPE

Input Data Prototype												
CRx	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	?	?	?	?	?	?	?	?	?	?	?	?

Table 4. SPI INPUT REGISTER DEFINITIONS

Defined Command Input Registers (CRx)							
		D15	D14	D13	D12	D11	D10
Register Name	**Alias**	**A3**	**A2**	**A1**	**A0**	**WD**	**D10**
Status Output Mode & HBx Enable	CR0	0	0	0	0	WD	D10
HBx Mode	CR1	0	0	0	1		D10
HBx PWM Control	CR2	0	0	1	0		0
HBx PWM Mode A	CR3A	0	0	1	1		0
HBx PWM Mode B	CR3B						1
HBx Calibration Control	CR4	0	1	0	0		D10
HB1 Configuration A	CR5A	0	1	0	1		0
HB1 Configuration B	CR5B						1
HB2 Configuration A	CR6A	0	1	1	0		0
HB2 Configuration B	CR6B						1
HB3 Configuration A	CR7A	0	1	1	1		0
HB3 Configuration B	CR7B						1
HB4 Configuration A	CR8A	1	0	0	0		0
HB4 Configuration B	CR8B						1
HB5 Configuration A	CR9A	1	0	0	1		0
HB5 Configuration B	CR9B						1
HB6 Configuration A	CR10A	1	0	1	0		0
HB6 Configuration B	CR10B						1
HB7 Configuration A	CR11A	1	0	1	1		0
HB7 Configuration B	CR11B						1
HBx Diagnosis	CR12	1	1	0	0		0
Not Used	CR13	1	1	0	1		0
HBx PWM De−glitch	CR14	1	1	1	0		0
Test Mode	CR15	1	1	1	1		D10

NOTE: Half−bridge gate drive settings must only be changed when HBx is in tri−state (HB_ENx = 0);
Gate drive pre−charge time settings must only be changed in single increments (i.e. 00 to 01, 01 to 10 etc.).

Table 5. CR0: STATUS OUTPUT MODE & HBx ENABLE REGISTER

CR0	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	SRA_MODE	SRA[2:0]			HB_EN7 … HB_EN1						

Table 6. CR0 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
SRA_MODE	0	The Status Register Address selected via CR0.SRA [2:0] will be used for a single read command. The address always points to SR0 after the read (default state).
	1	The Status Register Address selected via SRA [2:0] will be used for the next and all further read commands until a new address is selected.
SRA[2:0]	000	SR0 data is returned in the next frame (default state).
	001	SR1 data is returned in the next frame.
	010	SR2 data is returned in the next frame.
	011	SR3 data is returned in the next frame.
	100	SR4 data is returned in the next frame.
	101	SR5 data is returned in the next frame.
	110	SR6 data is returned in the next frame.
	111	SR7 data is returned in the next frame.
HB_ENx	0	HBx output disabled (default state).
	1	HBx output enabled.

Table 7. CR1: HBx MODE CONTROL REGISTER

CR1	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	DRV_EN	CP_SW	WD_CFG	HB_CFG7	HB_MODE7 … HB_MODE1						

Table 8. CR1 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
DRV_EN	0	Charge pump and gate drive currents are disabled (default state).
	1	Charge pump and gate drive currents are enabled.
CP_SW	0	Charge pump switched output is OFF: CPSW = Hi−Z (default state).
	1	Charge pump switched output is ON: CPSW = V(CP−VS).
WD_CFG	0	Watch dog timeout = 25 ms (default state).
	1	Watch dog timeout = 500 ms.
HB_CFG7	0	Half−bridge configuration (default state).
	1	Split configuration (see Figure 13 and Figure 16).
HB_MODEx	0	Low−side pre−driver active (default state).
	1	High−side pre−driver active.

Table 9. CR2: HBx PWM CONTROL REGISTER

CR2	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	HB_PWM7 … HB_PWM1						

Table 10. CR2 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
HB_PWMx	0	Output is in 100% ON mode (default).
	1	Output is in PWM mode.

Table 11. CR3: HBx PWM MODE CONTROL REGISTER

CR3A	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	PWM5[1:0]		PWM4[1:0]		PWM3[1:0]		PWM2[1:0]		PWM1[1:0]	
CR3B	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	1	0	0	0	0	0	0	PWM7[1:0]		PWM6[1:0]	

Table 12. CR3 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
PWMx[1:0]	00	Output PWM source is input PWM1 (default).
	01	Output PWM source is input PWM2.
	10	Output PWM source is input PWM3.
	11	Output PWM source is input PWM4.

Table 13. CR4: HBx CALIBRATION CONTROL REGISTER

CR4	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	CAL_DLY[3:0]				CAL_PC[3:0]				CAL_SEL[2:0]		

Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
CAL_DLY[3:0]	0000	Delay time: end of rising|falling slope 0.35 μs (default).
	0001	Delay time: end of rising|falling slope 0.55 μs.
	0010	Delay time: end of rising|falling slope 0.75 μs.
	0011	Delay time: end of rising|falling slope 0.95 μs.
	0100	Delay time: end of rising|falling slope 1.15 μs.
	0101	Delay time: end of rising|falling slope 1.35 μs.
	0110	Delay time: end of rising|falling slope 1.55 μs.
	0111	Delay time: end of rising|falling slope 1.75 μs.
	1000	Delay time: end of rising|falling slope 1.95 μs.
	1001	Delay time: end of rising|falling slope 2.15 μs.
	1010	Delay time: end of rising|falling slope 2.35 μs.
	1011	Delay time: end of rising|falling slope 2.55 μs.
	1100	Delay time: end of rising|falling slope 2.75 μs.
	1101	Delay time: end of rising|falling slope 2.95 μs.
	1110	Delay time: end of rising|falling slope 3.15 μs.
	1111	Delay time: end of rising|falling slope 3.35 μs.
CAL_PC[3:0]	0000	Pre−charge time: start of rising|falling slope 50 ns (default).
	0001	Pre−charge time: start of rising|falling slope 150 ns.
	0010	Pre−charge time: start of rising|falling slope 250 ns.
	0011	Pre−charge time: start of rising|falling slope 350 ns.
	0100	Pre−charge time: start of rising|falling slope 450 ns.
	0101	Pre−charge time: start of rising|falling slope 550 ns.
	0110	Pre−charge time: start of rising|falling slope 650 ns.
	0111	Pre−charge time: start of rising|falling slope 750 ns.
	1000	Pre−charge time: start of rising|falling slope 850 ns.
	1001	Pre−charge time: start of rising|falling slope 950 ns.
	1010	Pre−charge time: start of rising|falling slope 1050 ns.
	1011	Pre−charge time: start of rising|falling slope 1150 ns.
	1100	Pre−charge time: start of rising|falling slope 1250 ns.
	1101	Pre−charge time: start of rising|falling slope 1350 ns.
	1110	Pre−charge time: start of rising|falling slope 1450 ns.
	1111	Pre−charge time: start of rising|falling slope 1550 ns.

Table 14. CR4 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
CAL_SEL[2:0]	000	Calibration unit disabled (default).
	001	Select output HB1.
	010	Select output HB2.
	011	Select output HB3.
	100	Select output HB4.
	101	Select output HB5.
	110	Select output HB6.
	111	Select output SH7.

Table 15. CR5A – CR11A: HBx CONFIGURATION A REGISTER

CR5A – CR11A	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	BLANKx[1:0]		I_PCFx[2:0]			I_PCRx[2:0]			T_PCx[1:0]	

Table 16. CR5A – CR11A INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
BLANKx[1:0]	00	Select cross−conduction blanking time 1 μs (default).
	01	Select cross−conduction blanking time 2 μs.
	10	Select cross−conduction blanking time 3 μs.
	11	Select cross−conduction blanking time 4 μs.
I_PCFx[2:0]	000	Select falling slope pre−charge current 28.88mA (default).
	001	Select falling slope pre−charge current 35.63 mA.
	010	Select falling slope pre−charge current 42.00 mA.
	011	Select falling slope pre−charge current 48.38 mA.
	100	Select falling slope pre−charge current 55.13mA.
	101	Select falling slope pre−charge current 61.50 mA.
	110	Select falling slope pre−charge current 67.88 mA.
	111	Select falling slope pre−charge current 74.63 mA.
I_PCRx[2:0]	000	Select rising slope pre−charge current 1.50 mA (default).
	001	Select rising slope pre−charge current 5.25 mA.
	010	Select rising slope pre−charge current 8.63 mA.
	011	Select rising slope pre−charge current 12.38 mA.
	100	Select rising slope pre−charge current 16.50 mA.
	101	Select rising slope pre−charge current 20.25 mA.
	110	Select rising slope pre−charge current 24.00 mA.
	111	Select rising slope pre−charge current 28.13 mA.
T_PCx[1:0]	00	Select rising/falling slope pre−charge time 100 ns (default).
	01	Select rising/falling slope pre−charge time 200 ns.
	10	Select rising/falling slope pre−charge time 300 ns.
	11	Select rising/falling slope pre−charge time 400 ns.

Table 17. CR5B – CR11B: HBx CONFIGURATION B REGISTER

CR5B – CR11B	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	1	VDSx[2:0]			T_DLY[3:0]				SR_CTRL[2:0]		

Table 18. CR5B – CR11B INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
VDSx[2:0]	000	Select VDS sense threshold 300 mV (default).
	001	Select VDS sense threshold 400 mV.
	010	Select VDS sense threshold 500 mV.
	011	Select VDS sense threshold 600 mV.
	100	Select VDS sense threshold 700 mV.
	101	Select VDS sense threshold 800 mV.
	110	Select VDS sense threshold 900 mV.
	111	Select VDS sense threshold 1000 mV.
T_DLY[3:0]	0000	Select VDS overload detect delay 1.05 μs (default).
	0001	Select VDS overload detect delay 1.65 μs.
	0010	Select VDS overload detect delay 2.25 μs.
	0011	Select VDS overload detect delay 2.85 μs.
	0100	Select VDS overload detect delay 3.45 μs.
	0101	Select VDS overload detect delay 4.05 μs.
	0110	Select VDS overload detect delay 4.65 μs.
	0111	Select VDS overload detect delay 5.25 μs.
	1000	Select VDS overload detect delay 5.85 μs.
	1001	Select VDS overload detect delay 6.45 μs.
	1010	Select VDS overload detect delay 7.05 μs.
	1011	Select VDS overload detect delay 7.65 μs.
	1100	Select VDS overload detect delay 8.25 μs.
	1101	Select VDS overload detect delay 8.85 μs.
	1110	Select VDS overload detect delay 9.45 μs.
	1111	Select VDS overload detect delay 10.05 μs.
SR_CTRL[2:0]	000	Select rising/falling slope slew phase current 1.5 mA (default).
	001	Select rising/falling slope slew phase current 2.25 mA.
	010	Select rising/falling slope slew phase current 3.38 mA.
	011	Select rising/falling slope slew phase current 5.25 mA.
	100	Select rising/falling slope slew phase current 7.88 mA.
	101	Select rising/falling slope slew phase current 11.63 mA.
	110	Select rising/falling slope slew phase current 17.25 mA.
	111	Select rising/falling slope slew phase current 25.50 mA.

Table 19. CR12: HBx DIAGNOSIS CONTROL REGISTER

CR12	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	TST_LS7	TST_LS5	TST_LS3	TST_LS1	TST_HS7	TST_HS5	TST_HS3	TST_HS1

Table 20. CR12 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
TST_LSx	0	Disable low−side test current (default).
	1	Enable low−side test current.
TST_HSx	0	Disable high−side test current (default).
	1	Enable high−side test current.

Table 21. CR14: HBx PWM DE−GLITCH

CR14	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	DGL7	DGL6	DGL5	DGL4	DGL3	DGL2	DGL1

Table 22. CR14 INSTRUCTION DEFINITIONS

Mnemonic	Value	Comment
DGLx	0	Type 1 de−glitch: $t_{PWM_DGL} = t_{BLANKx} + t_{PRCx} + t_{DLYx}$ (default).
	1	Type 2 de−glitch: $t_{PWM_DGL} = t_{PRCx} + t_{DLYx}$

Table 23. CR15: TEST MODE REGISTER

CR15	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	Factory Use Only										

SPI Diagnosis Set

The first 3 bits D[15:13] serve as address bits, while the 13 bits D[12:0] are used as data bits. Output data for “not used” register adresses is D[11:0] = 0. The address of the Status Register (SRx) accessed for status information to be retrieved via a subsequent SPI frame is selected by the control register bits CR0.SRA_MODE and CR0.SRA[2:0] (see Table 5, Table 6).

Two different reading modes are provided depending on the SRA_MODE bit:

- when CR0.SRA_MODE = 0, the SRx address selected via bits CR0.SRA[2:0] will be used for a single status read command and the SR address returns to SR0 (device status register, default state) after reading;
- when CR0.SRA_MODE = 1, the SRx address selected via bits CR0.SRA[2:0] will be used for the next and all further status read commands until a new address or mode is selected.

The default reading mode and address after VCC POR or wake−up is CR0.SRA_MODE = 0, CR0.SRA[2:0] = 00.

All status diagnosis bits are initialized to logic 0 after a reset event and in normal operation except:

- the **NORMAL MODE** (NM) bit indicates **NORMAL MODE** when SRx.NM = 1;
- the Register Clear Flag (RCF) bit is set (SR0.RCF = 1) after a mode change to **NORMAL MODE** (see § *Operating Modes*).

The RCF bit indicates that all input and output registers were initialized; the bit is cleared after SR0 is read.

All status diagnosis bits are latched with the exception of the SR5.D[3:0] bits (see § *Output Status Monitoring*). To de−latch a diagnosis:

- the referring failure has to be removed;
- the referring failure bit has to be read by SPI diagnosis.

Refer to § *Protection and Diagnosis* to restart the outputs after a fault condition. The SPI diagnosis set (output data map) and output data structure prototype are shown in the following tables.

Table 24. SPI OUTPUT DATA FORMAT

Status Output Message Format															
MSB															LSB
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A2	A1	A0	NM	D11	D10	D9	D8	D7	D5	D5	D4	D3	D2	D1	D0
3−bit REGISTER ADDRESS			NORMAL MODE	12−bit OUTPUT DATA											

Table 25. OUTPUT DATA STRUCTURE PROTOTYPE

Output Data Prototype													
SRx	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	?	?	?	?	?	?	?	?	?	?	?	?

Table 26. SPI OUTPUT REGISTER DEFINITIONS

Defined Status Output Registers (SRx)					
		D15	D14	D13	D12
Register Name	**Alias**	**A2**	**A1**	**A0**	**NM**
Device Status	SR0	0	0	0	NM
HB 1…6 Status Monitor	SR1	0	0	1	
HB 7 Status & VDS Monitors	SR2	0	1	0	
HB 1…6 VDS Monitor	SR3	0	1	1	
HBx Calibration Result	SR4	1	0	0	
SH7, DL7 & HB 1…6 Output Status	SR5	1	0	1	
Not Used	SR6	1	1	0	
Device ID/Test Mode	SR7	1	1	1	

Table 27. SR0: DEVICE STATUS REGISTER

SR0	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	TM	RCF	FSM	SPIF	CPL	CPF	UVF	OVF	0	0	HB_QSB	0

Table 28. SR0 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
TM	0	Test mode inactive (default).
	1	Test mode active.
RCF	0	Registers not cleared (command input and status output registers).
	1	Registers cleared (after mode change to “NORMAL”).
FSM	0	FSM input pin = 0 (FSM not asserted).
	1	FSM input pin = 1 (FSM asserted).
SPIF	0	SPI message correct.
	1	SPI message failure.
CPL	0	Charge pump in regulation
	1	V(CP, VS) < CP_{LOW} –*OR*– VS < VSPWM (Charge Pump Low).
CPF	0	Half bridge high−side pre−driver activation allowed.
	1	Half bridge high−side pre−driver activation not allowed (Charge Pump Fail).
UVF	0	VS supply in normal range.
	1	VS supply below normal range.
OVF	0	VS supply in normal range.
	1	VS supply above normal range.
D3	0	Not used.
D2	0	Not used.
HB_QSB	0	Quick Status Bit: VDS normal − no overload detected.
	1	Quick Status Bit: VDS failure − overload detected (VDS_Hx or VDS_Lx).
D0	0	Not used.

Table 29. SR1: HBx STATUS MONITOR REGISTER

SR1	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	SWH6	SWL6	SWH5	SWL5	SWH4	SWL4	SWH3	SWL3	SWH2	SWL2	SWH1	SWL1

Table 30. SR1 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
SWHx	0	GHx output is “low” (default).
	1	GHx output is “high”.
SWLx	0	GLx output is “low” (default).
	1	GLx output is “high”.

Table 31. SR2: HB 7 STATUS & VDS MONITOR REGISTER

SR2	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	0	0	0	0	0	VDS_H7	VDS_L7	SWH7	SWL7

Table 32. SR2 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
VDS_H7	0	SH7 high−side power switch normal – no overload detected (default).
	1	SH7 high−side power switch failure – overload detected.
VDS_L7	0	DL7 low−side power switch normal – no overload detected (default).
	1	DL7 low−side power switch failure –overload detected.
SWH7	0	GH7 output is “low” (default).
	1	GH7 output is “high”.
SWL7	0	GL7 output is “low” (default).
	1	GL7 output is “high”.

Table 33. SR3: HBx VDS MONITOR REGISTER

SR3	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	VDS_H6	VDS_L6	VDS_H5	VDS_L5	VDS_H4	VDS_L4	VDS_H3	VDS_L3	VDS_H2	VDS_L2	VDS_H1	VDS_L1

Table 34. SR3 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
VDS_Hx	0	HBx high−side power switch normal – no overload detected (default).
	1	HBx high−side power switch failure – overload detected.
VDS_Lx	0	HBx low−side power switch normal – overload detected (default).
	1	HBx low−side power switch failure – overload detected.

Table 35. SR4: HBx CALIBRATION RESULT REGISTER

SR4	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	CAL_READY	CAL_DLY_R[1:0]		CAL_PC_R[1:0]		CAL_DLY F[1:0]		CAL_PC _F[1:0]	

Table 36. SR4 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
CAL_READY	0	Calibration result not ready or has been read via SPI (default).
	1	Calibration is successfully performed with a valid result (the bit is reset after SPI read command).
CAL_DLY_R[1:0]	00	Rising slope result: VHBx < 15% (default).
	01	Rising slope result: 15% < VHBx < 85%.
	10	Rising slope result: 85% < VHBx < 95%.
	11	Rising slope result: VHBx >95%.
CAL_PC_R[1:0]	00	Rising slope result: VHBx < 5% (default).
	01	Rising slope result: 5% < VHBx < 15%.
	10	Rising slope result: 15% < VHBx < 85%.
	11	Rising slope result: VHBx > 85%.

Table 36. SR4 RESPONSE DEFINITIONS

CAL_DLY_F[1:0]	00	Falling slope result: VHBx > 85% (default).
	01	Falling slope result: 85% > VHBx > 15%.
	10	Falling slope result: 15% > VHBx > 5%.
	11	Falling slope result: VHBx < 5%.
CAL_PC _F[1:0]	00	Falling slope result: VHBx > 95% (default).
	01	Falling slope result: 95% > VHBx > 85%.
	10	Falling slope result: 85% > VHBx > 15%.
	11	Falling slope result: VHBx < 15%.

Table 37. SR5: HBx OUTPUT STATUS REGISTER

SR5	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	0	SH_OUT7	DL_OUT7	HB_OUT6 … HB_OUT1					

Table 38. SR5 RESPONSE DEFINITIONS

Mnemonic	Value	Comment
SH_OUT7	0	Output < VHB_{THR} (default).
	1	Output > $VHB_{THR.}$
DL_OUT7	0	Output < VHB_{THR} (default).
	1	Output > $VHB_{THR.}$
HB_OUTx7	0	Output < VHB_{THR} (default).
	1	Output > $VHB_{THR.}$

Table 39. SR7: TEST MODE STATUS REGISTER – SR0.TM = 1: TEST MODE FORMAT

SR7	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	Factory Use Only											

Table 40. SR7: DEVICE ID/TEST MODE STATUS REGISTER – SR0.TM = 0: DEVICE ID FORMAT

SR7	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	DEV_ID[11:9]			DEV_ID[8:6]			DEV_ID[5:3]			DEV_ID[2:0]		

Table 41. SR7 RESPONSE DEFINITIONS: DEVICE ID FORMAT

Mnemonic	ID Type	Value	Comment
DEV_ID[11:9]	Device Name	000	NCV7547
		001	NCV7544
		010	NCV7546
		011–111	etc.
DEV_ID[8:6]	Generation	000	Generation 0
		001–110	Generation 1 etc.
		111	Generation 0 (NCV7547)
DEV_ID[5:3]	Silicon Revision	000	First Silicon (REV_n.m)
		001	Second Silicon (REV_n+1.m)
		010–111	etc.
DEV_ID[2:0]	Mask Revision	000	Initial Mask Revision (REV_n.m)
		001	First Mask Revision (REV_n.m+1)
		010–111	etc.

When not in test mode (SR0.TM = 0), a status request via CR0.D[10:7] returns SR7.D[11:0] = DEV_ID[11:0] as defined in Table 41. The default content of SR7 after VCC POR or wake−up is SR7.D[11:0] = 0.

The DEV_ID[5:0] revision value may be changed based on whether the entire die (silicon) or intermediate layer (mask) is affected. The revisions can be e.g. classified accordingly:

- silicon revision: defined area changed (isolation pocket or other boundary, bond pad etc. changed/moved) or digital core changed (isolation pocket changed or unchanged);
- mask revision: interconnect changed (metal and/or polysilicon/contact/via).

The mask revision value is set to DEV_ID[2:0] = 000 whenever the die revision is incremented. Table 42 shows how the value encoding scheme is used to indicate the device revision level.

Table 42. DEVICE REVISION LEVEL ENCODING

Silicon Revision		Mask Revision	
DEV_ID[5:3]	LEVEL	DEV_ID[2:0]	LEVEL
000	A	000	0
001	B	001	1
010	C	010	2
011	D	011	3
100	E	100	4
101	F	101	5
110	G	110	6
111	H	111	7

Half−bridge Gate Drivers

The half−bridge drivers are used to control the gates of external logic−level NMOS power switches. Drivers HB1 … HB6 are dedicated to e.g. motor control – the switches are normally connected in half−bridge configuration. HB7 is dedicated to e.g. heater control – the switches are normally connected independently in a split configuration but may be optionally connected in a half−bridge configuration (see Figure 2). The device is initialized at power−up into a reduced power state (CR1.DRV_EN = 0, see Table 7, Table 8):

- the charge pump is disabled;
- all gate drive currents are disabled.
- HBx diagnostic test currents are available (see § *Monitoring of Half−bridge Drivers in OFF−state*).

The device is placed into a full power state when CR1.DRV_EN = 1. The half−bridges are held in high−impedance state (external NMOS are off) via gate pull−down structures which are activated during power−up, while in reduced power state, or when in sleep mode.

Control of Half−bridge Drivers

The operation of the drivers is controlled by SPI configuration individually for each driver. All half−bridges can be operated in 100% “ON” mode as well as in PWM mode.

The control schema for HB1 … HB7 in half−bridge configuration and for HB7 in split configuration is shown in Table 44 (see also § *SPI Control Set*).

The CR0.HB_ENx bits are used to enable the operation of the selected half−bridges and to re−start the drivers after a fault condition:

- when CR0.HB_ENx=0, the GHx and GLx outputs are disabled (i.e. VGS ≈ 0 V);
- when CR0.HB_ENx=1, the GHx and GLx outputs are enabled.

The CR1.HB_CFG7 bit is used to enable the split configuration of half−bridge HB7:

- when CR1.HB_CFG7=0, HB7 is in operating in half−bridge configuration;
- when CR1.HB_CFG7=1, HB7 is in operating in split configuration.

NOTE: When operating HB7 in split configuration, both the high−side and low−side switches are in ON−state simultaneously. Therefore the CR1.HB_CFG7 bit should only be set to ‘1’ when the application hardware is configured correctly. In case of erratic hardware configuration, VDS overload monitoring protects the external power switches.

The CR1.HB_MODEx bits are used to control the polarity of the selected half−bridge:

- when CR1.HB_MODEx=0, the low−side driver (PDL) is in an ON state (i.e. GLx = VGS ≈ V_{PDLX}, see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*);
- when CR1.HB_MODEx=1, the high−side driver (PDH) is in an ON state (i.e. GHx = VGS ≈ V_{PDHX}, see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*).

The CR2.HB_PWMx bits are used to enable PWM mode control of the selected half−bridge:

- when CR2.HB_PWMx=0, an output is in 100% ON state according to its CR1.HB_MODEx bit;
- when CR2.HB_PWMx=1, an output is in PWM with state according to its CR1.HB_MODEx bit.

The application of a PWM mode selected via the CR2.HB_PWMx bits to the corresponding output is performed asynchronous to the PWMx input (i.e. a change is applied after the rising edge of the CSB signal). Each half−bridge can be controlled in PWM mode by one of the PWMx inputs as selected via the CR3.PWMx[1:0] bits according to Table 43 (see also Table 11, Table 12):

Table 43. CR3A/CR3B: PWM SOURCE SELECTION

PWMx1	PWMx0	PWM Source Selection
0	0	Output PWM source is input PWM1
0	1	Output PWM source is input PWM2
1	0	Output PWM source is input PWM3
1	1	Output PWM source is input PWM4

The application of a selected PWMx input signal routing to the corresponding output is performed asynchronous to the PWMx input (i.e. a change is applied after the rising edge of the CSB signal).

The selected output is controlled via the selected positive−logic PWMx input (see Figure 8):

- when input PWMx=0, the driver defined by its HB_MODEx bit is turned OFF (i.e. VGS ≈ 0 V) and its complementary gate driver is turned ON (i.e. VGS ≈ V_{PDHX} or VGS ≈ V_{PDLX});

Table 44. HBx DRIVER CONTROL

Output	CR0 HB_ENx	CR1 HB_CFG7*	CR1 HB_MODEx	CR2 HB_PWMx	External MOS Power Switches Operation Mode	Comment
HB1...HB7 Half−bridge Configuration	0	X	X	X	HBx “OFF”	Disable (HBx = Hi−Z)
	1	0	0	0	Low−side “ON”	100% “ON”
	1	0	1	0	High−side “ON”	
	1	0	0	1	Low−side PWM	PWM Mode
	1	0	1	1	High−side PWM	
HB7 Split Configuration	1	1	X	0	Low−side & high−side “ON”	100% “ON”
	1	1	0	1	Low−side “ON”, high−side PWM	PWM Mode
	1	1	1	1	High−side “ON”, low−side PWM	

*HB_CFG7 = X for HB1...HB6 operations.

- when input PWMx=1, the driver defined by its HB_MODEx bit is turned ON (i.e. VGS ≈ V_{PDHX} or V_{PDLX}) and its complementary gate driver is turned OFF (i.e. VGS ≈ 0 V).

When multiple PWMx inputs are needed to be active, the scheduled PWM signals should be offset in time to avoid degradation of the VDS overload detection due to crosstalk (see § *Overload Protection*). The minimum offset should be based on the t_{PWM_DGL} times appropriate for the respective channels (see § *Switching Behavior of Half−bridge Drivers*, Figure 10 and Figure 11).

NOTE: The PWM source selection logic does not prevent more than one half−bridge output to be controlled by the same PWMx input.

Switching Behavior of Half−bridge Drivers

The external high−side NMOS switches are controlled with gate pre−charge and slew phases, while the external low−side switches are controlled via simple drive stages supplying a nominal 4x multiple of the selected high−side driver slew current (see Figure 9 and § *Electrical Characteristics: Pre−driver Slope Control)*. The timing for the gate drivers is provided by the digital logic, where the key parameters can be programmed via SPI in order to adapt different MOSFET types and application switching speeds.

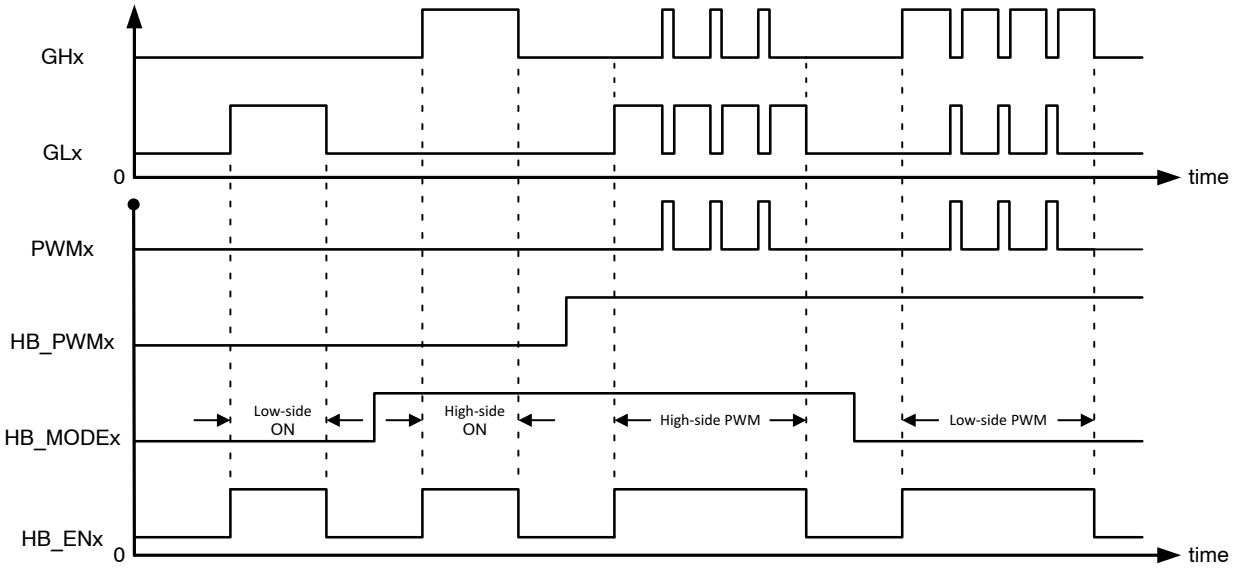
Each individual half−bridge can be programmed via three configuration registers, e.g. CR5A and CR5B for HB1, and CR14 (see § *SPI Control Set*, Table 15 − Table 17 and Table 21, summarized in Table 45):

Table 45. HALF−BRIDGE CONFIGURATION REGISTERS

CR5A − CR11A	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	BLANKx[1:0]		I_PCFx[2:0]			I_PCRx[2:0]			T_PCx[1:0]	

CR5B − CR11B	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	1	VDSx[2:0]			T_DLY[3:0]				SR_CTRL[2:0]		

CR14	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	0	0	0	0	DGL7	DGL6	DGL5	DGL4	DGL3	DGL2	DGL1



Note 1. GLx and GHx are for the same HBx output control (e.g. HB1: GL1, GH1).
Note 2. GLx and GHx time offset from PWMx via adaptive PWM input de-glitch not shown.

Figure 8. Gate Drive Operation in PWM Mode

For each individual half−bridge:

- cross−conduction blanking time is selected via the BLANKx[1:0] bits;
- pre−charge current is selected via the I_PCRx[2:0] bits for the rising slope and via the I_PCFx[2:0] bits for the falling slope;
- pre−charge time for both slopes is selected via the T_PCx[1:0] bits;
- slew current for both slopes is selected via the SR_CTRLx[2:0] bits – this parameter controls the external NMOS switches' rise/fall times to adopt proper EMC performance and minimize switching losses;
- VDS overload detection delay is selected via the T_DLYx[3:0] bits – this parameter controls when the VDS overload detection is performed (see § *Overload Protection*);
- VDS overload detection threshold is selected via the VDSx[2:0] bits – this parameter controls the VDS monitoring comparator threshold (see Table 17, Table 18);
- adaptive PWM input de−glitch construction when in half−bridge configuration is selected by DGLx[6:0] bits (see Figure 10, Figure 11, Table 21 and Table 22).

Please refer to § *Electrical Characteristics* for defined blanking (t_{BLANKX}), pre−charge (t_{PRCX}, I_{PRCX_R}, I_{PRCX_F}), slew (I_{SRX}), delay (t_{DLYX}) and VDS threshold (VDS_{THRX}) parametric values.

NOTE: A proper initial switching parameter set (e.g. VDS_{THRX}, t_{PRCX}, I_{PRCX_R}, I_{SRX}, I_{PRCX_F}) for a chosen MOSFET has to be evaluated for a desired switching speed (see also § *Overload Protection*).

When operated in PWM mode, the PWMx input signals are each provided with a symmetrical de−glitch within a half− bridge's control logic. The de−glitch time (t_{PWM_DGL}) is adapted to the SPI settings t_{BLANKX}, t_{PRCX}, t_{DLYX} and DGLx as selected for each channel (see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs & Pre−driver Slope Control*).

The adapted t_{PWM_DGL} avoids mistreatment of the half−bridge drivers by ensuring that a complete turn−on or turn−off sequence is executed (erratic pulse widths are thereby avoided) and assures correct operation of the VDS overload protection (see § *Overload Protection)*.

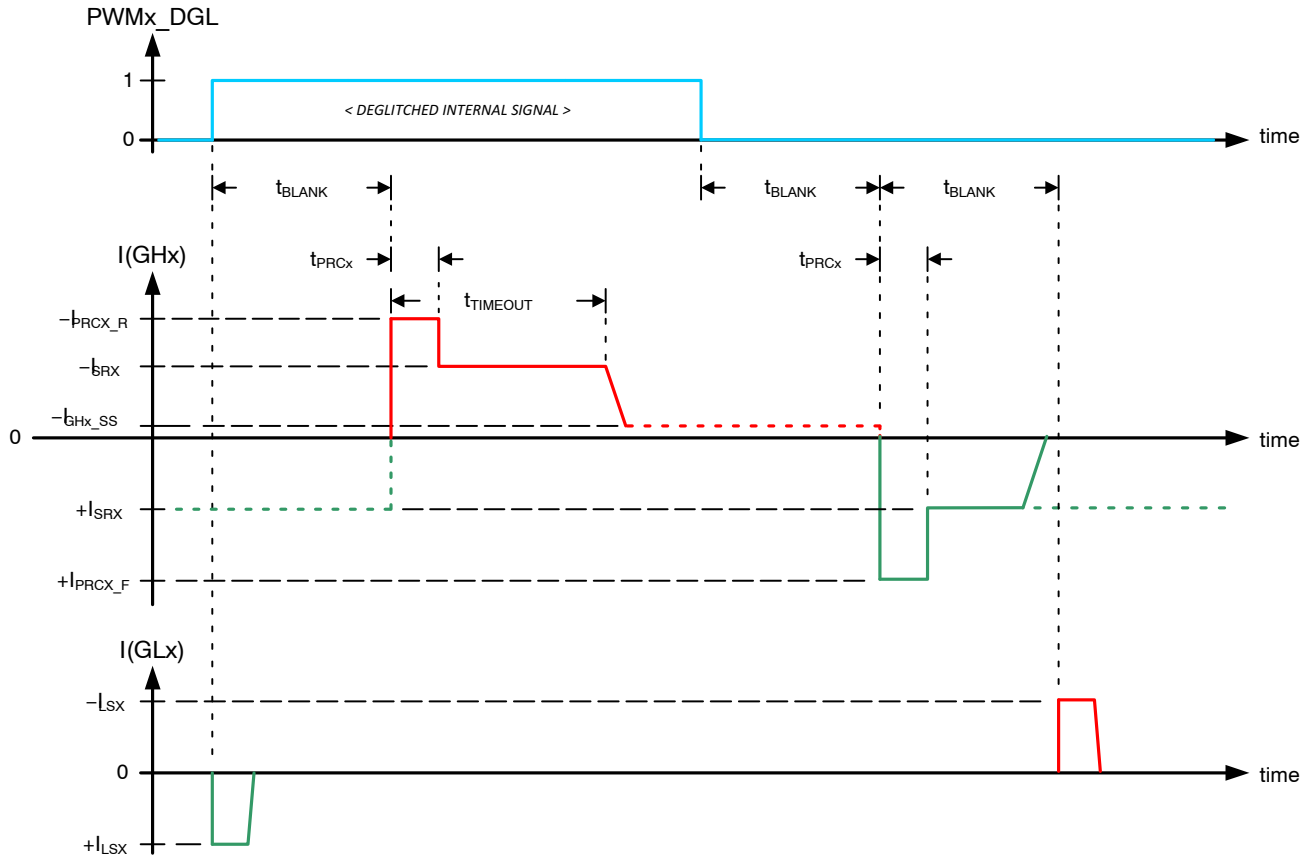


Figure 9. Gate Drive Current Evolution

In order to not overload the charge pump circuit in case of loss of VS or in case of a disconnected security switch, the steady state output current of the high−side gate drivers is limited to I_{GHX_SS} after $t_{TIMEOUT}$ (see I(GHx) in Figure 9 and § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*).

NOTE: Driver turn−ON/OFF via SPI (i.e. CR1.HB_MODEx bits) includes both the pre−charge and slew phases, but adapted de−glitch strategy is not applied.

When operating HB1…HB7 in PWM mode and in half−bridge configuration, type 1 de−glitch is selected when CR14.DGLx = 0 (see Figure 10) and the adapted time is given by:

$$t_{PWM_DGL} = t_{BLANKX} + t_{PRCX} + t_{DLYX} \quad \text{(eq. 1)}$$

Type 2 de−glitch is selected when CR14.DGLx = 1 (see Figure 11) and the adapted time is given by:

$$t_{PWM_DGL} = t_{PRCX} + t_{DLYX} \quad \text{(eq. 2)}$$

When operating HB7 in PWM mode and in split configuration, the adapted time is type 2 (CR14.DGL7 = X).

NOTE: To avoid synchronization issues, the de−glitch type must be selected before beginning PWM of a load.

Once a switching parameter set for EMC optimization and stable VDS overload detection has been chosen, the allowable duty ratio (D) is bounded by the selected adaptive de−glitch type and PWM frequency such that:

$$f_{PWM} \times t_{PWM_{DGL}} \le D \le 1 - \left(f_{PWM} \times t_{PWM_{DGL}}\right) \quad \text{(eq. 3)}$$

When operating HB1…HB7 in PWM mode and in half−bridge configuration, the timing of the gate drivers is according to Figure 12.

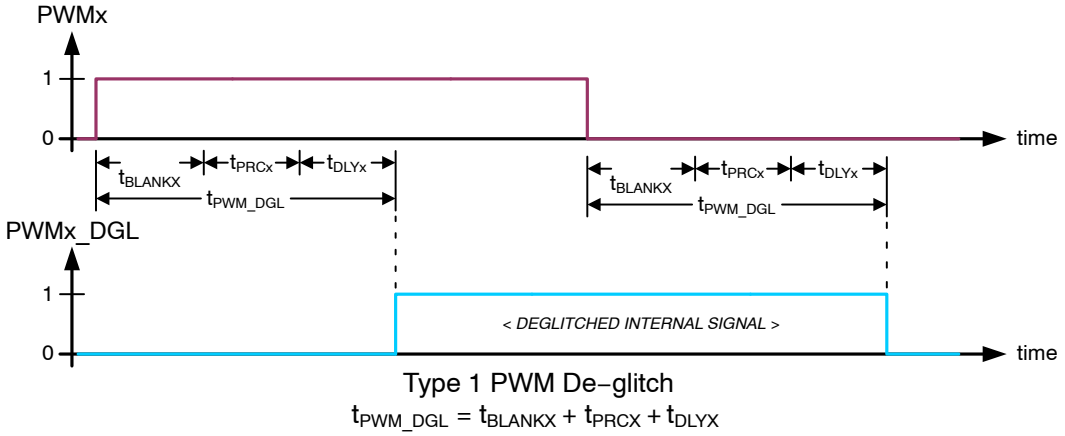


Figure 10. Type 1 PWMx Input De−glitch − CR14.DGLx = 0

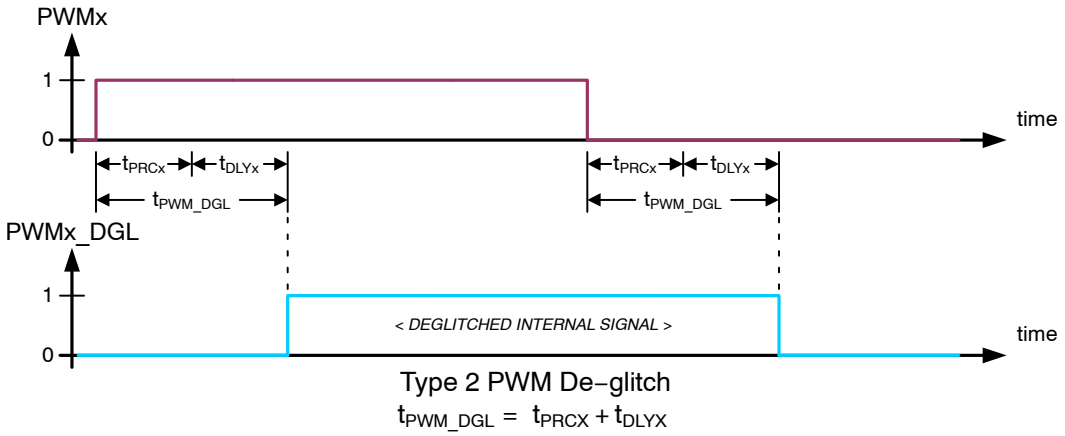


Figure 11. Type 2 PWMx Input De−glitch − CR14.DGLx = 1

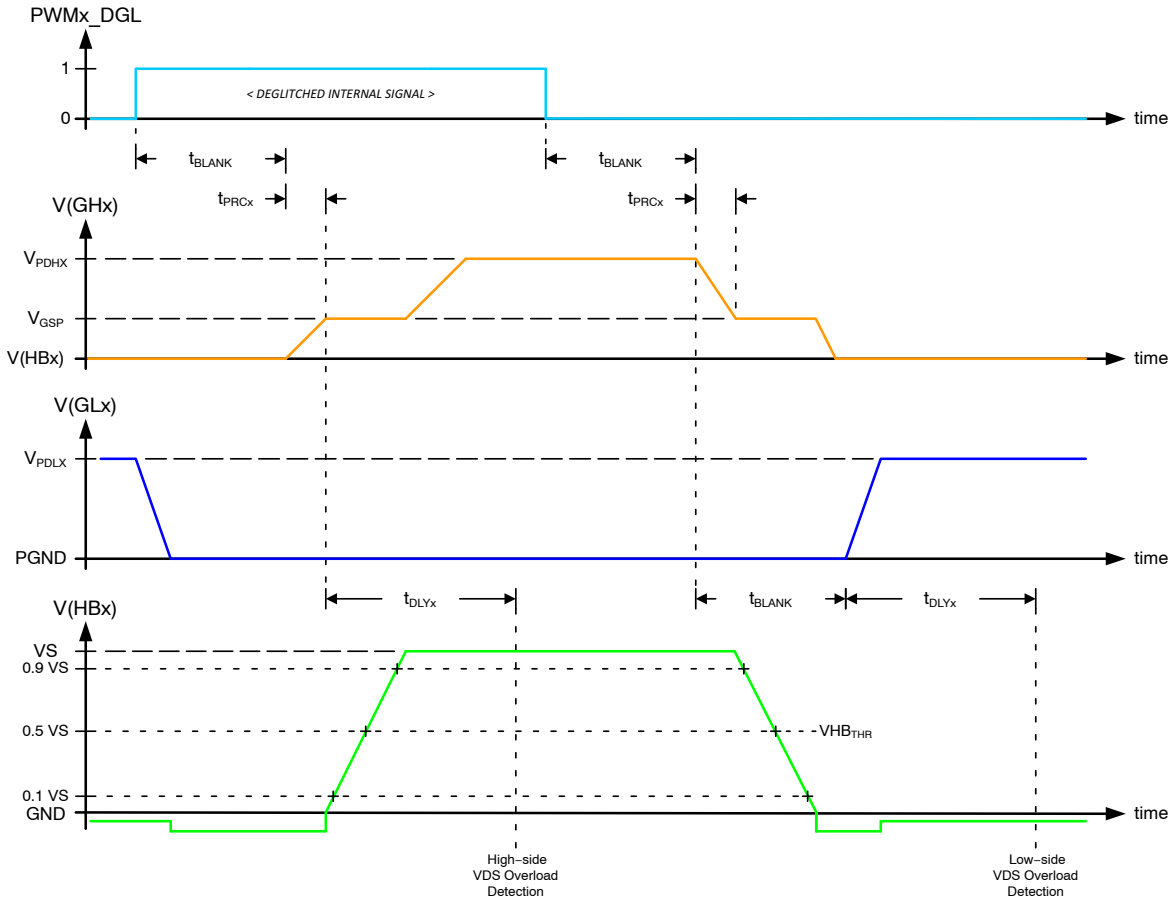


Figure 12. HBx Output Switching in Half−Bridge Configuration

When operating HB7 in PWM mode and in split configuration, both the high−side and low−side drivers can be in the ON−state simultaneously. Cross−conduction does not occur however, therefore t_{BLANK} is not needed and the timing of the gate is according to Figure 13 (e.g. HB_CFG7=1, HB_PWM7=1, HB_MODE7=0 is shown).

In either configuration, in the pre−charge phase ($V_{GHX} < V_{GSP}$) the GHx output delivers the selected rise (I_{PRCX_R}) or fall (I_{PRCX_F}) current for the selected time (t_{PRCx}), and in the slew phase ($V_{GSP} \le V_{GHX} \le V_{PDHX}$) the GHx output delivers the selected current (I_{SRX}) for up to the gate drive timeout time ($t_{TIMEOUT}$). After $t_{TIMEOUT}$, the GHx output delivers the timeout current (I_{GHx_SS}). The GLx output always delivers a multiple (I_{LSX}) of the selected slew current (see Figure 9 and § *Electrical Characteristics: Half− Bridge Pre−Driver Outputs, Pre−driver Slope Control*).

Slope Control Calibration Unit

A slope control calibration unit is implemented in order to allow adjustments to a selected MOSFET's initial switching parameter set and to verify proper setting of the high−side gate drivers (GHx). The calibration assists optimizing EMC performance and alignment of the GHx switching slopes with the VDS overload detection delay time and threshold to assure stable behavior of the protection strategy (see § *Overload Protection*).

A calibration detection unit, consisting of 4 multiplexed high−speed comparators, samples the voltage at the desired HBx input at a selected calibration sample time (see t_{CAL_PCx}, t_{CAL_DLYx} in § *Electrical Characteristics: Slope Control Calibration Unit*). A complete calibration cycle consists of sampling both the rising and falling switching slopes, and the encoded calibration result is stored in the device's calibration register (SR4).

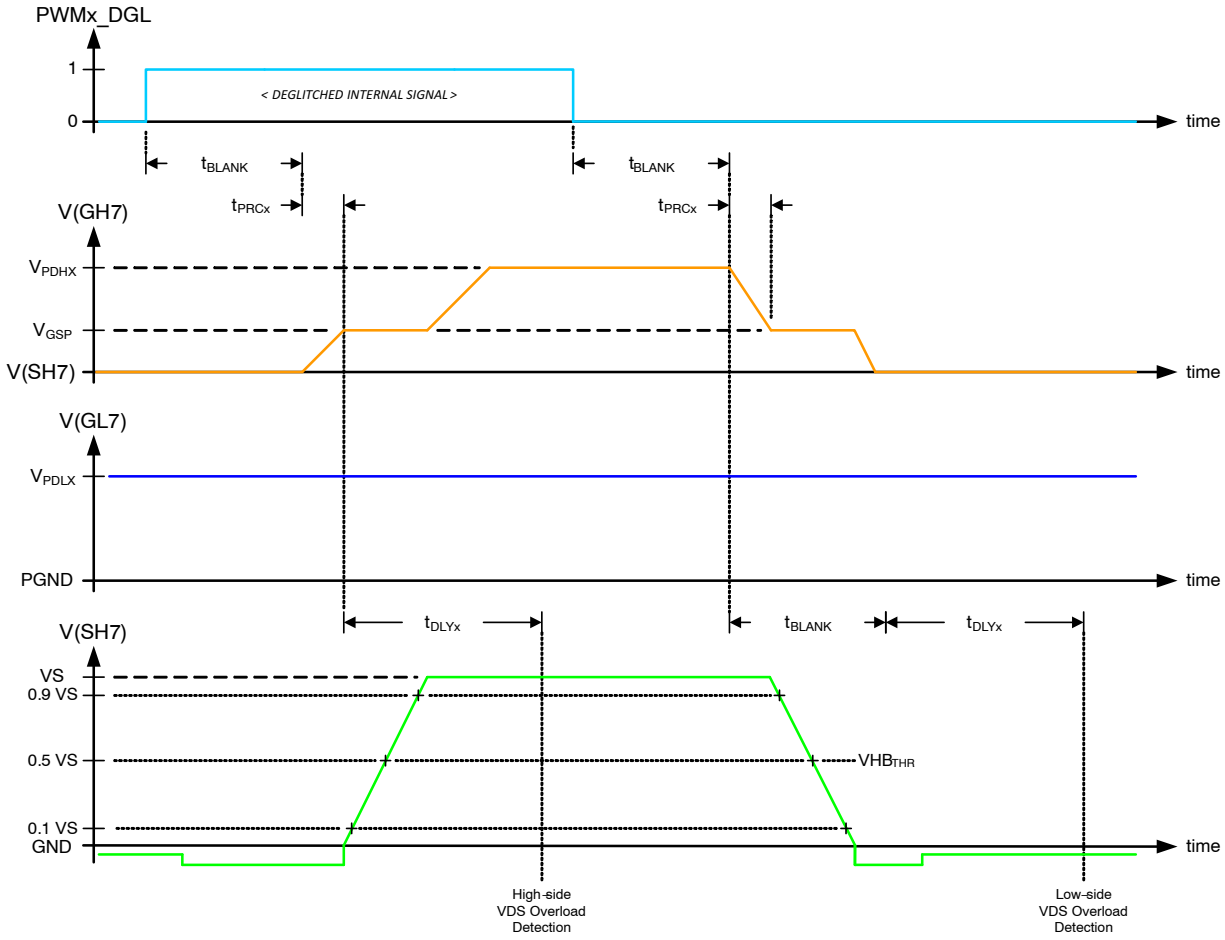


Figure 13. HB7 Output Switching in Split Configuration

Calibration is enabled when the calibration register (CR4) is written (summary Table 46 – see also Table 13):

- the desired HBx input is selected by the CR4.CAL_SEL[2:0] bits where the resulting binary code refers directly to the selected half−bridge (e.g. 100 = HB4);
- the detection pre−charge and delay sample times (t_{CAL_PCx} and t_{CAL_DLYx}) for calibration of the desired input are selected individually by the CR4.CAL_PC[3:0] bits and by the CR4.CAL_DLY[3:0] bits for both the rising and falling slopes.

The calibration unit is turned off when CR4.CAL_SEL[2:0] = 000 (POR default) is selected (see also Table 14).

Detection is started with the next edge of a routed PWMx input signal (see § *Control of Half−bridge Drivers*) on the selected channel and detection is finished when both rising and falling edges are completed (see Figure 13). The detection results are stored in the calibration result register SR4 (summary Table 46 – see also Table 33):

The CAL_READY bit indicates that when:

- SR4.CAL_READY = 0, calibration has not been executed OR the calibration result has been read;
- SR4.CAL_READY = 1, successful detection was performed for both slopes AND a valid comparator output state is delivered.

As long as the CAL_READY bit is not set (≠ 1), the calibration of a particular slope for the selected channel may be repeated. Calibration may be terminated by sending CR4.CAL_SEL[2:0] = 000.

The calibration result is encoded in the SR4. CAL_PC_R[1:0] bits and the SR4.CAL_DLY_R[1:0] bits for the rising slope and in the SR4. CAL_PC_F[1:0] bits and the SR4.CAL_DLY_F[1:0] bits for the falling slope according to Table 47.

Table 46. HBx CALIBRATION CONTROL AND RESULT REGISTERS

CR4	WD	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	WD	CAL_DLY[3:0]				CAL_PC[3:0]				CAL_SEL[2:0]		

SR4	NM	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	NM	0	0	0	CAL_READY	CAL_DLY_R[1:0]		CAL_PC_R[1:0]		CAL_DLY F[1:0]		CAL_PC _F[1:0]	

Table 47. CALIBRATION RESULT RELATIVE TO HBx SAMPLE TIME

Mnemonic	Value	Relative HBx Level Detected at Selected Sample Times	Comment
Start of Rising Slope			
CAL_PC_R[1:0]	00	VHBx < 5%	Pre−charge too low.
	01	5% < VHBx < 15%	Pre−charge within target.
	10	15% < VHBx < 85%	Pre−charge too high.
	11	VHBx > 85%	Pre−charge far too high.
End of Rising Slope			
CAL_DLY_R[1:0]	00	VHBx < 15%	Transition far too slow.
	01	15% < VHBx < 85%	Transition slightly too slow.
	10	85% < VHBx < 95 %	Gate drive setting correct.
	11	VHBx >95%	Transition too fast.
Start of Falling Slope			
CAL_PC _F[1:0]	00	VHBx > 95%	Pre−charge too low.
	01	95% > VHBx > 85%	Pre−charge within target.
	10	85% > VHBx > 15%	Pre−charge too high.
	11	VHBx < 15%	Pre−charge far too high.
End of Falling Slope			
CAL_DLY_F[1:0]	00	VHBx > 85%	Transition far too slow.
	01	85% > VHBx > 15%	Transition slightly too slow.
	10	15% > VHBx > 5%	Gate drive setting correct.
	11	VHBx < 5%	Transition too fast.

The temporal position (see Figure 13) of the target transition detection point (e.g. 10%, 90%) with respect to t_{CAL_PCx} or t_{CAL_DLYx} (or in normal operation, t_{DLYX}) of the channel selected for calibration is dependent upon:

- the PWMx_DGL resulting from the channel's operating configuration (see § *Switching Behavior of Half−bridge Drivers*, Figure 10 and Figure 11);
- the t_{BLANKX} cross−conduction blank time setting as applicable;
- the t_{PRCX}, I_{PRCX_R} and I_{PRCX_F} pre−charge phase time and current settings;
- the I_{SRX} slew phase current setting.

Calibration may be performed at the application level during module end−of−line (EOL) test where the (adjusted) settings may be stored in a microcontroller's EEPROM. In order to maintain stable function and proper EMC performance with temperature drift and output load variations, the calibration can be verified/updated on a sample basis during normal application operation.

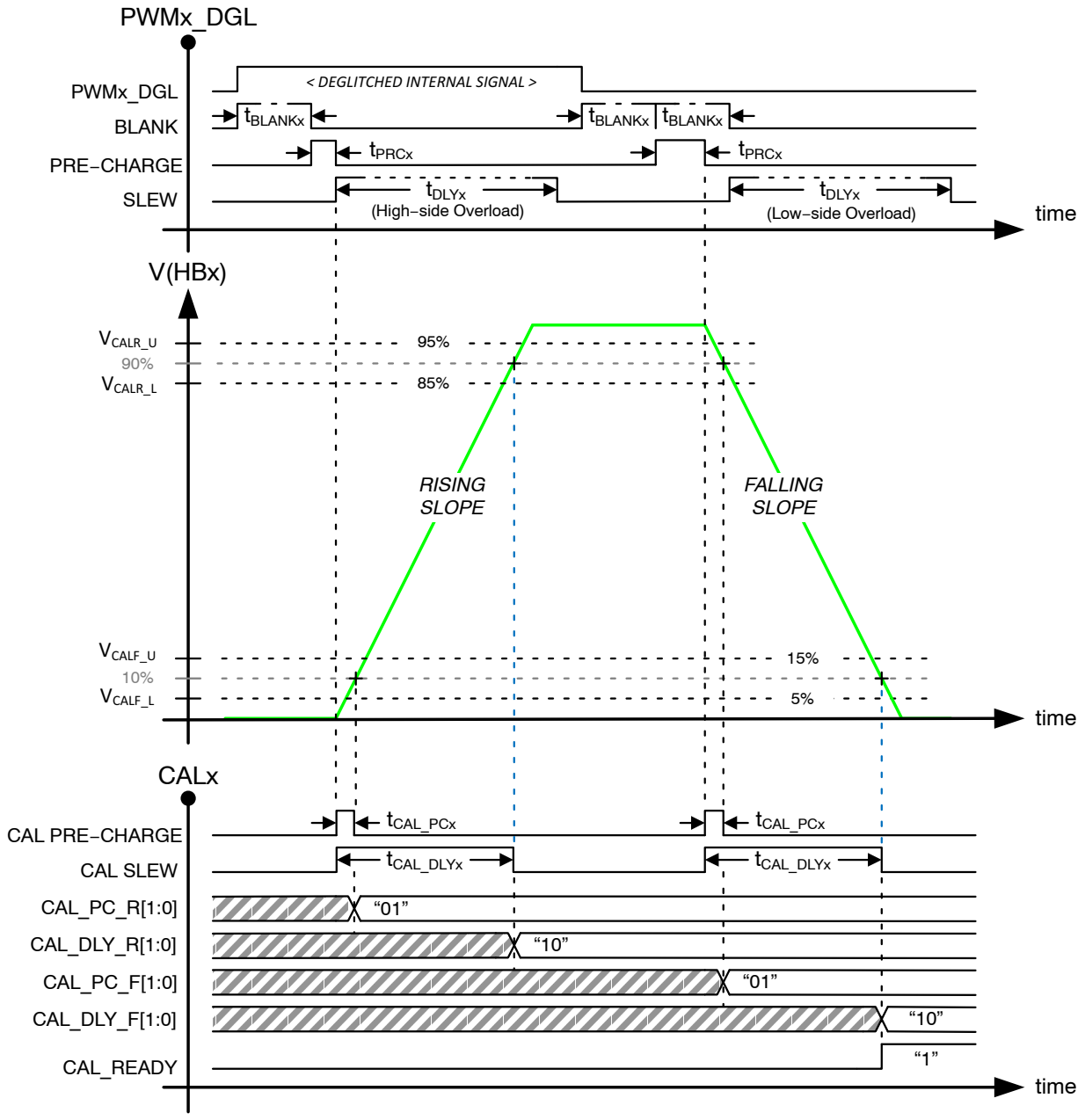


Figure 14. HBx Slope Control Calibration

OVERLOAD PROTECTION

Overload Protection

A VDS monitoring technique is used to protect the external MOS power switches in case of overload resulting from short circuit conditions applied before or during the turn−on process of the power switches (“short circuit 1” condition), and short circuit conditions applied after the turn−on process of the power switches (“short circuit 2” condition).

The thresholds of the VDS monitoring comparators (CMP1 and CMP2 in Figure 15 and Figure 16) are SPI programmable for each individual half−bridge via the VDSx[2:0] bits in the HBx configuration “B” registers. An overload detection delay time parameter (t_{DLYx}) – which controls when the VDS overload detection is performed – is also SPI programmable via the T_DLY[3:0] bits in the HBx configuration “B” registers (see Table 17, Table 18 and §*Electrical Characteristics: Half−Bridge Diagnostics*).

When a switch is in the turn−on process and its drain−source voltage already exceeds the programmed VDS threshold (“short circuit 1” condition):

- the corresponding half−bridge’s GHx and GLx drivers are latched off immediately after the selected delay time t_{DLY} plus a fixed de−glitch time t_{DGL_STAT};
- the SR0.HB_QSB Quick Status Bits and the appropriate VDS_Hx or VDS_Lx bit is latched in the corresponding VDS monitor status register (SR2: HB1...HB6 and SR3: HB7 − see Table 31 thru Table 34).

When a switch is in the ON−state and its drain−source voltage exceeds the programmed VDS threshold (“short circuit 2” condition, $t > t_{DLYx}$):

- the corresponding half−bridge’s GHx and GLx drivers are latched off immediately after the fixed de−glitch time t_{DGL_STAT};
- the SR0.HB_QSB Quick Status Bits and the appropriate VDS_Hx or VDS_Lx bit is latched in the corresponding VDS monitor status register.

Please refer to §*Output Fault (Local) Protection* to restart the half−bridge drivers after a shutdown event.

NOTE: Additional protection via use of current sensing in the low−side path of the power MOSFETs (see Figure 2) may be necessary in order to avoid destruction due to soft short condition.

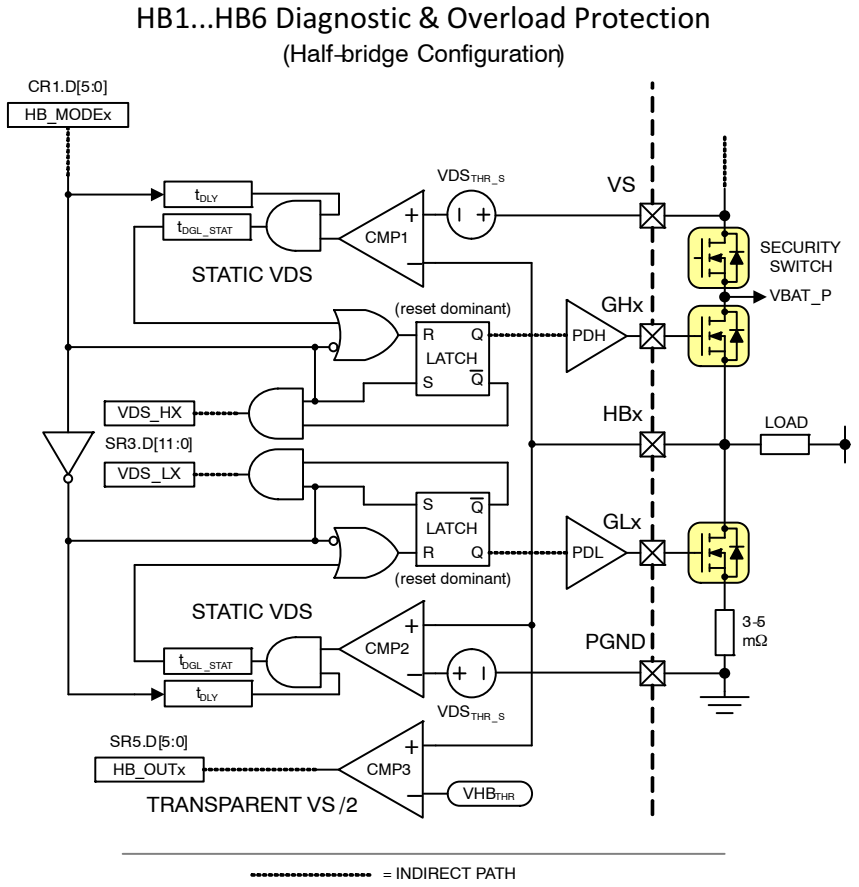


Figure 15. HB1…HB6 Diagnostic and Overload Protection

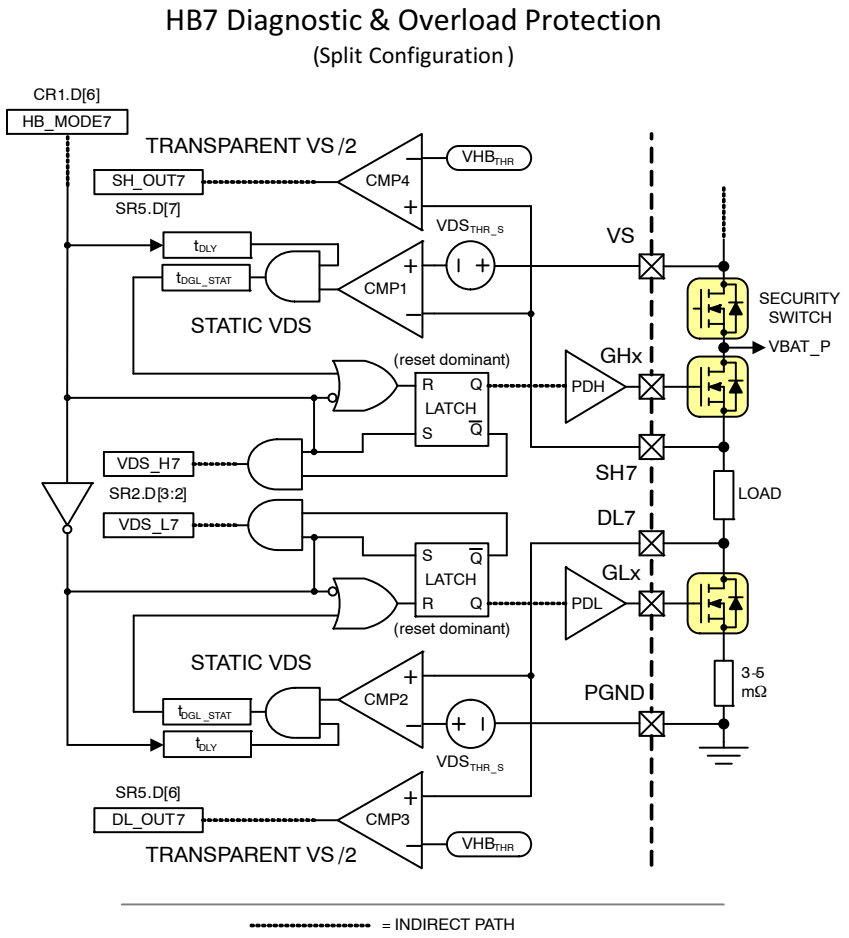


Figure 16. HB7 Diagnostic and Overload Protection

Gate Protection Features

The half−bridge gate drivers provide integrated gate protection features for the external power MOSFETs:

- a passive pull−down resistor R_{GSX} keeps the MOSFET in OFF−state, when no control of the device is available (see § *Package Pin Description* and § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*);
- a clamping structure limits the gate−source voltage to $+V_{GSX_CLP}$ or to $-V_{GSX_CLN}$ in order to protect the power MOSFETs from destruction via e.g. gate oxide failure (see § *Electrical Characteristics: Half−Bridge Pre−Driver Outputs*).

The resistors and clamping structures are available in all operating modes, including **SLEEP MODE** and in case of loss of supply voltage.

OFF−state Monitoring of Half−bridge Drivers

In order to support functional safety and to avoid unintended motor activation, the status of each of the half−bridge gate drivers can be monitored by SPI diagnosis (see § *Gate Driver Status Monitoring*). The switch nodes (i.e. HBx) status can be monitored by SPI communication via the half−bridge output status register (SR5.D[7:0] − see Table 35, Table 36). The system response depends on the load configuration; *the test procedure has to be provided by the supervising microcontroller.*

Several test current sources (I_{TST} − see § *Electrical Characteristics: Half−Bridge Diagnostics*) and comparators are implemented in order to provide OFF−state diagnosis of the power MOSFET half−bridges.

The diagnostic consists of (see Figure 14 and Figure 15):

- a high−side and a low−side test current source at each odd−numbered HBx feedback input;
- a comparator (CMP5) at each HBx feedback input.

Provided the device is in **NORMAL MODE** (see § *Operating Modes*) and no global failure (see § *Device Fault (Global) Protection*) has been detected, the test current sources can be activated individually by the TST_HSx and TST_LSx bits in the HB diagnosis register (CR12.D[5:0] − see Table 19, Table 20). Active pull−down current sources are disabled in all GHx when any test current is activated via CR12. Passive pull−down structures are always present.

NOTE: Both TST_HSx and TST_LSx test currents can be turned on simultaneously.

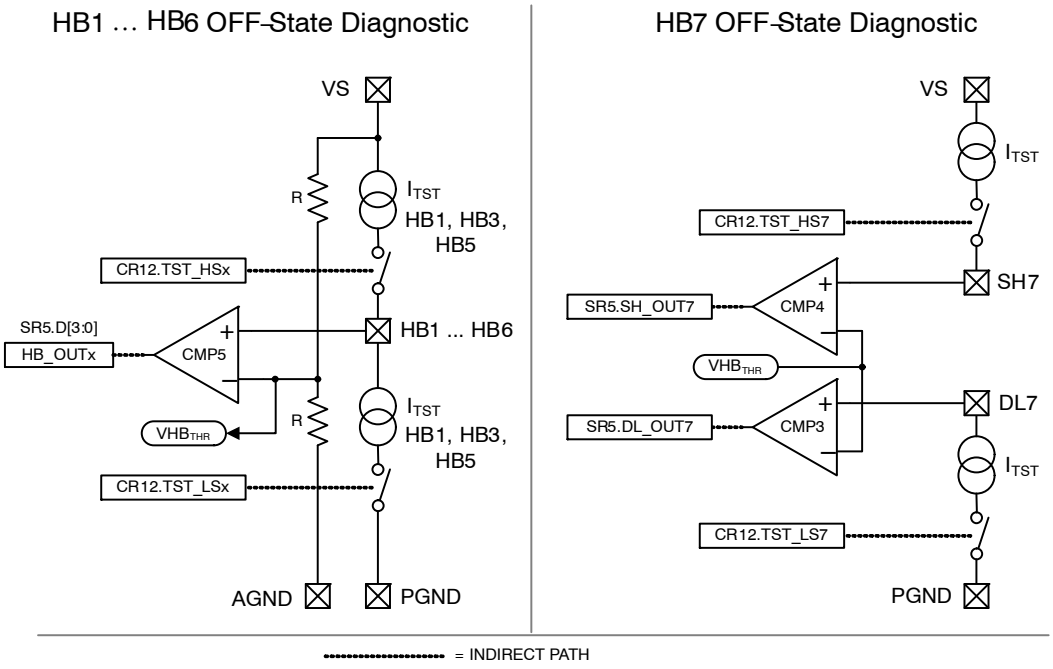


Figure 17. Half−bridge OFF−state Diagnostic

Operating Modes

The operating modes of the device are shown in the diagram of Figure 16. The logic input pin pull up / pull down resistors and the integrated gate protection pull−down resistors and clamping structures (see § *Gate Protection Features*) are available in all operating modes.

The **SLEEP MODE** is the default mode after applying VCC ($VCC < VCC_{PORF}$) and while $VCC > VCC_{PORR}$ (power−on reset) prior to wake−up of the device. During **SLEEP MODE**:

- the device is inactive and all outputs are disabled.

The device enters **NORMAL MODE** after applying the wake−up signal (i.e. RSTB 0 → 1). During **NORMAL MODE**:

- the device is active (RSTB = 1);
- the entire device functionality is available;
- the SPI can be used to provide control and diagnosis of the device.

When the device enters **NORMAL MODE** the internal registers and settings are cleared to default values and the SR0.RCF bit inside the device status register is set (see Table 27, Table 28).

The device enters **FAILSAFE MODE** when the device is active and either a SPI failure condition is detected or the external fail input (FSM) is activated i.e. FAILSAFE = (RSTB = 1) *AND* [(SPIF=1) –*OR*– (FSM=1)].

In **FAILSAFE MODE**:

- the half−bridge gate drive outputs (GHx, GLx) are disabled immediately;
- the HBx test currents (see § *OFF−state Monitoring of Half−bridge Drivers*) are disabled immediately;
- the CPSW output is deactivated (the external MOS half−bridge switches may be locked additionally by an optional external security switch which can be under control of a separate supervisory microcontroller (see “WD_EN” in Figure 2) in order to support functional safety even in case of logic issues/single point failures);
- the charge pump is disabled;
- SPI control is not possible.

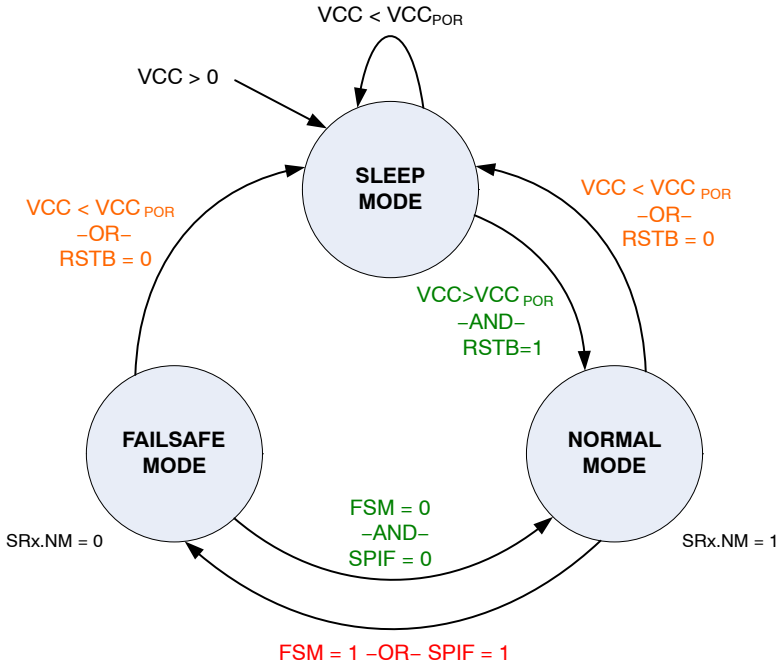


Figure 18. Operating Modes State Diagram

Although SPI control of the outputs is not possible in **FAILSAFE MODE**, the status registers are not cleared during the transition from **NORMAL MODE** to **FAILSAFE MODE**. The device status therefore is accessible in **FAILSAFE MODE** as long as the SPI interface is available (i.e. as long as VCC is present). The SPI can thus be used in **FAILSAFE MODE** to provide limited diagnosis of the device (CR0.SRA_MODE, CR0.SRA[2;0]) and to re−enter **NORMAL MODE**.

Re−entering **NORMAL MODE** after **FAILSAFE MODE** is achieved by toggling the WD bit while FSM = 0. After this mode change the internal registers and settings are cleared and the SR0.RCF bit inside the device status register is set (see Table 27, Table 28).

PROTECTION AND DIAGNOSIS

NOTE: An external aluminum electrolytic capacitor at the VS terminal is necessary to handle the turn−off energy of the motors in emergency condition.

Output Fault (Local) Protection

The external power MOSFET switches are protected against overload condition (see § *Overload Protection*) in **NORMAL MODE** by VDS monitoring. In case of a VDS overload failure, the corresponding pre−driver outputs are latched off (GHx = L *AND* GLx = L) after a de−glitch time and the status is reported in the VDS monitor register SR3 (see Table 32).

To restart a faulted half−bridge:

- the diagnosis has to be de−latched by reading the corresponding failure flag;
- the output has to be restarted via the corresponding bits in the CR0.HB_ENx register (see § *SPI Control Set*).

As long as a failure flag is not de−latched via SPI status read, a faulted output cannot be turned back on. If the failure condition is still present at a restart, the error flag will be set again and the restart will not be successful. The restart will be only successful after the error condition is removed. It is recommended to use OFF state diagnosis (see § *OFF−state Monitoring of Half−bridge Drivers*) to check the HBx node for any failure condition before restarting the output.

Device Fault (Global) Protection

The device is protected against all relevant failure conditions inside the automotive application. In case of a fault condition, the affected outputs are latched off immediately after a de−glitch time and the status is reported the device status register (SR0 − see Table 27, Table 28).

To restart the device:

- the diagnosis has to be de−latched by reading the corresponding failure flag (see § *SPI Diagnosis Set*);
- the functionality has to be restarted by use of the corresponding control bit (see § *SPI Control Set*).

Charge Pump Monitoring

The high−side pre−driver outputs are protected by charge pump monitoring (see § *Charge Pump*, Figure 5 and Figure 6):

- when the battery supply voltage VS is below the minimum supply voltage for a regulated charge pump voltage OR V(CP,VS) drops below the minimum output voltage CP_{LOW} this status is reported by the SR0.CPL bit in the device status register immediately after a de−glitch time t_{CPL_DGL} (see Table 27, Table 28). During this condition it should be considered for the microcontroller to adopt a PWM duty ratio management schema in order to minimize charge pump loading while ensuring smooth motor operation.
- when the charge pump output voltage V(CP, VS) drops below the charge pump fail threshold CP_{FAIL}, the half bridge high−side and low−side gate drivers are latched off immediately after a de−glitch time t_{CPF_DGL} and the status is reported by the SR0.CPF bit in the device status register (see Table 27, Table 28).
- when the battery supply voltage VS is in the nominal operation range $VS_{PWM} < VS < VS_{OVSDR}$ the full PWM operation of the GHx and GLx outputs is allowed;
- when the battery supply voltage is in over−voltage condition $VS > VS_{OVSDR}$, the SR0.CPF bit is masked;
- when the battery supply voltage is in over−voltage condition $VS_{OVSDF} < VS < CP_{OV}$ the charge pump − including the CPSW output − is functional but the GHx outputs are shut down;
- when the battery supply voltage exceeds the maximum supply voltage for the charge pump $VS > CP_{OV}$ the charge pump is disabled and the charge pump buffer capacitor is discharged to VS in order to protect the device from destruction.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

Over−voltage Condition

During VS over−voltage, the behavior of the gate drivers (GHx and GLx) depends on the programmed operation mode:

- the high side gate drivers (GHx) are latched off immediately after de−glitch time t_{OVDGL} (see § *Electrical Characteristics: VS Supply*) in order to protect the application from over load condition; while the low−side gate driver outputs (GLx) are operable in order to provide controlled braking (e.g. for lift gate motors);
- GH_X pull−down current is reduced to 1 mA typ.(register contents are not changed − the current will revert to its prior value after VS over−voltage is resolved);
- the HBx test currents (see § *OFF−state Monitoring of Half−bridge Drivers*) are disabled immediately.

The VS over−voltage condition is reported by the SR0.OVF bit in the device status register (see Table 27, Table 28). When the battery supply voltage is in over−voltage condition $VS > VS_{OVSDR}$ the SR0.CPF bit is masked. Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

A VCC overvoltage condition can occur during breakdown of the external voltage regulator. Please refer to § *Failure of External Voltage Regulator* for details.

Under Voltage Condition

In case of VS under voltage condition:

- all outputs (GHx, GLx) are disabled immediately after the de−glitch time t_{UVDGL} and the condition is reported by the SR0.UVF bit in the device status register (see Table 27, Table 28);
- the charge pump circuit and the switched charge pump output (CPSW) are still functional in order to keep the optional reverse battery and security switches active.

Please refer to § *Device Fault (Global) Protection* to restart the outputs after a shutdown event.

In case of VCC under voltage condition (power−on reset condition, $VCC < VCC_{POR}$):

- the device enters **SLEEP MODE** immediately without de−glitch time;
- logic input pull−up/down resistors, GHx & GLx output pull−down resistors, and VCC under voltage lockout assure safe operating states for all outputs.

To restart the device after this condition a wake−up sequence is necessary (see § *Operating Modes*).

Logic I/O Plausibility Check

The logic I/O pins are protected against mistreatment by input de−glitch circuits. The de−glitch circuits are implemented digitally, refer to § *Electrical Characteristics: Digital I/O for values*.

FUNCTIONAL SAFETY SUPPORT STRATEGY

The device uses a closed−loop verification strategy in order to avoid mistreatment of the outputs and to support functional safety. The verification strategy is implemented based on the features in the following sections.

SPI Communication Monitoring

The SPI is protected against communication errors by use of the WD toggle bit and protocol check features (see § *SPI Interface*). In case of SPI communication error the device enters **FAILSAFE MODE** immediately (see § *Operating Modes*). A correct communication is reported in the NM bit (see § *SPI Diagnosis Set*).

Gate Driver Status Monitoring

The correct activation of the half−bridge drivers can be monitored by the microcontroller by means of SPI communication (see § *SPI Diagnosis Set*). The switching status of the output drivers is indicated by the SWLx and SWHx bits in the half− bridge status monitor register SR1. The bit value corresponds to the logic status of the driver. In PWM mode, both SWHx = 1 and SWLx = 1.

In case of a discrepancy between control data and status information from the device, the microcontroller has to drive the device into **FAILSAFE MODE** in order to avoid mistreatment of the motor drives, then transition the device to **NORMAL MODE** for reprogramming.

Output Status Monitoring

The status of the MOS switches and the motor connection lines can be monitored during **NORMAL MODE** by the microcontroller by means of the SPI communication (see Figure 14 and § *SPI Diagnosis Set*):

The output voltage levels of the half−bridge switches are monitored by the transparent VS/2 comparators. The comparator states are not latched and the current node states are indicated by the HB_OUTx bits in the SR5 half−bridge output status register. The controller can use the motor status information for correlation of the operating mode, OFF state diagnosis, or for controlled brake activation.

External Fail Mode Activation

The **FAILSAFE MODE** can be also activated by an external signal (e.g. watchdog circuitry) via the FSM input. In case of a malfunction of the microcontroller, an external watchdog can cause the device to enter **FAILSAFE MODE** (see § *Operating Modes*).

Failure of External Voltage Regulator

In case of breakdown of the external voltage regulator, the device and the application's VCC node may be protected against overload by use of an optional external voltage limiter circuit which must limit the voltage to VCC_{MAX} (see Figure 2 and § *MAXIMUM RATINGS*).

The SPI port's SO pin is protected against reverse biasing by use of a back−to−back switch. The reverse voltage for this condition is limited to V_SO_{MAX} (see § *MAXIMUM RATINGS*).

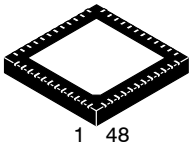
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

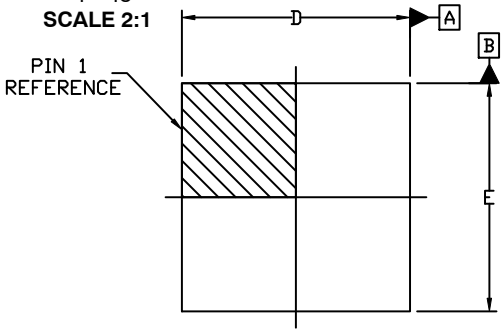
ON Semiconductor®

QFNW48 7x7, 0.5P
CASE 484AJ
ISSUE C

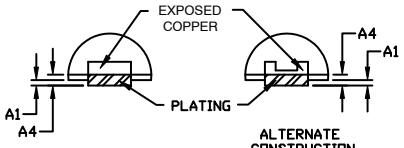
DATE 20 NOV 2019



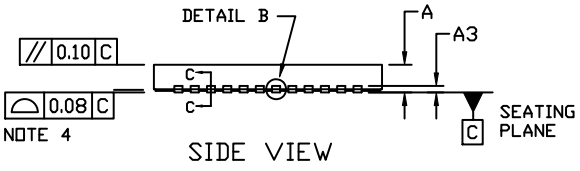
SCALE 2:1



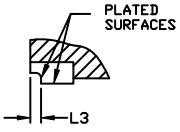
TOP VIEW



DETAIL B



SIDE VIEW

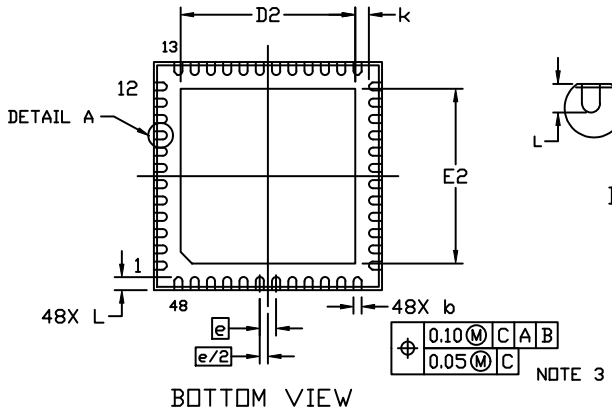


SECTION C-C

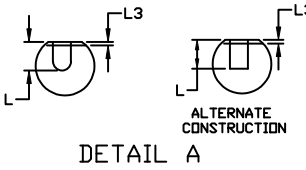
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

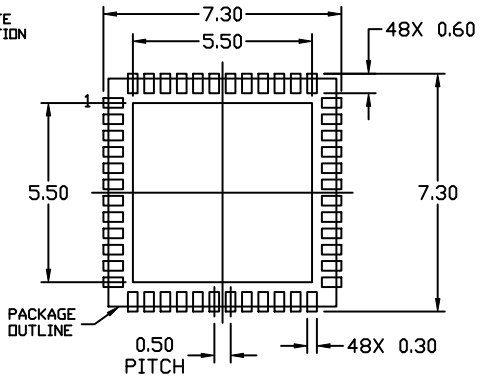
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	5.26	5.36	5.46
E	6.90	7.00	7.10
E2	5.26	5.36	5.46
e		0.50 BSC	
K		0.29 REF	
L	0.30	0.40	0.50
L3	---	---	0.09



BOTTOM VIEW



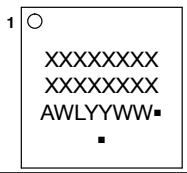
DETAIL A



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFNW48 7x7, 0.5P**	**PAGE 1 OF 1**

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