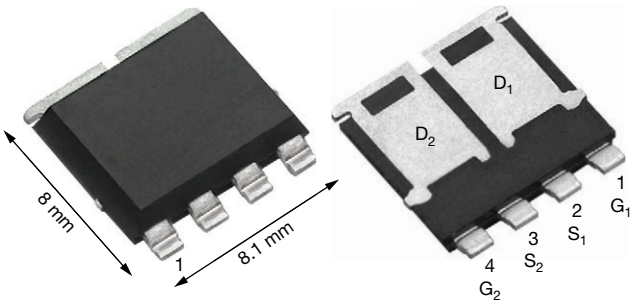
Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8L Dual



Top View Bottom View

FEATURES

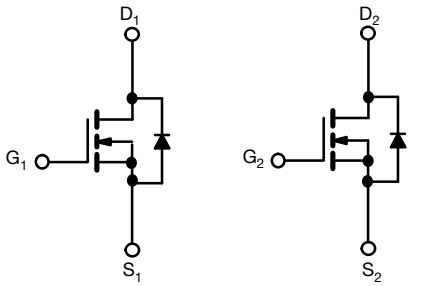
- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Fully lead (Pb)-free device
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



N-Channel MOSFET N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	40
$R_{DS(on)}$ (Ω) at V_{GS} = 10 V	0.0023
I_D (A) per leg	100
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAK 8 x 8L
Lead (Pb)-free and halogen-free	SQJQ936E (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C [a]	I_D	100	A
	T_C = 125 °C		82	
Continuous source current (diode conduction) [a]		I_S	68	
Pulsed drain current [b]		I_{DM}	400	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	46.5	
Single pulse avalanche energy		E_{AS}	110	mJ
Maximum power dissipation	T_C = 25 °C	P_D	75	W
	T_C = 125 °C		25	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount [c]	R_{thJA}	60	°C/W
Junction-to-case (drain)		R_{thJC}	2	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)
d. See solder profile (www.vishay.com/doc?73257). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0, I_D = 250 µA		40	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.5	3.0	3.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 20 V	-	-	1	µA
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 40 V, T_J = 175 °C	-	-	150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = 10 V	V_{DS} ≥ 5 V	40	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5 A	-	0.0019	0.0023	Ω
		V_{GS} = 10 V	I_D = 5 A, T_J = 125 °C	-	-	0.0033	
		V_{GS} = 10 V	I_D = 5 A, T_J = 175 °C	-	-	0.0039	
Forward transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 15 A		-	120	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 25 V, f = 1 MHz	-	4600	6600	pF
Output capacitance	C_{oss}			-	1450	2030	
Reverse transfer capacitance	C_{rss}			-	120	170	
Total gate charge [c]	Q_g	V_{GS} = 10 V	V_{DS} = 20 V, I_D = 15 A	-	75	113	nC
Gate-source charge [c]	Q_{gs}			-	22	-	
Gate-drain charge [c]	Q_{gd}			-	16	-	
Gate resistance	R_g	f = 1 MHz		0.9	1.9	2.6	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 1.3 Ω, I_D ≅ 15 A, V_{GEN} = 10 V, R_g = 1 Ω		-	18	27	ns
Rise time [c]	t_r			-	24	36	
Turn-off delay time [c]	$t_{d(off)}$			-	34	51	
Fall time [c]	t_f			-	14	21	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	272	A
Forward voltage	V_{SD}	I_F = 40 A, V_{GS} = 0 V		-	1	1.1	V
Body diode reverse recovery time	t_{rr}	I_F = 40 A, di/dt = 100 A/µs		-	63	126	ns
Body diode reverse recovery charge	Q_{rr}			-	86	172	nC
Reverse recovery fall time	t_a			-	29	-	ns
Reverse recovery rise time	t_b			-	33	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$			-	2.6	-	A

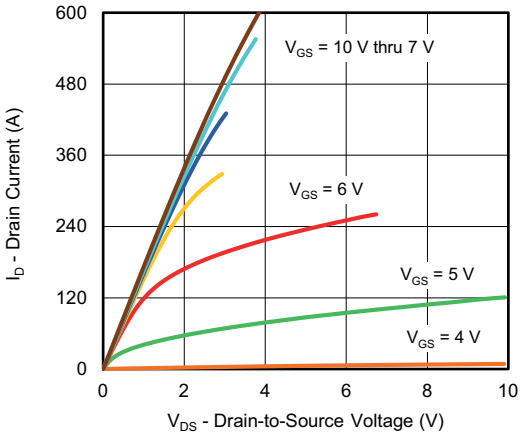
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

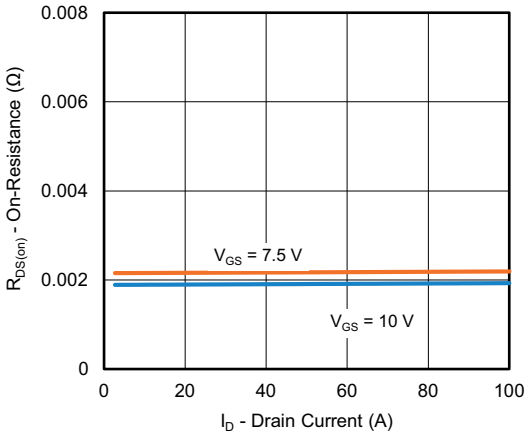
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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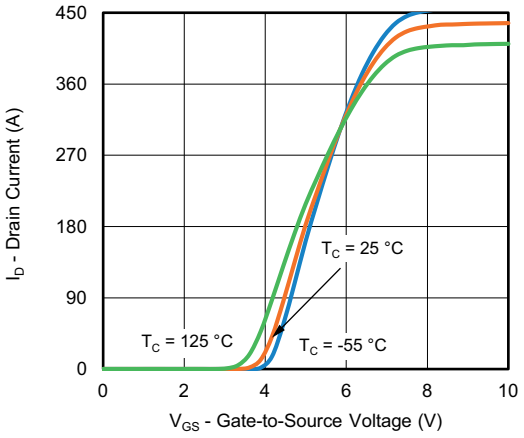
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



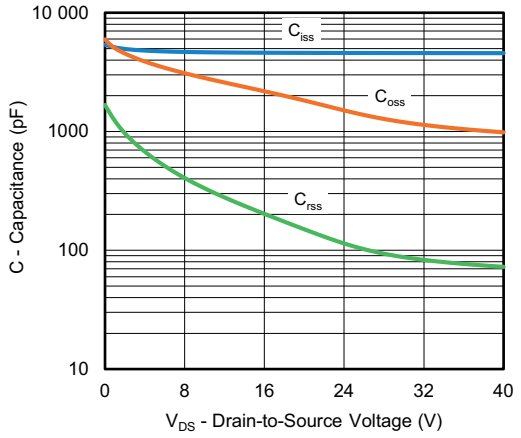
Output Characteristics



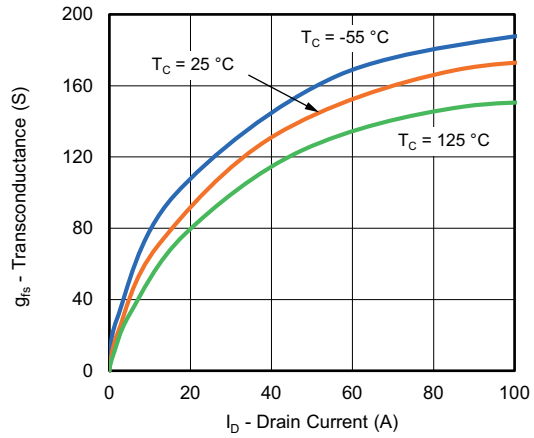
On-Resistance vs. Drain Current



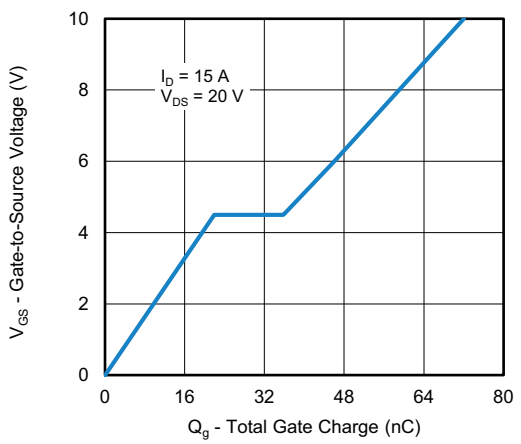
Transfer Characteristics



Capacitance



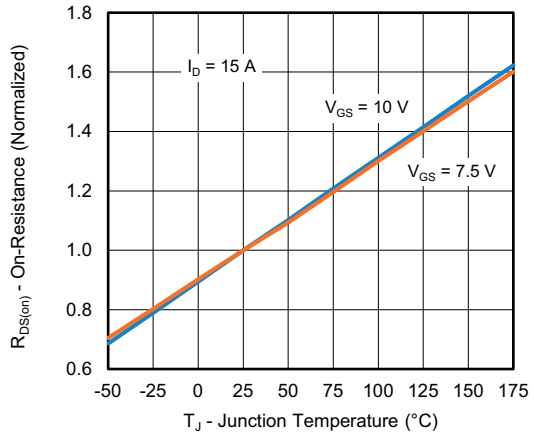
Transconductance



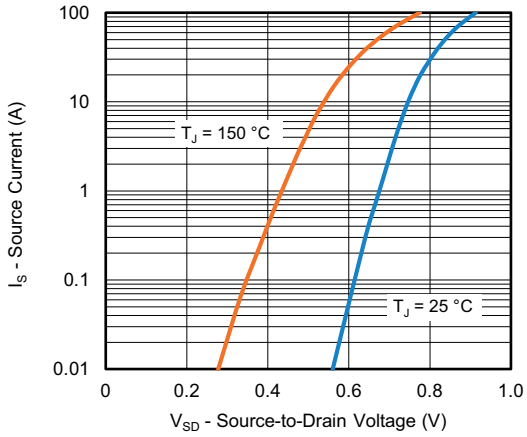
Gate Charge

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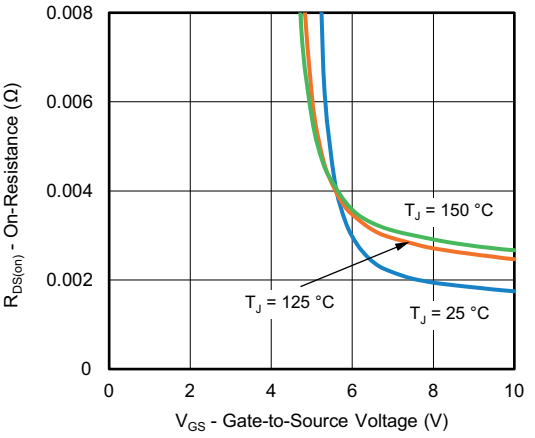
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



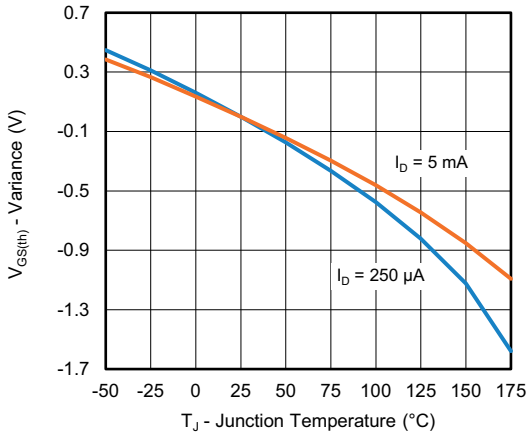
On-Resistance vs. Junction Temperature



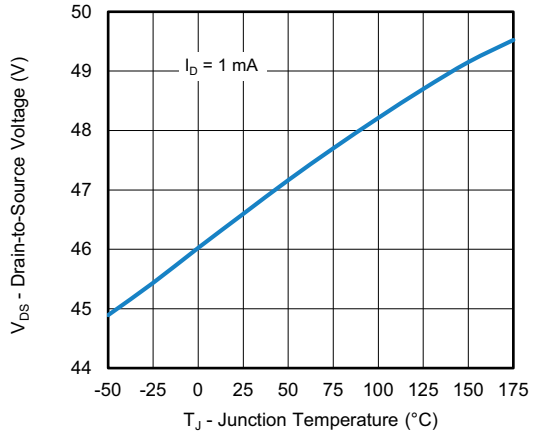
Source Drain Diode Forward Voltage



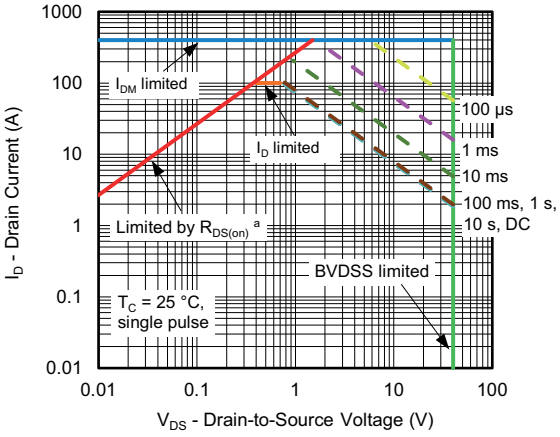
On-Resistance vs. Gate-to Source Voltage



Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



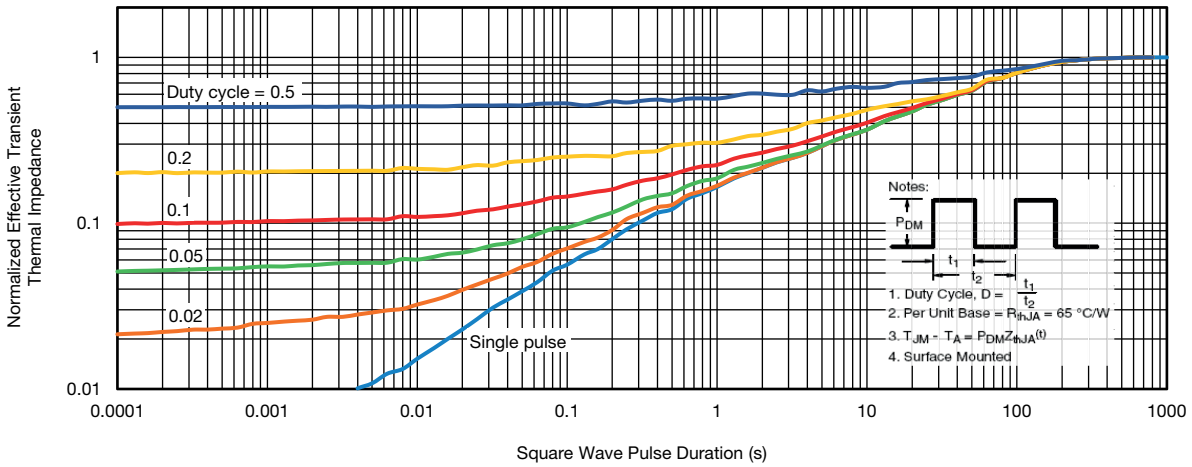
Safe Operating Area

Note

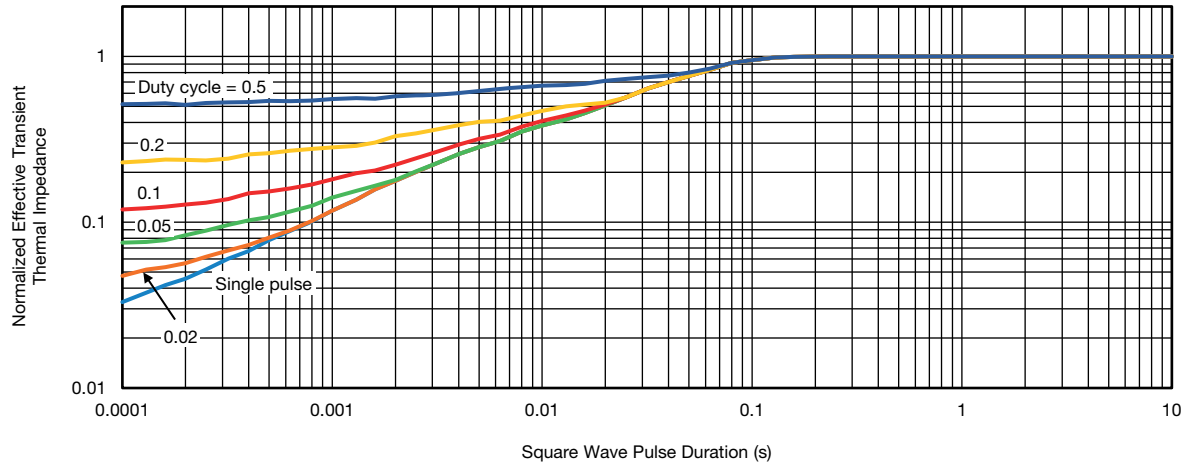
a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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