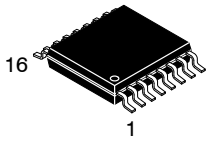
Inductive Position Sensor Interface

NCV77320



TSSOP−16
CASE 948F−01

Introduction

The NCV77320 is a single−chip inductive position sensor interface that, in combination with a *PCB,* forms a system that measures angular or linear positions accurately.

The operating principle of the inductive sensor is based on mutual inductance. The chip contains an excitation source, which generates an AC magnetic field through a primary coil on the PCB. The field mutually couples to the rotor. The rotor on its turn induces voltages in secondary coils. These voltages, measured by the chip, depend on the rotor position and give a measure for the position.

The NCV77320 contains 3 interfaces: A single ended analog output, a SENT interface with fast and slow channel and a SPI channel for direct interconnection to a micro controller.

The analog output is proportionally ratio metric with the supply voltage.

The NCV77320 has several fault detection circuitries. When a fault is detected, fault flags are set and available for readout. In case the analog output is used, OUT pin is put to HiZ and its voltage goes to fail band close to GND or VCC based on the pull−up or pull−down resistor assembled.

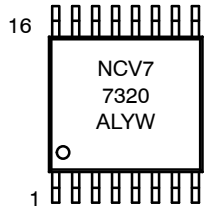
To address automotive functional safety, different kind of topologies can be implemented, e.g.:

- Two devices with independent supplies. There is no galvanic connection between the ICs. Each IC drives its own excitation coil and measures its own set of receiver coils.
- Two devices with their own supply but with a shared excitation coil connected to both ICs.

Features

- Integrated DSP Position Calculation with Flexible 15 Point Linearization
- Diagnostics, Including for Missing Wire / Wire Misconnection Tolerant
- Analog Output or SENT Output Configurable
- Temperature Sensor Embedded
- SPI Watchdog Feature
- Supply Voltage 5 V; −15 V to 30 V Tolerant Robustness
- Flexible SPI Operation with 3.3 V or 5 V Micro Controllers
- Maximum Rotational Speed of 10800 rpm
- Operating Ambient Temperature −40 to 150°C
- Developed According to the Automotive Safety Standard ISO26262
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM



NCV77320 = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

ORDERING INFORMATION

Device	Package	Shipping†
NCV77320DB0R2G	TSSOP−16	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Typical Applications

- Angular Position Sensors Up to 360°, e.g. Pedal Position, Throttle Position, Chassis Height, Actuators Position Feedback etc.
- Linear Position Sensors, e.g. Lever Position, Linear Actuator, Level Sensors etc.

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QUICK REFERENCE DATA

Table 1. MAXIMUM RATINGS (Voltages are referred to the device ground GND and are DC level)

Rating	Min	Max	Unit
Power Supply VCC	−15	30	V
SPI Power Supply VIO	−0.3	6	V
Analog Output	−15	30	V
SPI Inputs	−0.3	VIO + 0.3 V, 6 V absolute	V
SPI Output	−0.3	VIO + 0.3 V, 6 V absolute	V
Storage Temperature, T_{STG}	−55	160	°C
Junction Temperature (Note 1)	−40	170	°C
Peak Reflow Soldering Temperature: Pb−Free, 60 to 150 Seconds at 217°C (Note 2)	−	265 peak	°C
HBM Electrostatic Discharge Voltage	−2	+2	kV
CDM Electrostatic Discharge Voltage; Corner Pins	−750	+750	V
CDM Electrostatic Discharge Voltage; All Other Pins	−500	+500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For limited time during the operational lifetime, based on the mission profile.
2. For additional information, see or download **onsemi**'s Soldering and Mounting Techniques Reference Manual, SOLDERRM/D, and Application Note AND8003/D.

RECOMMENDED OPERATING RANGES

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	Power Supply	4.5	5.5	V
VIO	SPI Interface Power Supply	3.0	5.5	V
TST	Digital Inputs for Test Mode / to be Tied to GND for Normal Operation	−0.3	0.3	V
SPI_SI, SPI_CS\, SPI_CLK	SPI Inputs	−0.3	5.5	V
T_J	Junction operating temperature (Note 3)	−40	170	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over lifetime, the system's environmental conditions and the thermal design of the customer's system.

APPLICATIONS

The NCV77320 is an inductive position sensor interface that is suited for applications where a contactless angular or linear position has to be measured with high accuracy. Figure 1 to Figure 3 give simplified application diagrams of the NCV77320 in single chip operation. Table 3 gives the parameters for system level operation.

Table 3. SYSTEM PARAMETERS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ICC_A	Current Consumption with Active Primary Coil Driven. Analog Output Operation without SPI.	VCC = 5.5 V (Note 4)	–	–	11	mA
ICC_SENT	Current Consumption with Active Primary Coil Driven. SENT Output Operation without SPI.	VCC = 5.5 V (Note 4)	–	–	12.5	mA
ICC_SPI	Current Consumption with Active Primary Coil Driven. SPI Operation.	VCC = 5.5 V, VIO 5.5 V (Note 4)	–	–	9.5	mA
IDD_SPI_VIO	Current Consumption in VIO Pin with Active Primary Coil Driven. SPI Operation Idle.	VCC = 5.5 V, VIO 5.5 V SPI communication idle (Note 4)	–	–	100	μA
V_MAX	Angular Speed (Electrical)		–	–	180	Rps
POS_ACC	Static Position Linearity Error (Excluding the Sensor)	V_REC > 4 mV (Note 5, 8)	–	–	0.15	% FS
POS_NOISE	Output Position rms Noise	V_REC = 4 mV (Note 6, 7, 8)	–	0.02	–	% FS
POS_RES	Static Position Resolution Expressed as Effective Number of Bits (ENOB)	(Note 8)	–	14.5	–	Bit
POS_DLY	Delay Time between Average Input Position to DSP Output		–	100	–	μs
t_PER	Position DSP Update Rate		–	216	–	μs
t_INIT	Power On Time		–	–	2	ms

4. Values based on design and characterization, not tested in production
5. Not including error of Analogue driver
6. Analogue driver – OUT rms noise is reduced by factor √(t_PER / (2 * RF * CF)) for RF * CF > 0.2 ms
7. Noise is inversely proportional to input voltage V_REC. RMS noise level = POS_NOISE * V_REC / 4 mV
8. PWL correction table set to slope equal to gain = 1

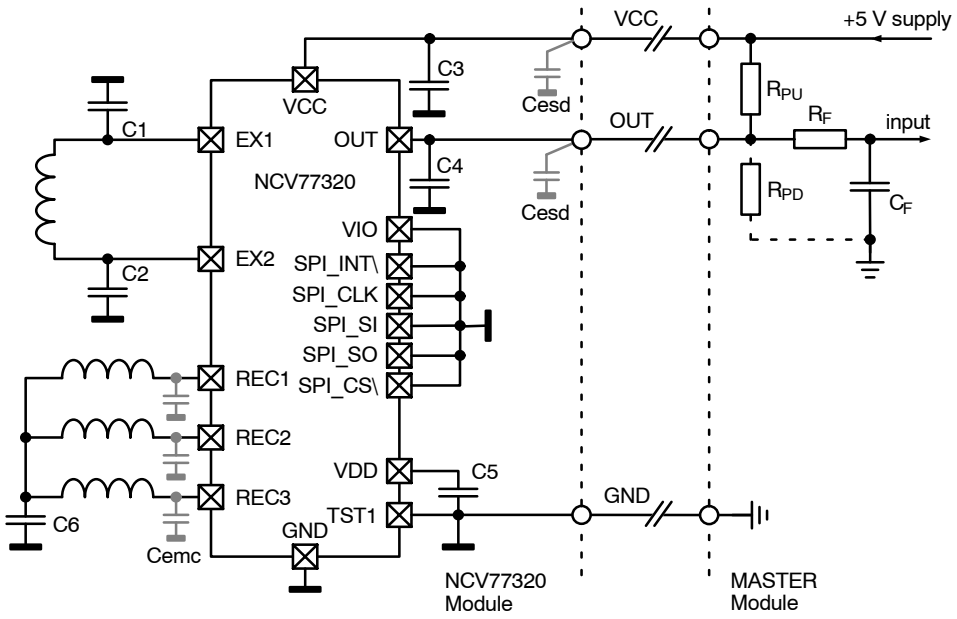


Figure 1. NCV77320 Single Chip Application Diagram with Analog Output

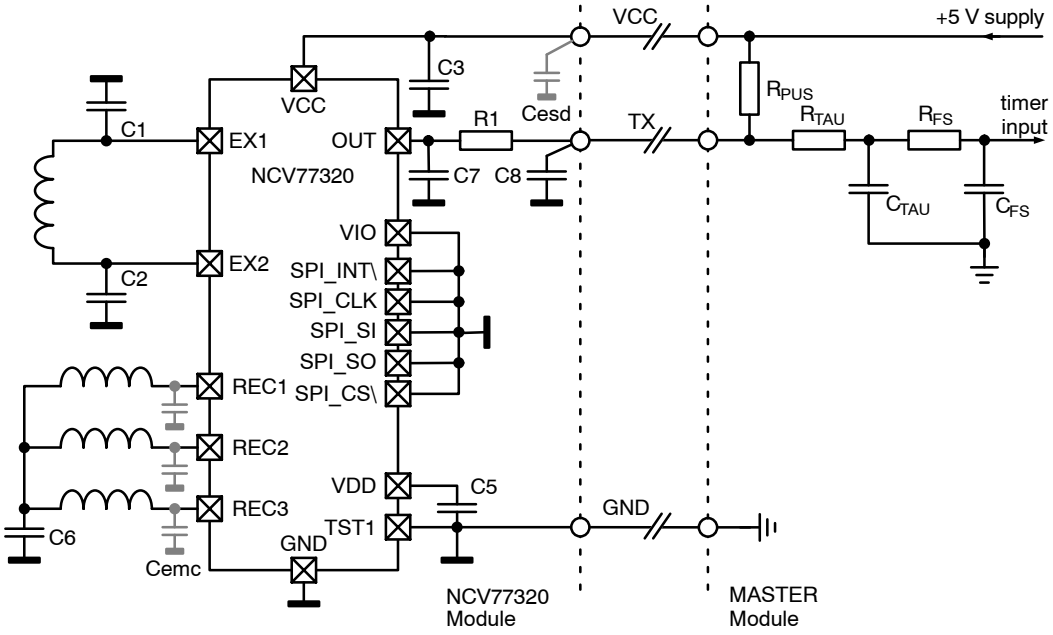


Figure 2. NCV77320 Single Chip Application Diagram with SENT Output

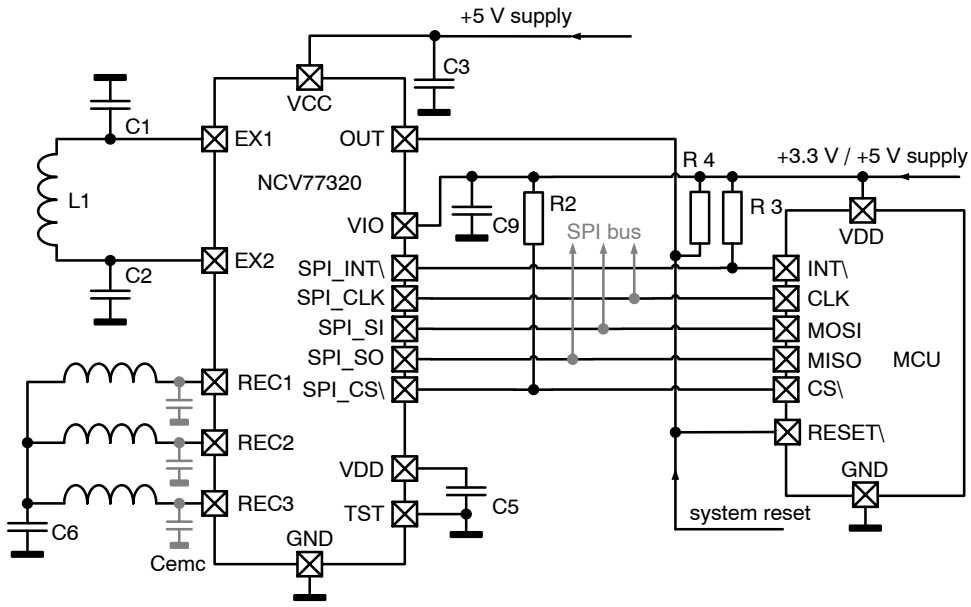


Figure 3. NCV77320 Single Chip Application Diagram with SPI Interface

Table 4. EXTERNAL COMPONENTS

Component	Description	Min. Value	Typ. Value	Max. Value	Note
C1, C2	Primary Coil Resonator Capacitor	–	Refer to LC Oscillator chapter	3.3 nF	C0G type ceramic
C3	Decoupling Capacitors	–	100 nF	–	X7R type ceramic
C4	Output Stabilization Capacitor for Analogue OUT Configuration	80 nF	100 nF	390 nF	X7R type ceramic C4 + Cesd < 390 nF Place the output capacitor C4 as close as possible to the OUT pin and returning GND pin.
C5	Decoupling and Stabilization Capacitor	70 nF	100 nF	100 μF	X7R type ceramic
C6	Common Mode Decoupling Capacitor Recommended for EMC Purposes	–	–	1 nF	X7R, C0G type ceramic
C7	Output Capacitor for SENT OUT Configuration	–20%	6.8 nF	+20%	X7R type ceramic Place the output capacitor C7 as close as possible to the OUT pin and returning GND pin.
C8	π Filter Capacitor for SENT OUT Configuration	–20%	6.8 nF	+20%	X7R type ceramic
C9	Decoupling Capacitors	–	100 nF	–	X7R type ceramic
Cemc	3 x Input Capacitor Optional for Improved EMC Performance	–	–	100 pF	C0G type ceramic
Cesd	System Level ESD Optional Protection Capacitor	100 pF	–	100 nF	X7R type ceramic C4 + Cesd < 390 nF
C_F	Master Side Filter Capacitor for Analogue OUT Configuration	–	–	33 nF	
C_{TAU}	SENT Receiver 1st Stage Capacitor	–30%	2.2 nF	+30%	Shall comply with SAE J2716
C_{FS}	SENT Receiver 2nd Stage Capacitor	0.6 μs / R_{FS}	Refer to SAE J2716	1.4 μs / R_{FS}	Shall comply with SAE J2716
R1	π Filter Resistor for SENT OUT Configuration	–5%	120 Ω	+5%	Power loss ≥ 125 mW
R2	SPI CS\ Pull–up Resistor	68 kΩ	–	220 kΩ	
R3	INT\ Pull–up Resistor for SPI Operation	3.3 kΩ	10 kΩ	22 kΩ	
R4	RESET\ Pull–up Resistor for SPI Operation	68 kΩ	–	–	
R_{PU}, R_{PD}	Pull–up or Pull–down Resistor at Master Side for Analogue OUT Configuration	4.7 kΩ	–	22 kΩ	R_{PD} or R_{PU} shall be assembled. Max value can be increased following rules described in Analog Output chapter.
R_F	Master Side Filter Resistor for Analogue OUT Configuration	10 kΩ	–	–	
R_{PUS}	SENT Receiver Pull–up Resistor	10 kΩ	–	55 kΩ	Shall comply with SAE J2716
R_{TAU}	SENT Receiver 1st Filter Stage Resistor	–20%	560 Ω	+20%	Shall comply with SAE J2716
R_{FS}	SENT Receiver 2nd Filter Stage Resistor	4 kΩ	–	–	Shall comply with SAE J2716

BLOCK DIAGRAM

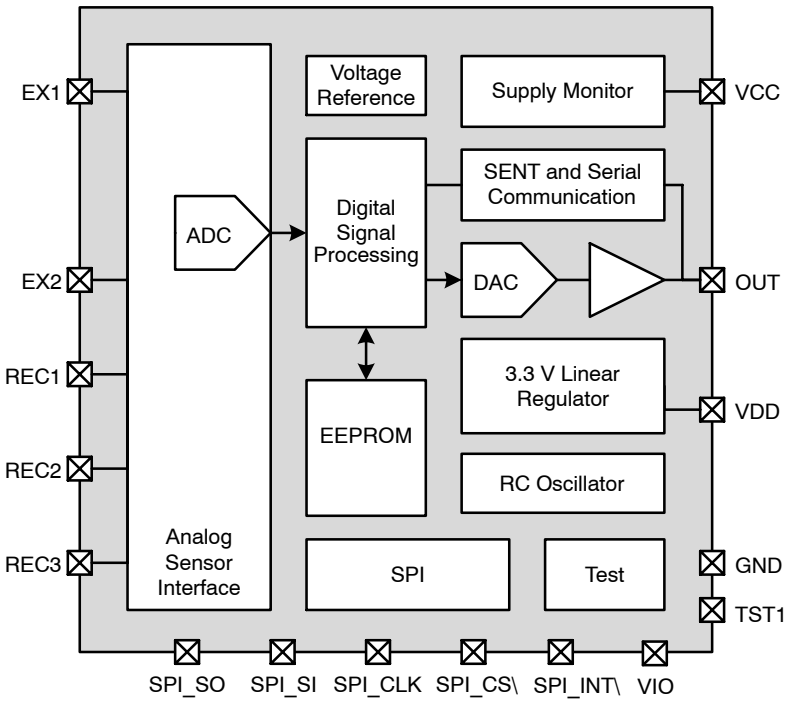


Figure 4. NCV77320 Block Diagram

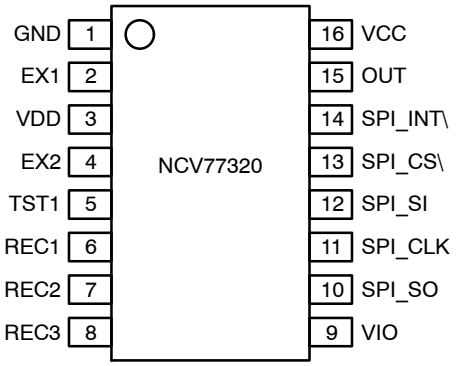


Figure 5. NCV77320 Pinout

Table 5. PIN FUNCTION DESCRIPTION FOR TSSOP16

Pin No.	Name	Description	Pin No.	Name	Description
1	GND	Sensor ground	16	VCC	Sensor Power supply 5 V
2	EX1	Primary coil oscillator	15	OUT	Analog output / SENT output / RST function in SPI mode
3	VDD	Digital 3.3 V Supply (only decoupling)	14	SPI_INT\	SPI Interrupt output (tri−state)
4	EX2	Primary coil oscillator	13	SPI_CS\	SPI Chip Select input
5	TST1	Test Pin (to be tied to GND)	12	SPI_SI	SPI Serial input
6	REC1	Secondary coil input phase1	11	SPI_CLK	SPI Clock input
7	REC2	Secondary coil input phase2	10	SPI_SO	SPI Serial output (tri−state)
8	REC3	Secondary coil input phase3	9	VIO	SPI supply pin 5 V / 3.3 V

Table 6. OPERATING PARAMETERS (These parameters are guaranteed over temperature and all supplies in the operating range, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.)

Parameter	(Test) Conditions	Min	Typ	Max	Unit
VCC RELATED					
VCC		4.5	5.0	5.5	V
VCC_OV; VCC over Voltage Threshold Level where the Outputs are going in High Z		5.55	6.15	6.7	V
t_service_max; Maximum Time after POR wherein the Service Mode Can be Entered		–	–	100	ms
VCC_UV; VCC under Voltage Threshold Level where the Outputs are going in High Z		3.9	4.2	4.40	V
t_INIT	Power On Initialization Time	–	–	2	ms
VIO SUPPLY					
VIO; SPI Interface Supply Voltage		3.0	–	5.5	V
INTERNAL SUPPLY					
VDD; Regulated Voltage on Pin VDD	VCC applied, full internal load	3.1	3.3	3.6	V
VDD_OV; Regulated Voltage High Threshold where the OUT goes High Z		3.65	–	4.45	V
VDD_OVLD; VDD Regulator Overload Threshold where OUT goes High Z		3.0	–	–	V
POWER ON RESET					
POR_hi; POR Threshold Level	VCC applied	2.5	–	3.0	V
EXCITATION OSCILLATOR					
$V_{_osc;}$ Primary Oscillator Voltage Amplitude	V_osc = (V(EX1) − V(EX2))	1.0	–	1.6	Vp
$V_{osc_CMM;}$ DC Common Mode Voltage		–	0.5 x VDD	–	V
$f_{_PRIM;}$ Primary Resonator Frequency		3.0	–	4.0	MHz
$R_{P_PRIM;}$ Primary Resonator Effective Loss Resistance	@ $f_{_PRIM}$	0.4	–	5	kΩ
$Q_{_PRIM;}$ Primary Resonator Q−factor	$Q_{PRIM} = \frac{R_{P_PRIM}}{L1} \cdot \frac{1}{2\pi \cdot f_{_PRIM}}$	4.7	–	170	
RECEIVER COILS					
V_REC; Input Voltage Amplitude Range for Operation		4	–	100	mV
ANALOG OUTPUT					
Vout_hi; Voltage for Maximum Position Value		–	–	0.95	VCC
Vout_lo; Voltage for Minimum Position Value		0.05	–	–	VCC
Vout_offset		−16	–	16	mV
Vout_offset_drift	(Note 9)	−5	–	5	mV
Vout_gainerr		−1.3	–	1.3	%
Vout_gainerr_drift	(Note 9)	−0.15	–	0.15	%
Vout_Diag_Low; Diagnostics Low Level Output		–	–	4	%VCC
Vout_Diag_High; Diagnostics High Level Output		96	–	–	%VCC
Output Linearity Error		–	–	0.1	%VCC
Analog Output Step Output Settling Time to +/−1%	VOUT step from 5 to 95 % VCC, VCC = 5 V, C4 < 390 nF	–	–	1.2	ms
TAU_OUT; Analogue Output Time Constant	(Note 9)	40	110	160	μs
t_DIAG_HOLD; Hold Time for Diagnostic State at OUT Line		–	50	–	ms
Output Current Limitation		4	–	8	mA

Table 6. OPERATING PARAMETERS (These parameters are guaranteed over temperature and all supplies in the operating range, unless otherwise specified. Convention: currents flowing into the circuit are defined as positive.) (continued)

Parameter	(Test) Conditions	Min	Typ	Max	Unit
ANALOG OUTPUT					
Output Current Leakage with Deactivated OUT Drivers	Tj = 170°C	–7	–	7	μA
SENT OUTPUT					
t_SENT; SENT Clock Tick Time		–7%	3	+7%	μs
t_Fall; Fall Time Referred to the Receiver Input	From Vth = 3.8 V to Vtl = 1.1 V (Note 10)	–	–	6.5	μs
t_Rise; Rise Time Referred to the Receiver Input	From Vtl = 1.1 V to Vth = 3.8 V (Note 10)	–	–	18	μs
t_Stable; Signal Time below 1.39 V or above 3.8 V	(Note 10)	6	–	–	μs
t_Δ_Fall; Edge to Edge Jitter	(Note 10)	–	–	0.1	μs
V_OH; High State Voltage	(Note 10)	4.1	–	–	V
V_OL; Low State Voltage	(Note 10)	–	–	0.5	V
I_Output_Max	Under short circuit condition, average current	–	–	10	mA
WATCHDOG RESET OUTPUT					
V_WD_RST; Vol; Open Drain Output Voltage	68 k pull up to VIO	–	–	0.5	V
T_WD_RST; Watchdog Reset Time		18.6	20	21.4	ms
SPI DIGITAL INPUTS AND OUTPUTS					
Vih; Input High Level Voltage	VIO = 3.3 V or VIO = 5 V	2.3	–	VIO	V
Vil; Input Low Level Voltage		0	–	0.8	V
Voh; SPI_SO Push Pull Driver with 3 State	VIO = 3.3 V or VIO = 5 V, 2 mA load current	VIO – 0.4	–	VIO	V
Vohd; SPI_INT\ Push Pull Driver with 3 State		VIO – 1.3	–	VIO	V
Vol; SPI_SO, SPI_INT\ Push Pull Driver with 3 State		0	–	0.4	V
$t_{SCK;}$ SPI Clock Period		700	–	–	ns
t_{SCK_HI}; SPI_CLK High Time		200	–	–	ns
t_{SCK_LO}; SPI_CLK Low Time		200	–	–	ns
t_{SET_CSB}; SPI_CS\ Setup Time		400	–	–	ns
t_{CSB_INACT}; SPI_CS\ Inactive Time		500	–	–	ns
$t_{SET_MOSI;}$ SPI_SI Setup Time		200	–	–	ns
$t_{HOLD_MOSI;}$ SPI_SI Hold Time		200	–	–	ns
$t_{SET_MISO;}$ SPI_SO Setup Time	SPI_SO load capacitance: 200 pF	–	–	200	ns
t_{MISO_DLY} SPI_SO Delay Time	SPI_SO load capacitance: 200 pF	–	–	200	ns
$t_{SCK_DLY;}$ SPI_CS\ High after Last SPI_CLK Falling Edge		–	–	200	ns
EEPROM					
T_{PROG}; EEPROM Programming Time after PRG Command	N is number of addresses	–	–	N x 9.9	ms
T_{VERIFY}; EEPROM Verification Time	N is number of addresses	–	–	N x 0.41 + 14.2	μs
nEEPROMwrite; Number of Write Cycles per Address	Tj < 70°C	–	–	100	

9. Values based on design and characterization, not tested in production
10. The NCV77320 is designed to be compliant with requirements of SAE J2716, if the external components fulfill requirements described in Table 4. EXTERNAL COMPONENTS and the supply voltage VCC is in range from 4.85 V to 5.15 V

Table 7. THERMAL ASPECTS

Parameter	Description	Typ	Unit
VCC		5.0	V
Rthja	Thermal resistance from junction to the ambient (Note 11)	170	K/W
Soldering Information	Please refer to our Soldering and Mounting Techniques Reference Manual	SOLDERRM/D	

11. The thermal resistance has been obtained by a simulation for the package assembled on 2S0P PCB with 10% copper coverage density with no forced convection at Ta = 180°C.

SPI TIMING PARAMETERS

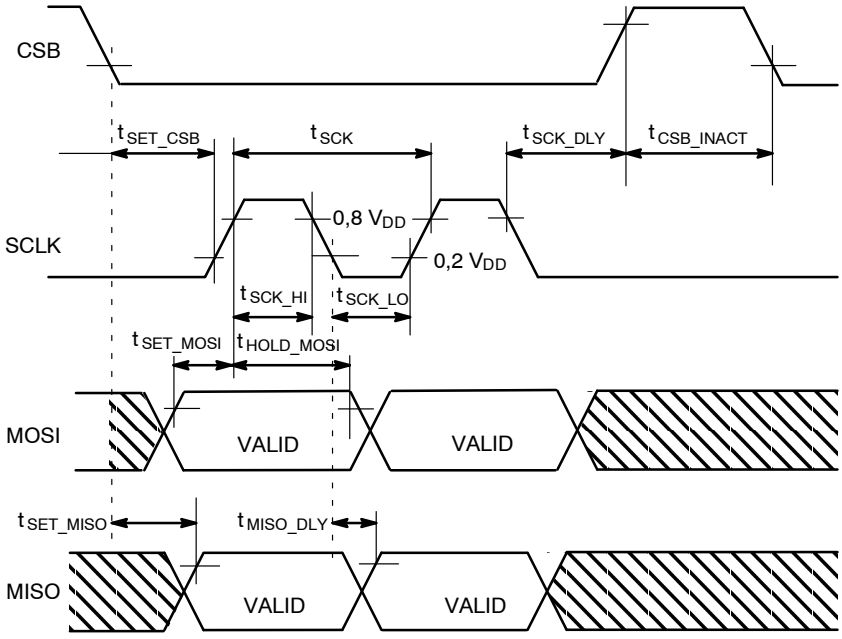


Figure 6. SPI Timing Diagram

SENT OUTPUT TIMING PARAMETERS

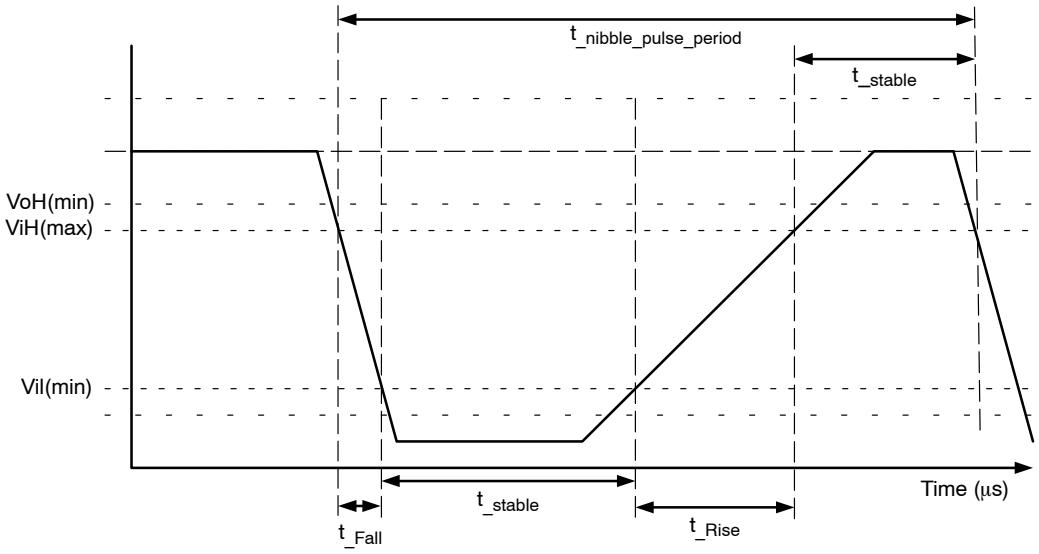


Figure 7. SENT Pulse Timing Diagram

DESCRIPTION

Memory Mapping

The NCV77320 contains non−volatile EEPROM memory to store the programmed data. It contains two banks of volatile memory – Configuration memory and Run time memory. After POR, the contents of the EEPROM memory is loaded into Configuration memory. It contains calibration, configuration, PWL and programmed sent information. The Run time memory bank contains the real time information: the actual position, the ADC data and diagnostics.

Be aware, that there are different commands for accessing Configuration memory and Run time memory content.

LC Oscillator

The LC oscillator is the primary excitation generator. The oscillator runs at the LC resonance frequency of around 3.5 MHz. For the maximum Q factor and phase relation, the LC values have to be selected to tune the resonance frequency.

The amplitude of the LC oscillator is kept within a certain window by an amplitude regulation circuit (Refer to the Operating parameter table: "V_{osc}").

The LC oscillator needs two external capacitors. The selected value needs to be matched to achieve the optimum resonance frequency for the coil. The capacitors can be calculated as follows:

$$f_PRIM \approx \frac{1}{2\pi \sqrt{\frac{C1 \cdot C2}{C1 + C2} \cdot L1}} \quad \text{(eq. 1)}$$

Where C1 and C2 are the external capacitors and L1 is the primary coil inductance. The resonant frequency shall conform to the limits given in Table 6.

The R_{P_PRIM} represents losses at resonance frequency associated with the resonator. Exceeding the limits given in Table 6 might result in inability of the oscillator to keep the excitation voltage amplitude in the given limits for "V_OSC".

In a practical design of the primary coil as PCB structure, the effective losses are often created by inductor series resistance R_S. In such a case, the following equation can be used:

$$R_{P_PRIM} \approx \frac{L1}{R_S \cdot \frac{C1 \cdot C2}{C1 + C2}} \quad \text{(eq. 2)}$$

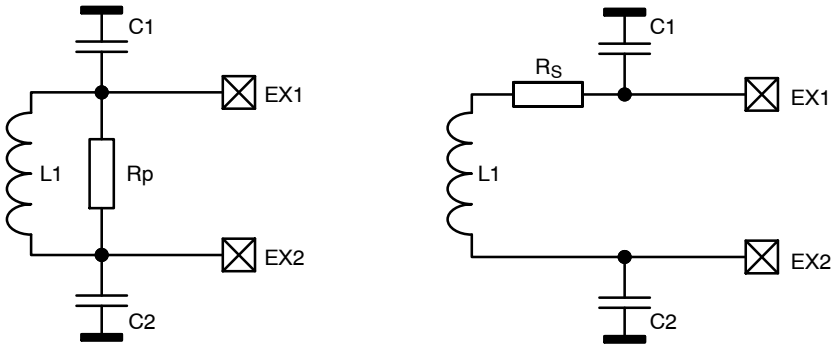


Figure 8. Resonator Schematics Including Losses Equivalent Resistor

Primary coil diagnostics:

- *Primary frequency out of limits*: The oscillator frequency of the primary coil is compared with a frequency of a free running on−chip oscillator. The error flag is set if the "f_PRIM" frequency is out of range.
- *Primary common mode out of range*: error flag is set if the common mode voltage is outside of the operating range.
- *Primary amplitude too low*: error flag is set when "V_OSC" amplitude is too low.

Output states and "fail_flags[15:0]" register mapping are listed in Table 18.

Main Receiver Coils Signal Inputs

The NCV77320 contains three semi differential inputs. The secondary coils of the sensor have to be connected in a star configuration. The mid−point of the star should be connected to the board GND via a decoupling capacitor (<1 nF).

The coils connected should have a 120 phase related geometry to achieve the best full angular resolution of the system. The number of poles at the sensor board and rotor determine the unique electrical period to mechanical angular relationship (ratio is equal to one in Figure 9).

The AC signal at resonant frequency from the primary coil induces voltages in the secondary coils. The amplitude of the induced signal depends on mutual placement of a conductive rotor and the geometry of the input coils. A ratio of the amplitudes at RECx inputs depends on the rotor angular position.

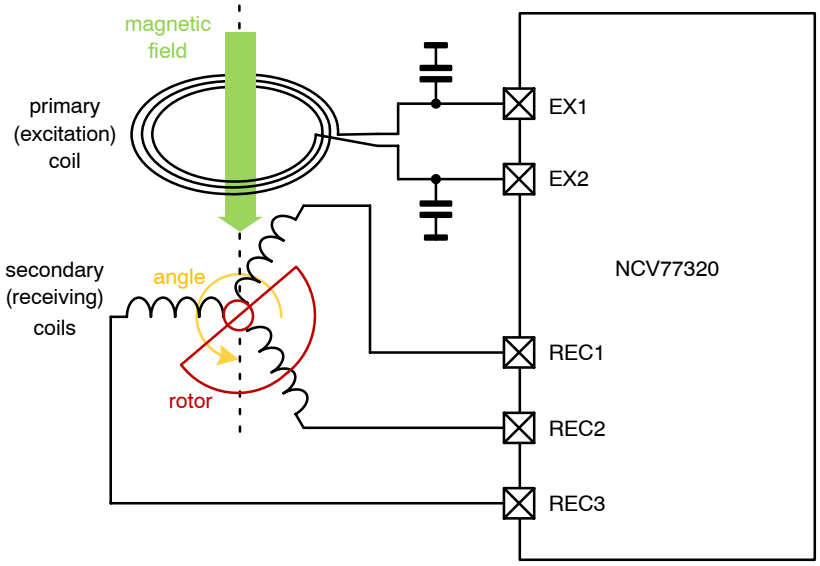


Figure 9. Principle of Inductive Coupling Sensor

Secondary Coil Diagnostics

- *Open of secondary coil* is detected during measurement. Failure flag is set when open connection between two RECx pins is detected (including chip leads and bond wires).
- *Short of secondary coil* structure to supplies (GND, VDD, VCC) or primary coil (EX1, EX2) is detected during measurement. When a short is detected, the error flag is set.

Output states and “fail_flags[15:0]” register mapping are listed in Table 18.

Analog Sensor Interface & DSP

The analog input signals are filtered and amplified for the AD conversion. The angular position is determined by a ratio of amplitudes of 120° shifted signals at the “f_PRIM” frequency induced from the primary coil. The angular position and its corresponding value in a DSP register “pos_raw[15:0]” with respect to signal ratios are shown in Figure 10. The calculated position in “pos_raw[15:0]” register is updated with period “t_PER”.

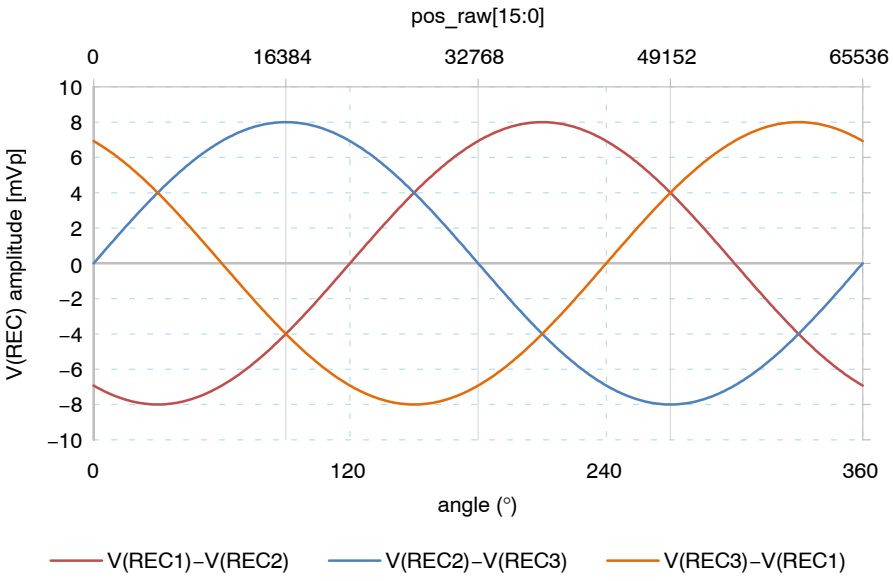


Figure 10. RECx Differential Signal Amplitude at f_PRIM vs. Angular Position

The calculated 16−bit position “pos_raw[15:0]” can be adjusted to application “zero” position by “pos_shift[15:0]” EEPROM parameter. This operation can replace a need for mechanical alignment of a rotor with a sensor PCB. The adjustment is shown in Figure 11 and follows the modulo equation:

$$pos_adj[15:0] = mod(pos_raw[15:0] + pos_shift[15:0], 65536) \quad \text{(eq. 3)}$$

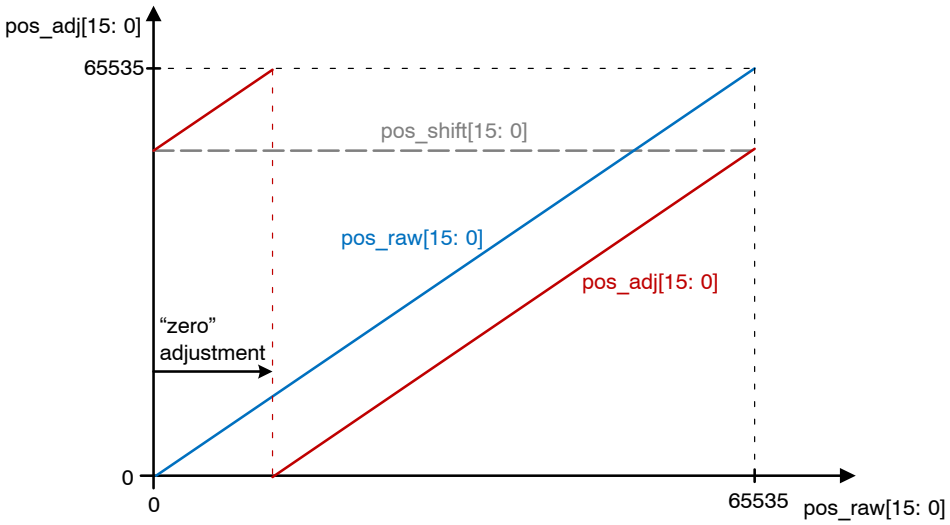


Figure 11. Zero Angle Adjustment Using “pos_shift[15:0]” Register

Multipoint PWL Correction Table

The adjusted position “pos_adj[15:0]” is processed by an 15−point PWL (piece−wise−linear) correction unit. Up to 15 points “$P_k[X_k,Y_k]$” are available ($k \in <0;14>$). The points 0 and 14 have x−position bound to the minimum and the maximum of the “pos_adj[15:0]” range, other points can be set to arbitrary values in ascending order as shown in Figure 12. Correction starts always with point P_0 and continues with next points P_1, P_2, … until a point which has value X_k = 65535.

When the analog output interface is used, it should be limited by programming the PWL table (Y_k) to stay within range of 5% to 95% Vcc, defined by parameters “V_{out_hi}” and “V_{out_lo}” in Table 6. The SENT output should be programmed with the PWL correction table to comply with the SENT specification for the output ranging between 1 and 4088. For the SPI interface, the full output range can be used.

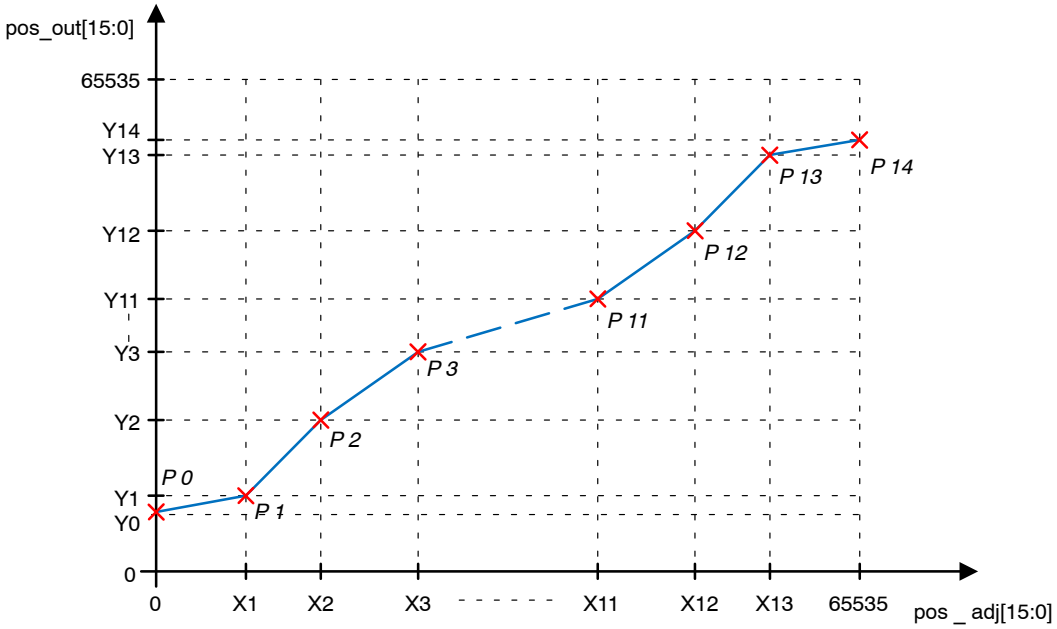


Figure 12. Multi−point PWL Correction Unit

Table 8. PWL CORRECTION TABLE – POINTS DEFINITION

Point	X Coordinate	Y Coordinate
P0	0	pwl_y0[15:0]
P1	pwl_x1[15:0]	pwl_y1[15:0]
P2	pwl_x2[15:0]	pwl_y2[15:0]
P3	pwl_x3[15:0]	pwl_y3[15:0]
P4	pwl_x4[15:0]	pwl_y4[15:0]
P5	pwl_x5[15:0]	pwl_y5[15:0]
P6	pwl_x6[15:0]	pwl_y6[15:0]
P7	pwl_x7[15:0]	pwl_y7[15:0]
P8	pwl_x8[15:0]	pwl_y8[15:0]
P9	pwl_x9[15:0]	pwl_y9[15:0]
P10	pwl_x10[15:0]	pwl_y10[15:0]
P11	pwl_x11[15:0]	pwl_y11[15:0]
P12	pwl_x12[15:0]	pwl_y12[15:0]
P13	pwl_x13[15:0]	pwl_y13[15:0]
P14	65535	pwl_y14[15:0]

PWL Example 1: Full−range Transfer Function with Processing Gain = 1

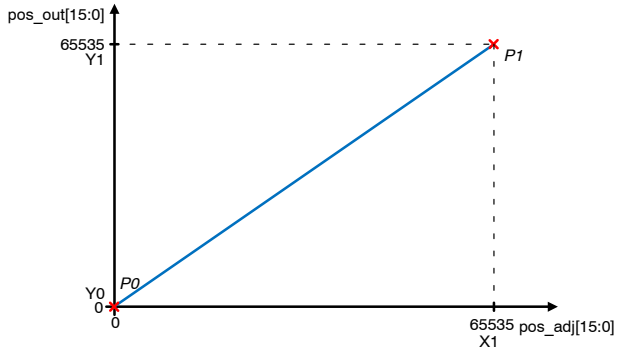


Table 9. PWL EXAMPLE 1 SETTINGS

Point	Register	Value
P0	pwl_y0[15:0]	0
P1	pwl_x1[15:0]	65535
P1	pwl_y1[15:0]	65535

Figure 13. Multi−point PWL Correction − Example 1

PWL Example 2: Full−range Input Inverted Transfer Function with 5% to 95% Output Range Scale

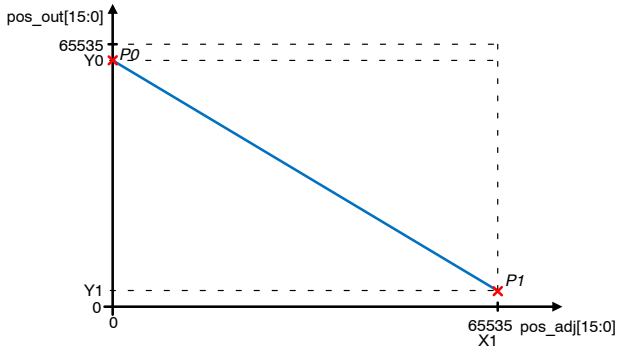


Table 10. PWL EXAMPLE 2 SETTINGS

Point	Register	Value
P0	pwl_y0[15:0]	62260
P1	pwl_x1[15:0]	65535
P1	pwl_y1[15:0]	3277

Figure 14. Multi−point PWL Correction − Example 2

PWL Example 3: 120 ° Input Range Scaled over 5% to 95% Output

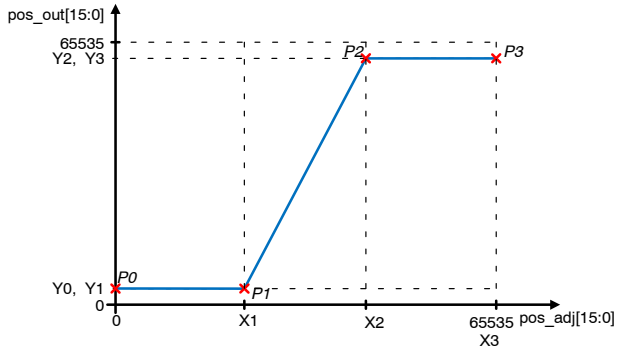


Table 11. PWL EXAMPLE 2 SETTINGS

Point	Register	Value
P0	pwl_y0[15:0]	3277
P1	pwl_x1[15:0]	21846
P1	pwl_y1[15:0]	3277
P2	pwl_x2[15:0]	43691
P2	pwl_y2[15:0]	62260
P3	pwl_x3[15:0]	65535
P3	pwl_y3[15:0]	62260

Figure 15. Multi−point PWL Correction − Example 3

DSP diagnostics

- *"Signal amplitude too low"* is detected when the input signal amplitude drops below "V_REC" low limit.
- *"Direct coupling compensation error"* is detected when "dcc_cXY[7:0]" and "dcc_pwr[2:0]" coefficients are off range, inconsistent or if the compensation vector is too large. The failure flag is also set in a case of missing rotor.
- *"Internal failure error"* flag is set when a failure is detected on internal circuitry (ADC overload, DSP over− or under−flow, gain error, etc.)
- *"PWL table monotonicity failure"* flag is set if Xi coordinates of used calibration points are not set in ascending order (e.g. X0 < X1 < X2 < …etc.) and also is set if the last used Xi coordinate is not equal to 65535.

Output states and "fail_flags[15:0]" register mapping are listed in Table 18.

POWER UP AND OPERATING MODES

The NCV77320 is in POR (power−on−reset) when regulated voltage (VDD pin) drops below “POR_hi” voltage level. The release from POR is additionally conditioned by VCC supply voltage going above “VCC_UV” threshold. A power−up sequencer is implemented in the NCV77320 to bring the device in different modes. The chip can be in two modes after power up:

1. Service mode
2. Operating mode

1) *Service mode* can be entered after POR within the “t_service_max” time window as specified in Table 6. Service mode can be achieved in two ways:
   a. With the serial communication bus operated via the OUT pin:
      This interface is suitable for end of line programming for automotive applications, where only 3 output terminals are used to interface the sensor (GND, OUT and VCC). The interface is described in application note AND90288/D, which is available under NDA.
   b. Via SPI:
      To enter Service mode, the SPI Key−code should be send to the device. After reception of the Key−code, the specific calibration registers can be addressed (Service mode). The SPI Key−code must be received as a first SPI frame and must be received before “t_service_max” time elapses. The NCV77320 is ready to decode SPI Key−code after initialization phase “t_INIT”. The SPI Key−code can be received and SPI Service mode can be opened regardless of SPI activation EEPROM bit “spi_ena”. Figure 16 shows the diagram for entering Service mode via SPI.
      For normal operation, the device needs to be brought to Operating mode via the “EXIT” SPI command.
2) *Operating mode* is achieved after appliance of the normal VCC operating voltage. After POR, the chip will load the operational EEPROM parameters into the device registers. The content of the registers defines behavior of the chip. When the device is brought into Operating mode from Service mode using the ”EXIT” command, the EEPROM parameters are not loaded to the device registers.
   Accessibility of the chip and pin function in Operating mode is summarized in Table 12. The OUT driver and/or SPI interface is activated after initialization phase “t_INIT” elapses.

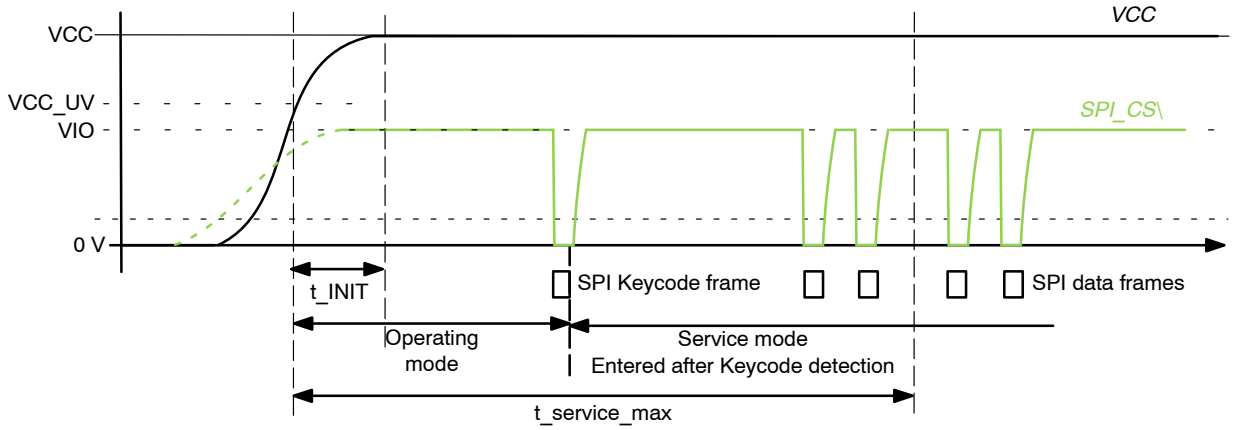


Figure 16. Service Mode Entry Using SPI

Table 12. OPERATING MODE OUTPUT ACCESS CONFIGURATION

EEPROM Parameters			Outputs	
sent_drv	**spi_ena**	**wd_cfg[1:0]**	**SPI Active**	**OUT Pin**
X	1	>0	YES	RST\
0	1	0	YES	Analogue
1	1	0	YES	SENT
0	0	X	NO	Analogue
1	0	X	NO	SENT

Analog Output

The analog driver consists of 16−bit DAC and voltage buffer operating in AB class. The DAC is supplied with the PWL correction unit output “pos_out[15:0]”. The possible voltage range of the Analogue OUT is specified from 5% to 95% VCC.

The output DAC uses the VCC supply voltage as reference. This gives a ratio−metric behavior of the output. For “pos_out[15:0]”, the OUT voltage follows equation:

$$V(OUT) = V(VCC) \cdot \frac{pos_out[15:0]}{65536} \quad \text{(eq. 4)}$$

The NCV77320 signal delay in the Analog OUT configuration is equal to Tau_OUT + t_PER / 2 + POS_DLY. Additionally, filter delay at master module input formed by R_F, C_F has to be taken into account.

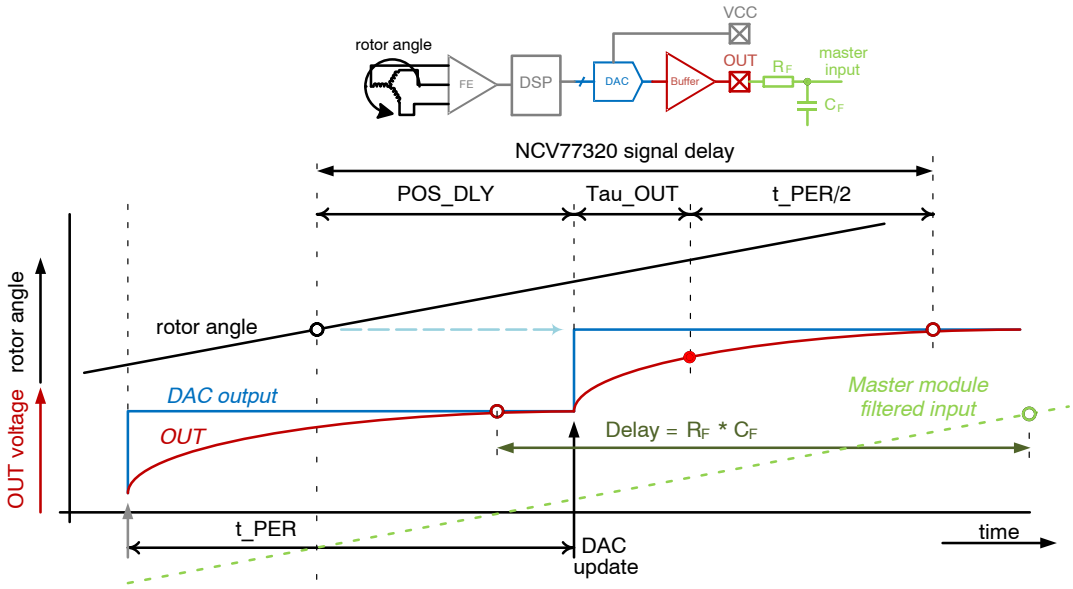


Figure 17. Signal Propagation Using Analog OUT Configuration

The default output setting of the NCV77320 is the Analog mode. In this case, the SENT driver stage is in shut down and in high−Z state. When the device is programmed for SENT operation, the analog driver is placed in High−Z state.

Diagnostic Bands in Analogue OUT Configuration

In the case of failure detection, the OUT pin is switched off as defined in Table 18.

When diagnostic state is entered, minimum duration of the OUT voltage in diagnostic level is “t_DIAG_HOLD”.

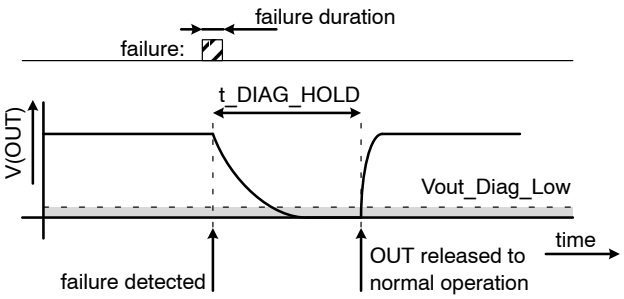


Figure 18. OUT Voltage in Diagnostic State

Pull−down R_{PD} or pull−up R_{PU} resistors assembled at the Master module are necessary to define the OUT wire potential in the case the OUT driver is switched off or when there is a missing VCC or GND connection. The voltage on the OUT wire measured by the master module (ECU) is defined by external resistors and the leakage currents of connected devices and the potential stray resistances on the wiring harness. NCV77320 OUT leakage current for the off state at specific die temperature T_J can be derived from the chart in Figure 20. If allowed by the maximum application temperature and by an application specific diagnostic voltage band, maximum specified value of R_{PD} or R_{PU} as given in Table 4 can be increased.

With OUT driver in off state, transition to Diagnostic level depends on external components, too. Total capacitance on OUT wire C4 + C_F together with R_{PD} or R_{PU} defines the time constant which should be short enough to allow the OUT voltage to settle within “t_DIAG_HOLD” time.

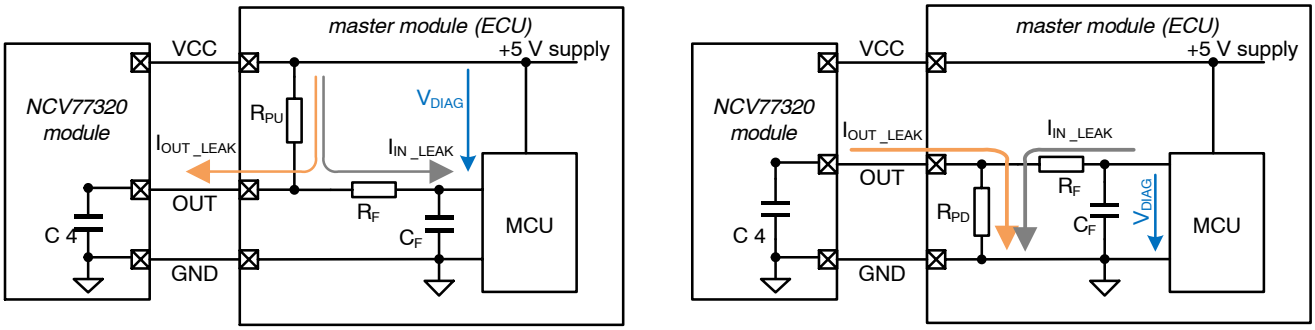


Figure 19. OUT Diagnostic Voltage Level Definition for Switched−off Driver for a) Pull−up, b) Pull−down Resistor

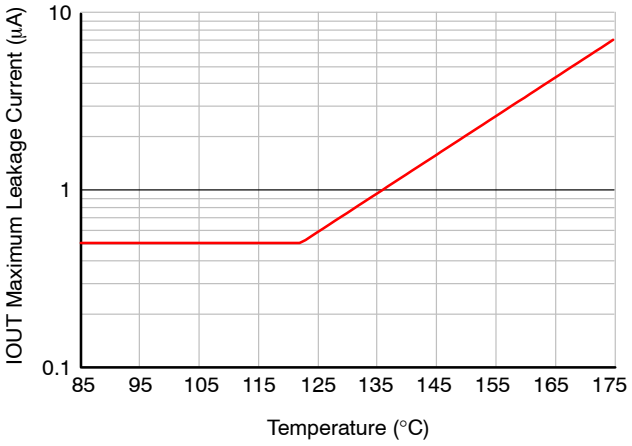


Figure 20. OUT leakage current

SENT Output

The SENT output complies with the standard SAE J2716 protocol. Refer to the SENT Protocol Standard SAE J2716 published April 2016 for the full description of the protocol. Figure 21 shows the standard SENT frame format.

There are two SENT frame formats implemented in NCV77320:

- H.1 – two 12 bit fast channels: position/angle in channel 1, temperature in channel 2
- H.4 – secure sensor with 12 bit fast channel: position/angle in channel 1, 8−bit counter incremented in each frame with rollover from 255 to 0 in channel 2.

Detail composition of the SENT frame is shown in Table 13.

The NCV77320 makes use of the Enhanced serial channel for diagnostic and device information.

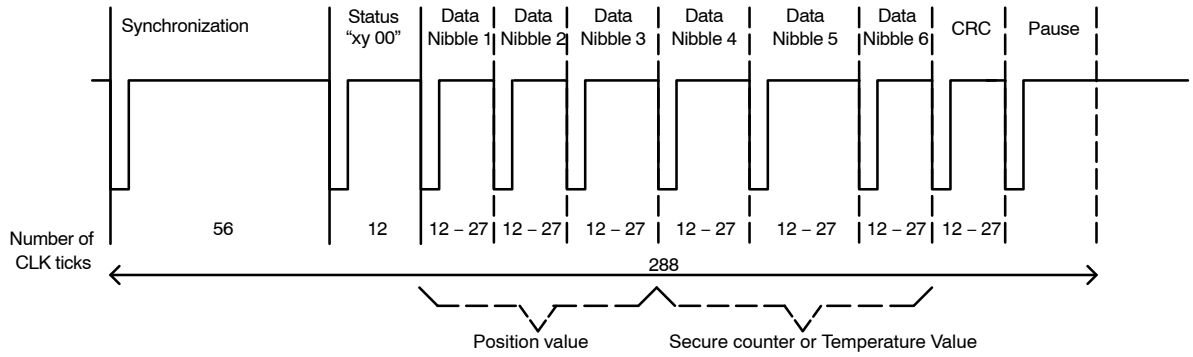


Figure 21. Fast Channels SENT Frame Format

Table 13. SENT FRAME FORMAT

Pulse / Nibble	Nibble content	
	H.1 SENT Frame Format sent_ch2_cnt = 0	**H.4 SENT Frame Format sent_ch2_cnt = 1**
Calibration/Synchronization pulse	56 SENT ticks pulse	
Status and Communication Nibble	Bit 1, 0: channel error Bit 3, 2: Serial message	Bit 0: channel1 data error Bit 1: zero Bit 3, 2: Serial message
Fast Channel 1, data nibble 1	Clamped position/angle pos_out[15:12]	Clamped position/angle pos_out[15:12]
Fast Channel 1, data nibble 2	Clamped position/angle pos_out[11:8]	Clamped position/angle pos_out[11:8]
Fast Channel 1, data nibble 3	Clamped position/angle pos_out[7:4]	Clamped position/angle pos_out[7:4]
Fast Channel 2, data nibble 4	Temperature temp[3:0]	Secure counter bits [7:4]
Fast Channel 2, data nibble 5	Temperature temp[7:4]	Secure counter bits [3:0]
Fast Channel 2, data nibble 6	Temperature temp[11:8]	Bit inversion of data nibble 1
CRC/Checksum Nibble	CRC is calculated according to SAE J2716, section 5.4.2.2 Recommended Implementation	
Pause pulse (optional)	If enabled by sent_pause_pls = 1, pause pulse follows CRC nibble to adjust SENT frame length to 4 * t_PER	

Calibration / Synchronization Pulse

Pulse length is derived from time elapsed between two falling edges. Calibration / Synchronization pulse is 56 SENT tick period long. Nominal tick pulse length is set to “t_SENT” (3 μs).

Calibration / Synchronization pulse is used for determination of the frame start and measurement of the tick time. Actual tick time per frame is obtained as calibration pulse length divided by 56.

Following nibbles value is then equal to nibble length / tick time minus 12. The value of the nibble is a 4 bit number in a range <0 .. 15>.

Status and Communication Nibble

Nibble bit 0: error associated with data of fast channel 1 appeared.

Nibble bit 1: error associated with data of fast channel 2 appeared.

Nibble bits 2 and 3: Serial Data message bits.

Data Nibbles (Fast Channels)

Reserved signal ranges are defined by SAE J2716. Position/angle and temperature signal value ranges are limited to codes 1..4088 as shown in Table 14.

Table 14. DATA NIBBLE RESERVED VALUES

Signal	Value	Description
Error indicator	4089 .. 4095	Codes reserved for error indicators. Only value 4091 (Generic error) is used in NCV77320
Channel data	1 .. 4088	Valid data range
Initialization	0	Not used in NCV77320. SENT driver is not enabled in t_INIT phase

Position / Angle Signal

Position/angle is provided on Fast Channel 1. The SENT nibble encoder is supplied with the PWL correction unit output “pos_out[15:4]”.

The total signal delay in the SENT configuration with pause pulse enabled is equal to (SENT_delay + POS_DLY). The delay is taken to the 1st falling edge of the status nibble. Without pause pulse, additional delay varies between 0 µs and SENT frame length. SENT_delay = 71 µs at typ. clock.

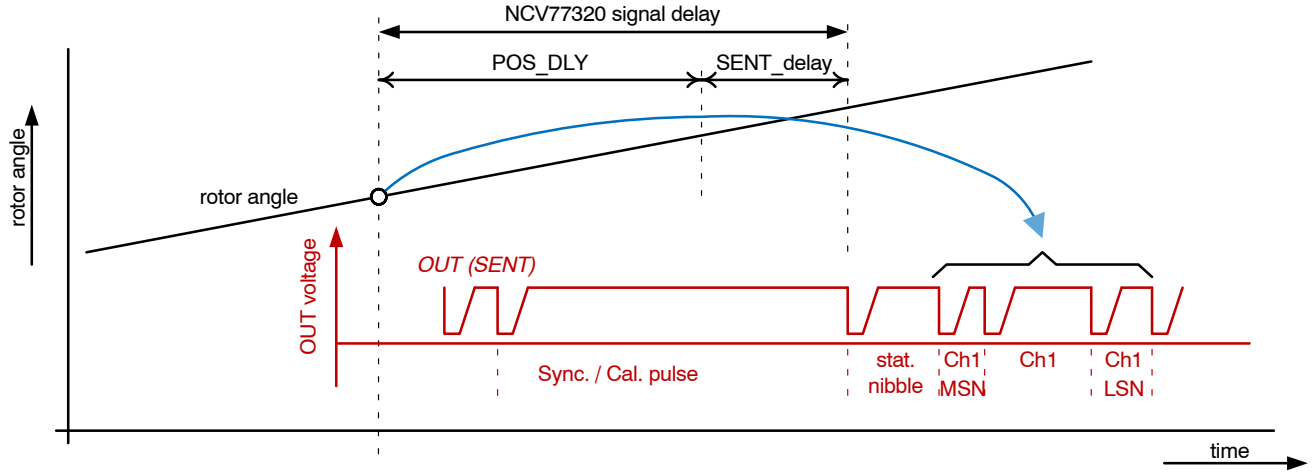


Figure 22. Signal Delay in the SENT Frame

Temperature Signal

Temperature information is provided on Fast Channel 2. Temperature is coded as a 12−bit number according to SAE J2716 E.2.2.1:

- Slope S_{TF} = 8 LSB / K
- Offset T_{OFFSET} = 200 K

$$temperature[11:0] = round(S_{TF} \cdot (T[K] - T_OFFSET) / [K]) \quad \text{(eq. 5)}$$

Numerical temperature output range is limited to 1 .. 4088 which corresponds to −73.025°C to 437.85°C.

SENT Enhanced Serial Message

The NCV77320 makes use of the Enhanced serial channel for diagnostic and device information.

The Status bits 2 and 3 of the NCV77320 are used for the Enhanced serial channel operation. The drawing below shows the frame format. In total 18 SENT frames are used to build a full Enhanced serial message.

Bit 3 indicates the start of the Enhanced channel frame data when 6 consecutive “1” bits followed by one “0” is send. The configuration bit as being “0” and the 8 bits ID are following. Bit 2 contains only the CRC and 12 bits data content over the full Enhanced frame.

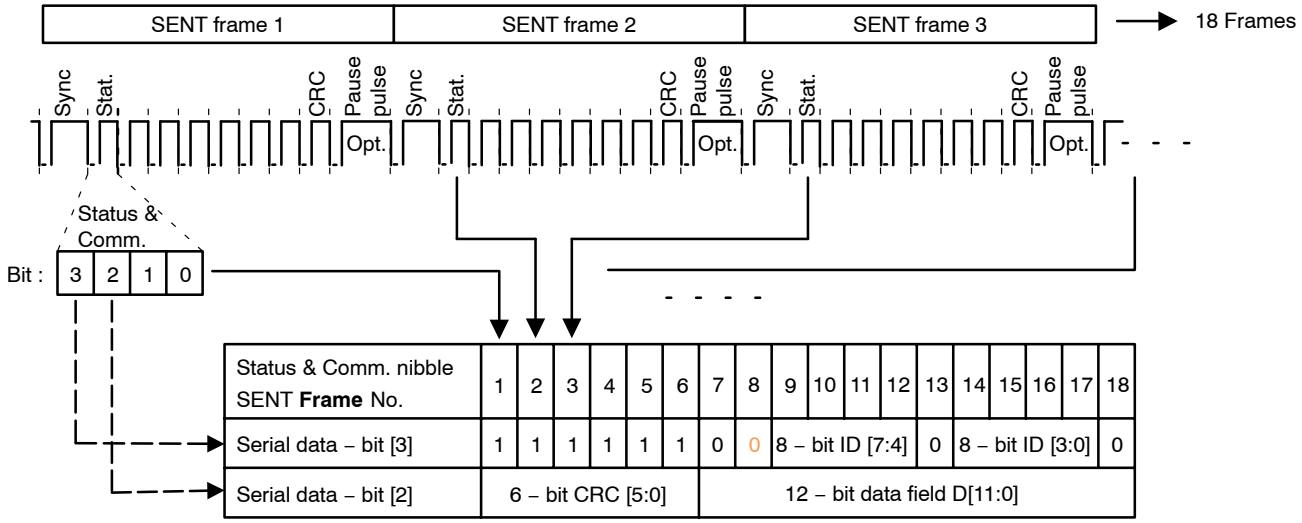


Figure 23. Enhanced Slow Channels SENT Frame Format

SENT serial communication is free running and not synchronized with any on chip failure. This means that depending on the error detected, the SENT driver is switched off (e.g. short at the output pin). The SENT serial communication does not necessarily start with SENT frame No.1 after the error is released and by that, the Master module always should resynchronize to the next full frame indicated by the start bits.

Table 15. ENHANCED SERIAL MESSAGE SEQUENCE

Serial Message No.	Message ID	Description	Data Field D[11:0]
1	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
2	0x23	Temperature code	temp[11:0]
3	sent_idpg1[3:0] * 16 + sent_id11[3:0]	user data	sent_data_11[11:0]
4	sent_idpg1[3:0] * 16 + sent_id12[3:0]	user data	sent_data_12[11:0]
5	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
6	0x03	SENT sensor type	sent_sensor_type[11:0]
7	sent_idpg1[3:0] * 16 + sent_id13[3:0]	user data	sent_data_13[11:0]
8	sent_idpg1[3:0] * 16 + sent_id14[3:0]	user data	sent_data_14[11:0]
9	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
10	0x05	SENT manufacturer code	sent_manufacturer_code[11:0]
11	sent_idpg2[3:0] * 16 + sent_id21[3:0]	user data	sent_data_21[11:0]
12	sent_idpg2[3:0] * 16 + sent_id22[3:0]	user data	sent_data_22[11:0]
13	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
14	0x06	SENT protocol revision	sent_protocol_rev[11:0]
15	sent_idpg2[3:0] * 16 + sent_id23[3:0]	user data	sent_data_23[11:0]
16	sent_idpg2[3:0] * 16 + sent_id24[3:0]	user data	sent_data_24[11:0]
17	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
18	0x23	Temperature code	temp[11:0]
19	sent_idpg3[3:0] * 16 + sent_id31[3:0]	user data	sent_data_31[11:0]
20	sent_idpg3[3:0] * 16 + sent_id32[3:0]	user data	sent_data_32[11:0]
21	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
22	0x83	EX current code	D[11:8] = 0x0, D[7:0] = preset_curr[7:0]
23	sent_idpg3[3:0] * 16 + sent_id33[3:0]	user data	sent_data_33[11:0]
24	sent_idpg3[3:0] * 16 + sent_id34[3:0]	user data	sent_data_34[11:0]
25	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
26	0x85	V_REC amplitude	D[11:0] = vrec_amp[16:5]
27	sent_idpg4[3:0] * 16 + sent_id41[3:0]	user data	sent_data_41[11:0]
28	sent_idpg4[3:0] * 16 + sent_id42[3:0]	user data	sent_data_42[11:0]
29	0x01	Failure flags	D[11:9] = 0x0, D[8:0] = fail_flags[8:0]
30	0x87	SENT device ID	sent_dev_id[11:0]
31	sent_idpg4[3:0] * 16 + sent_id43[3:0]	user data	sent_data_43[11:0]
32	sent_idpg4[3:0] * 16 + sent_id44[3:0]	user data	sent_data_44[11:0]

Refer to the EEPROM data Table 19 and Table 20 for further information on the frame contents.

SENT Serial Message CRC

The CRC is computed as a function of the contents of serial data message bits [2] and [3] for status and communication nibbles / SENT frames 7−18 according to SAE J2716, section 5.2.4.3 Enhanced Serial Message Format CRC.

The SENT serial message CRC uses the polynomial X6 + X4 + X3 + X0 with initial seed of ’b010101. The CRC is calculated from serial data bits [2] and [3] starting with Frame 7 ending Frame 18. The order of bits is:

Frame 7 bit #2 (MSB of Data),
Frame 7 bit #3 (as being 0),
Frame 8 bit #2 (Bit 10 of Data),
Frame 8 bit #3 (as being 0),
–
–
–
Frame 18 bit #2 (Bit 0 of Data),
Frame 18 bit #3 (as being 0).

SPI INTERFACE

Physical Interface

The NCV77320 has an SPI interface that is aside of the Analog output or SENT output operation active.

When the application does not require SPI operation, the “spi_ena” bit in the EEPROM should be set to “0”, the SPI_CS\, SPI_SI, SPI_CLK and SPI_SO pins should be tied to GND.

The VIO pin should be connected to the supply voltage (3.3 V or 5 V) of the micro controller that is used.

With the SPI interface, the NCV77320 is fully accessible and allows for event driven operation with the SPI_INT\ pin.

The SPI interface works in 32 bit mode but is compatible with 16 and 8 bit SPI interfaces. The high level block diagram of the SPI slave is shown in the following figure.

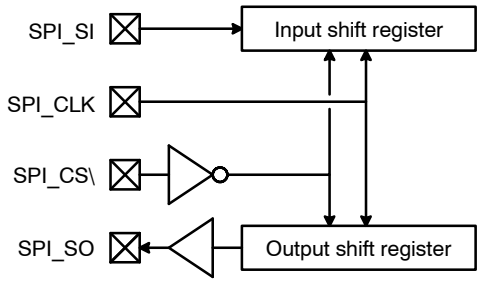


Figure 24. SPI High Level Block Diagram

Each frame contains 32 clock cycles that might be composed from 1 x 32 bits, 2 x 16 bits or 4 x 8 bits. When the NCV77320 does not receive 32 bits within one frame or received frame has wrong CRC, the message is discarded and an error bit indicates the “spi_err” for the next successful SPI cycle. Error bit “pos_err” is set when “pos_out[15:0]” does not contain correct position data.

The data transfer is initiated by the SPI_CS\ going low. The data that is then loaded in the output shift register is defined by the address of the previous valid SPI transfer. The output shift register is clocked out on the rising edge of the SPI_CLK, the input shift register is clocked at the rising edge as well.

When the SPI_CS\ is high, any signal at the SPI_CLK and SPI_SI pins is ignored and SPI_SO is forced into a high impedance state.

The NCV77320 has two different frame structures. In Service mode, all registers of the device are accessible. In Operational mode only single word read operations are available.

SPI in Operational Mode

During Operational mode, there are 4 commands available. Table 16 shows the commands. Figure 25 shows the frame structure.

Table 16. COMMANDS OF THE SPI OPERATIONAL MODE

Command	CMD [1:0]	ADDRESS [5:0]	SPI_SO DATA[15:0]	SPI_SO CNT[3:0]	SPI_SO spi_err	SPI_SO pos_err	SPI_SI DATA[15:0]	Description
Read Run Time Data	0	Memory_RT ADDRESS [5:0]	Memory_RT DATA[15:0]	cnt[3:0]	spi_err	pos_err	*ignored*	read of a register indexed with the run time data address
Read Memory	1	Memory ADDRESS [5:0]	Memory DATA[5:0]	cnt[3:0]	spi_err	pos_err	*ignored*	read of a register indexed with the address
Kick Watchdog	2	0x3F	pos_out[15:0]	cnt[3:0]	spi_err	pos_err	[15:8] = WD_stop_time [7:0] = WD_start_time	write watchdog refresh, update WD window start and stop time in ms; read of the position/angle and failure flags
Write Key−code	3	0x3E	pos_out[15:0]	cnt[3:0]	spi_err	pos_err	ignored	write Key code to enter Service mode; read of the position/angle and failure flags

Counter cnt[3:0] is freely overflowing counter, which shall be incremented per each correctly received SPI frame.

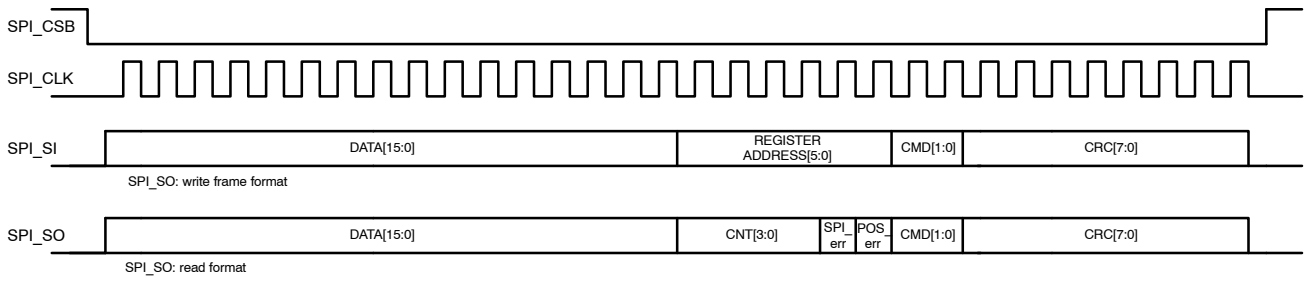


Figure 25. SPI Frame Structure for Operational Mode Operation

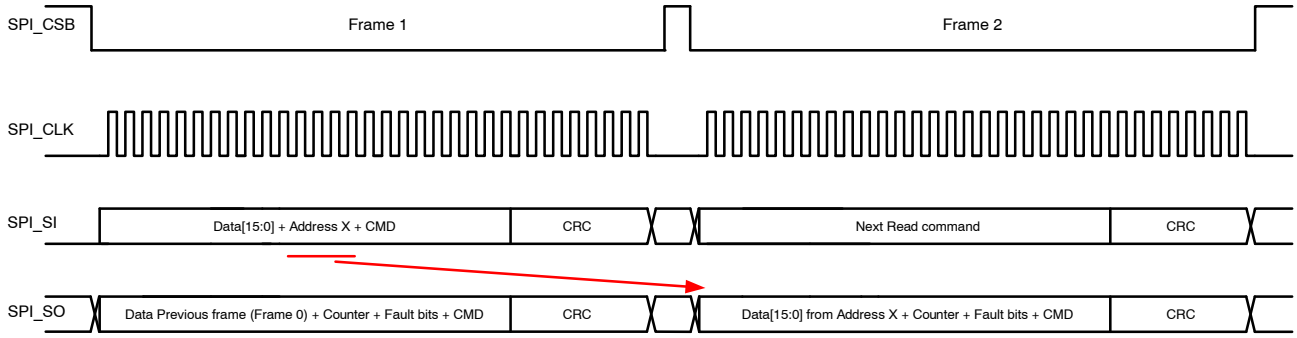


Figure 26. SPI Read Structure for Operational Mode Operation

SPI CRC 8−bit code (ATM−8) is calculated over the whole data in the frame using polynomial 0x107, seed value is 0xFF.

Polynomial:

$$x^8 + x^2 + x^1 + x^0 \quad \text{(eq. 6)}$$

SPI in Service Mode

Figure 27 shows the command structure for Service mode. Sixteen bits are used for data. Next is a 6 bit start address, which selects an SPI address from where the data should be written or read. The command is given in the third byte, it is 3 bits long. The end address is given by the last 6 bits. While the Service mode is only used for End of line calibration, the messages do not contain a CRC for error detection and correction.

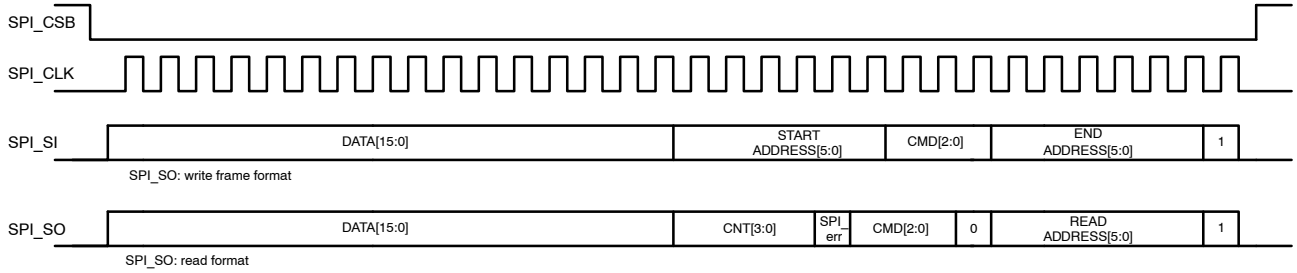


Figure 27. SPI Frame Structure for Service Mode Operation

Table 17. COMMANDS OF THE SPI SERVICE MODE

Command	CMD[2]	CMD[1]	CMD[0]	Description
WRITE	0	1	0	Write DATA[15:0] to memory bank to START ADDRESS[5:0]; END ADDRESS[5:0] is not used
READ	1	0	0	Read DATA[15:0] from memory bank from address START ADDRESS[5:0]; END ADDRESS[5:0] is not used
PROG	1	1	0	Program EEPROM address space between START ADDRESS[5:0] and END ADDRESS[5:0] with content from memory bank; DATA[15:0] not used
RFRH	0	0	0	Refresh EEPROM address space between START ADDRESS[5:0] and END ADDRESS[5:0] to memory bank; DATA[15:0] not used
VERIFY	0	0	1	Verify EEPROM content of address space between START ADDRESS[5:0] and END ADDRESS[5:0] with memory bank; DATA[15:0] not used
WRITE_RT	0	1	1	Write DATA[15:0] to run time memory bank to START ADDRESS[5:0]; END ADDRESS[5:0] is not used
READ_RT	1	0	1	Read DATA[15:0] from run time memory bank from address START ADDRESS[5:0]; END ADDRESS[5:0] is not used
EXIT	1	1	1	Exit from Service mode to Operational mode; DATA[15:0], START ADDRESS[5:0] and STOP ADDRESS[5:0] are not used

After “PROG” command, the device is busy for “T_{PROG}” time with EEPROM programming. During that period, SPI response has all bits set to 1 and all incoming SPI frames are ignored.

After “VERIFY” command, master device should wait for “T_{VERIFY}” and then “ee_verify” (bit 15) can be checked by “READ_RT” command of address 12.

Tables 19 and 20 show all the accessible registers and the description for the bit and word functions.

SPI Interrupt Output

The SPI interrupt is used to indicate to the micro controller that a new position/angle is available from the digital sampler or new ADC data is available in case of direct ADC data read out. After reset, the SPI_INT\ pin is high (Pull−up required to VIO). When a sample scan is finished, the SPI_INT\ pin goes low. After the SPI read of the position the SPI_INT\ pin is brought back to a high state again.

Position/Angle Data Read Out (direct_adc = 0)

There are two modes of operation determined by the “spi_int_edge” parameter:

Level sensitive interrupt (spi_int_edge = 0) provides always latest available data via the “pos_out[15:0]” register. If during the SPI transmission a new position becomes available, the SPI_INT\ pin will stay low, to indicate that there is new data available again.

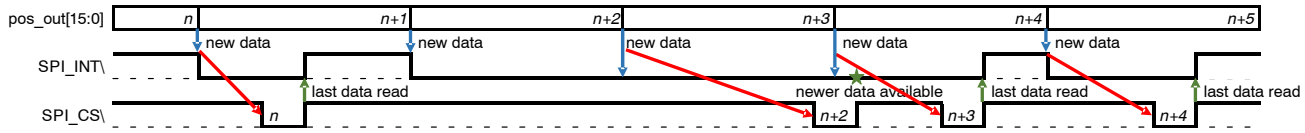


Figure 28. SPI Level Sensitive Interrupt spi_int_edge = 0

Edge sensitive interrupt (spi_int_edge = 1) provides the “pos_out[15:0]” register data which was present at the SPI_INT\ falling edge moment. If during the SPI transmission a new position becomes available, the SPI_INT\ pin will return to high level after the SPI transmission and the presence of the new data is not indicated.

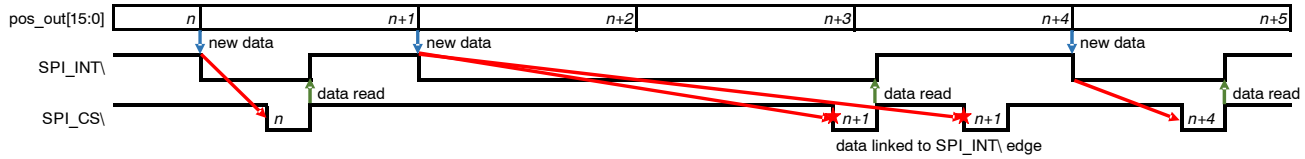


Figure 29. SPI Edge Sensitive Interrupt spi_int_edge = 1

Direct ADC Data Read Out (direct_adc = 1)

Direct ADC mode is implemented for systems, which use the NCV77320 only for input sample acquisition. With this acquired channel information, the master module can calculate the position externally.

As direct ADC mode requires sampling to be bound together and acquired under the same condition (AGC etc), it is recommended that the SPI operation is always using the interrupt.

When the direct ADC mode is enabled, ADC data (registers “rec32 amp[15:0]” and “rec21_amp[15:0]” in runtime memory) are available to be read out and SPI_INT\ always behaves like Edge sensitive. Very important is that the master device is well aware of correct pairing based on the interrupt signal and that it never will ask for data when the interrupt signal is high. In direct ADC mode, internally calculated position is not correct and therefore register “pos_out[15:0]” is kept reset to 0.

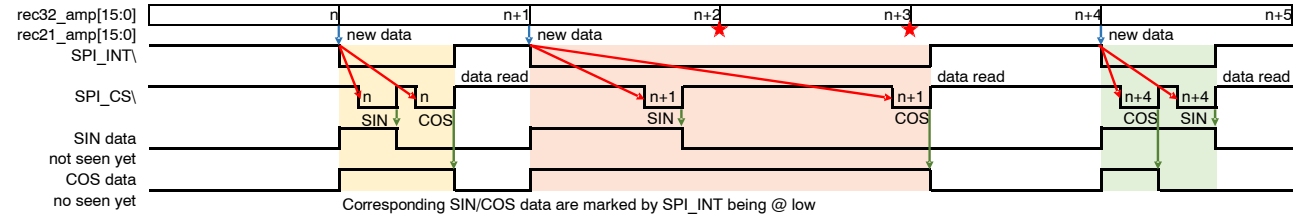


Figure 30. SPI Edge Sensitive Interrupt Direct_adc = 1

SPI_INT\ monitoring:

- *SPI_INT\ error*: Is set when logic 0 is detected at SPI_INT\ while no new position data is available (SPI_INT\ should be high). Monitoring is active when SPI is enabled and independently of whether level/edge sensitive interrupt is selected.

Output states and “fail_flags[15:0]” register mapping are listed in Table 18.

Watchdog

The NCV77320 contains a watchdog that can be operated when SPI mode (“SPI_ENA” bit) is selected. The Watchdog should be enabled in Service mode by writing a value in the EEPROM bit ”WD_CFG[1:0]“ that is >0. When the value is ‘0’, the watchdog is disabled.

The value of “WD_CFG[1:0]” is specifying the initial watchdog comparator value that is used after power on reset. The initial watchdog comparator value is applied also after NCV77320 initiates reset pulse on the OUT pin and after the Service mode is finished by issuing of EXIT command.

Watchdog is inactive in Service mode.

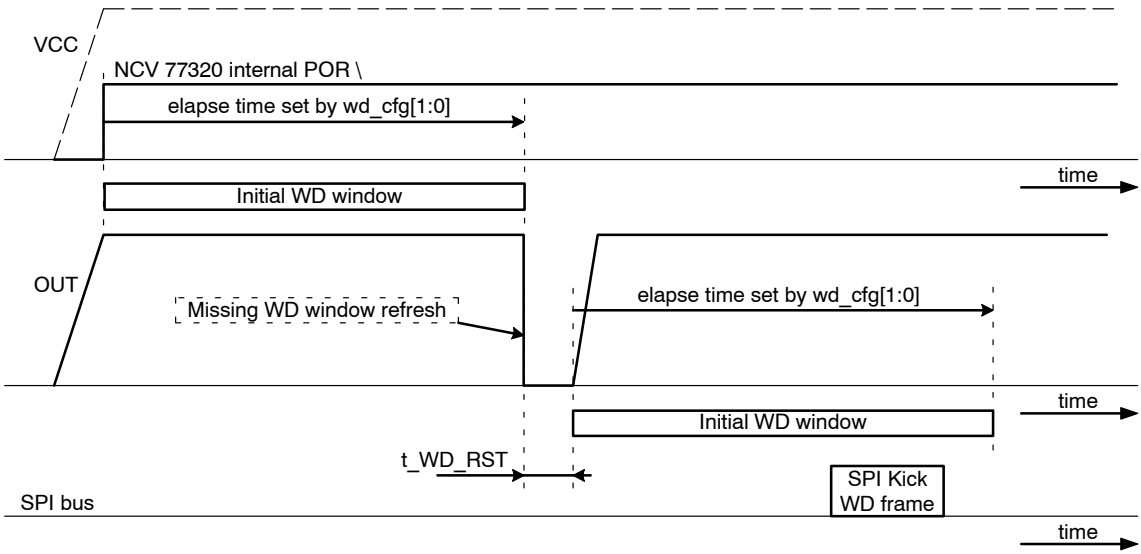


Figure 31. Initial Watchdog Window Settings

When the Watchdog is enabled, repetitive SPI write frames Kick Watchdog (CMD[1:0] = 2) should be received by the NCV77320 to stay in operation. This command resets the watchdog counter and writes the new values WD_start_time [ms] for the window start and WD_stop_time [ms] for window stop times. The next Kick Watchdog (CMD[1:0] = 2) SPI command should be send within the written window. When the Kick Watchdog SPI command arrives before start of the window (Early refresh) or didn’t arrive before the end of the window (Late refresh), the OUT pin is forced low for a duration of “t_WD_RST“ to reset or interrupt the system micro controller. The OUT pin is also forced low when Watchdog refresh contains invalid start and stop time, meaning start = 0 or start ≥ stop.

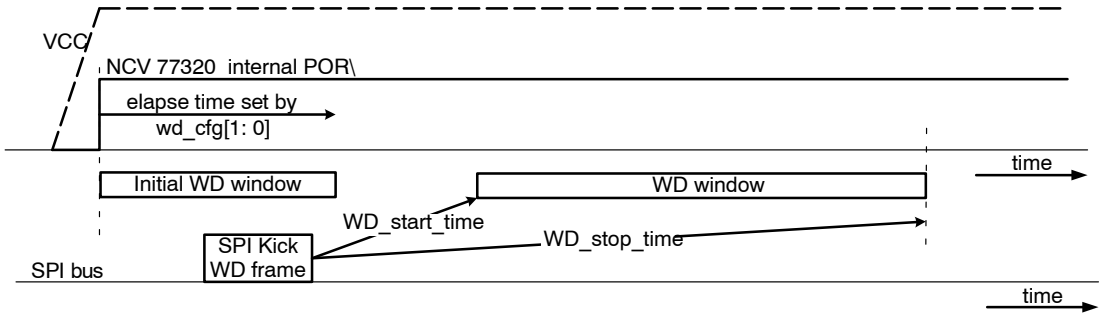


Figure 32. Watchdog Window Control

DIAGNOSTICS

The NCV77320 has several diagnostic circuitries to check for errors in the chip and connected coil structure in− and outputs.

Table 18. Diagnostics

Detected Failure	fail_flags[15:0]	V(OUT) Analogue Config	OUT SENT Config	SPI
Primary frequency out of limits	0	High Z (Note 12)	active	active
Primary amplitude too low	1	High Z (Note 12)	active	active
Primary common mode voltage out of range	2	High Z (Note 12)	active	active
Secondary coil open	3	High Z (Note 12)	active	active
Secondary coil short	4	High Z (Note 12)	active	active
Signal amplitude too low	5	High Z (Note 12)	active	active
Direct coupling compensation failure	6	High Z (Note 12)	active	active
Internal failure	7	High Z (Note 12)	active	active
PWL table monotonicity failure	8	High Z (Note 12)	active	active
GND loss	9	High Z (Note 12)	High Z	active
SPI_INT\ error	10	N.A.	N.A.	active
OUT pin overdriven	11	High Z (Note 12)	High Z	active
Supply voltage too high or low V(VCC) > VCC_OV or V(VCC) < VCC_UV	12	High Z (Note 12)	High Z	active
Regulated voltage pulled high V(VDD) > VDD_OV	13	High Z (Note 12)	High Z	active
Regulated voltage overloaded V(VDD) < VDD_OVLD	14	High Z (Note 12)	High Z	active
Memory CRC failure	15	High Z (Note 12)	High Z	active

12. Pull−up RPU or pull−down RPD defines failure band

Diagnostic:

- *GND loss*: Detection of the GND pin connection loss
- *OUT pin overdriven*: Detection of the overdrive of the driver at OUT pin, works in both configurations – Analog/SENT

In Operating mode, part of failure flag register “fail_flags[8:0]” is accessible via SENT Enhanced serial channel Message ID = 0x01.

Complete “fail_flag[15:0]” is accessible in Service mode and in SPI mode.

MEMORY MAP (EEPROM + STATE REGISTERS) CONTENTS TABLES

Table 19. CONFIGURATION MEMORY CONTENT

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value
7	15:0	R/W	crc_cal[15:0]	CRC code protecting addresses 7 to 11	2866
8	1:0	R/W	wd_cfg[1:0]	Watchdog configuration 0 … WD disabled 1 … 5 ms Initial WD window 2 … 20 ms Initial WD window 3 … 200 ms Initial WD window	0
8	2	R/W	spi_ena	SPI interface 0 = inactive, SPI_SO = HiZ 1 = active	0
8	3	R/W	spi_int_edge	SPI interrupt SPI_INT\ mode 0 = Level triggered mode 1 = Edge triggered mode	0
8	4	R/W	direct_adc	Selection of the position data calculation 0 = internally 1 = externally (only direct ADC data provided)	0
8	10:8	R/W	dcc_pwr[2:0]	Direct coupling compensation magnifier	0
8	11	R/W	inp_diag_per	Input diagnostic period 0 = default / dual system chip A 1 = dual system chip B	0
8	12	R/W	sent_drv	OUT pin configuration 0 = Analogue driver 1 = SENT driver	0
8	13	R/W	sent_pause_pls	SENT Pause Pulse 0 = disabled 1 = enabled, length of SENT frame = t_PER	0
8	14	R/W	sent_ser_msg	SENT Enhanced serial message 0 = disabled 1 = enabled	0
8	15	R/W	sent_ch2_cnt	SENT channel 2 data content 0 = temperature (temp[11:0]) 1 = frame counter	0
9	15:0	R/W	pos_shift[15:0]	Position zero adjustment	0
10	6:0	R/W	dcc_c23[6:0]	Direct coupling compensation REC2−REC3 coefficient	0
10	7	R/W	dcc_sgn23	Direct coupling compensation REC2−REC3 sign	0
10	14:8	R/W	dcc_c12[6:0]	Direct coupling compensation REC1−REC2 coefficient	0
10	15	R/W	dcc_sgn12	Direct coupling compensation REC1−REC2 sign	0
11	14:0	R/W	fail_flag_dis[14:0]	Disables detections according to fail_flag[14:0] assignment	0
11	15	R/W	lock_cal	Lock bit for CAL part: addresses 7 – 11. When lock_cal is set, appropriate EEPROM addresses cannot be modified	0
12	15:0	R/W	crc_pos1[15:0]	CRC protection for addresses 12 – 20	29696
13	15:0	R/W	pwl_y0[15:0]	15−point PWL correction point P0	3296
14	15:0	R/W	pwl_x1[15:0]	15−point PWL correction point P1	65535
15	15:0	R/W	pwl_y1[15:0]	15−point PWL correction point P1	62240
16	15:0	R/W	pwl_x2[15:0]	15−point PWL correction point P2	0
17	15:0	R/W	pwl_y2[15:0]	15−point PWL correction point P2	0

Table 19. CONFIGURATION MEMORY CONTENT (continued)

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value
18	15:0	R/W	pwl_x3[15:0]	15−point PWL correction point P3	0
19	15:0	R/W	pwl_y3[15:0]	15−point PWL correction point P3	0
20	15:0	R/W	pwl_x4[15:0]	15−point PWL correction point P4	0
21	15:0	R/W	crc_pos2[15:0]	CRC protection for addresses 21 − 29	8412
22	15:0	R/W	pwl_y4[15:0]	15−point PWL correction point P4	0
23	15:0	R/W	pwl_x5[15:0]	15−point PWL correction point P5	0
24	15:0	R/W	pwl_y5[15:0]	15−point PWL correction point P5	0
25	15:0	R/W	pwl_x6[15:0]	15−point PWL correction point P6	0
26	15:0	R/W	pwl_y6[15:0]	15−point PWL correction point P6	0
27	15:0	R/W	pwl_x7[15:0]	15−point PWL correction point P7	0
28	15:0	R/W	pwl_y7[15:0]	15−point PWL correction point P7	0
29	15:0	R/W	pwl_x8[15:0]	15−point PWL correction point P8	0
30	15:0	R/W	crc_pos3[15:0]	CRC protection for addresses 30 − 38	8412
31	15:0	R/W	pwl_y8[15:0]	15−point PWL correction point P8	0
32	15:0	R/W	pwl_x9[15:0]	15−point PWL correction point P9	0
33	15:0	R/W	pwl_y9[15:0]	15−point PWL correction point P9	0
34	15:0	R/W	pwl_x10[15:0]	15−point PWL correction point P10	0
35	15:0	R/W	pwl_y10[15:0]	15−point PWL correction point P10	0
36	15:0	R/W	pwl_x11[15:0]	15−point PWL correction point P11	0
37	15:0	R/W	pwl_y11[15:0]	15−point PWL correction point P11	0
38	15:0	R/W	pwl_x12[15:0]	15−point PWL correction point P12	0
39	15:0	R/W	crc_pos4[15:0]	CRC protection for addresses 39 − 43	2866
40	15:0	R/W	pwl_y12[15:0]	15−point PWL correction point P12	0
41	15:0	R/W	pwl_x13[15:0]	15−point PWL correction point P13	0
42	15:0	R/W	pwl_y13[15:0]	15−point PWL correction point P13	0
43	15:0	R/W	pwl_y14[15:0]	15−point PWL correction point P14	0
44	11:0	R/W	sent_sensor_type[11:0]	SENT enhanced message: Sensor type	0
44	15:12	R/W	sent_idpg1[3:0]	SENT enhanced message ID field	0
45	11:0	R/W	sent_manufacturer_code[11:0]	SENT enhanced message: Manufacturer code	0
45	15:12	R/W	sent_idpg2[3:0]	SENT enhanced message ID field	0
46	11:0	R/W	sent_protocol_rev[11:0]	SENT enhanced message: Protocol Revision	0
46	15:12	R/W	sent_idpg3[3:0]	SENT enhanced message ID field	0
47	11:0	R/W	sent_dev_id[11:0]	SENT enhanced message: Device ID	0
47	15:12	R/W	sent_idpg4[3:0]	SENT enhanced message ID field	0
48	11:0	R/W	sent_data_11[11:0]	SENT enhanced message data field	0
48	15:12	R/W	sent_id11[3:0]	SENT enhanced message ID field	0
49	11:0	R/W	sent_data_12[11:0]	SENT enhanced message data field	0
49	15:12	R/W	sent_id12[3:0]	SENT enhanced message ID field	0
50	11:0	R/W	sent_data_13[11:0]	SENT enhanced message data field	0
50	15:12	R/W	sent_id13[3:0]	SENT enhanced message ID field	0
51	11:0	R/W	sent_data_14[11:0]	SENT enhanced message data field	0

Table 19. CONFIGURATION MEMORY CONTENT (continued)

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value
51	15:12	R/W	sent_id14[3:0]	SENT enhanced message ID field	0
52	11:0	R/W	sent_data_21[11:0]	SENT enhanced message data field	0
52	15:12	R/W	sent_id21[3:0]	SENT enhanced message ID field	0
53	11:0	R/W	sent_data_22[11:0]	SENT enhanced message data field	0
53	15:12	R/W	sent_id22[3:0]	SENT enhanced message ID field	0
54	11:0	R/W	sent_data_23[11:0]	SENT enhanced message data field	0
54	15:12	R/W	sent_id23[3:0]	SENT enhanced message ID field	0
55	11:0	R/W	sent_data_24[11:0]	SENT enhanced message data field	0
55	15:12	R/W	sent_id24[3:0]	SENT enhanced message ID field	0
56	11:0	R/W	sent_data_31[11:0]	SENT enhanced message data field	0
56	15:12	R/W	sent_id31[3:0]	SENT enhanced message ID field	0
57	11:0	R/W	sent_data_32[11:0]	SENT enhanced message data field	0
57	15:12	R/W	sent_id32[3:0]	SENT enhanced message ID field	0
58	11:0	R/W	sent_data_33[11:0]	SENT enhanced message data field	0
58	15:12	R/W	sent_id33[3:0]	SENT enhanced message ID field	0
59	11:0	R/W	sent_data_34[11:0]	SENT enhanced message data field	0
59	15:12	R/W	sent_id34[3:0]	SENT enhanced message ID field	0
60	11:0	R/W	sent_data_41[11:0]	SENT enhanced message data field	0
60	15:12	R/W	sent_id41[3:0]	SENT enhanced message ID field	0
61	11:0	R/W	sent_data_42[11:0]	SENT enhanced message data field	0
61	15:12	R/W	sent_id42[3:0]	SENT enhanced message ID field	0
62	11:0	R/W	sent_data_43[11:0]	SENT enhanced message data field	0
62	15:12	R/W	sent_id43[3:0]	SENT enhanced message ID field	0
63	11:0	R/W	sent_data_44[11:0]	SENT enhanced message data field	0
63	15:12	R/W	sent_id44[3:0]	SENT enhanced message ID field	0

Memory CRC Checksum

Memory CRC 16−bit code (CRC−16−DNP) is calculated using polynomial 0x13D65, seed value is 0xFFFF

Polynomial:

$$x^{16} + x^{13} + x^{12} + x^{11} + x^{10} + x^{8} + x^{6} + x^{5} + x^{2} + x^{0} \quad \text{(eq. 7)}$$

Table 20. RUN TIME MEMORY CONTENT

ADDRESS[5:0]	DATA[15:0] Bit Position	Access	Parameter	Description	Default Value
0	15:0	R.O.	pos_out[15:0]	Internal DSP variables	N.A.
1	15:0	R.O.	vrec_amp[16:1]	Internal DSP variables	N.A.
2	15:0	R.O.	rec32_amp[15:0] /rec32_amp[15:0] (dcc_cal[1:0]=1)/ rec21_amp[15:0] (dcc_cal[1:0]=2)	Internal DSP variables selected by dcc_cal[1:0] (data are valid only when direct_adc = 1 or dcc_cal[1:0] = 1 or 2)	N.A.
3	15:0	R.O.	rec21_amp[15:0]/ rec21_amp[15:0] (dcc_cal[1:0]=1) / rec13_amp[15:0] (dcc_cal[1:0]=2)	Internal DSP variables selected by dcc_cal[1:0] (data are valid only when direct_adc = 1 or dcc_cal[1:0] = 1 or 2)	N.A.
4	13:0	R.O.	ex_amp[13:0]	LC oscillator amplitude value	N.A.
5	2:0	R.O.	ex_scale[2:0]	Primary to secondary scale factor	N.A.
6	11:0	R.O.	temp_code[11:0]	Die temperature temp[11:0] = round((8 * (T[K] − 200 K)) / [K])	N.A.
7	10:0	R.O.	vout_amp[10:0]	sent_drv=0 & (spi_ena=0 | wd_cfg[1:0]=0)	N.A.
8	15:0	R.O.	fail_flags[15:0]	Refer to table 18: Diagnostics	N.A.
9	1:0	R/W	dcc_cal[1:0]	Read−out data selection bit	0
9	2	R/W	gain_frz	Freeze of the gain	0
9	3	R/W	osc_frz	Freeze of the oscillator	0
10	4:0	R/W	agc_gain[4:0]	AGC gain, writable if gain_frz = 1	N.A.
10	14:8	R/W	adc_off[6:0]	Frond−end ADC offset, writable if gain_frz = 1	0
11	7:0	R/W	preset_curr[7:0]	Oscillator driving current, writable if osc_frz = 1	0
12	15	R.O.	ee_verify	EEPROM verify operation status	N.A.
63	7:0	R.O.	wd_cnt[7:0]	Watchdog counter	N.A.

APPLICATION SPECIFIC INFORMATION

Application Set−ups for Functional Safety

The NCV77320 has the capability to operate with a second chip to achieve a conclusive position. Several application diagrams can be imagined ranging from ASIL B to a higher functional safety level. In the following pictures some topologies are depicted.

In dual chip configuration, “inp_diag_per” bit shall be programmed differently for each device.

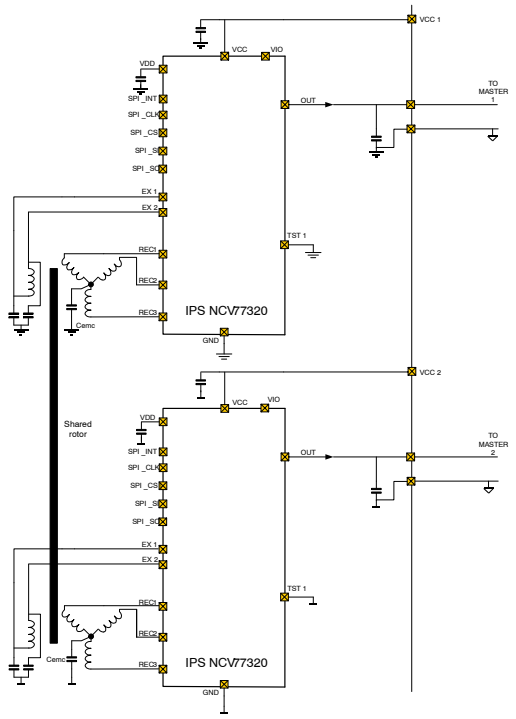


Figure 33. Dual Chip Configuration with Split Supplies and Common Rotor

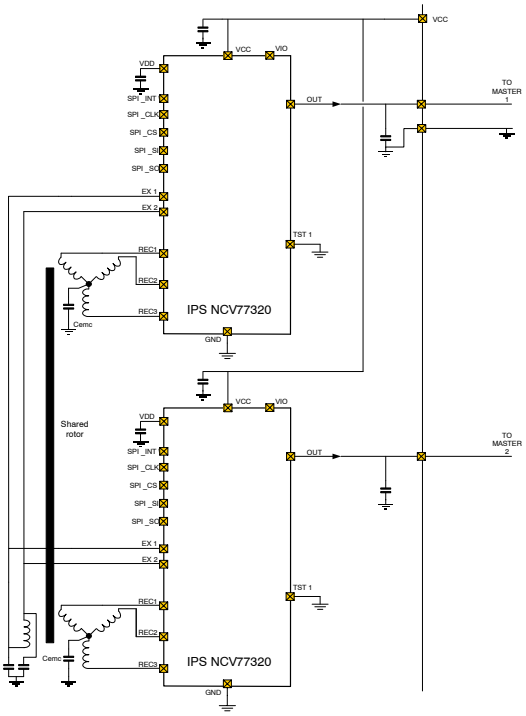


Figure 34. Dual Chip Configuration with Shared Supplies and Excitation Source with Common Rotor

CRC Calculations Language Examples

SPI CRC 8−bit Code (ATM−8)

Input parameter for function is 32 bit SPI frame with 0x00 at CRC positon (bits [7:0]) of the SPI frame.

```
uint8_t calc_crc_spi(uint32_t data) {          //8-bit CRC with seed 0xFF and polynom 0x107

    uint32_t polynom = 0x10700000 << 3, crc = 0;
    uint8_t shift = 0, roll_back = 0;

    crc = 0xFF000000 | ((data >> 8) & 0x00FFFFFF); //data init

    while (shift <= 23) {                      //shift and if 1 perform XOR

        if ((crc & (1 << (31 - shift))) != 0) {
            crc = crc^(polynom);
        }
        shift++;
        polynom = polynom >> 1;

        if (shift == 8 && roll_back == 0) {   //shift back 8 bits to add 8 zeros at the end
            shift = 0;                        //of the frame for proper result
            crc = crc << 8;
            roll_back = 1;
            polynom = polynom << 8;
        }
    }
    return crc;
}

//example of use

int main(void) {
    volatile uint8_t result;
    uint32_t SPI_frame = 0x0A02FE00;     //command for watchdog kick with window 2 to 10 ms
    result = calc_crc_spi(SPI_frame);    //result = 0x88
}
```

CRC Calculation for checksum Nibble of the SENT Frame

```
uint8_t calc_crc_fast_msg(uint32_t data) {     //4-bit CRC with seed 5 and polynom 0x1D

    uint32_t polynom = 0x1D000000 << 3, crc = 0;
    uint8_t shift = 0;

    crc = 0x50000000 | (data & 0x0FFFFFF0);    //data init

    while (shift <= 27) {                      //shift and if 1 perform XOR
        if ((crc & (1 << (31 - shift))) != 0) {
            crc = crc^(polynom >> (shift));
        }
        shift++;
    }
    return crc;
}

//example of use

int main(void) {
    uint32_t SENT_frame = 0x8301F332;          //32 bits, from MSB to LSB: status and comm
    volatile uint8_t result;                   //nbl, data nbl 1 … data nbl 6, CRC nibble
    result = calc_crc_fast_msg(SENT_frame);    //result = 0x02, SENT frame is valid
}
```

SENT Serial Message CRC – Slow Channel

```
ID   = 0x85  =      0b1000 0101
data = 0x2B1 = 0b0010 1011 0001
crc_frame = 0b0000 1100 1000 1010 0100 0110;   //organized according to SENT serial message
                                               //CRC chapter and figure 24 from ID and data

uint8_t calc_crc_slow_msg(uint32_t data) {     //6-bit CRC with seed 0x15 and polynom 0x59

    uint32_t polynom = 0x59000000 << 1, crc = 0;
    uint8_t shift = 0, roll_back = 0;

    crc = 0x15000000 | (data & 0x00FFFFFF);    //data init

    while (shift <= 25) { //shift and if 1 perform XOR
        if ((crc & (1 << (31 - shift))) != 0) {
            crc = crc^(polynom >> (shift));
        }
        shift++;

        if (shift == 6 && roll_back == 0) {    //shift back 6 bits to add 6 zeros at the end
            shift = 0;                         //of the message for proper result
            crc = crc << 6;
            roll_back = 1;
        }
    }
    return crc;
}

int main(void) {               //example of use
    volatile uint8_t result;
    uint32_t crc_frame = 0b000011001000101001000110;
    result = calc_crc_slow_msg(crc_frame);   //result = 0x3D
}
```

Memory CRC 16−bit code (CRC−16−DNP)

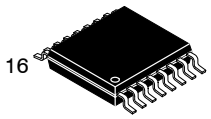
CRC calculation in the chip is starting with seed, then data from MSB of the high address to LSB low address in the chip memory and tailing zeros (e.g. 0xFFFF, data from MSB addr 29 to LSB addr 22 and 0x0000).

```
uint16_t calc_memory_crc16(uint8_t address_start, uint8_t address_end, uint16_t *data) {

    uint32_t polynom = 0x13D65000 << 3, crc;
    uint8_t polynom_shift = 0, current_step = 0, step_count;

    crc = 0xFFFF0000 | data[address_end];                       //data init
    step_count = address_end - address_start + 1;

    do {
        current_step++;
        for (polynom_shift = 0; polynom_shift < 16; polynom_shift++) {
            if ((crc & (1 << (31 - polynom_shift))) != 0) {     //XOR and shifting
                crc = crc^(polynom);
            }
            polynom = polynom >> 1;
        }
        polynom = 0x13D65000 << 3;
        crc = crc << 16;
        if (current_step < step_count){
            crc = crc | data[address_end - current_step];       //load new 16 bit data
        }
    }while (current_step <= step_count);
    crc = crc >> 16;
    return crc;
}
//example of use

int main(void) {
    volatile uint16_t IPS_Memory [64], result;

    IPS_Memory[22] = 50000;
    IPS_Memory[23] = 10000;
    IPS_Memory[24] = 42000;
    IPS_Memory[25] = 21000;
    IPS_Memory[26] = 30000;
    IPS_Memory[27] = 29000;
    IPS_Memory[28] = 18000;
    IPS_Memory[29] = 40000;

    result = calc_memory_crc16(22,29, IPS_Memory);          //result = 31446 (0x7AD6)
}
```

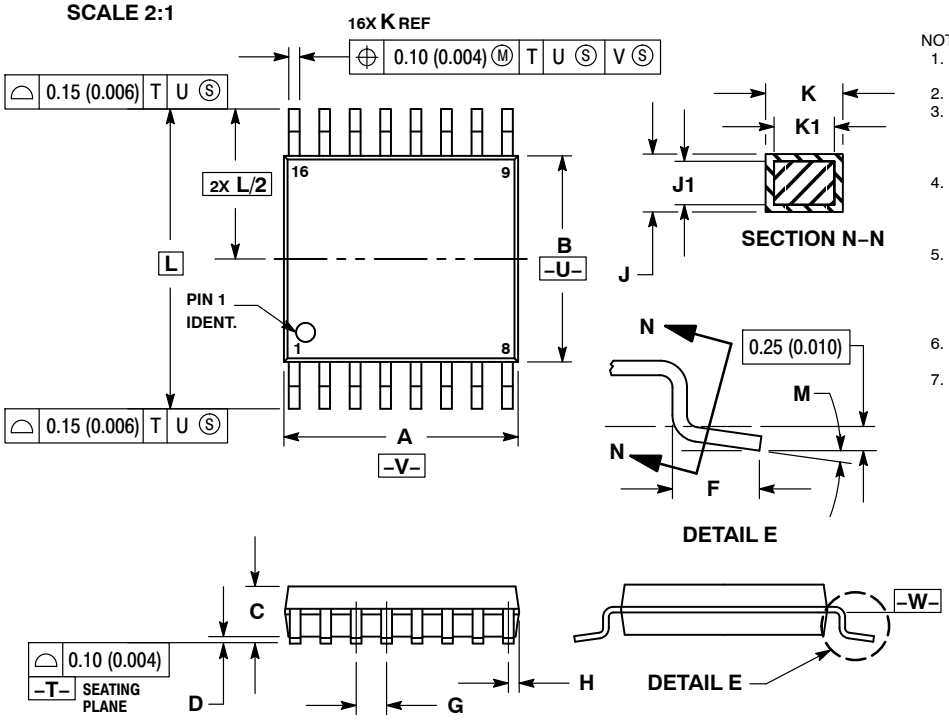
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



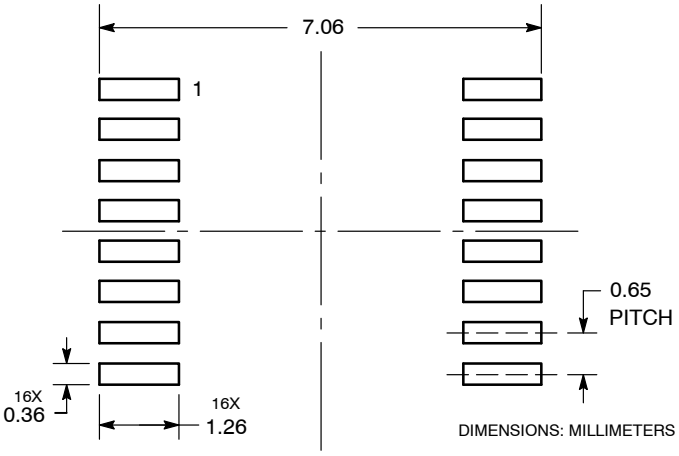
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

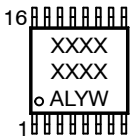
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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