MP6652

18V, Single-Phase BLDC Motor Driver with Integrated Hall Sensor

DESCRIPTION

The MP6652 is a single-phase brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. It drives a single-phase brushless DC fan motor, with an input voltage (V_{IN}) range of 3V to 18V.

The MP6652 controls the rotational speed through the pulse-width modulation (PWM) signal on the PWM pin. The device features a built-in, configurable curve speed function that is ideal for cooling fan applications, which require flexible speed curve control.

The MP6652 provides rotational speed detection. The rotational speed detector (the FG/RD pin) is an open-drain output. It outputs a high or low voltage relative to the internal Hall comparator's output. Higher speeds produce higher frequency signals.

Full protections include input over-voltage protection (OVP), under-voltage lockout (UVLO), locked rotor protection, and thermal shutdown.

The MP6652 is available in a TSOT23-6-SL package and a TSOT23-6-L package.

FEATURES

- On-Chip Hall Sensor
- Wide 3V to 18V Operating Input Voltage (V_{IN}) Range
- Integrated Power MOSFETs: Total 850mΩ High-Side MOSFET (HS-FET) and Low-Side MOSFET (LS-FET)
- Configurable Starting Duty Cycle
- Rotational Speed Indicator FG Signal
- Rotor Lock Protection Fault Indication
- 1kHz to 100kHz Pulse-Width Modulation (PWM) Input Frequency Range
- Fixed 27kHz Output Switching Frequency (f_{SW})
- Configurable Soft-On/Off Commutation Angle (Max 90°)
- Configurable Soft Start (SS)
- Rotor Lock Protection with Auto-Recovery
- FG Outputs 0.5x, 1x, or 2x Original Hall Frequency
- Thermal Protection with Auto-Recovery
- Built-In Input Over-Voltage Protection (OVP) and Under-Voltage Lockout (UVLO) with Auto-Recovery
- Available in TSOT23-6-SL and TSOT23-6-L Packages

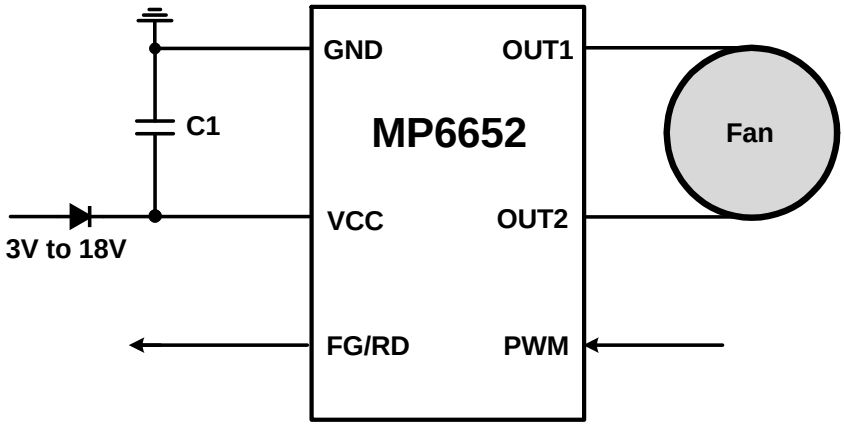
APPLICATIONS

- CPU and GPU Fans
- Brushless DC (BLDC) Motors
- Cooling Fans

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6652GJS-xxxx**	TSOT23-6-SL	*See Below*	1
MP6652GJL-xxxx**	TSOT23-6-L	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP6652GJS-xxxx-Z).

** “xxxx” is the configuration code identifier. The four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the “0000” code (default).

TOP MARKING (MP6652GJS-xxxx)

BLNY

LLL

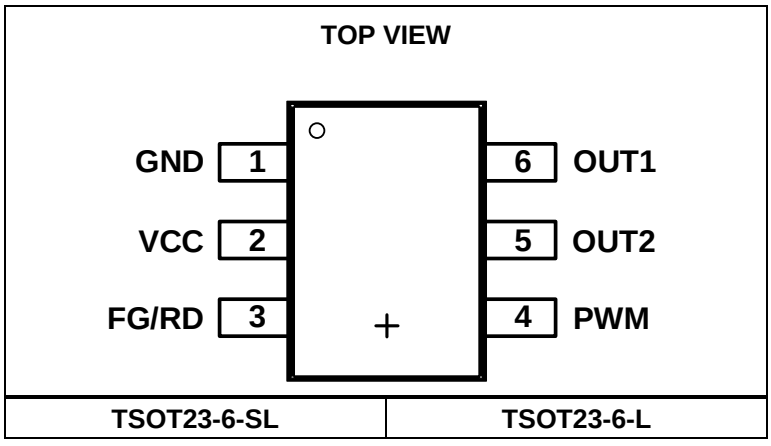
BLN: Product code of MP6652GJS-xxxx
Y: Year code
LLL: Lot number

TOP MARKING (MP6652GJL-xxxx)

BLNY

BLN: Product code of MP6652GJL-xxxx
Y: Year code

PACKAGE REFERENCE



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PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.** VCC must be locally bypassed.
3	FG/RD	**Rotational speed detection (default) or dead lock indication.** FG and RD are open-drain outputs. Pull FG/RD high externally.
4	PWM	**PWM input for rotational speed control.** A 1kHz to 100kHz PWM input is recommended during normal operation.
5	OUT2	**Motor driver output 2.**
6	OUT1	**Motor driver output 1.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC}, PWM .....-0.3V to +25V
$V_{OUT1/2}$ .....-0.3V to V_{CC} + 0.3V
FG/RD.....-0.3V to +18V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)…..
..... 1.25W
Junction temperature .....150°C
Operating temperature..... -40°C to +125°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....3V to 18V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6.....100..... 55... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{VCC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			2.3	2.5	V
Input UVLO hysteresis				0.2		V
Operating supply current	I_{CC}			4		mA
Pulse-width modulation (PWM) input high voltage	V_{PWMH}		2			V
PWM input low voltage	V_{PWML}				0.8	V
PWM input internal pull-up resistance				100		kΩ
High-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)}$	I_{OUT} = 100mA		0.85		Ω
Over-current protection (OCP) threshold	I_{OCP}			1.3		A
Input over-voltage protection (OVP) threshold	V_{OVP}		18	19.1	20.2	V
Input OVP hysteresis	V_{OVP_HYS}			1.3		V
Switching frequency	f_{SW}	T_J = 25°C	24.3	27	29.7	kHz
FG output low-level voltage	V_{FG_L}	$I_{FG/RD}$ = 3mA, V_{PULL} = 5V			0.35	V
FG and RD leakage current					1	μA
Soft-on commutation angle	θ_{SON}	SON_ANG = 0x0F		46.8		deg
Soft-off commutation angle	θ_{SOFF}	SOFF_ANG = 0x0F		44.8		deg
Hall offset angle	θ_E	HAL_ANG = 0x07		24.5		deg
Rotor lock detection time (5)	t_{RD}			0.6		s
Rotor lock off time (5)	t_{RD_OFF}	LOCK_SEL = 00		3.6		s
Minimum recommended magnetic field			-1		+1	mT
Thermal shutdown threshold (5)				170		°C
Thermal shutdown hysteresis (5)				20		°C

Note:

5) Guaranteed by design.

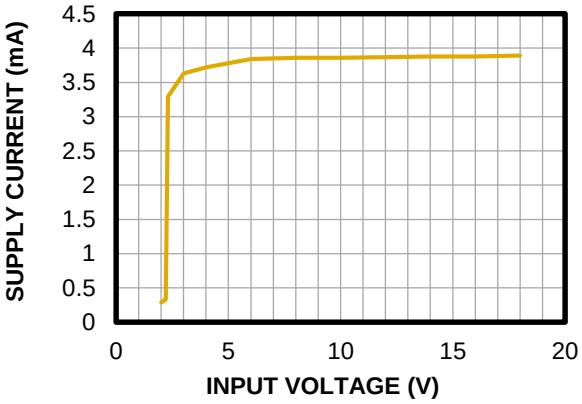
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TYPICAL CHARACTERISTICS

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

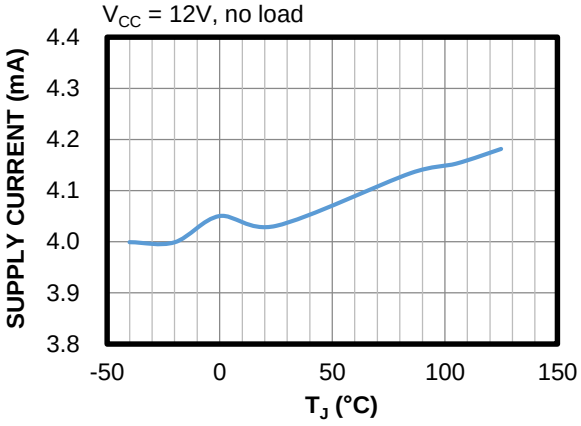
Supply Current vs. Input Voltage

V_{CC} = 2V to 18V, no load

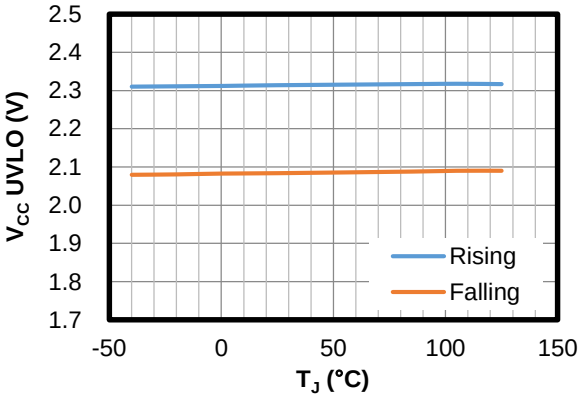


Supply Current vs. Operating Junction Temperature

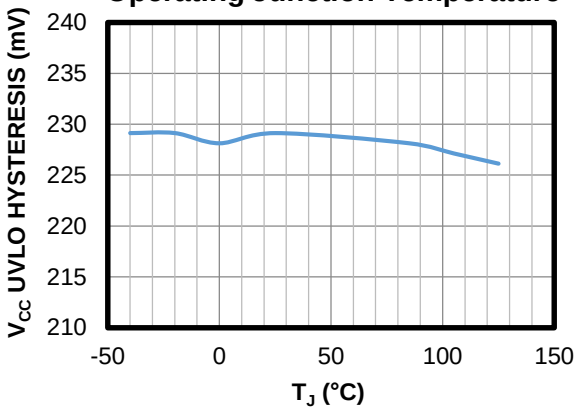
V_{CC} = 12V, no load



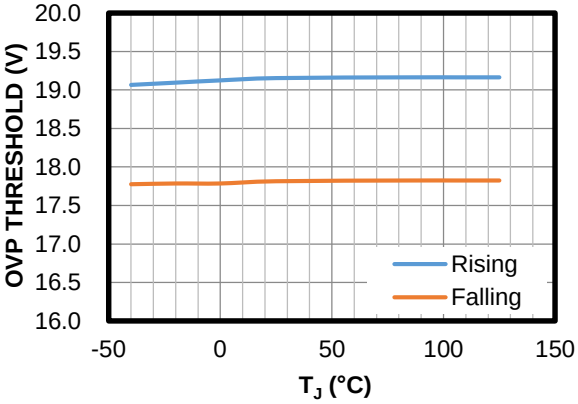
V_{CC} UVLO vs. Operating Junction Temperature



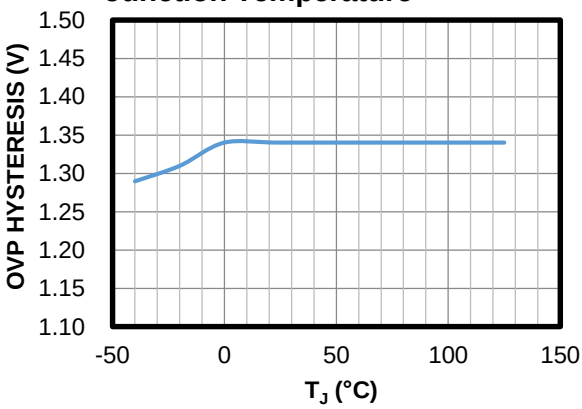
V_{CC} UVLO Hysteresis vs. Operating Junction Temperature



OVP Threshold vs. Operating Junction Temperature



OVP Hysteresis vs. Operating Junction Temperature



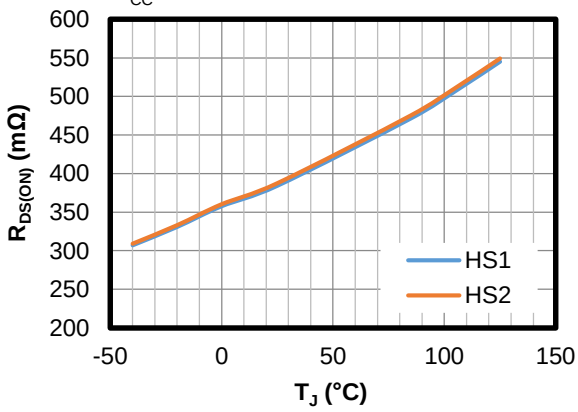
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TYPICAL CHARACTERISTICS *(continued)*

V_{CC} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

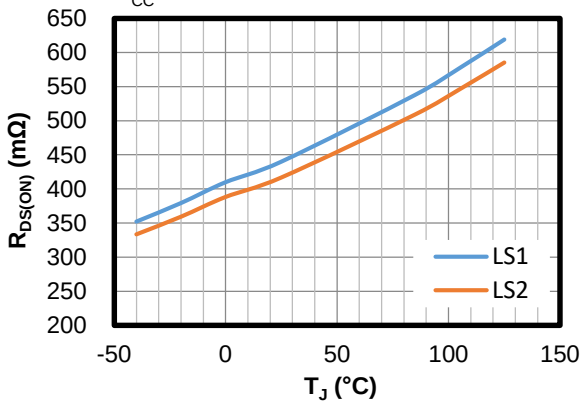
HS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V



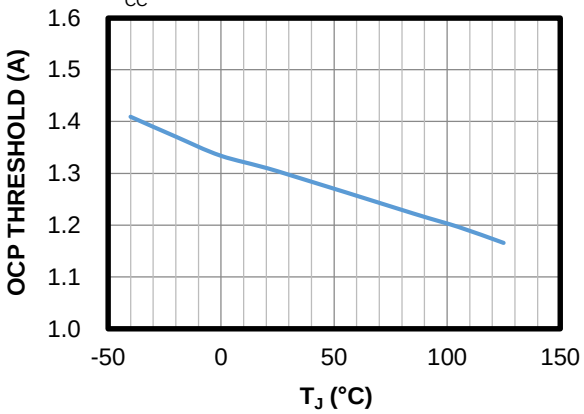
LS-FET On Resistance vs. Junction Temperature

V_{CC} = 12V



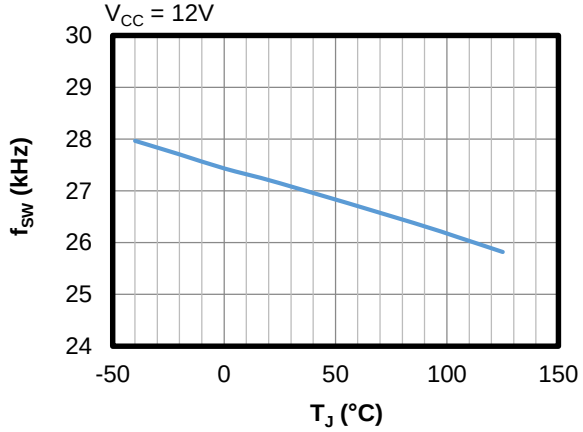
OCP Threshold vs. Operating Junction Temperature

V_{CC} = 12V



PWM Output Frequency vs. Junction Temperature

V_{CC} = 12V

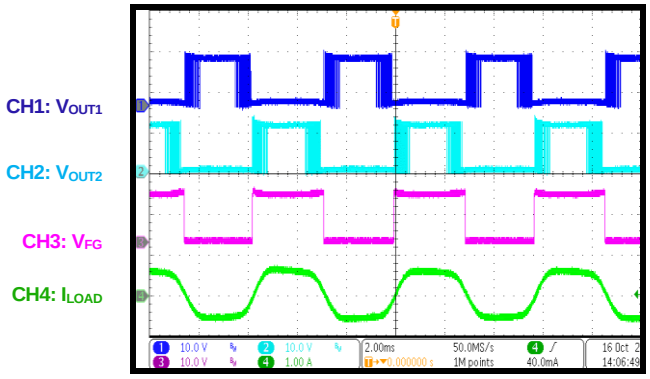


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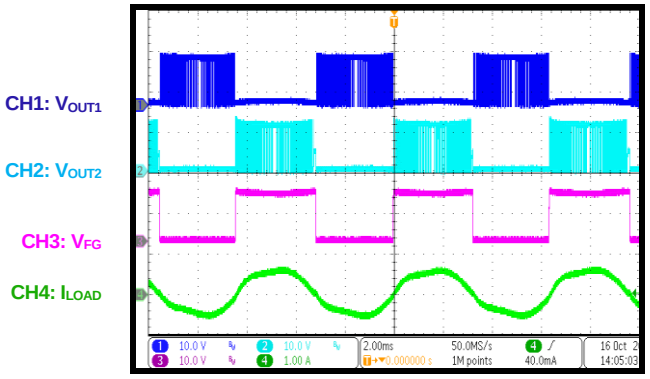
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, I_{IN} = 500mA, 8025 axial fan, input PWM frequency = 20kHz, T_A = 25°C, unless otherwise noted. (6)

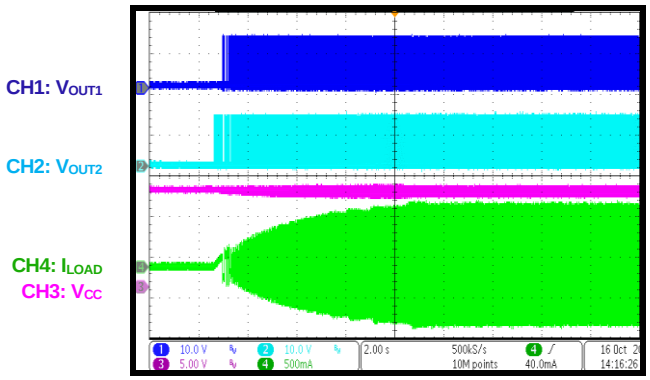
Steady State
Soft-on/off commutation angle = 45°



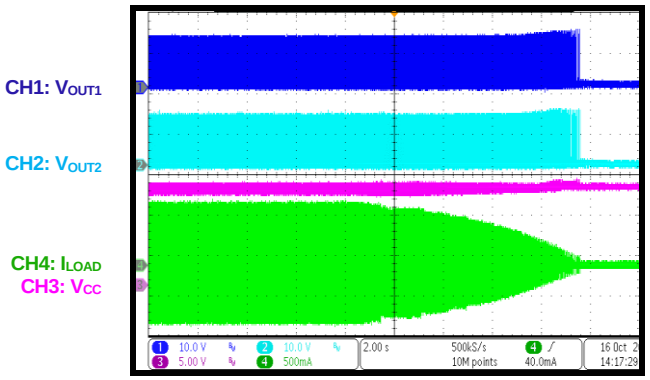
Steady State
Soft-on/off commutation angle = 90°



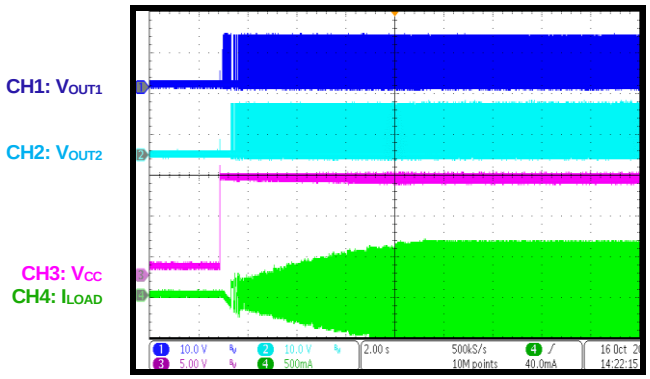
PWM On
Input PWM duty cycle rises from 0% to 100%



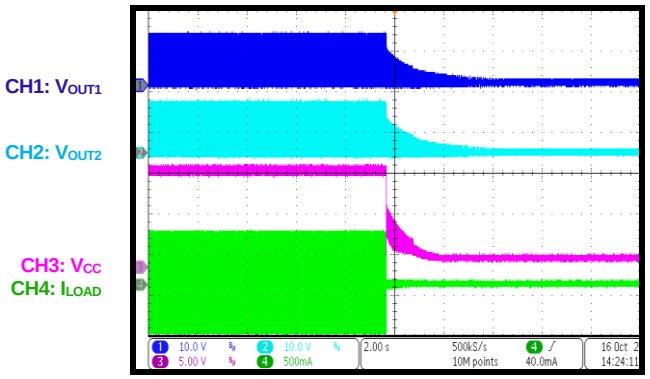
PWM Off
Input PWM duty cycle falls from 100% to 0%



VCC Start-Up
Hot plug-in



VCC Shutdown
Hot plug-out



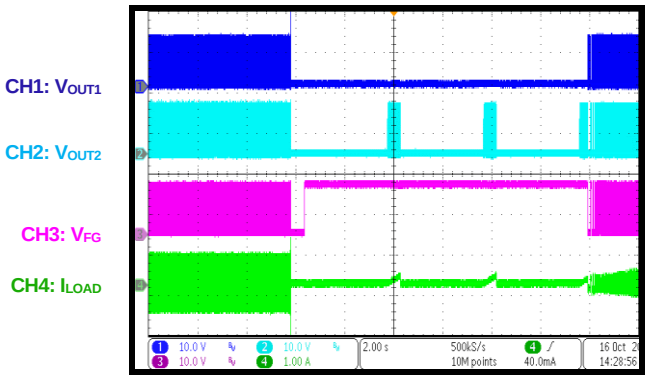
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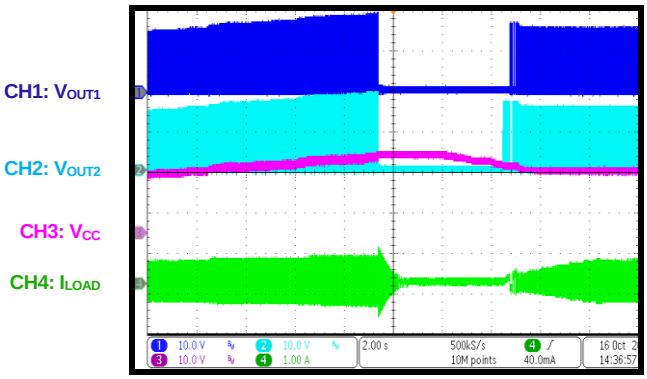
Rotor Lock

Lock the rotor, then release



Input OVP

Ramp up VCC, then ramp down



Note:

6) Performance waveforms are tested on the evaluation board.

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FUNCTIONAL BLOCK DIAGRAM

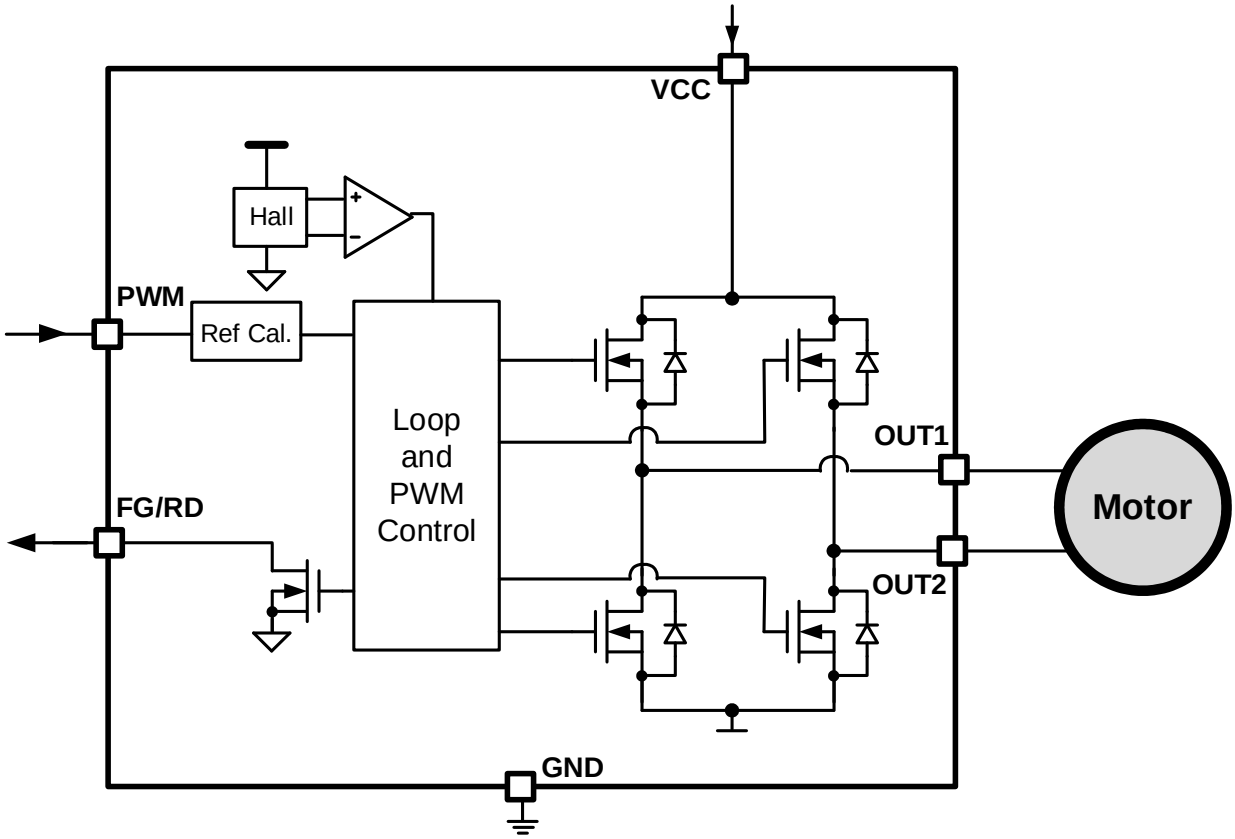


Figure 1: Functional Block Diagram

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OPERATION

Speed Control

The PWM signal on the PWM pin accepts a wide input frequency range (1kHz to 100kHz). The device adjusts the motor speed by detecting the PWM signal duty cycle.

The OUT1/2 pins' output duty cycle follows the PWM input duty cycle. The DIN_MIN bits, combined with hysteresis, set the starting duty cycle.

The minimum output duty cycle is set by DOUT_MIN, which supports two modes:

Mode 1: If DOUT_MIN = 0, the device stops switching when the input duty cycle falls below the value set by DIN_MIN (see Figure 2).

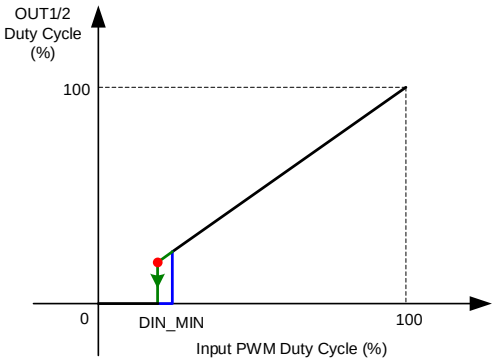


Figure 2: Speed Curve (DOUT_MIN = 0)

Mode 2: If DOUT_MIN is set to a non-zero value, then the minimum output duty cycle is limited by DOUT_MIN (see Figure 3).

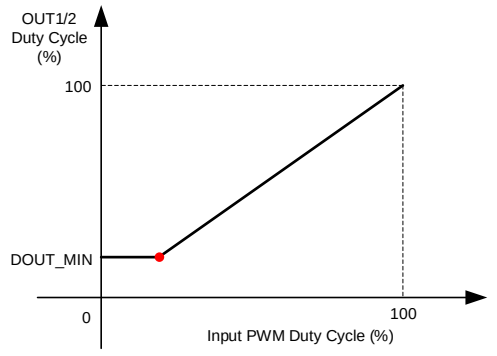


Figure 3: Speed Curve (DOUT_MIN ≠ 0)

OUT1/2 Normal Operation

During normal operation, the MP6652 controls the H-bridge MOSFET switching according to the timing sequence (see Figure 4).

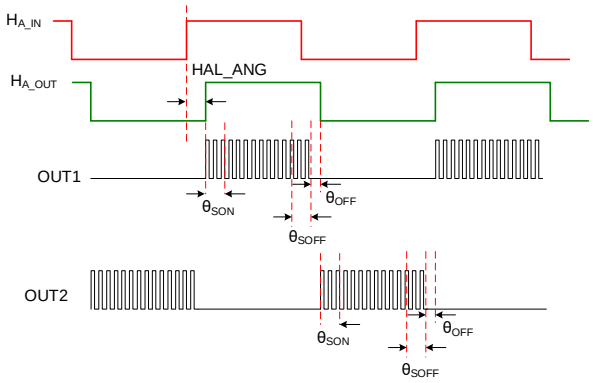


Figure 4: Hall Offset Angle and Soft Commutation

All operation sequences are based on the Hall signal coming from the embedded Hall sensor. H_{A_IN} is the original signal from the embedded Hall sensor, and H_{A_OUT} is generated based on H_{A_IN} with a phase shift. The phase shift is set by the register HAL_ANG. H_{A_OUT} is the control signal for phase commutation.

When the H_{A_OUT} signal is high, OUT2 stays low while OUT1 switches. When the H_{A_OUT} signal is low, OUT1 stays low while OUT2 switches.

In addition, the phase shift can be set by the Hall signals:

- The phase shift between H_{A_IN} and H_{A_OUT} is set by the HAL_ANG bits.
- The phase shift leading/lag direction is set by the HAL_FLAG bit.

Soft-On Commutation

During soft-on commutation, the switching phase's output duty cycle gradually rises from 0% duty cycle to the target duty cycle (see θ_{SON} in Figure 4). The other phase stays low.

The soft-on commutation angle is configured by SON_ANG. The angle is between 2.8° and 90°, with 32 steps.

Soft Off-Commutation

During soft-off commutation, the switching phase's output duty gradually drops from the

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maximum duty cycle to 0% duty cycle (see θ_{SOFF} in Figure 4 on page 11). The other phase stays low.

The soft-off commutation angle is configured by SOFF_ANG. The angle is between 2.8° and 90°, with 32 steps.

Curve Configuration

The MP6652 provides an 8-point curve configuration function where the register sets the output duty cycle at 8 proportioned points from 12.5% through 100% (see Figure 5). With this 8-point register setting, the MP6652 can support flexible speed curves.

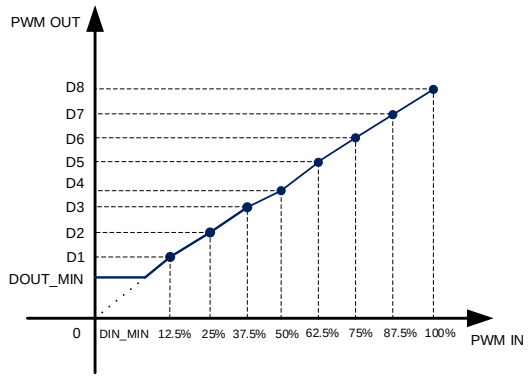


Figure 5: Curve Configuration

Soft-Start (SS) Transition Time

To reduce the input inrush current during the duty cycle transition, the MP6652 provides a configurable soft-start (SS) transient time by setting T_SS (from 2.4s to 9.6s). The register sets the time during which the output duty cycle changes from 0% to 100%, or vice versa.

Rotor Speed Indication (FG)

The FG/RD pin is selectable for the speed indicator (FG) or rotor lock indicator (RD), depending on FGRD.

- FGRD = 00: FG/RD is 1x original Hall
- FGRD = 01, FG/RD is 0.5x original Hall
- FGRD = 10, FG/RD is 2x original Hall
- FGRD = 11, FG/RD is set as the rotor lock indicator

Protection Behavior

The MP6652 is fully protected against over-voltage (OV), under-voltage (UV), over-current, and over-temperature (OT) events.

Short-Circuit Protection (SCP)

The MP6652 has internal overload and short-circuit protection (SCP) mode by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the protection threshold (typically 2A), all MOSFETs turn off immediately after a set blanking time.

Over-Current Limit (OCP)

During normal switching, if the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold, the HS-FET turns off immediately after a blanking time. It resumes switching in the next switching cycle.

Thermal Shutdown

Thermal monitoring is also integrated in the MP6652. If the die temperature exceeds the thermal protection threshold (typically 170°C), the device enters protection mode. Once the die temperature falls to a safe level, the device automatically resumes normal operation.

Under-Voltage Lockout (UVLO)

When the voltage on the VCC pin falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Once V_{CC} exceeds the UVLO threshold, the device resumes normal operation.

Rotor Dead Lock Protection (RD)

In motor rotor lock protection, the MP6652 detects the internal Hall signal and outputs a dead lock indication signal to the FG/RD pin if FGRD is set to 11. If no Hall signal edge is detected during the 0.6s detection time, lock protection is triggered and both low-side MOSFETs (LS-FETs) of the H-bridges turn on. The FG/RD outputs depend on RD_H_L. The device automatically restarts after the lock retry time, set by the LOCK_SEL register. After the rotor lock condition is released and three Hall signal edges are detected, FG/RD releases.

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Over-Voltage Protection (OVP)

If the VCC pin's voltage exceeds the OV threshold (about 19V), the device turns on both LS-FETs. Once V_{CC} drops below 18V, the device resumes normal operation.

Test Mode and Factory Mode

To program the internal registers, the MP6652 has a test mode. In test mode, all internal registers can be read/written. After the design is finalized, the register value can be configured to the non-volatile memory (NVM). Refer to the MPS Fan Driver GUI Software for more details on easy parameter changes and memory configuration.

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REGISTER MAP

Add	D7	D6	D5	D4	D3	D2	D1	D0
00h (OTP/REG)	DOUT_MIN[7:0]							
01h (OTP/REG)	D1[7:0]							
02h (OTP/REG)	D2[7:0]							
03h (OTP/REG)	D3[7:0]							
04h (OTP/REG)	D4[7:0]							
05h (OTP/REG)	D5 [7:0]							
06h (OTP/REG)	D6[7:0]							
07h (OTP/REG)	D7[7:0]							
08h (OTP/REG)	D8[7:0]							
09h (OTP/REG)	RESERVED	DIN_MIN[6:0]						
0Ah (OTP/REG)	RESERVED	SPD_SEL[1:0]		SON_ANG[4:0]				
0Bh (OTP/REG)	RESERVED	TPRE[1:0]		SOFF_ANG[4:0]				
0Ch (OTP/REG)	RESERVED		RD_HL	HAL_FLAG	HAL_ANG[3:0]			
0Dh (OTP/REG)	LOCK_SEL[1:0]		OCP_SEL[1:0]		RESERVED			TADV_EN
0Eh (OTP/REG)	RESERVED	TADV[1:0]		OVP	T_SS[1:0]		FGRD[1:0]	
14h (REG)	RESERVED		OTP_PAGE[1:0]		RESERVED			

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REG00h

Addr: 0x00				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	DOUT_MIN[7:0]	OTP/REG	0x20	Sets the minimum output duty cycle limit. Minimum output duty cycle = DOUT_MIN[7:0] / 256. The default is 12.5%. If DOUT_MIN = 0, the device stops switching once the input duty cycle falls below the duty cycle set by DIN_MIN.

REG01h

Addr: 0x01				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D1[7:0]	OTP/REG	0x20	Sets the output duty cycle when the input duty cycle = 12.5%. Output duty cycle = D1[7:0] / 256. The default is 12.5%.

REG02h

Addr: 0x02				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D2[7:0]	OTP/REG	0x40	Sets the output duty cycle when the input duty cycle = 25%. Output duty cycle = D2[7:0] / 256. The default is 25%.

REG03h

Addr: 0x03				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D3[7:0]	OTP/REG	0x60	Sets the output duty cycle when the input duty cycle = 37.5%. Output duty cycle = D3[7:0] / 256. The default is 37.5%.

REG04h

Addr: 0x04				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D4[7:0]	OTP/REG	0x80	Sets the output duty cycle when the input duty cycle = 50%. Output duty cycle = D4[7:0] / 256. The default is 50%.

REG05h

Addr: 0x05				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D5[7:0]	OTP/REG	0xA0	Sets the output duty cycle when the input duty cycle = 62.5%. Output duty cycle = D5[7:0] / 256. The default is 62.5%.

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REG06h

Addr: 0x06				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D6[7:0]	OTP/REG	0xC0	Sets the output duty cycle when the input duty cycle = 75%. Output duty cycle = D6[7:0] / 256. The default is 75%.

REG07h

Addr: 0x07				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D7[7:0]	OTP/REG	0xE0	Sets the output duty cycle when the input duty cycle = 87.5%. Output duty cycle = D7[7:0] / 256. The default is 87.5%.

REG08h

Addr: 0x08				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:0	D8[7:0]	OTP/REG	0xC0	Sets the output duty cycle when the input duty cycle = 100%. Output duty cycle = D8[7:0] / 256. The default is 100%.

REG09h

Addr: 0x09				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6:0	DIN_MIN[6:0]	OTP/REG	0x20	Sets the starting duty cycle. Starting duty cycle = DIN_MIN[6:0] / 256. The default is 12.5%.

REG0Ah

Addr: 0x0A				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6:5	SPD_SEL[1:0]	OTP/REG	00	Selects the digital clock. A higher frequency leads to a higher calculation resolution; however, it also leads to a higher minimum speed. These bits indicate the supported minimum speeds. 00: 100r/min (default) 01: 400r/min 10: 800r/min 11: 1600r/min
4:0	SON_ANG[4:0]	OTP/REG	10000	Sets the soft-on commutation angle. 00000: 2.8° 00001: 5.6° … 11111: 90° Soft-on angle = (SON_ANG[4:0]+1) x 2.8°. 2.8° per step.

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REG0Bh

Addr: 0x0B				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6:5	T_PRE[1:0]	OTP/REG	00	Sets the pre start-up timer. 00: 18.6ms/step (default) 01: 9.3ms/step 10: 4.6ms/step 11: 2.3ms/step
4:0	SOFF_ANG[4:0]	OTP/REG	10000	Sets the soft-off commutation angle. 00000: 2.8° 00001: 5.6° … 11111: 90° Soft-off angle = (SOFF_ANG[4:0] + 1) x 2.8°. 2.8° per step.

REG0Ch

Addr: 0x0C				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	00	Reserved.
5	RD_HL	OTP/REG	0	Selects the RD output polarity bit when lock protection is triggered. 0: Low output when rotor lock protection is triggered (default) 1: High output when rotor lock protection is triggered
4	HAL_FLAG	OTP/REG	0	Sets the Hall offset angle lag/leading set. 0: Lag (default) 1: Leading
3:0	HAL_ANG[3:0]	OTP/REG	0000	Sets the Hall offset angle. 0000: 2.8° (default) 0001: 5.6° … 1111: 45° Hall offset angle = (HAL_ANG[3:0] + 1) x 2.8°. 2.8° per step.

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REG0Dh

Addr: 0x0D				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	LOCK_SEL[1:0]	OTP/REG	00	Selects the lock protection retry time. 00: 3.6s (default) 01: 4.8s 10: 6s 11: 8.5s
5:4	OCP_SEL[1:0]	OTP/REG	11	Selects the current limit threshold. 00: 0.45A 01: 0.8A 10: 1.1A 11: 1.3A
3:1	RESERVED	N/A	001	Reserved.
0	TADV_EN	OTP/REG	0	Enables the advanced off time. 0: Disabled 1: Enabled

REG0Eh

Addr: 0x0E				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7	RESERVED	N/A	0	Reserved.
6:5	TADV	OTP/REG	00	Sets the advanced off angle. 00: Auto 01: 5.6° 01: 11.2° 11: 22.5°
4	OVP	OTP/REG	0	Enables OVP. 0: Enabled 1: Disabled
3:2	T_SS[1:0]	OTP/REG	00	Sets the soft transition time. This is the time that it takes for the output duty to change from 0 to 100%. 00: 2.4s 01: 4.8s 10: 7.2s 11: 9.6s
1:0	FGRD	OTP/REG	00	Selects the FG/RD pin output. 00: 1x 01: 1/2x 10: 2x 11: RD

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REG14h

Addr: 0x14				
Bits	**Bit Name**	**Access**	**Default**	**Description**
7:6	RESERVED	N/A	00	Reserved.
5:4	OTP_PAGE[1:0]	REG	00	Sets the OTP page indicator (read-only). 00: No OTP page is configured 01: First OTP page is configured 10: Second OTP page is configured
3:0	RESERVED	N/A	0000	Reserved.

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APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor near VCC, as close as possible to the VCC and GND pins, to keep the input voltage (V_{IN}) stable and reduce input switching voltage noise and ripple. The input capacitor impedance must be low at the switching frequency (f_{SW}).

Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. The capacitance of the ceramic capacitor drops when the voltage across the capacitor rises; the ceramic capacitor can lose more than 50% of its capacitance when the voltage across the capacitor is close to its rated voltage.

Leave enough voltage rating margin when selecting the component. For most applications, a 1µF to 10µF ceramic capacitor is sufficient.

For certain applications, it is recommended to add an additional, large electrolytic capacitor to absorb motor energy.

Embedded Hall Position

Figure 6 shows the MP6552's embedded Hall sensor position in the lower-left corner of the TSOT23-6-SL and TSOT23-6-L packages.

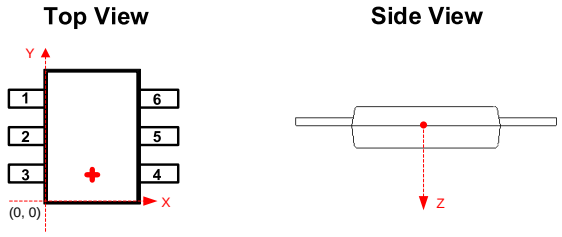


Figure 6: Hall Position with the TSOT23-6-SL and TSOT23-6-L Packages

Where X = 800µm, Y = 783µm, and Z = 80µm.

Input Clamping Circuit (TVS)

To avoid high-voltage spikes from the energy stored in the motor charging back to the input capacitor side, a voltage-clamping TVS diode is recommended for high-current and large inertia applications. A 15V/SOD-123 package TVS diode is sufficient for 12V applications.

Input Snubber

Due to the input capacitor energy charge/discharge during phase commutation, the input current has switching cycle ringing. If necessary, add a 2Ω resistor in series with a 1µF capacitor as an RC snubber in parallel with an input capacitor. This prevents efficient switching cycle ringing.

Selecting the Reverse Blocking Diode

To avoid damage when the fan experiences a reverse plug-in, a reverse blocking diode is required. The reverse blocking diode prevents the bus voltage from charging via the fan's reverse current.

The blocking diode's maximum reverse voltage must exceed 30V, and its forward current rating must exceed the input current (I_{IN}).

System-Level ESD Enhancement

Some fan products must pass system-level ESD testing. Compared to the HBM ESD ratings, system-level ESD follows the IEC61000-4-2 standard. There are two different modes for the IEC61000-4-2 ESD test: air discharge and contact discharge. Contact discharge mode is the first choice for testing. Figure 7 shows that the IEC61000-4-2 sets the equivalent circuit.

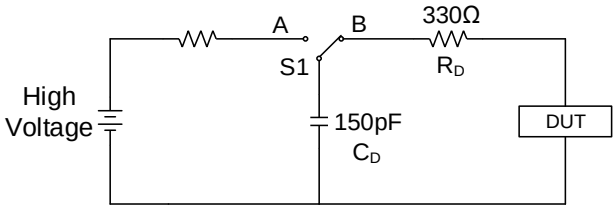


Figure 7: Equivalent Circuit of System-Level ESD

Compared to the HBM ESD ratings, the discharge capacitance exceeds the human body's effective capacitance, and the discharge resistor of the IEC level ESD is much smaller. The transient energy during system-level ESD discharge exceeds the HBM's ESD discharge.

To pass IEC61000-4-2 ESD testing, external ESD-enhanced circuits are required (see Figure 8 on page 20). The external resistors (R1 and R2) and the external clamping diodes (D2 and D3) are used to enhance ESD capability. R1 and R2 are resistors with a recommended typical range of 30Ω to 100Ω. D2 and D3 are clamping diodes, and can be a Zener diode, ESD diode, or TVS diode. The clamping diode's

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package can be SOD-323 or SOD-523 for most applications.

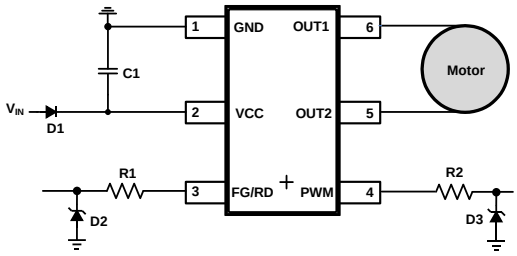


Figure 8: External ESD-Enhanced Circuit

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 9 and follow the guidelines below:

1. Place the input capacitor as close as possible to the VCC and GND pins (see the Selecting the Input Capacitor section on page 20).

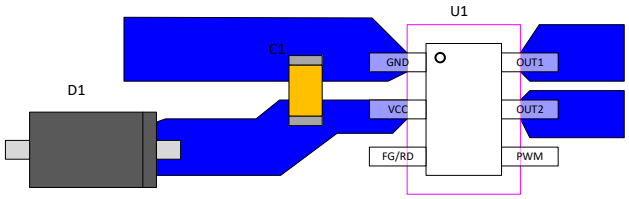


Figure 9: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

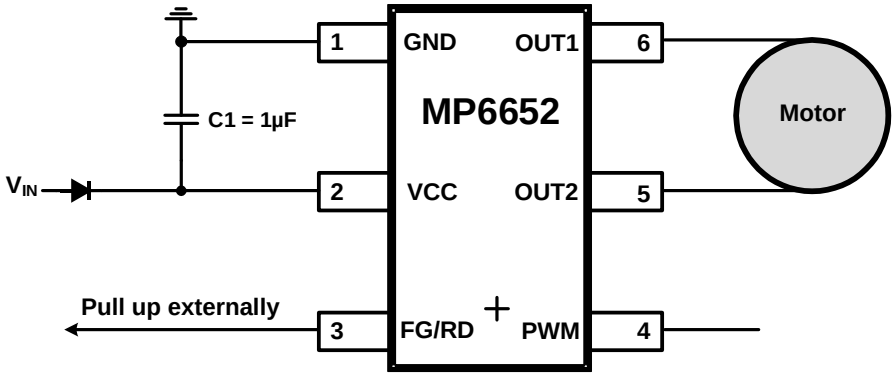


Figure 9: Typical Application Circuit for Normal Applications

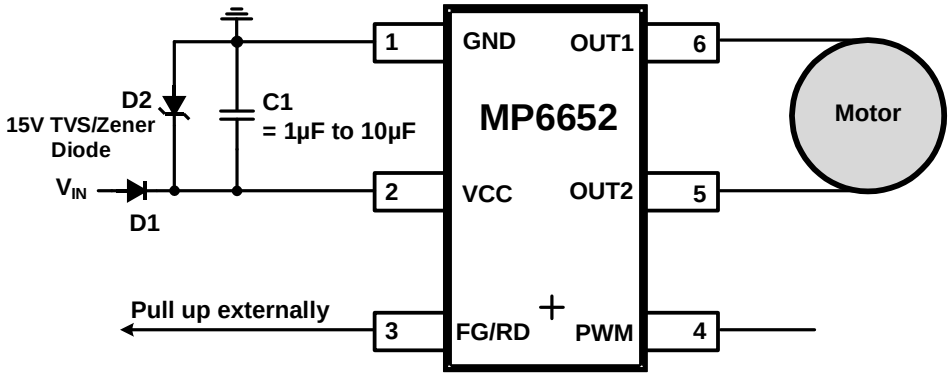
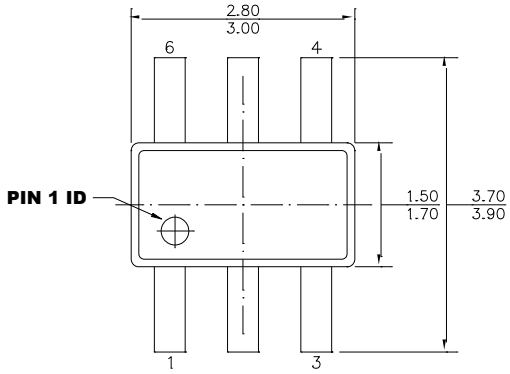


Figure 10: Typical Application Circuit for High-Current, Large-Inertia Fan Applications

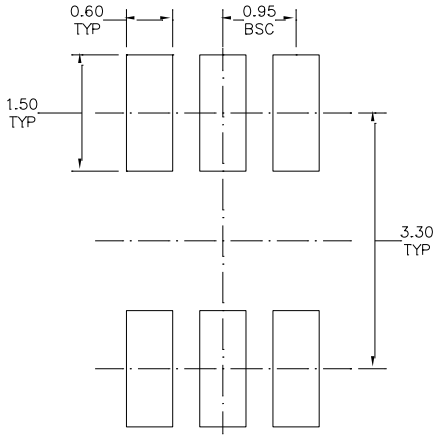
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PACKAGE INFORMATION

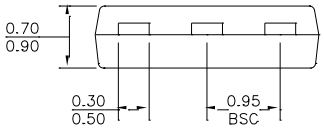
TSOT23-6-SL



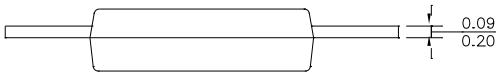
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

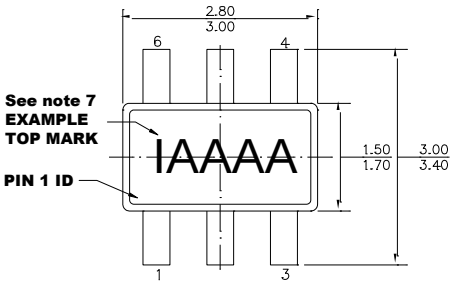
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

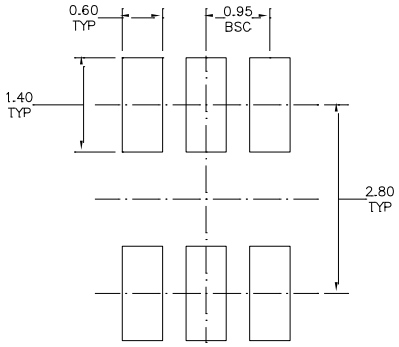
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PACKAGE INFORMATION *(continued)*

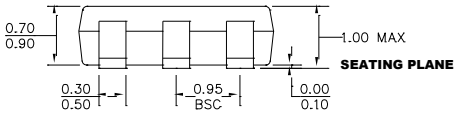
TSOT23-6-L



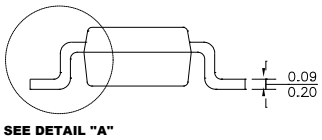
TOP VIEW



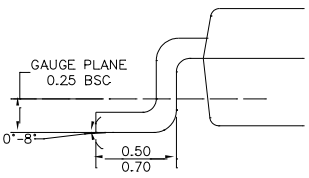
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



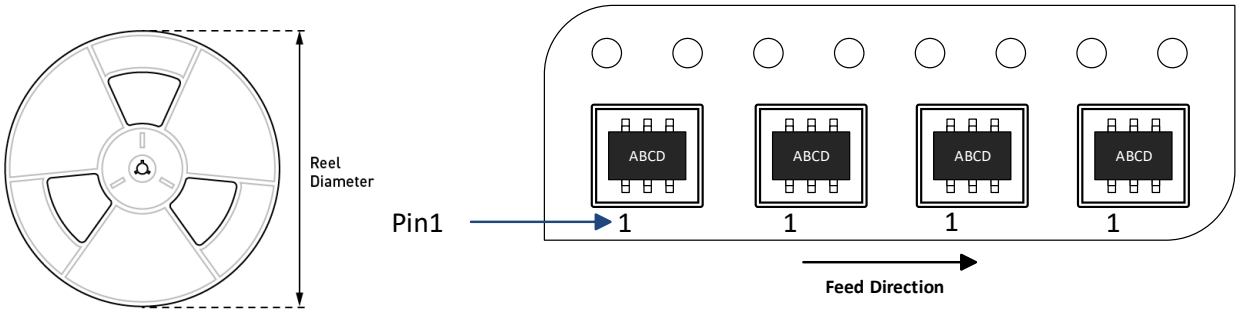
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6652GJS-xxxx-Z	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MP6652GJL-xxxx-Z	TSOT23-6-L	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/21/2021	Initial Release	-

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