EVBL2166-D-00A

6V, Dual 2A/2A or 3A/1A, Low Quiescent Current, Synchronous Buck with PG and SS Evaluation Board

DESCRIPTION

The EVBL2166-D-00A is an evaluation board for the MP/MPQ2166 with MPS power inductor stuffed.

MP/MPQ2166 is an internally compensated, dual, PWM, synchronous, step-down regulator, which operates from a 2.7V to 6V input and generates an output voltage as low as 0.6V. It can be configured as a 2A/2A or 3A/1A output current regulator and is ideal for powering portable equipment that runs on a single-cell lithium-ion (Li+) battery due to a low 60μA quiescent current.

The MP2166/MPQ2166 integrates dual, 55mΩ, high-side switches and 20mΩ synchronous rectifiers for high efficiency without an external Schottky diode. The MP2166/MPQ2166 has peak-current-mode control and internal compensation and is capable of low dropout configurations. Both channels can operate at 100% duty cycle.

Full protection features include cycle-by-cycle current limit and thermal shutdown.

The EVBL2166-D-00A is assembled and tested with QFN-18 (2mmX3mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	2.7-6	V
Output Voltage	V_{OUT1}/ V_{OUT2}	1.8/1.2	V
Output Current	I_{OUT1}/ I_{OUT2}	2/2	A
		3/1	

FEATURES

- 2.7V to 6V Operating Input Range
- 2A/2A or 3A/1A Continuous Current
- 55mΩ/20mΩ $R_{DS(ON)}$
- Programmed Frequency up to 3MHz
- External Sync Clock Up to 3MHz
- 180° Phase Shifted Operation
- PG Indicators
- External SS and Track
- Adjustable Advanced Asynchronous Mode (AAM) or Forced Continuous Conduction Mode (CCM)
- Output Adjustable from 0.6V to VIN
- 100% Duty Cycle Operation
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode and Valley Current Detection
- Thermal Shutdown
- Fully Assembled and Tested
- MPS Power Inductor Stuffed

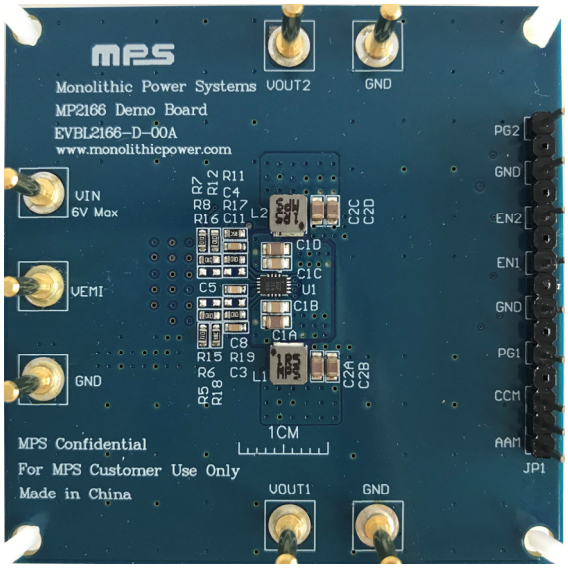
APPLICATIONS

- Small/Handled Devices
- DVD Drivers
- Smartphones and Feature Phones
- Battery-Powered Devices
- Portable Instruments

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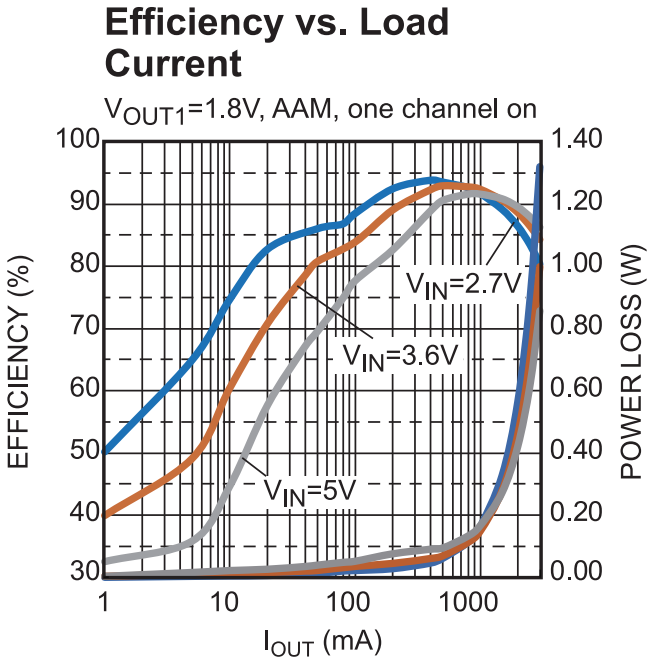
EVBL2166-D-00A EVALUATION BOARD



(L x W x H) 2.5” x 2.5” x 0.2”

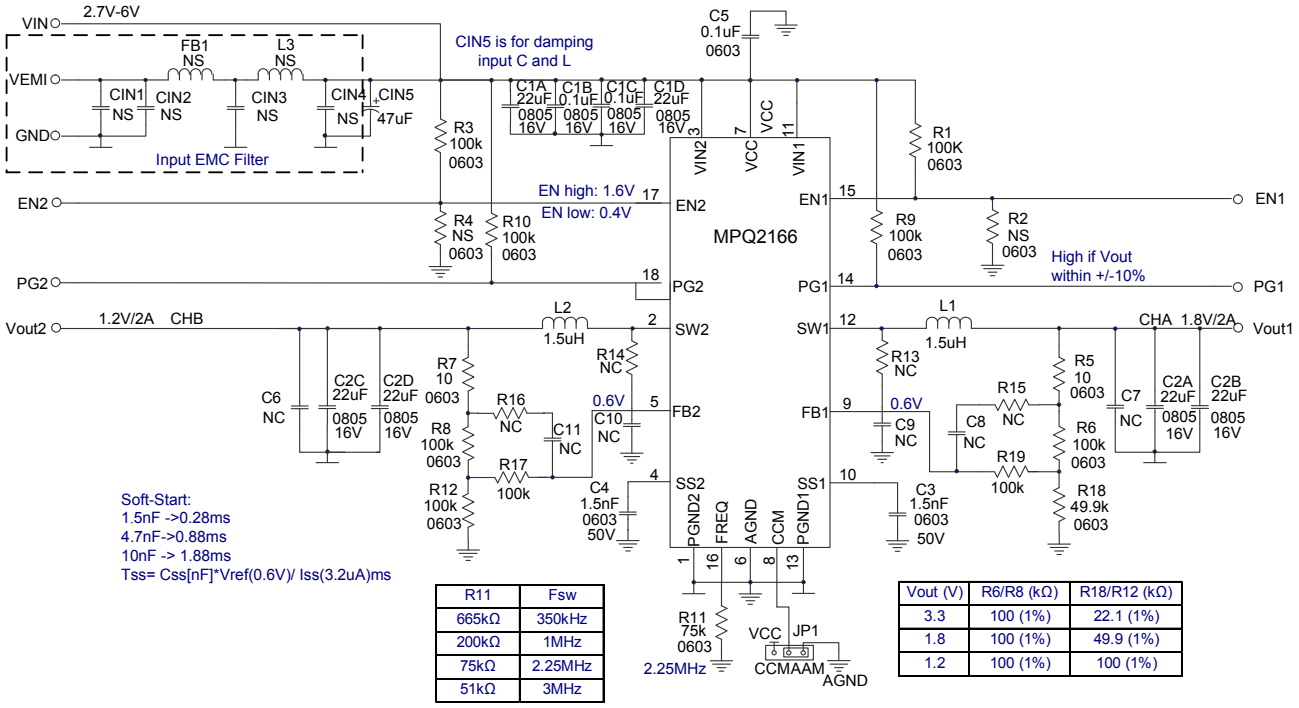
(6.35cm x 6.35cm x0.5cm)

Board Number	MPS IC Number
EVBL2166-D-00A	MP/MPQ2166GD



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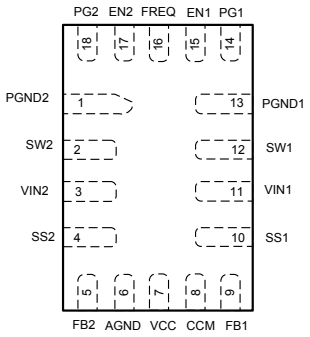
EVALUATION BOARD SCHEMETIC



R11	Fsw
665kΩ	350kHz
200kΩ	1MHz
75kΩ	2.25MHz
51kΩ	3MHz

Vout (V)	R6/R8 (kΩ)	R18/R12 (kΩ)
3.3	100 (1%)	22.1 (1%)
1.8	100 (1%)	49.9 (1%)
1.2	100 (1%)	100 (1%)

Package Reference



EVBL2166-D-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufactuer_P/N
4	CIN1,CIN2, CIN3,CIN4	NS				
1	FB1	NS				
1	L3	NS				
1	CIN5	47µF	Electrolytic Capacitor; 16V	SMD	Jianghai	VZ1-16V47
6	C1A, C1D, C2A, C2B, C2C, C2D	22µF	Ceramic Capacitor;16V;X5R	0805	muRata	GRM21BR61C226ME44L
2	C1B, C1C	0.1µF	Ceramic Capacitor;16V;X7R	0805	muRata	GRM219R71C104KA01D
2	C3, C4	1.5nF	Ceramic Capacitor;50V;X7R	0603	muRata	GRM188R71H153KA01D

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EVBL2166-D-00A BILL OF MATERIALS (*continued*)

Qty	Ref	Value	Description	Package	Manufacturer	Manufactuer_P/N
1	C5	0.1μF	Ceramic Capacitor;16V;X5R	0603	muRata	GRM188R61C104KA01D
6	C6, C7, C8, C9, C10, C11	NS				
2	L1, L2	1.5μH	Inductor; 14.5m; 6.4A	SMD	MPS	MPL-AL4020-1R5
9	R1, R3, R6, R8, R9, R10, R12, R17,R19	100k	Film Resistor;1%;	0603	Yageo	RC0603FR-07100KL
2	R5,R7	10	Film Resistor;1%;	0603	Yageo	RC0603FR-0710RL
1	R18	49.9k	Film Resistor;1%;	0603	Yageo	RC0603FR-07105KL
6	R2, R4, R13, R14, R15,R16	NS				
1	R11	75k	Film Resistor;1%;	0603	Yageo	RC0603FR-0775KL
1	U1		Step-Down Converter	QFN-18	MPS	MP2166GD
7	VIN, VEMI, GND, VOUT1, GND, VOUT2, GND	Test Point	2.0 Golden Pin		HZ	
9	PG2, GND, EN2, EN1, GND, PG1, JP1		2.54mm Test Pin		any	

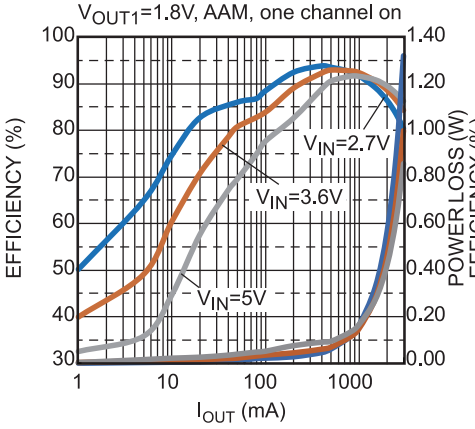
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EVB TEST RESULTS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, F_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

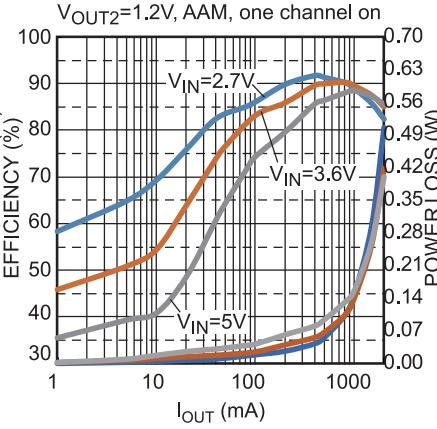
Efficiency vs. Load Current

V_{OUT1}=1.8V, AAM, one channel on



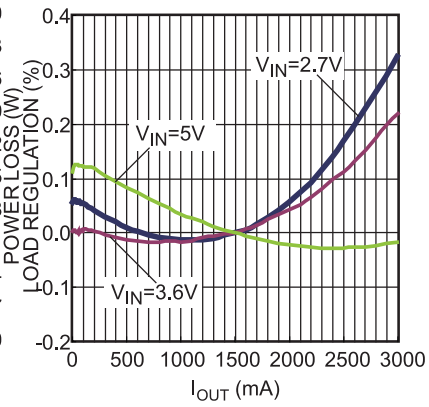
Efficiency vs. Load Current

V_{OUT2}=1.2V, AAM, one channel on



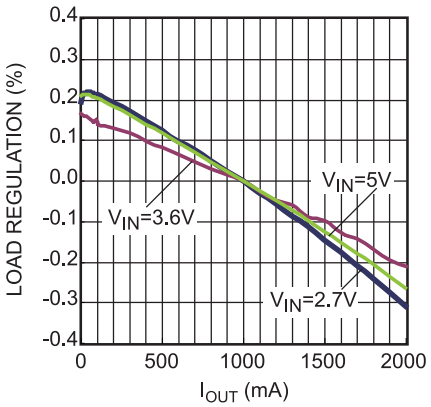
Load Regulation

V_{OUT1}=1.8V, AAM, one channel on



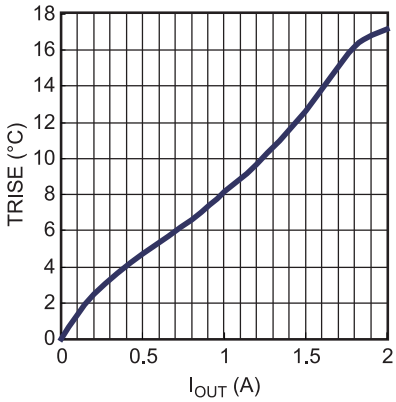
Load Regulation

V_{OUT2}=1.2V, AAM, one channel on



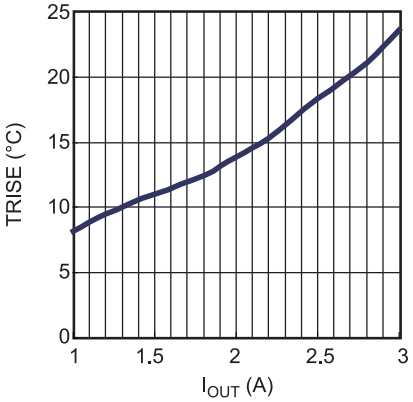
Case Thermal Rise

V_{IN}=5V, I_{OUT1}=I_{OUT2}=2A, AAM, both channels on



Case Temp Rise

V_{IN}=5V, I_{OUT1}=1A-3A, I_{OUT2}=1A, both channels on

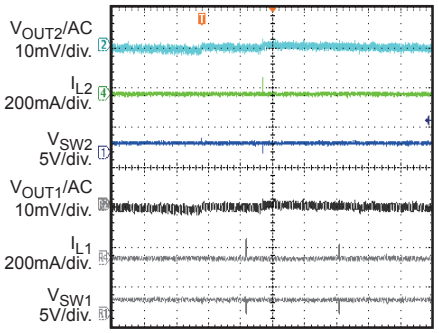


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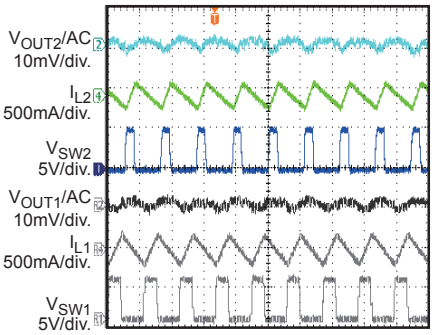
EVB TEST RESULTS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, F_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

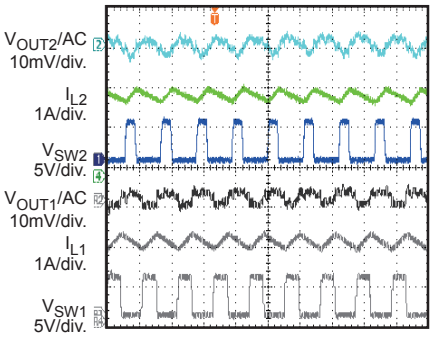
Steady State
I_{OUT1}=I_{OUT2}=0, AAM Mode



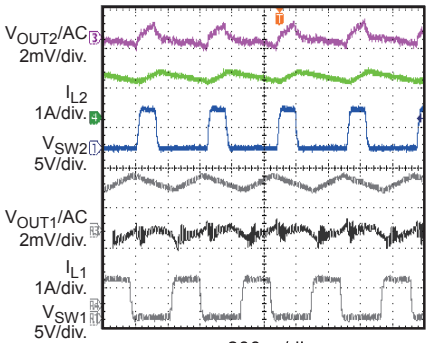
Steady State
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



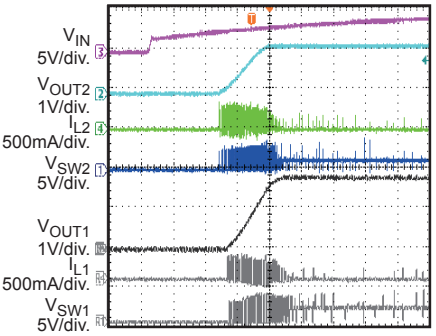
Steady State
I_{OUT1}=I_{OUT2}=2A



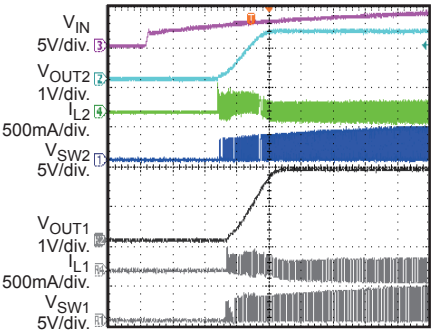
Steady State
I_{OUT1}=3A, I_{OUT2}=1A



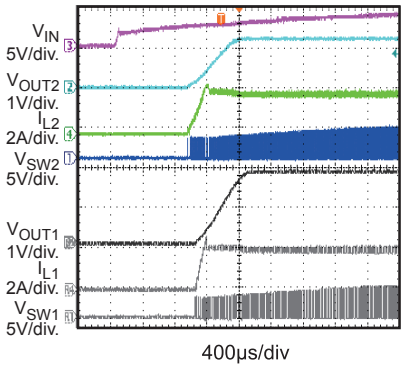
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=0, AAM Mode



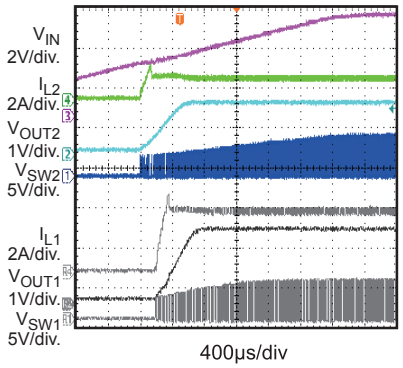
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



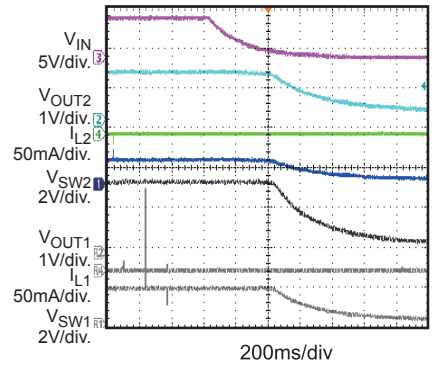
Start-Up through V_{IN}
I_{OUT1}=I_{OUT2}=2A



Start-Up through V_{IN}
I_{OUT1}=3A, II_{OUT2}=1A



Shutdown through V_{IN}
I_{OUT1}=I_{OUT2}=0, AAM Mode



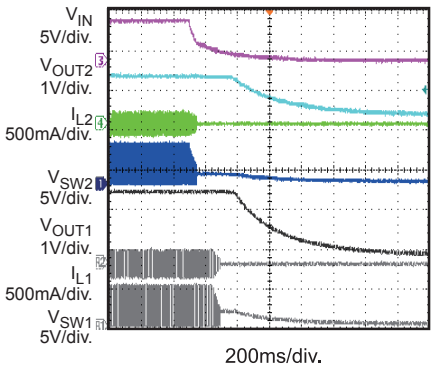
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EVB TEST RESULTS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, F_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

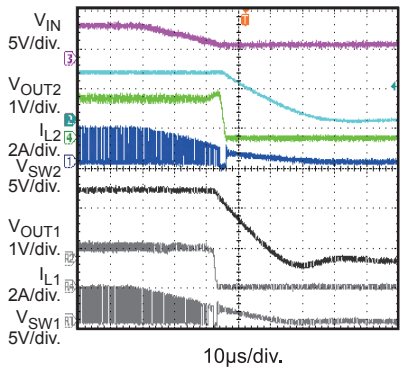
Shutdown through V_{IN}

I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



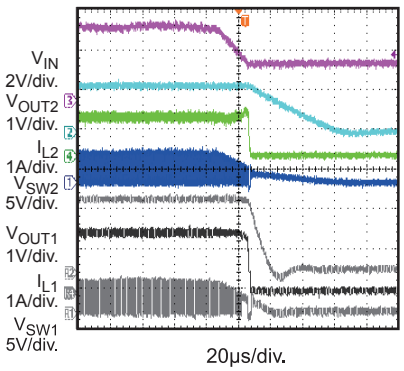
Shutdown through V_{IN}

I_{OUT1}=I_{OUT2}=2A



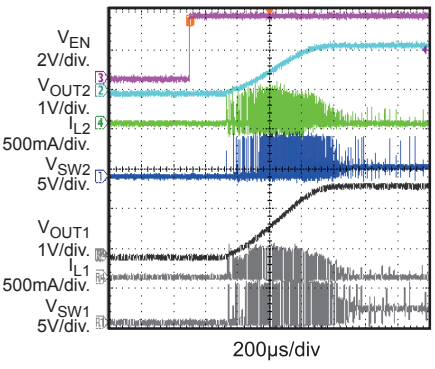
Shutdown through V_{IN}

I_{OUT1}=3A, I_{OUT2}=1A



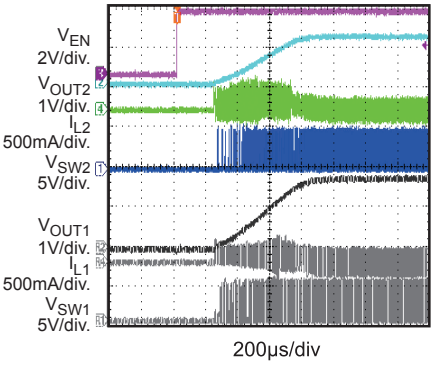
Start-Up through EN

I_{OUT1}=I_{OUT2}=0, AAM Mode



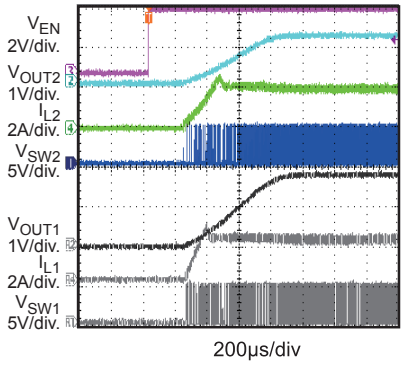
Start-Up through EN

I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



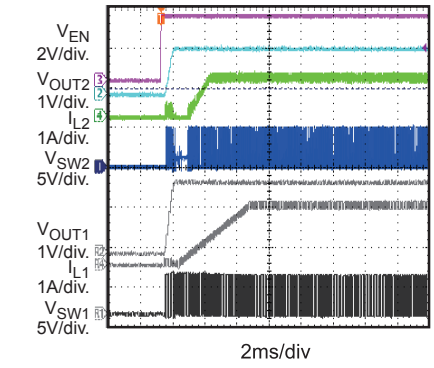
Start-Up through EN

I_{OUT1}=I_{OUT2}=2A



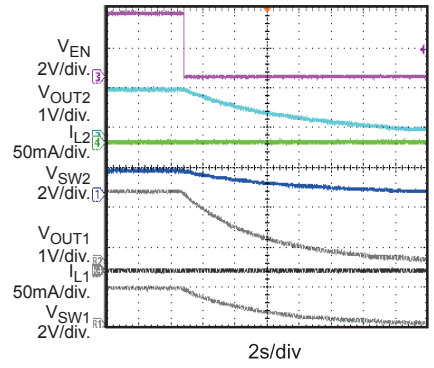
Start-Up through EN

I_{OUT1}=3A, I_{OUT2}=1A



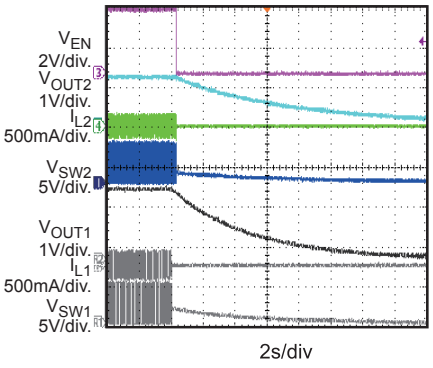
Shutdown through EN

I_{OUT1}=I_{OUT2}=0, AAM Mode



Shutdown through EN

I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



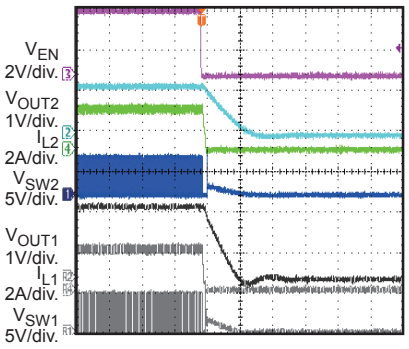
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EVB TEST RESULTS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, F_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

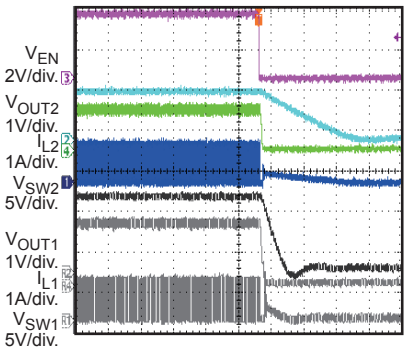
Shutdown through EN

I_{OUT1}=I_{OUT2}=2A



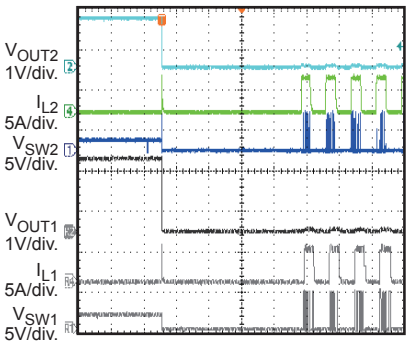
Shutdown through EN

I_{OUT1}=3A, I_{OUT2}=1A



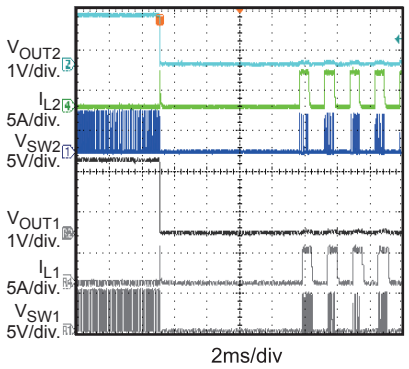
SCP Entry

I_{OUT1}=I_{OUT2}=0, AAM Mode



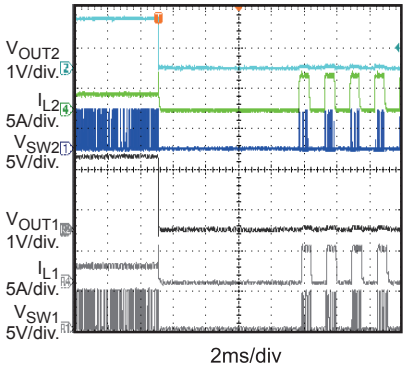
SCP Entry

I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



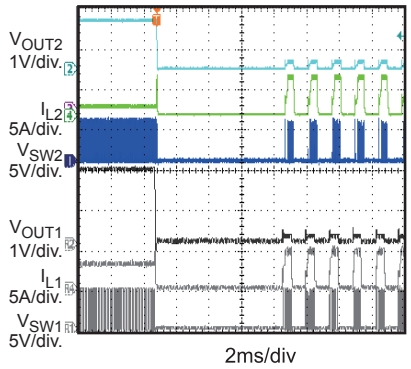
SCP Entry

I_{OUT1}=I_{OUT2}=2A



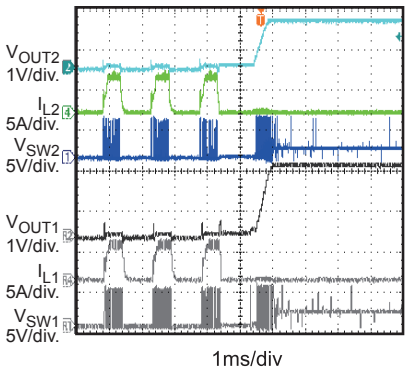
SCP Entry

I_{OUT1}=3A, I_{OUT2}=1A



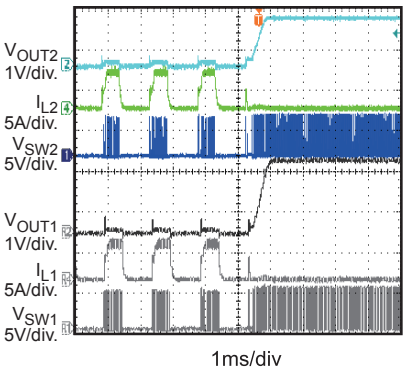
SCP Recovery

I_{OUT1}=I_{OUT2}=0, AAM Mode



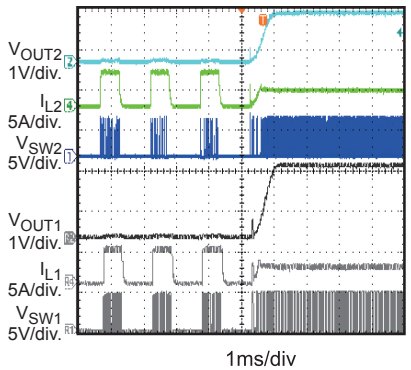
SCP Recovery

I_{OUT1}=I_{OUT2}=0, Forced CCM Mode



SCP Recovery

I_{OUT1}=I_{OUT2}=2A



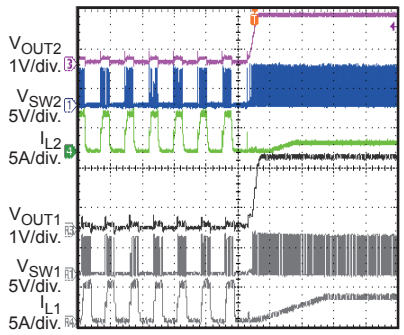
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EVB TEST RESULTS *(continued)*

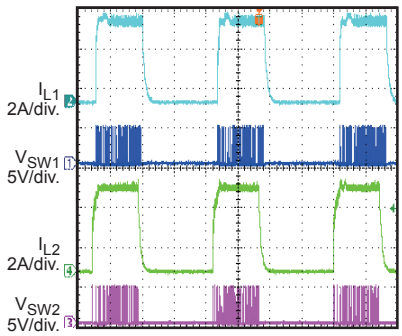
V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L1 = L2 = 1.5µH, F_{SW} = 2.25MHz, T_A = 25°C, unless otherwise noted.

SCP Recovery

I_{OUT1}=3A, I_{OUT2}=1A

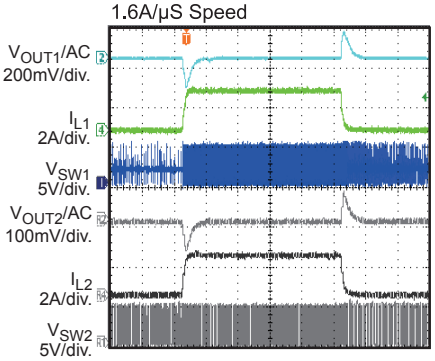


SCP Steady State



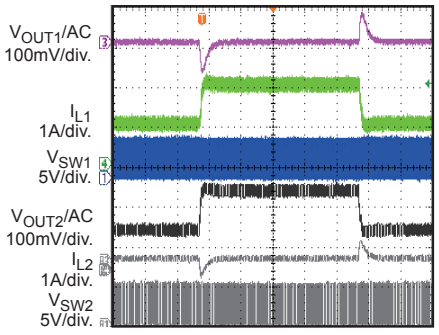
Load Transient

I_{OUT1}=I_{OUT2}=0 to 2A, AAM Mode, 1.6A/µS Speed



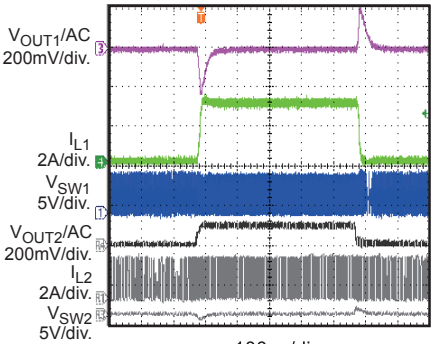
Load Transient

I_{OUT1}=I_{OUT2}=1 to 2A, AAM Mode, 1.6A/µS Speed



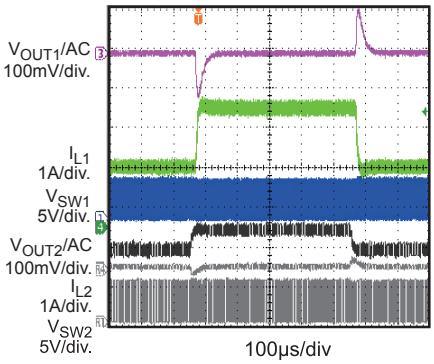
Load Transient

I_{OUT1}=0 to 3A, I_{OUT2}=0 to 1A, 1.6A/µS Speed



Load Transient

I_{OUT1}=1.5 to 3A, I_{OUT2}=0.5 to 1A, 1.6A/µS Speed



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PRINTED CIRCUIT LAYOUT

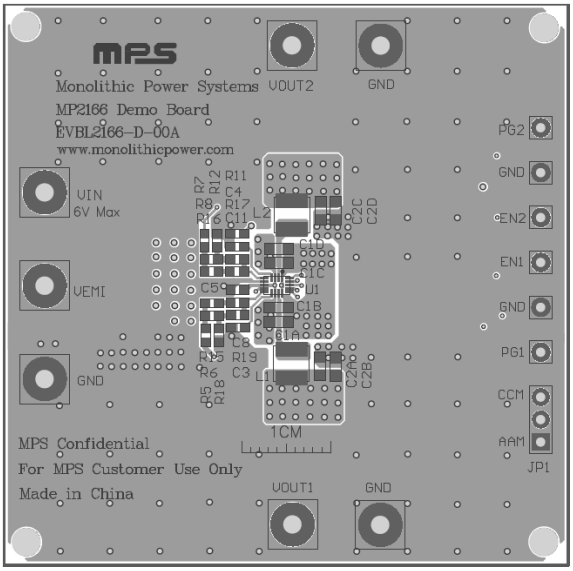


Figure 1: Top & TOP Silk Layer

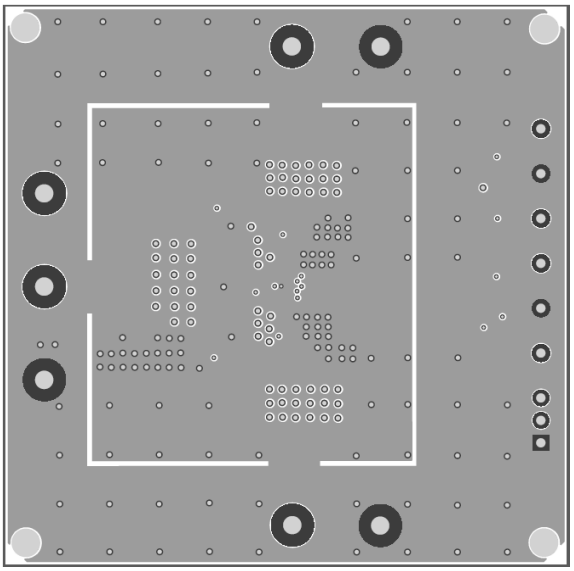


Figure 2: Inner1 Layer

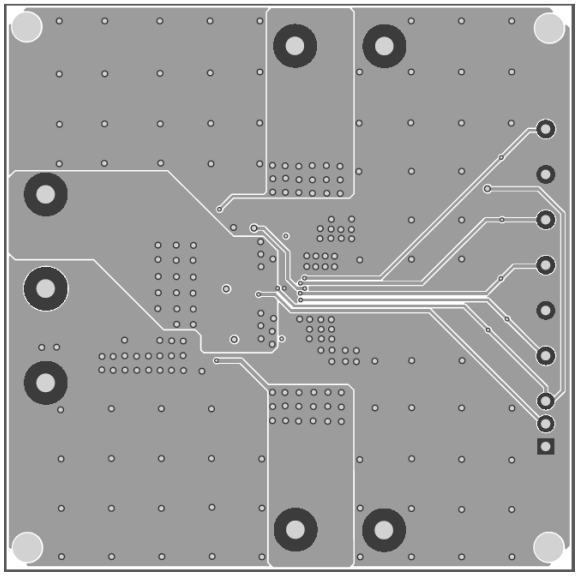


Figure 3: Inner2 Layer

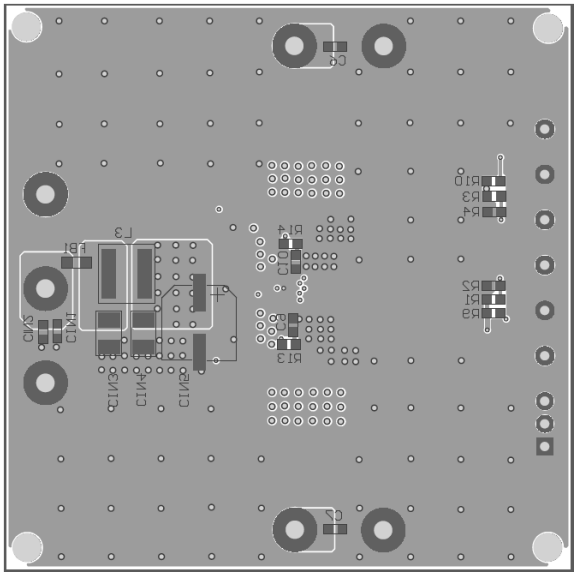


Figure 4: Bottom & Bottom Silk Layer

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QUICK START GUIDE

1. Connect the positive and negative terminals of the load to the VOUT and GND pins, respectively. Be aware that electronic loads represent a negative impedance to the regulator and if set to a too high current will trigger Hiccup mode.
2. Preset the power supply output to expected value (2.7V-6V), and then turn it off.
3. Connect the positive and negative terminals of the power supply output to the VIN and GND pins, respectively.
4. Turn the power supply on (the MP/MPQ2166GD will automatically startup).
5. To get better EMI performance, add the EMI components at bottom layer of the board and connect the input power supply between VEMI and GND.
6. To use the Enable function, apply a digital input to the EN pin. Drive EN higher than 1.6V to turn on the regulator, drive EN less than 0.4V to turn it off. EN can also be connected to VIN directly if don't use the Enable function.
7. A resistor is connected between FREQ and GND to set up the internal oscillator frequency. FREQ can also be used to synchronize the internal oscillator to an external clock. The rising edge of the channel 1 clock is synchronized to the external clock rising edge, while the channel 2 clock remains at 180° out-of-phase to channel 1. The recommended external SYNC frequency is in the range of 350kHz to 3MHz.
8. An AAM mode or forced CCM mode can be selected at JP1.
9. The soft-start time can also be programmed by an external capacitor connected to SS, shown in Equation (1):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{RFF}(V)}{I_{SS}(\mu A)}$$

   Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.6V), and I_{SS} is the 3.2μA SS charge current. The soft-start time is about 0.5ms when SS pin is floating.
10. Use R6(R8) and R18(R12) to set the output voltage with V_{FB}=0.6V. For R6(R8)=100kΩ, R18(R12) can be determined by:

$$R18(R12) = \frac{R6(R8)}{\frac{V_{OUT}}{0.6} - 1}$$

    Follow the Application Information section in the device datasheet to recalculate the compensation, inductor and output capacitor values when output voltage is changed.

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Revision History

Revision #	Revision Date	Description	Pages Updated
1.0	10/17/2019	Initial Release	-
1.1	9/21/2020	Correct the inductor part number from “MPL-AY4020-1R5” to “MPL-AL4020-1R5” in the BOM.	P4

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