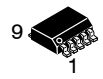
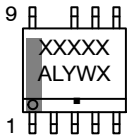
# High-Voltage Quasi-Resonant Flyback Controller With USB-PD Optimization

# NCP1345



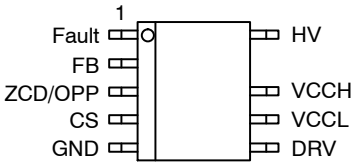

**SOIC−9 NB**
**CASE 751BP**

## MARKING DIAGRAM




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

## PIN CONNECTIONS




## ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

The NCP1345 is a highly integrated quasi−resonant flyback controller suitable for designing high−performance off−line USB−PD and USB Type−C power converters. The included dual−pin $V_{CC}$ architecture allows direct connection to the aux winding for simplified $V_{CC}$ management with a reduced parts count and increased performance.

The NCP1345 also features a precise, primary side based output current limiting circuit to ensure a constant output current limit regardless of programmed output voltage, or nameplate output power.

The quasi−resonant (QR) current−mode flyback stage features proprietary valley−lockout circuitry to ensure stable valley switching down to the 6$^{th}$ valley, then transitions to frequency foldback mode to reduce switching losses. As the load decreases further, the NCP1345 enters skip mode to manage the power delivery.

To help ensure converter ruggedness, the NCP1345 implements several key protective features such as internal brownout detection, a maximum output current limit regardless of input voltage, a latched over voltage and NTC−ready overtemperature protection through a dedicated pin, and line removal detection to safely discharge the X2 capacitors when the line is removed.

### Features

- Integrated High−Voltage Startup Circuit with Brownout Detection
- Integrated X2 Capacitor Discharge Capability
- Wide $V_{CCL}$ Range from 8 V to 38 V
- 150 V $V_{CCH}$ Pin for Connection to High−Voltage Aux Winding
- 36.5 V $V_{CC}$ Overvoltage Protection
- Primary Side Based Constant Output Current Limiting
- Abnormal Overcurrent Fault Protection for Winding Short Circuit Detection
- Internal Temperature Shutdown
- Valley Switching Operation with Valley−Lockout for Noise−Free Operation
- Rapid Frequency Foldback for Fast Reduction of Switching Frequency
- Skip Mode with Output Voltage Compensation
- Minimized No Load Power Consumption
- Frequency Jittering for Reduced EMI Signature
- Latching or Auto−Recovery Overload Protection
- Adjustable Overpower Protection
- Fixed/Adjustable Maximum Frequency Clamp
- Fault Pin for Severe Fault Conditions, NTC Compatible for OTP

© Semiconductor Components Industries, LLC, 2021

## APPLICATION DETAILS

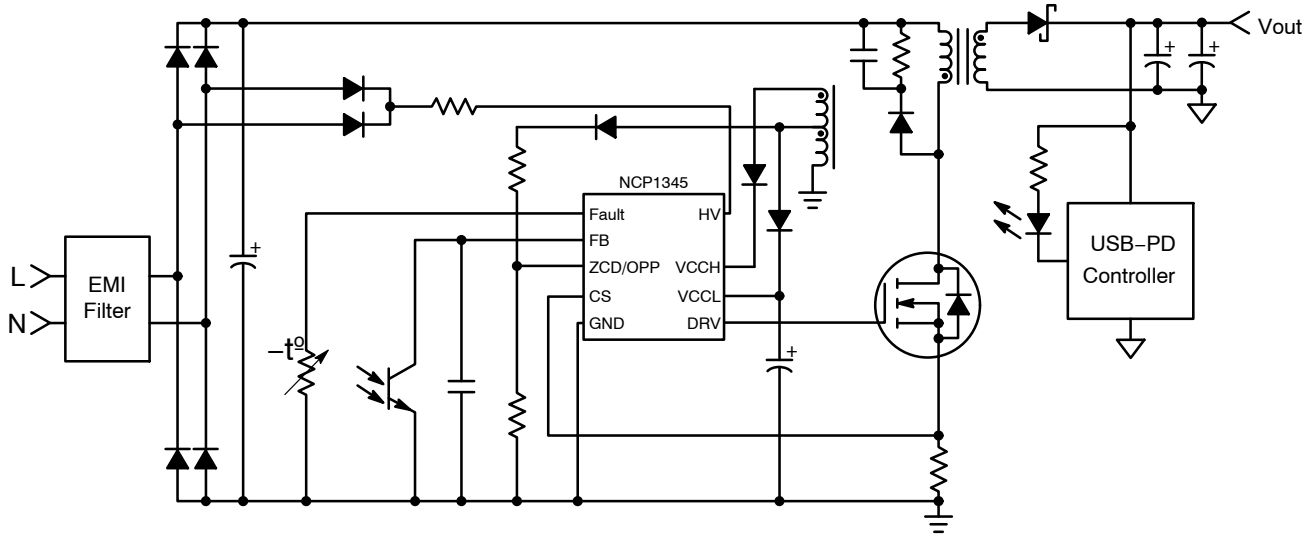



**Figure 1. Typical Application Circuit**

## FUNCTIONAL DETAILS

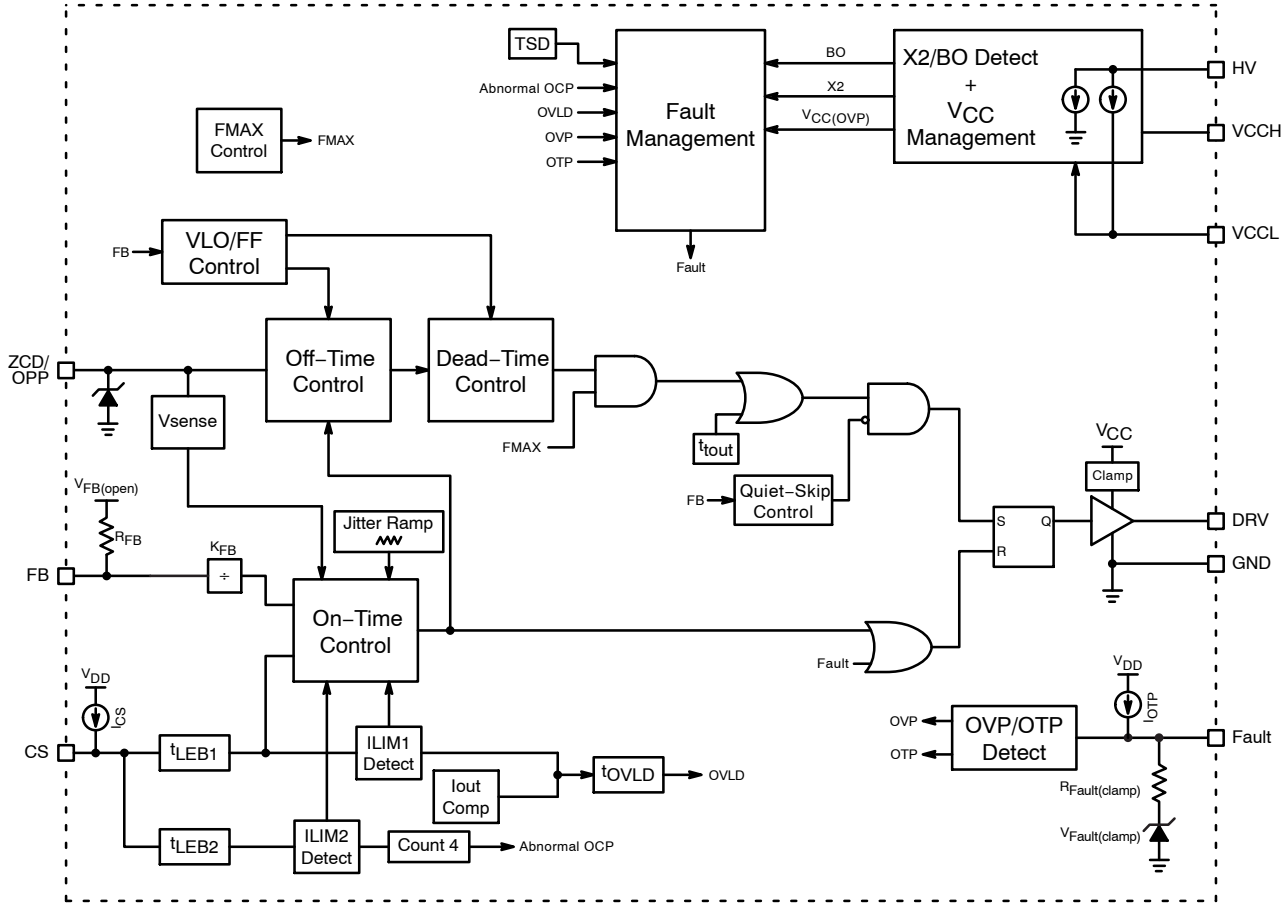



**Figure 2. NCP1345 Simplified Block Diagram**

**Table 1. PIN FUNCTIONAL DESCRIPTION**

| Pin Name | Pin Number | Function |
|---|---|---|
| Fault | 1 | The controller enters fault mode if the voltage on this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. |
| FB | 2 | Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler. |
| ZCD/OPP | 3 | A resistor divider from the auxiliary winding to this pin provides input to the demagnetization detection comparator and sets the OPP compensation level. It is also used to detect the output voltage for Auto−Tuning Skip Mode. |
| CS | 4 | Input to the cycle−by−cycle current limit comparator. |
| GND | 5 | Ground reference. |
| DRV | 6 | This is the drive pin of the circuit. The DRV high−current capability (−0.5 /+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs. |
| VCCL | 7 | This pin is the positive supply of the IC. The circuit starts to operate when $V_{CC}$ exceeds 17 V and turns off when $V_{CC}$ goes below 9 V (typical values). After start−up, the operating range is 9 V up to 36.5 V. |
| VCCH | 8 | This pin is the high voltage Aux winding input and is rated up to 150 V. |
| N/C | 9 | Removed for creepage distance. |
| HV | 10 | This pin is the input for the high voltage startup and brownout detection circuits. It also contains the line removal detection circuit to safely discharge the X2 capacitors when the line is removed. |

**Table 2. MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| High Voltage Startup Circuit Input Voltage | $V_{HV(MAX)}$ | −0.3 to 800 | V |
| High Voltage Startup Circuit Input Current | $I_{HV(MAX)}$ | 20 | mA |
| Supply Input Voltage | $V_{CCH(MAX)}$ | −0.3 to 150 | V |
| Supply Input Current | $I_{CCH(MAX)}$ | 20 | mA |
| Supply Input Voltage | $V_{CCL(MAX)}$ | −0.3 to 38 | V |
| Supply Input Current | $I_{CCL(MAX)}$ | 20 | mA |
| Supply Input Voltage Slew Rate | $dV_{CC}/dt$ | 1 | V/μs |
| Fault Input Voltage | $V_{Fault(MAX)}$ | −0.3 to $V_{CC}$ + 0.7 | V |
| Fault Input Current | $I_{Fault(MAX)}$ | 10 | mA |
| Zero Current Detection and OPP Input Voltage | $V_{ZCD(MAX)}$ | −0.3 to $V_{CC}$ + 0.7 | V |
| Zero Current Detection and OPP Input Current | $I_{ZCD(MAX)}$ | −2/+5 | mA |
| Maximum Input Voltage (Other Pins) | $V_{MAX}$ | −0.3 to 5.5 | V |
| Maximum Input Current (Other Pins) | $I_{MAX}$ | 10 | mA |
| Driver Maximum Voltage (Note 1) | $V_{DRV}$ | −0.3 to $V_{DRV(high)}$ | V |
| Driver Maximum Current | $I_{DRV(SRC)}$<br>$I_{DRV(SNK)}$ | 500<br>800 | mA |
| Operating Junction Temperature | $T_J$ | −40 to 125 | °C |
| Storage Temperature Range | $T_{STG}$ | −60 to 150 | °C |
| Power Dissipation ($T_A$ = 25°C, 1 Oz Cu, 0.155 Sq Inch Printed Circuit Copper Clad)<br>D1 Suffix, SOIC−9 | $P_{D(MAX)}$ | <br>450 | mW |
| Thermal Resistance, Junction to Ambient (1 Oz Cu Printed Circuit Copper Clad)<br>D1 Suffix, SOIC−9 | $R_{\theta JA}$ | <br>225 | °C/W |
| ESD Capability<br>Human Body Model per JEDEC Standard JESD22−A114E<br>Charge Device Model per JEDEC Standard JESD22−C101E<br>Latch−Up Protection per JEDEC Standard JESD78 | | <br>2000<br>1000<br>±100 | <br>V<br>V<br>mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when $V_{CC}$ exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is $V_{CC}$.

## ORDERING DETAILS

**Table 3. PART NUMBER DECODE**

| NCP1345 | $V_{CC(on)}$ (V) | $V_{CC(off)}$ (V) | AC/DC Input | RFF (mV) | RFF Exit Voltage (mV) | FB Pin Pullup Resistance (kΩ) | FB Pin Source Current (μA) | FB Pin Mode | $R_{FB}$ Apparent (kΩ) | $CS_{MIN}$ Threshold (mV) | QuietSkip Frequency (kHz) | Adaptive Gate Drive Valley | Frequency Clamp (kHz) | ZCD Blanking (ns) | Jitter Frequency (kHz) | Jitter Voltage (mV) | LEB1/2 Duration (ns) | Overload Protection (ms) | Overload Fault Behavior | OTP Fault Behavior | VCC(off) Fault Mode | X2 Discharge | Brownin/Brownout (Vdc) | Vout OVP (V) | Iout Limit Reference (mV) | VCC OVP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Options / Suffix | A – 17<br>B – 15 | A – 9.0<br>B – 8.5<br>C – 8.0<br>D – 7.5 | A – AC<br>B – DC | A – 400<br>B – 350<br>C – 300<br>D – 250<br>E – Off | A – 750<br>B – 740<br>C – 730<br>D – 720<br>E – N/A | A – 20<br>B – 400<br>C – N/A | A – 100<br>B – Off | A – Voltage<br>B – Current | A – 19<br>B – 38<br>C – 57<br>D – 75<br>E – 94<br>F – 112<br>G – 131<br>H – 149<br>I – N/A | A – Auto<br>B – 200<br>C – 150<br>D – 100 | A – 0.8<br>B – 1.2<br>C – 1.6<br>D – Off | A – 1st<br>B – 2nd<br>C – 3rd<br>D – 4th<br>E – 5th<br>F – 6th<br>G – Off | A – 69<br>B – 75<br>C – 81<br>D – 93<br>E – 109<br>F – 140<br>G – 164<br>H – Adj<br>I – Off | A – 3000<br>B – 700<br>C – 500<br>D – 100 | A – 0.25<br>B – 0.5<br>C – 1<br>D – 1.5<br>E – 1.95<br>F – 2.6<br>G – 3.9<br>H – 7.7<br>I – Off | A – 50<br>B – 75<br>C – 100<br>D – 150<br>E – 200<br>F – N/A | A – 80/32<br>B – 125/50<br>C – 200/80<br>D – 275/110 | A – 40<br>B – 80<br>C – 160<br>D – 420<br>E – N/A | A – AR<br>B – Latch<br>C – Off | A – AR<br>B – Latch | A – UVLO<br>B – AR | A – On<br>B – Off | A – On<br>B – Off | A – 112/98<br>B – Off | A – 11.5<br>B – 12.0<br>C – 12.5<br>D – 13.0<br>E – Off | A – 310<br>B – 450<br>C – Adj<br>D – Off | A – On<br>B – Off |
| Q00 | A | A | A | E | E | A | B | A | I | A | D | B | I | B | G | E | B | C | A | A | A | A | A | B | B | A |
| Q01 | A | A | A | B | C | A | B | A | I | A | D | C | I | B | G | C | B | C | A | A | A | A | A | B | A | A |
| Q02 | A | A | B | B | C | A | B | A | I | A | D | C | I | B | G | C | B | C | A | A | A | B | A | B | A | A |

**Table 4. ORDERING INFORMATION**

| Part Number | Device Marking | Package | Shipping† |
|---|---|---|---|
| NCP1345Q00D1R2G | 1345Q00 | SOIC−9 NB (Pb−Free) | 2500 / Tape & Reel |
| NCP1345Q01D1R2G | 1345Q01 | SOIC−9 NB (Pb−Free) | |
| NCP1345Q02D1R2G | 1345Q02 | SOIC−9 NB (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**Table 5. ELECTRICAL CHARACTERISTICS**
($V_{CCL}$ = 12 V, $V_{CCH}$ = $V_{CCL}$, $V_{HV}$ = 120 V, $V_{Fault}$ = open, $V_{FB}$ = 2.4 V, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{VCCL}$ = 100 nF, $C_{VCCH}$ = 100 nF, $C_{DRV}$ = 1 nF, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is − 40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **START−UP AND SUPPLY CIRCUITS** | | | | | | |
| Supply Voltage | dV/dt = 0.1 V/ms | | | | | V |
| Startup Threshold | $V_{CC}$ increasing | $V_{CC(on)}$ | 16.0 | 17.0 | 18.0 | |
| Minimum Operating Voltage | $V_{CC}$ decreasing | $V_{CC(off)}$ | 8.5 | 9.0 | 9.5 | |
| Operating Hysteresis ($V_{CC(on)}$ − $V_{CC(off)}$) | | $V_{CC(HYS)}$ | 7.5 | – | – | |
| Internal Latch / Logic Reset Level | $V_{CC}$ decreasing | $V_{CC(reset)}$ | 6.0 | 6.5 | 7.2 | |
| Transition from $I_{start1}$ to $I_{start2}$ | $V_{CC}$ increasing, $I_{HV}$ = 650 μA | $V_{CC(inhibit)}$ | 0.40 | 0.70 | 1.05 | |
| $V_{CC(off)}$ Delay | $V_{CC}$ decreasing | $t_{delay(VCC_off)}$ | 25 | 32 | 40 | μs |
| Startup Delay | Delay from $V_{CC(on)}$ to DRV Enable | $t_{delay(start)}$ | – | – | 500 | μs |
| Minimum Voltage for Start−Up Current Source | | $V_{HV(MIN)}$ | – | – | 30 | V |
| Inhibit Current Sourced from $V_{CC}$ Pin | $V_{cc}$ = 0 V | $I_{start1}$ | 0.2 | 0.5 | 0.65 | mA |
| Start−Up Current Sourced from $V_{CC}$ Pin | $V_{cc}$ = $V_{cc(on)}$ − 0.5 V<br>HV Discharge Active | $I_{start2}$<br>$I_{start3}$ | 2.4<br>– | 3.75<br>– | 5.8<br>0 | mA |
| Start−Up Circuit Off−State Leakage Current | $V_{HV}$ = 800 V | $I_{HV(off)}$ | – | – | 30 | μA |
| Supply Current | | | | | | mA |
| Fault or Latch | $V_{CC}$ = $V_{CC(on)}$ − 0.5 V | $I_{CCL1}$ | – | 0.115 | 0.250 | |
| Skip Mode (excluding FB current) | $V_{FB}$ = 0 V | $I_{CCL2}$ | – | 0.250 | 0.455 | |
| Operating Current | $f_{sw}$ = 50 kHz, $C_{DRV}$ = open | $I_{CCL3}$ | – | 1.35 | 2.00 | |
| **DUAL VCC MANAGEMENT** | | | | | | |
| Regulation Voltage | $I_{CCH}$ = 5 mA | $V_{REG}$ | 9.5 | 10.0 | 10.6 | V |
| Dropout Voltage ($V_{VCCH}$ − $V_{CCL}$) | Adjust $V_{CCH}$ such that $V_{CCL}$ = $V_{REG}$ − 1 V<br>$I_{CCH}$ = 5 mA<br>$I_{CCH}$ = 500 μA | $V_{DO}$ | <br>–<br>– | <br>600<br>75 | <br>1300<br>200 | mV |
| Input Off−State Leakage Current | | $I_{VCCH(off)}$ | – | – | 15 | μA |
| **INPUT FILTER CAPACITOR DISCHARGE (ALL EXCEPT Q02)** | | | | | | |
| Line Voltage Removal Detection Timer | | $t_{line(removal)}$ | 80 | 100 | 120 | ms |
| Upslope Detection Reset Timer | HV increasing | $t_{HV(up)}$ | – | 14 | – | ms |
| Downslope Detection Reset Timer | HV decreasing | $t_{HV(down)}$ | – | 1 | – | ms |
| HV Discharge Current | <br>$V_{HV}$ = $V_{HVdisch(end)}$ + 100 mV | $I_{HV(disch)}$ | 0.75<br>0.04 | 2<br>– | 3.75<br>0.6 | mA |
| $V_{CC}$ Discharge Current | $V_{CC}$ = $V_{CC(on)}$ | $I_{CC(disch)}$ | 13 | 18 | 23 | mA |
| Minimum Voltage for Discharge Current Source | $I_{HV}$ = 0.8 * $I_{HV(disch)}$<br>HV Discharge Active | $V_{HVdisch(min)}$ | – | – | 40 | V |
| HV Discharge Stop Level | | $V_{HVdisch(end)}$ | – | – | 30 | V |
| Delta Between $V_{CC(on)}$ and HV Discharge Stop Level | | $\Delta_{discharge}$ | 0.1 | – | – | V |
| **BROWNOUT DETECTION** | | | | | | |
| System Start−Up Threshold | $V_{HV}$ increasing | $V_{BO(start)}$ | 107 | 112 | 117 | V |
| Brownout Threshold | $V_{HV}$ decreasing | $V_{BO(stop)}$ | 93 | 98 | 103 | V |
| Hysteresis | $V_{HV}$ increasing | $V_{BO(HYS)}$ | 9 | 14 | – | V |
| Brownout Detection Blanking Time | $V_{HV}$ decreasing | $t_{BO(stop)}$ | 40 | 70 | 100 | ms |

2. NTC with $R_{110}$ = 8.8 kΩ

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($V_{CCL}$ = 12 V, $V_{CCH}$ = $V_{CCL}$, $V_{HV}$ = 120 V, $V_{Fault}$ = open, $V_{FB}$ = 2.4 V, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{VCCL}$ = 100 nF, $C_{VCCH}$ = 100 nF, $C_{DRV}$ = 1 nF, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is − 40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **GATE DRIVE** | | | | | | |
| Adaptive Gate Drive Engagement Valley<br>Q00<br>Q01/Q02 | | $n_{DRV(valley)}$ | | <br>2<br>3 | | |
| Rise Time<br><br><br><br>During Adaptive Gate Drive | $V_{DRV}$ from 10% to 90%<br>$C_{DRV}$ = 100 pF<br>$C_{DRV}$ = 1 nF<br>$V_{FB}$ = 0.8 V, $C_{DRV}$ = 100 pF<br>$V_{FB}$ = 0.8 V, $C_{DRV}$ = 1 nF | $t_{DRV(rise)}$ | <br>–<br>–<br>–<br>350 | <br>20<br>50<br>200<br>550 | <br>–<br>90<br>–<br>850 | ns |
| Fall Time | $V_{DRV}$ from 90% to 10% | $t_{DRV(fall)}$ | – | 20 | 60 | ns |
| Source Current Capability<br>During Adaptive Gate Drive | $V_{FB}$ = 2 V<br>$V_{FB}$ = 0.7 V | $I_{DRV(SRC)}$ | –<br>– | 500<br>50 | –<br>– | mA |
| Sink Current Capability | | $I_{DRV(SNK)}$ | – | 800 | – | mA |
| Drive Clamp Voltage | $V_{CC}$ = 30 V, $R_{DRV}$ = 10 kΩ | $V_{DRV(clamp)}$ | 10 | 12 | 14 | V |
| High State Voltage | $V_{CC}$ = $V_{CC(off)}$ + 0.2 V, $R_{DRV}$ = 10 kΩ | $V_{DRV(high)}$ | 8 | – | – | V |
| Low Stage Voltage | $V_{Fault}$ = 0 V | $V_{DRV(low)}$ | – | – | 0.25 | V |
| **FEEDBACK** | | | | | | |
| Open Pin Voltage | | $V_{FB(open)}$ | 4.8 | 5.0 | 5.2 | V |
| $V_{FB}$ to Internal Current Setpoint Division Ratio | | $K_{FB}$ | 3.6 | 4.0 | 4.4 | – |
| Internal Pull−Up Resistor | $V_{FB}$ = 0.4 V | $R_{FB}$ | 17.0 | 20.0 | 25.0 | kΩ |
| Valley Thresholds<br>Transition from 1st to 2nd valley<br>Transition from 2nd to 3rd valley<br>Transition from 3rd to 4th valley<br>Transition from 4th to 5th valley<br>Transition from 5th to 6th valley<br>Transition from 6th to 5th valley<br>Transition from 5th to 4th valley<br>Transition from 4th to 3rd valley<br>Transition from 3rd to 2nd valley<br>Transition from 2nd to 1st valley | <br>$V_{FB}$ decreasing<br>$V_{FB}$ decreasing<br>$V_{FB}$ decreasing<br>$V_{FB}$ decreasing<br>$V_{FB}$ decreasing<br>$V_{FB}$ increasing<br>$V_{FB}$ increasing<br>$V_{FB}$ increasing<br>$V_{FB}$ increasing<br>$V_{FB}$ increasing | <br>$V_{1to2}$<br>$V_{2to3}$<br>$V_{3to4}$<br>$V_{4to5}$<br>$V_{5to6}$<br>$V_{6to5}$<br>$V_{5to4}$<br>$V_{4to3}$<br>$V_{3to2}$<br>$V_{2to1}$ | <br>1.316<br>1.128<br>1.034<br>0.940<br>0.846<br>1.410<br>1.504<br>1.598<br>1.692<br>1.880 | <br>1.400<br>1.200<br>1.100<br>1.000<br>0.900<br>1.500<br>1.600<br>1.700<br>1.800<br>2.000 | <br>1.484<br>1.272<br>1.166<br>1.060<br>0.954<br>1.590<br>1.696<br>1.802<br>1.908<br>2.120 | V |
| Maximum On Time | | $t_{on(MAX)}$ | 26 | 32 | 38 | μs |
| **FEEDBACK (CASCODE/HIGH BW OPTION)** | | | | | | |
| Clamp Voltage | $I_{FB}$ = 150 μA | $V_{clamp}$ | 2 | 2.5 | – | V |
| Dynamic Resistance | 5.0 μA < $I_{FB}$ < 250 μA | $R_{dyn(FB)}$ | 0.5 | 1 | 1.6 | kΩ |
| **DEMAGNETIZATION INPUT** | | | | | | |
| ZCD threshold voltage | $V_{ZCD}$ decreasing | $V_{ZCD(trig)}$ | 35 | 60 | 95 | mV |
| ZCD hysteresis | $V_{ZCD}$ increasing | $V_{ZCD(HYS)}$ | 10 | 25 | 55 | mV |
| Demagnetization Propagation Delay | $V_{ZCD}$ step from 2.1 V to 0 V | $t_{demag}$ | – | 80 | 150 | ns |
| ZCD Clamp Voltage<br>Negative Clamp | Not including $R_{Vout}$<br>$I_{QZCD}$ = −2.0 mA | <br>$V_{ZCD(MIN)}$ | <br>−0.9 | <br>−0.7 | <br>0 | V |
| Blanking Delay After Turn−Off | | $t_{ZCD(blank)}$ | 0.60 | 0.70 | 0.80 | μs |
| Timeout After Last Demagnetization Detection | While in soft−start<br>After soft−start complete | $t_{(tout1)}$<br>$t_{(tout2)}$ | 80<br>5.1 | 100<br>6 | 120<br>6.9 | μs |

2. NTC with $R_{110}$ = 8.8 kΩ

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($V_{CCL}$ = 12 V, $V_{CCH}$ = $V_{CCL}$, $V_{HV}$ = 120 V, $V_{Fault}$ = open, $V_{FB}$ = 2.4 V, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{VCCL}$ = 100 nF, $C_{VCCH}$ = 100 nF, $C_{DRV}$ = 1 nF, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is − 40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DEMAGNETIZATION INPUT** | | | | | | |
| Maximum Frequency Clamp<br>Q00, Q01, Q02 | | $f_{MAX}$ | <br>– | <br>– | <br>– | kHz |
| Number of Consecutive Open Pin Triggers to Enter Latch Mode | | $n_{ZCD}$ | – | 4 | – | |
| ZCD Pull−Down Resistor | | $R_{Vout}$ | 0.97 | 1.00 | 1.04 | kΩ |
| ZCD Pull−Up Current | | $I_{ZCD}$ | 0.8 | 1 | 1.2 | μA |
| **CURRENT SENSE** | | | | | | |
| Soft−Start Period | Measured from 1st DRV pulse to $V_{CS}$ = $V_{ILIM1}$ | $t_{SSTART}$ | 2.8 | 4.0 | 5.0 | ms |
| Current Limit Threshold Voltage | $V_{CS}$ increasing | $V_{ILIM1}$ | 0.765 | 0.800 | 0.835 | V |
| Leading Edge Blanking Duration<br>Q00, Q01, Q02 | DRV minimum width minus $t_{delay(ILIM1)}$ | $t_{LEB1}$ | <br>100 | <br>125 | <br>150 | ns |
| Current Limit Threshold Propagation Delay | Step $V_{CS}$ 25 mV below $V_{ILIM1}$ to 75 mV above $V_{ILIM1}$, $V_{FB}$ = 4 V | $t_{delay(ILIM1)}$ | – | – | 80 | ns |
| Overpower Protection Delay | Step $V_{CS}$ 25 mV below $V_{ILIM1}$ − $V_{OPP}$ to 75 mV above $V_{ILIM1}$ − $V_{OPP}$, $V_{FB}$ = 4 V | $t_{OPP(delay)}$ | – | – | 90 | ns |
| PWM Comparator Propagation Delay | Step $V_{CS}$ 25 mV below $V_{FB}/k_{FB}$ to 75 mV above $V_{FB}/k_{FB}$ | $t_{delay(PWM)}$ | – | – | 110 | ns |
| Minimum Peak Current | <br>$V_{ZCD(hi)}$ = 10.5 V<br>$V_{ZCD(hi)}$ = 1.25 V | $V_{CS(MIN)}$ | <br>170<br>60 | <br>200<br>80 | <br>230<br>100 | mV |
| CSmin Comparator Propagation Delay | Step $V_{CS}$ 25 mV below $V_{CS(MIN)}$ to 75 mV above $V_{CS(MIN)}$ | $t_{delay(CSMIN)}$ | – | – | 140 | ns |
| RFF Current Shift<br>Q00<br>Q01/Q02 | $V_{FB}$ = 800 mV | $V_{RFF(delta)}$ | <br>–<br>300 | <br>–<br>350 | <br>–<br>400 | mV |
| RFF Entry Threshold<br>(All Except Q00) | $V_{FB}$ Decreasing | $V_{RFF(entry)}$ | 775 | 800 | 840 | mV |
| RFF Exit Threshold<br>Q01/Q02 | $V_{FB}$ Increasing | $V_{RFF(exit)}$ | <br>700 | <br>730 | <br>760 | mV |
| RFF Transition Timer<br>(All Except Q00) | | $t_{RFF}$ | 0.80 | 1.00 | 1.10 | ms |
| Abnormal Overcurrent Fault Threshold | $V_{CS}$ increasing, $V_{FB}$ = 5.0 V | $V_{ILIM2}$ | 1.125 | 1.200 | 1.275 | V |
| Abnormal Overcurrent Fault Blanking Duration<br>Q00, Q01, Q02 | DRV minimum width minus $t_{delay(ILIM2)}$ | $t_{LEB2}$ | <br>25 | <br>50 | <br>75 | ns |
| Abnormal Overcurrent Fault Propagation Delay | Step $V_{CS}$ 25 mV below $V_{ILIM2}$ to 75 mV above $V_{ILIM2}$, $V_{FB}$ = 5 V | $t_{delay(ILIM2)}$ | – | – | 90 | ns |
| Number of Consecutive Abnormal Overcurrent Faults to Enter Latch Mode | | $n_{ILIM2}$ | – | 4 | – | |
| Pull−Up Current Source | $V_{CS}$ = 1.5 V | $I_{CS}$ | 0.7 | 1.0 | 1.5 | μA |
| **OVERPOWER PROTECTION (OPP)** | | | | | | |
| OPP Programming Current | Start−up Only | $I_{OPP}$ | 19 | 20 | 21 | μA |
| **OUTPUT CURRENT LIMIT** | | | | | | |
| IOUT Pin Source Current (10−Pin Only) | | $I_{IOUT}$ | 9.0 | 10.0 | 11.0 | μA |

2. NTC with $R_{110}$ = 8.8 kΩ

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
($V_{CCL}$ = 12 V, $V_{CCH}$ = $V_{CCL}$, $V_{HV}$ = 120 V, $V_{Fault}$ = open, $V_{FB}$ = 2.4 V, $V_{CS}$ = 0 V, $V_{ZCD}$ = 0 V, $C_{VCCL}$ = 100 nF, $C_{VCCH}$ = 100 nF, $C_{DRV}$ = 1 nF, for typical values $T_J$ = 25°C, for min/max values, $T_J$ is − 40°C to 125°C, unless otherwise noted)

| Characteristics | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OUTPUT CURRENT LIMIT** | | | | | | |
| Demagnetization End Detection Drop | | $V_{demag(det)}$ | 120 | 150 | 180 | mV |
| Feedback Voltage Overload Threshold | Apply 100 kHz Square Wave to ZCD Pin +6.9V / 0 V, and Inverse Square Wave to CS Pin 0.9V/0V | $V_{FB(OVLD)}$ | | | | V |
| Q01/Q02 | 60% Duty Cycle, $V_{REFiout}$ = 310 mV | | 1.475 | 1.750 | 2.025 | |
| | 95% Duty Cycle, $V_{REFiout}$ = 310 mV | | 0.85 | 0.99 | 1.15 | |
| Q00 | 60% Duty Cycle, $V_{REFiout}$ = 450 mV | | 2.280 | 2.680 | 3.080 | |
| | 95% Duty Cycle, $V_{REFiout}$ = 450 mV | | 1.340 | 1.575 | 1.810 | |
| **JITTERING** | | | | | | |
| Jitter Frequency<br>Q00, Q01, Q02 | | $f_{jitter}$ | 3.31 | 3.90 | 4.49 | kHz |
| Peak−to−Peak Jitter Voltage<br>Q01/Q02<br>Q00 | | $V_{jitter}$ | <br>85<br>170 | <br>100<br>200 | <br>115<br>230 | mV |
| **FAULT PROTECTION** | | | | | | |
| Flyback Overload Fault Timer | $V_{CS}$ = $V_{ILIM1}$ | $t_{OVLD}$ | 120 | 160 | 200 | ms |
| Overvoltage Protection (OVP) Threshold | $V_{Fault}$ increasing | $V_{Fault(OVP)}$ | 2.99 | 3.20 | 3.41 | V |
| Overvoltage Protection (OVP) Delay | $V_{Fault}$ increasing | $t_{delay(OVP)}$ | 22.5 | 30.0 | 37.5 | μs |
| Output OVP Threshold | | $V_{out(OVP)}$ | 11.4 | 12.0 | 12.4 | V |
| Number of Consecutive OVP Detections to Trigger Fault | | $n_{out(OVP)}$ | – | 3 | – | |
| $V_{CC}$ Overvoltage Protection Threshold | | $V_{CC(OVP)}$ | 35.0 | 36.5 | 38.0 | V |
| $V_{CC}$ Overvoltage Protection Delay | | $t_{delay(VCC_OVP)}$ | 25 | 32 | 40 | μs |
| Overtemperature Protection (OTP) Threshold (Note 2) | $V_{Fault}$ decreasing | $V_{Fault(OTP_in)}$ | 0.388 | 0.40 | 0.412 | V |
| Overtemperature Protection (OTP) Exiting Threshold (Note 2) | $V_{Fault}$ increasing | $V_{Fault(OTP_out)}$ | 0.880 | 0.920 | 0.960 | V |
| OTP Detection Delay | $V_{Fault}$ decreasing | $t_{delay(OTP)}$ | 22.5 | 30.0 | 37.5 | μs |
| OTP Pull−Up Current Source | $V_{Fault}$ = $V_{Fault(OTP_in)}$ + 0.2 V<br>$T_J$ = 25°C to 125°C | $I_{OTP}$ | 43.75 | 45.0 | 46.25 | μA |
| Fault Input Clamp Voltage | | $V_{Fault(clamp)}$ | 1.15 | 1.7 | 2.25 | V |
| Fault Input Clamp Series Resistor | | $R_{Fault(clamp)}$ | 1.52 | 1.75 | 1.98 | kΩ |
| Autorecovery Timer | | $t_{restart}$ | 1.8 | 2 | 2.2 | s |
| **LIGHT/NO LOAD MANAGEMENT** | | | | | | |
| Minimum Frequency Clamp | | $f_{MIN}$ | 21.0 | 24.5 | 28.0 | kHz |
| Dead−Time Added During Frequency Foldback | $V_{FB}$ = 400 mV | $t_{DT(MAX)}$ | 32 | – | – | μs |
| Quiet−Skip Timer | | $t_{quiet}$ | 1.18 | 1.25 | 1.40 | ms |
| Skip Threshold | $V_{FB}$ decreasing | $V_{skip}$ | 304 | 320 | 336 | mV |
| Skip Hysteresis | $V_{FB}$ increasing | $V_{skip(HYS)}$ | 35 | 50 | 75 | mV |
| **THERMAL PROTECTION** | | | | | | |
| Thermal Shutdown | Temperature increasing | $T_{SHDN}$ | – | 140 | – | °C |
| Thermal Shutdown Hysteresis | Temperature decreasing | $T_{SHDN(HYS)}$ | – | 40 | – | °C |

2. NTC with $R_{110}$ = 8.8 kΩ

## OPERATIONAL DESCRIPTION

### HIGH VOLTAGE START−UP CIRCUIT

The NCP1345 contains a multi−functional high voltage (HV) pin. While the primary purpose of this pin is to reduce standby power while maintaining a fast start−up time, it also incorporates brownout detection and line removal detection.

The HV pin must be connected directly to the ac line in order for the HV discharge circuit to function correctly. Line and neutral should be diode “ORed” before connecting to the HV pin as shown in Figure 3.

The diodes prevent the pin voltage from going below ground. A resistor in series with the pin should be used to protect the pin during EMC or surge testing. A low value resistor should be used (<5 kΩ) to reduce the voltage offset during start−up. The start−up circuit block diagram is shown in Figure 4.

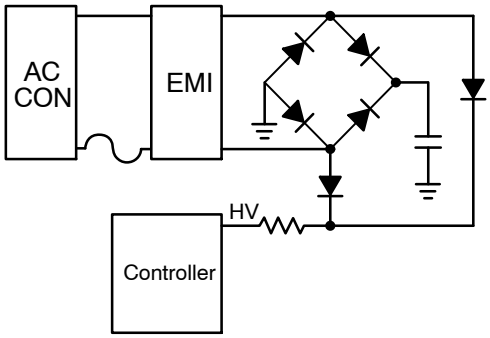



**Figure 3. High−Voltage Input Connection**

### Start−up and $V_{CC}$ Management

During start−up, the current source turns on and charges the $V_{CC}$ capacitor with $I_{start2}$ (typically 6 mA). When $V_{cc}$ reaches $V_{CC(on)}$ (typically 16.0 V), the current source turns off. If the input voltage is not high enough to ensure a proper start−up (i.e. $V_{HV}$ has not reached $V_{BO(start)}$), the controller will not start. $V_{CC}$ then begins to fall because the controller bias current is at $I_{CC2}$ (typically 1 mA) and the auxiliary supply voltage is not present. When $V_{CC}$ falls to $V_{CC(off)}$ (typically 10.5 V), the current source turns back on and charges $V_{CC}$. This cycle repeats indefinitely until $V_{HV}$ reaches $V_{BO(start)}$. Once this occurs, the current source immediately turns on and charges $V_{CC}$ to $V_{CC(on)}$, at which point the controller starts (see Figure 5).

When $V_{CC}$ is brought below $V_{CC(inhibit)}$, the start−up current is reduced to $I_{start1}$ (typically 0.5 mA). This limits power dissipation on the device in the event that the $V_{CC}$ pin is shorted to ground. Once $V_{CC}$ rises back above $V_{CC(inhibit)}$, the start−up current returns to $I_{start2}$.

Once $V_{CC}$ reaches $V_{CC(on)}$, the controller is enabled and the controller bias current increases to $I_{CC3}$ (typically 2.0 mA). However, the total bias current is greater than this due to the gate charge of the external switching MOSFET. The increase in $I_{CC}$ due to the MOSFET is calculated using Equation 1.

$$\Delta I_{CC} = f_{sw} \cdot Q_G \qquad \text{(eq. 1)}$$

where $\Delta I_{CC}$ is the increase in milliamps, $f_{sw}$ is the switching frequency in kilohertz and $Q_G$ is the gate charge of the external MOSFET in nanocoulombs.

$C_{VCC}$ must be sized such that a $V_{CC}$ voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage increases during start−up. If $C_{VCC}$ is too small, $V_{CC}$ will fall below $V_{CC(off)}$ and the controller will turn off before the auxiliary winding supplies the IC. The total $I_{CC}$ current after the controller is enabled ($I_{CC3}$ plus $\Delta I_{CC}$) must be considered to correctly size $C_{VCC}$.

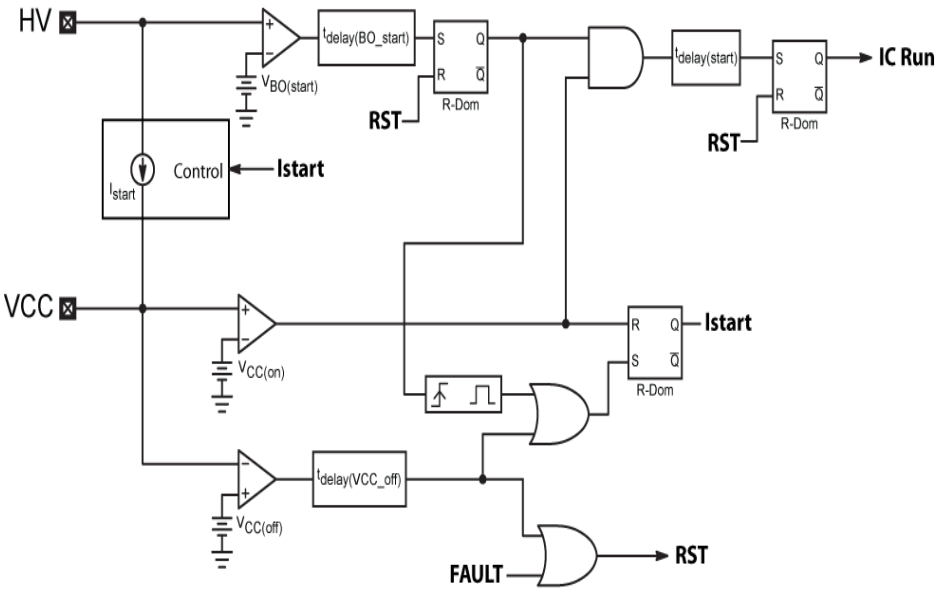



**Figure 4. Start−up Circuitry Block Diagram**

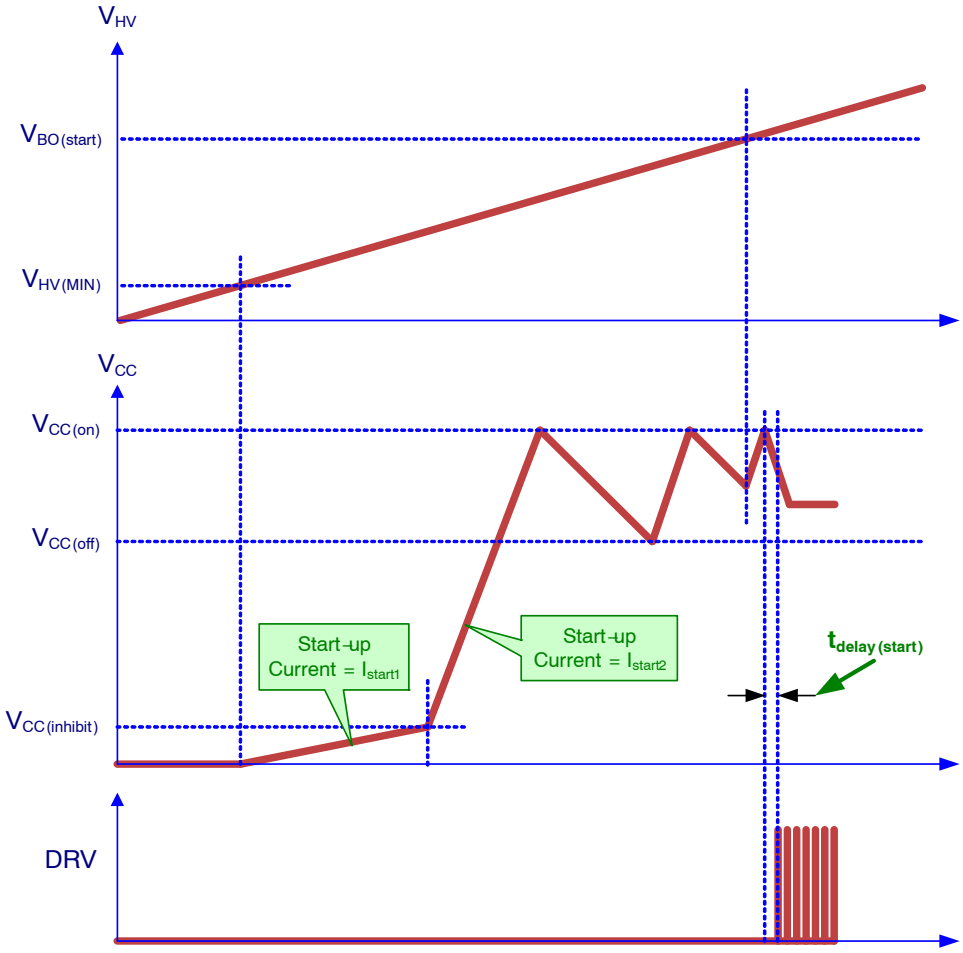



**Figure 5. Start−up Timing**

### Dual−Range $V_{CC}$ Management

For typical USB−PD 3.0 adpter designs, the output voltage ranges from 3.3V up to 21V. This wide variation of output voltage places a burden on the primary controller to support a wide range of VCC voltages. , the NCP1345 incorporates a dual range $V_{CC}$ architecture. This consists of a second $V_{CC}$ pin, VCCH, rated at 200 V. The VCCH pin is designed to connect directly to a second aux winding providing a bias voltage roughly 3x−4x the output voltage, and thus 3x−4x the main aux winding voltage.

When the output voltage is at the minimum voltage of 3.3V, the main aux winding voltage will be too low to supply the NCP1345. During this period, the VCCH pin will receive ~12.6 V from the VCCH winding. This voltage is passed to VCCL through an internal regulator with dropout voltage, $V_{DO}$, of 0.5 V, resulting in a VCCL voltage of 12.1 V. As the output voltage increases, the VCCH voltage increases accordingly, and the internal regulator ensures that VCCL is kept at 10 V.

As the output voltage continues to rise, the VCCL aux winding voltage eventually exceeds $V_{REG}$, 10 V typical, and back−biases the internal regulator, thus disabling it. Figure 6 shows the simplified $V_{CC}$ management block.

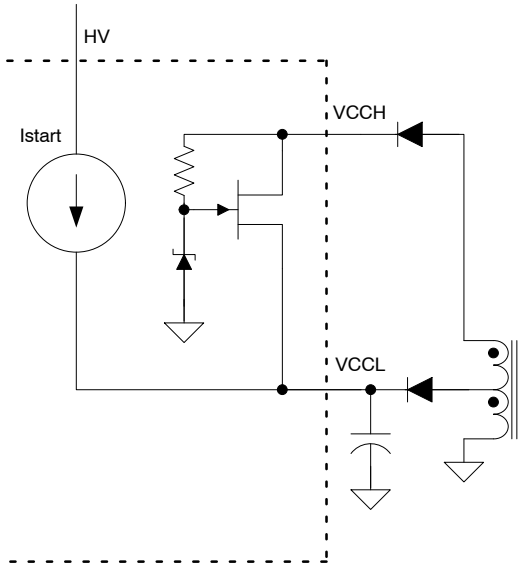



**Figure 6. Simplified $V_{CC}$ Management Circuit**

## DRIVER

The NCP1345 maximum supply voltage, $V_{CC(MAX)}$, is 40 V. Typical high−voltage MOSFETs have a maximum gate voltage rating of 20 V. The DRV pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$ is typically 12 V with a maximum limit of 14 V.

### Adaptive Gate Drive

Due to the loss of valley switching during frequency foldback, the output rectifier can be subjected to large voltage spikes during the primary switch turn−on. The NCP1345 includes special circuitry to reduce the driver turn−on strength during frequency foldback, and thus reduce the severity of the secondary voltage spike. Figure 7 shows the operation of the adaptive gate drive.

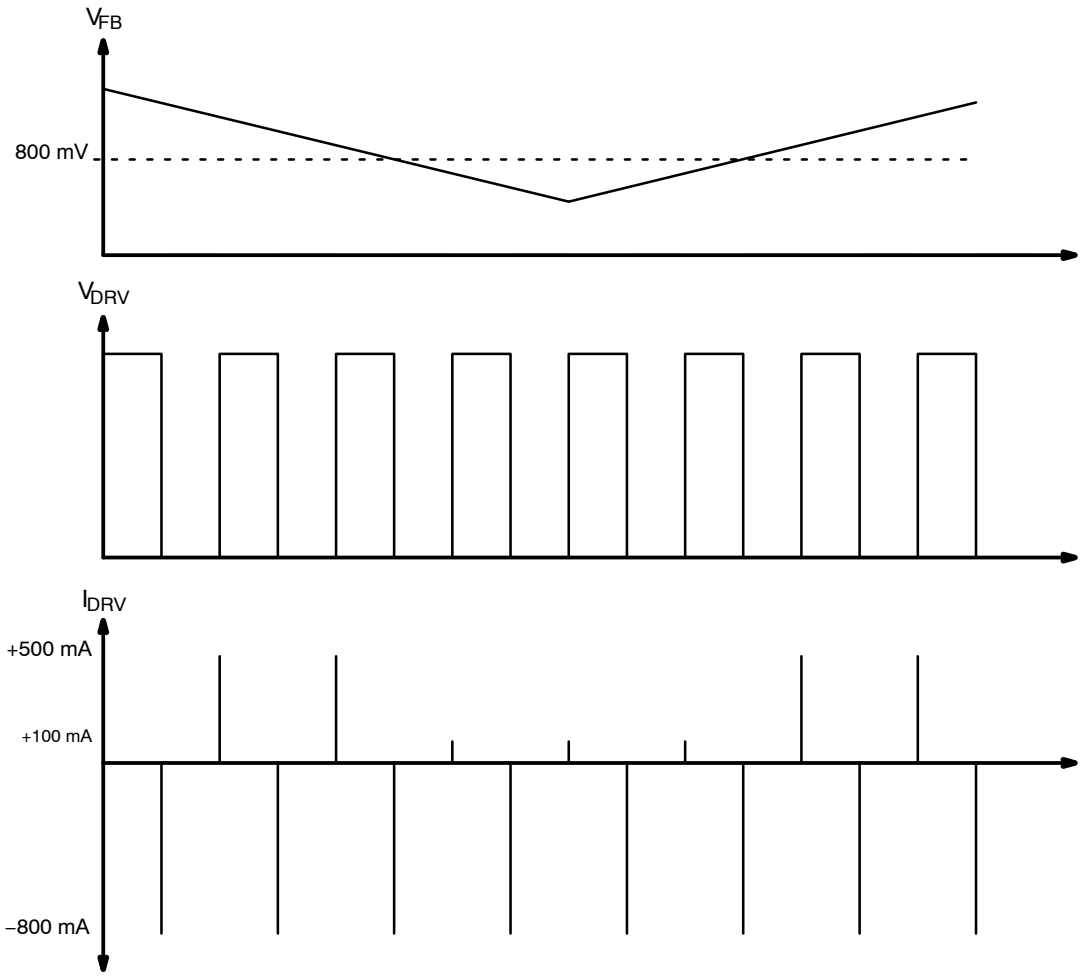



**Figure 7. Adaptive Gate Drive Waveforms**

## FEEDBACK INTERFACE

### Option 1: Register Pullup

The 1st (default) option will be a resistor pullup, voltage controlled architecture as shown in Figure 8. In this architecture the FB pin is supplied by a 5 V rail through a pullup resistor, $R_{FB}$. The default value of $R_{FB}$ in this architecture is 20 kΩ and there will be IPT options for $R_{FB}$ of 400 kΩ. In addition to the pullup resistor, a current source $I_{FB}$ in parallel with $R_{FB}$, can be enabled via IPT options. The purpose of this current source is to increase the dynamic range when using an external pull down resistor. By default, $I_{FB}$ is disabled, however it can be set via IPT options to 100 μA. The FB pin open circuit voltage, $V_{FB(open)}$, is specified with a typical value of 5 V.

Internally the voltage at the FB pin divided down by a 4:1 voltage divider. The voltage directly at the FB (atop the 4:1 divider) is fed into the skip and valley comparators while the divided down signal is fed into the PWM comparator and the current limit comparator.

The resistor pullup is a conventional voltage controlled architecture which translates the error signal communicated through the optocoupler into an error voltage that controls the duty cycle of the SMPS. In this architecture, a capacitor to GND is placed in parallel to the collector of the optocoupler to control the location of the optocoupler pole. Due to the resistance of $R_{FB}$, the optocoupler pole will typically be in the range of 2 kHz to 4 kHz which limits the closed loop bandwidth of the SMPS in the range of 1 – 2 kHz. The capacitor placed in parallel to the collector of the optocoupler will typically be in the range of 470 pF to 4.7 nF with 1 nF being a fairly common value.

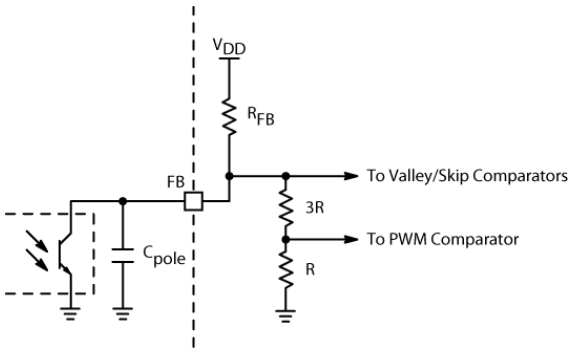



**Figure 8. Pull−up Resistor FB Interface**

### Option 2: Cascode Buffer High BW Architecture

The 2nd option for the FB pin interface will be a Cascode buffer, current controlled architecture and is shown in Figure 9.

In this architecture, the collector of the optocoupler interfaces with a voltage clamp, $V_{clamp}$, set by the cascode buffer. The minimum value of the voltage clamp is specified at 2 V when tested at a pull down current of 150 μA. The clamp voltage set by the cascode transforms the conventional voltage controlled architecture into a current controlled architecture as the FB pin voltage remains approximately constant regardless of the collector current through the optocoupler. The benefit of this architecture is that the effective impedance seen by the collector of the optocoupler is greatly reduced when compared to the voltage controlled architecture, allowing the SMPS to achieve a higher closed loop bandwidth. The specified dynamic resistance for the FB pin, $R_{dyn(FB)}$, ranges from 850 Ω to 1.15 kΩ when the pulldown current is swept from 5 μA to 250 μA. With the specified dynamic resistance, it is also still possible for the designer to place a capacitor across the collector to GND to set a high frequency pole for stabilization of the SMPS control loop. Typical capacitor values will be in the range of 470 pF – 47 nF. A small 25 μA offset current, $I_{FB(offset)}$, is added to ensure stability of the FB pin.

An additional capacitor, $C_{filter}$, is placed after $R_{FB}$ for noise filtering. This capacitor is 10 pF, typical. It can also be disconnected via IPT option.

Internal to the cascode interface is a pair of current mirrors which sense the optocoupler collector current and transpose an image of the collector current to the pullup resistor, $R_{FB}$. The pair of current mirrors also ensures that the polarity of the error signal communicated though the optocoupler has the intended effect of increasing or decreasing the pulse width of the primary controlled switch in the SMPS.

In the voltage controlled architecture, the midband gain of the AC open loop transfer function is determined by $R_{FB}$. However, in the current controlled architecture, the midband gain is determined by $R_{FB(app)}$, the apparent pullup resistance.

As previously mentioned, there will be IPT options for $R_{FB}$. In order to reduce current consumption, $R_{FB}$ is set to the maximum option of 400 kΩ. The internal current divider is then configured to provide a default $R_{FB(app)}$ value of 20 kΩ, with IPT options of 20 kΩ up to 320 kΩ in 20 kΩ increments.

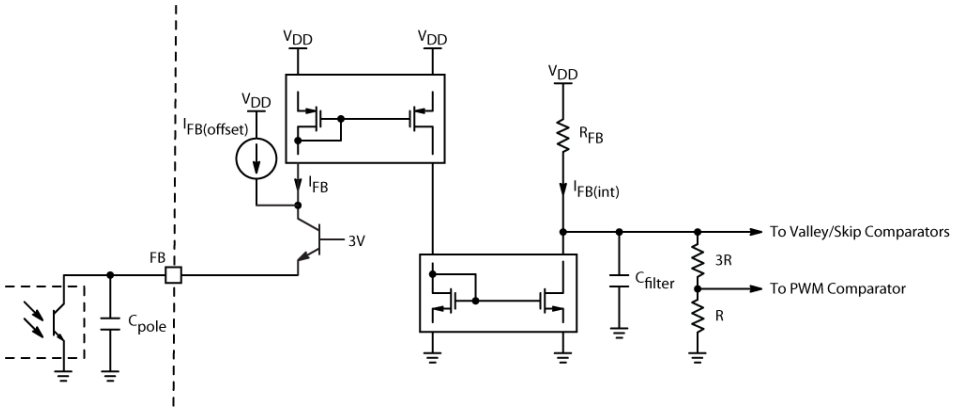



**Figure 9. Cascode Buffer High Bandwidth Feedback Interface**

## ON TIME CONTROL

### Peak Current Control

The NCP1345 is a peak current−mode controller, thus the FB voltage sets the peak current flowing in the transformer and the MOSFET. This is achieved by sensing the MOSFET current across a resistor and applying the resulting voltage ramp to the non−inverting input of the PWM comparator through the CS pin. The current limit threshold is set by applying the FB voltage divided by $K_{FB}$ (typically 4) to the inverting input of the PWM comparator. When the current sense voltage ramp exceeds this threshold, the output driver is turned off, however, the peak current is affected by several functions (see Figure 10):

The peak current level is clamped during the soft−start phase. The setpoint is actually limited by a clamp level ramping from 0 to 0.8 V within 4 ms.

In addition to the PWM comparator, a dedicated comparator monitors the current sense voltage, and if it reaches the maximum value, $V_{ILIM}$ (typically 800 mV), the gate driver is turned off and the overload timer is enabled. This occurs even if the limit imposed by the feedback voltage is higher than $V_{ILIM1}$. Due to the parasitic capacitances of the MOSFET, a large voltage spike often appears on the CS Pin at turn−on. To prevent this spike from falsely triggering the current sense circuit, the current sense signal is blanked for a short period of time, $t_{LEB1}$ (typically 275 ns), by a leading edge blanking (LEB) circuit. Figure 10 shows the schematic of the current sense circuit.

The peak current is also limitied to a minimum level, $V_{CS(MIN)}$ (0.2 V, typically). This results in higher efficiency at light loads by increasing the minimum energy delivered per switching cycle, while reducing the overall number of switching cycles during light load.

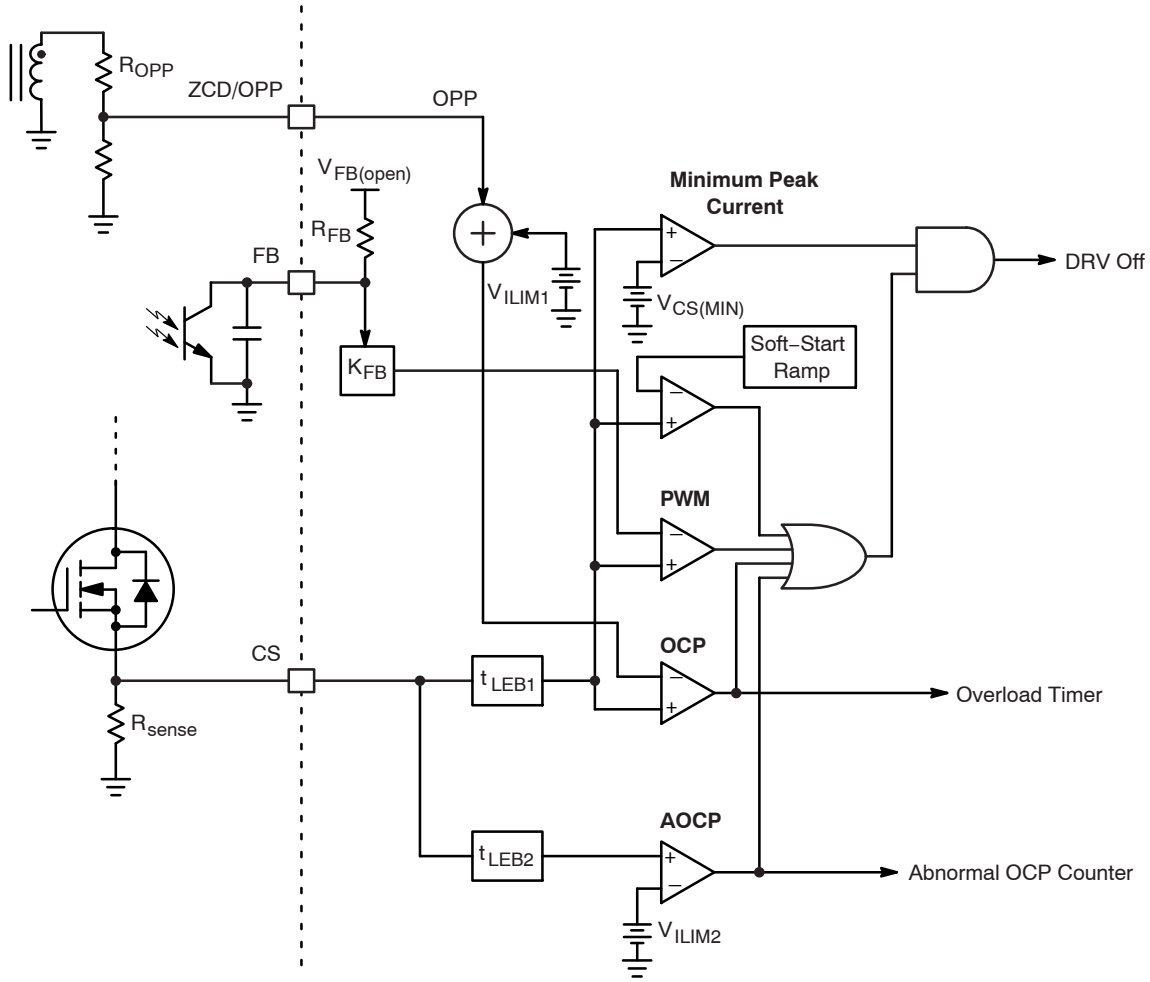



**Figure 10. Peak Current Setpoint**

### Soft−Start

Soft−start is achieved by ramping up an internal reference, $V_{SSTART}$, and comparing it to the current sense signal. $V_{SSTART}$ ramps up from 0 V once the controller initially powers up. The peak current setpoint is then limited by the $V_{SSTART}$ ramp resulting in a gradual increase of the switch current during start−up. The soft−start duration, $t_{SSTART}$, is typically 4 ms.

During startup, demagnetization phases are long and difficult to detect since the auxiliary winding voltage is very small. In this condition, the 6 μs steady−state timeout is generally shorter than the inductor demagnetization period. If it is used to restart a switching cycle, it can cause operation in CCM for several cycles until the voltage on the ZCD pin is high enough to prevent the timer from running. Therefore, a longer timeout period, $t_{tout1}$ (typically 100 μs), is used during soft−start to prevent CCM operation.

### Frequency Jittering

In order to help meet stringent EMI requirements, the NCP1345 features frequency jittering to average the energy peaks over the EMI frequency range. As shown in Figure 12: Jitter Implementation, the function consists of summing a 0 to 50 mV, 250 Hz triangular wave ($V_{jitter}$) with the CS signal immediately before the PWM comparator. This current acts to modulate the on−time and hence the operation frequency.

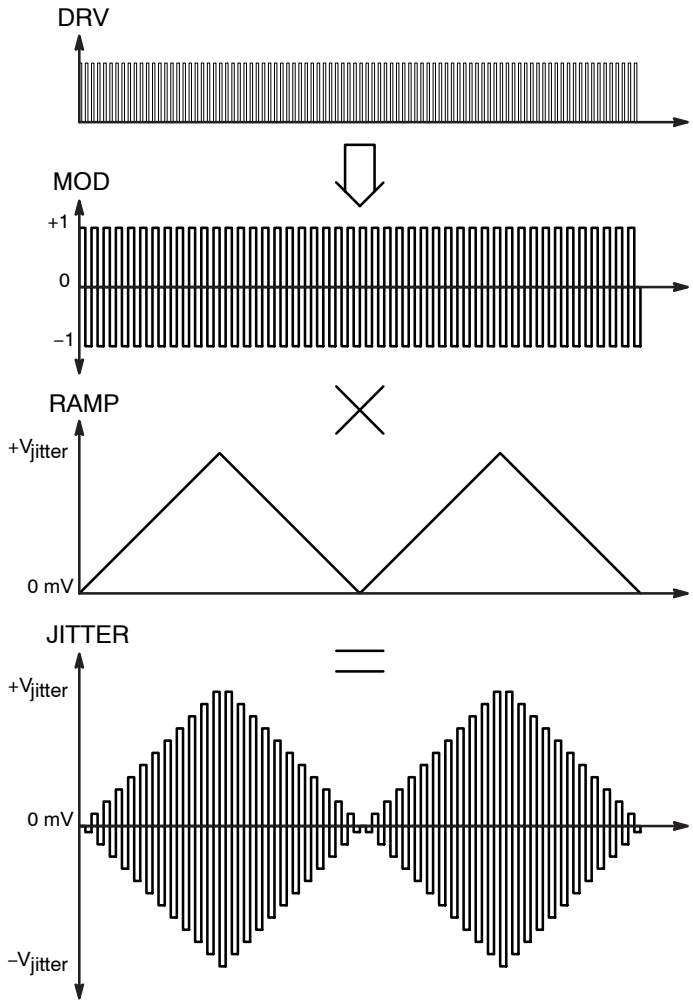



**Figure 11. Jitter Timing**

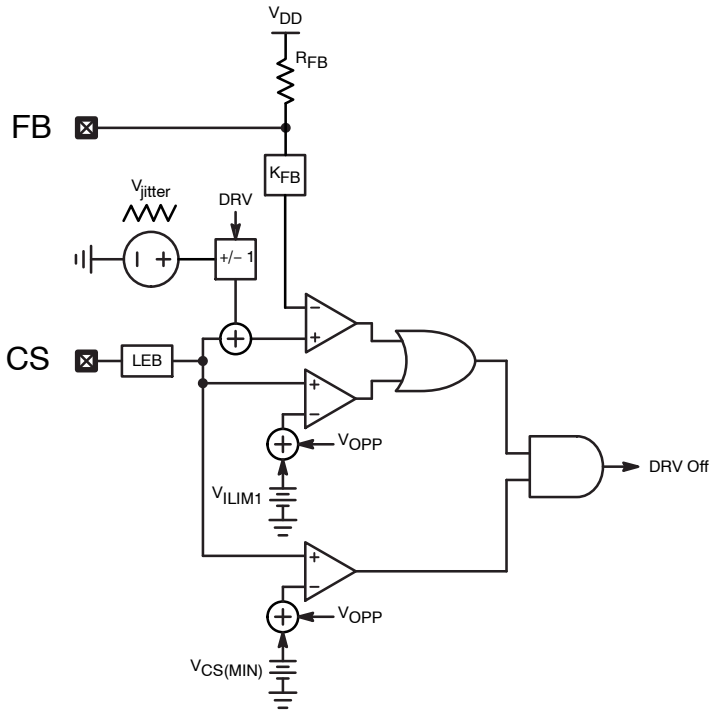



**Figure 12. Jitter Implementation**

Since the jittering function modulates the peak current level, the FB signal would normally attempt to compensate for this effect in order to limit the output voltage ripple, thus cancelling out the effect of the jitter. Therefore, the NCP1345 incorporates a special circuit to alternate the polarity of the jitter at each switching cycle. That is, during each successive switching cycle, the jitter ramp voltage is multiplied by 1 and −1 alternately. This causes the average FB voltage ripple to tend to zero, and removes the cancelling effect.

Due to the minimum peak current, the effect of the jittering circuit will not be seen during frequency foldback mode.

## OFF TIME CONTROL

### Zero Current Detection

The NCP1345 is a quasi−resonant (QR) flyback controller. While the power switch turn−off is determined by the peak current set by the feedback loop, the switch turn−on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized has the benefit of reduced switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance, eventually settling at the input voltage. A QR flyback controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or "valley" to reduce switching losses and electromagnetic interference (EMI).

As shown by Figure 14, a valley is detected once the ZCD pin voltage falls below the demagnetization threshold, $V_{ZCD(trig)}$, typically 55 mV. The controller will either switch once the valley is detected or increment the valley counter, depending on the FB voltage.

### Valley Lockout Operation

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when used by itself, such an approach often causes instabilities since when this clamp is active, the controller tends to jump (or hesitate) between two valleys, thus generating audible noise.

Instead, the NCP1345 also incorporates a patented valley lockout (VLO) circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. This technique extends the QR mode operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency.

The operating valley ($1^{st}$, $2^{nd}$, $3^{rd}$, $4^{th}$, $5^{th}$ or $6^{th}$) is determined by the FB voltage. An internal counter increments each time a valley is detected by the ZCD/OPP Pin. Figure 13 shows a typical frequency characteristic obtainable at low line in a 65 W application.

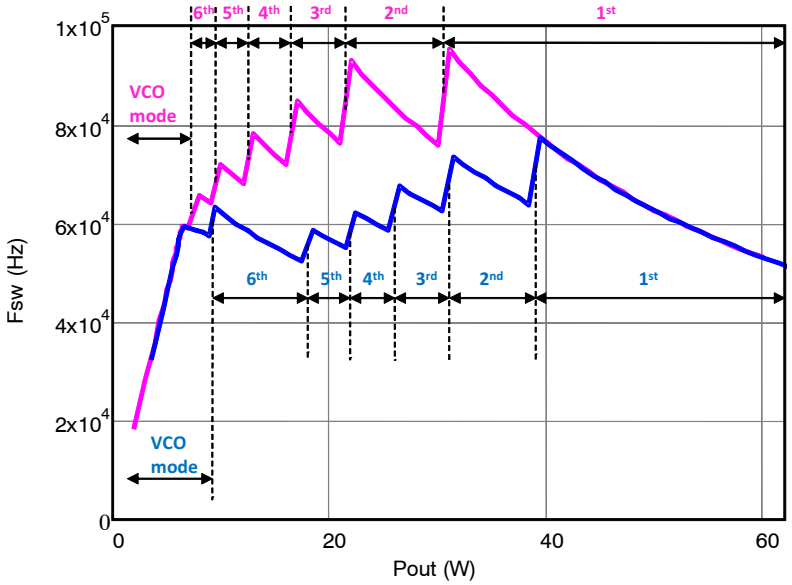



**Figure 13. Valley Lockout Frequency vs. Output Power**

When an "n" valley is asserted by the valley selection circuitry, the controller is locked in this valley until the FB voltage decreases to the lower threshold ("n+1" valley activates) or increases to the "n valley threshold" + 600 mV ("n−1" valley activates). The regulation loop adjusts the peak current to deliver the necessary output power. Each valley selection comparator features a 600 mV hysteresis that helps stabilize operation despite the FB voltage swing produced by the regulation loop.

**Table 6. NCP1345 VALLEY FB THRESHOLDS (TYPICAL VALUES)**

| FB falling | | FB rising | |
|---|---|---|---|
| 1st to 2nd valley | 1.400 V | 2nd to 1st valley | 2.000 V |
| 2nd to 3rd valley | 1.200 V | 3rd to 2nd valley | 1.800 V |
| 3rd to 4th valley | 1.100 V | 4th to 3rd valley | 1.700 V |
| 4th to 5th valley | 1.000 V | 5th to 4th valley | 1.600 V |
| 5th to 6th valley | 0.900 V | 6th to 5th valley | 1.500 V |

*Valley Timeout*

In case of extremely damped oscillations, the ZCD comparator may not be able to detect the valleys. In this condition, drive pulses will stop while the controller waits for the next valley or ZCD event. The NCP1345 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal acts as a substitute for the ZCD signal to the valley counter. Figure 14 shows the valley timeout circuit schematic. The steady state timeout period, $t_{tout2}$, is set at 6 μs (typical) to limit the frequency step.

During startup, the voltage offset added by the OPP diode, $D_{OPP}$, prevents the ZCD Comparator from accurately detecting the valleys. In this condition, the steady state timeout period will be shorter than the inductor demagnetization period causing CCM operation. CCM operation lasts for a few cycles until the voltage on the ZCD pin is high enough to detect the valleys. A longer timeout period, $t_{tout1}$, (typically 100 μs) is set during soft−start to limit CCM operation.

In VLO operation, the number of timeout periods are counted instead of valleys when the drain−source voltage oscillations are too damped to be detected. For example, if the FB voltage sets VLO mode to turn on at the fifth valley, and the ZCD ringing is damped such that the ZCD circuit is only able to detect:

- Valleys 1 to 4: the circuit generates a DRV pulse 6 μs (steady−state timeout delay) after the 4th valley detection.
- Valleys 1 to 3: the timeout delay must run twice, and the circuit generates a DRV pulse 12 μs after the 3rd valley detection.

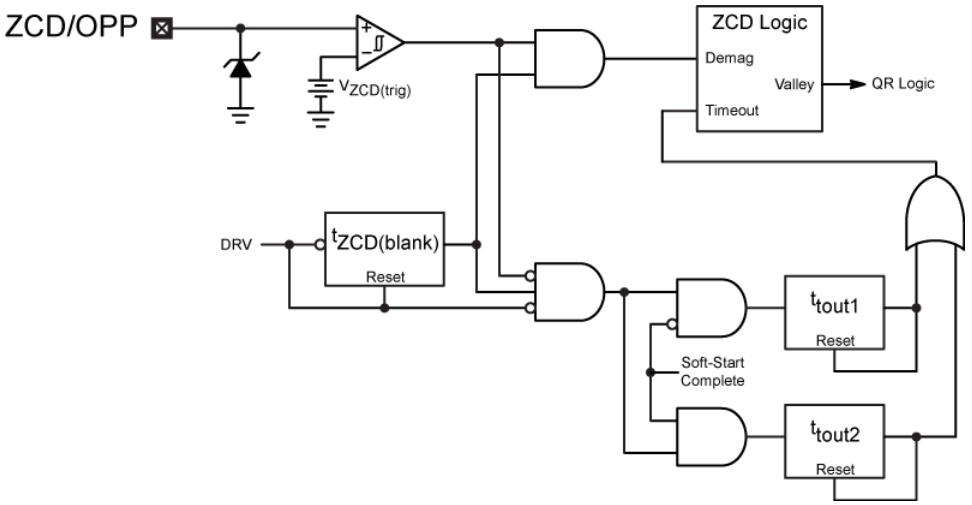



**Figure 14. Valley Timeout Circuitry**

### Maximum Frequency Clamp

The NCP1345 includes a maximum frequency clamp. In all versions, the clamp is available disabled or fixed at 140 kHz. In the 10−pin versions, the clamp can be adjusted via an external resistor from the FMAX Pin to ground. It can also be disabled by pulling the FMAX pin above 3 V.

## LIGHT LOAD MANAGEMENT

### Frequency Foldback with Rapid Frequency Foldback (RFF)

As the output load decreases (FB voltage decreases), the valleys are incremented from 1 to 6. When the sixth valley is reached and the FB voltage further decreases to 0.8 V, the minimum peak current setpoint is increased by $V_{RFF(delta)}$ (0.4 V typically), and the controller enters frequency foldback mode (FF). The increase in peak current serves to force the switching frequency to a much lower value, thus improving the efficiency at light loads. During this mode, the controller regulates the power delivery by modulating the switching frequency.

Once in frequency foldback mode, the controller reduces the switching frequency by adding dead−time after the 6$^{th}$ valley is detected. This dead−time increases as the FB voltage decreases.

The dead−time circuit is designed to add 0 μs dead−time when $V_{FB}$ = 0.8 V and linearly increases the total dead−time to $t_{DT(MAX)}$ (36 μs typical) as $V_{FB}$ falls down to 0.4 V. The minimum frequency clamp prevents the switching frequency from dropping below 25 kHz to eliminate the risk of audible noise. Note that the dead−time is not added until RFF is engaged to ensure valley switching and prevent reduction of the RFF entry load threshold.

In addition to dead−time, the peak current setpoint is linearly reduced as $V_{FB}$ falls down to 0.4 V. This ensures that the peak current is not too high during the lightest loads, and has the effect of reducing the skip entry power level. Figure 15 shows the RFF with respect to the feedback voltage.

To reduce the hysteresis between entering and exiting RFF, the exit threshold is actually slightly below the entry threshold (0.75 V). A 1 ms timer, $t_{RFF}$, is engaged every time RFF is entered or exited to prevent oscillations during the operating point transition. If at any time FB falls to skip mode, or rises to 5$^{th}$ valley, RFF will be immediately exited regardless of the state of the lockout timer. Figure 16 summarizes the VLO to foldback operation with respect to the FB voltage.

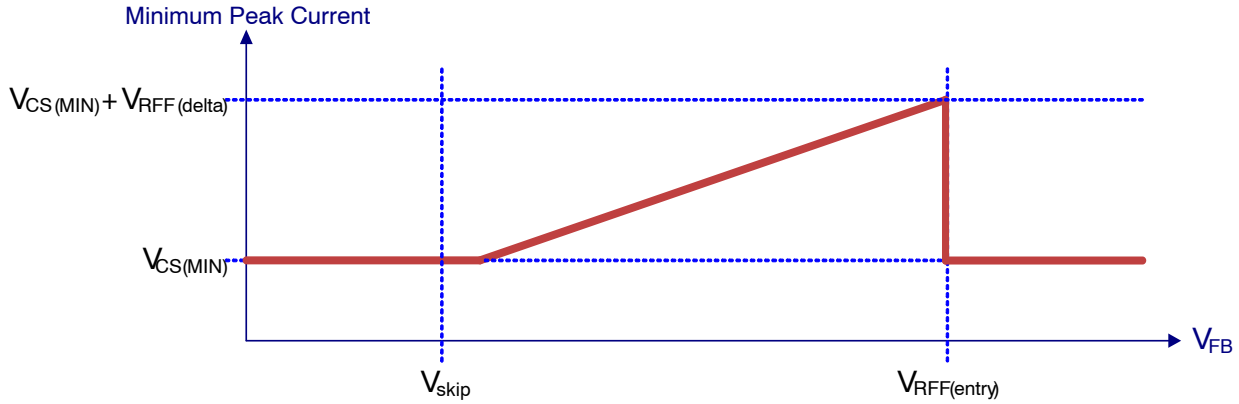



**Figure 15. Rapid Frequency Foldback**

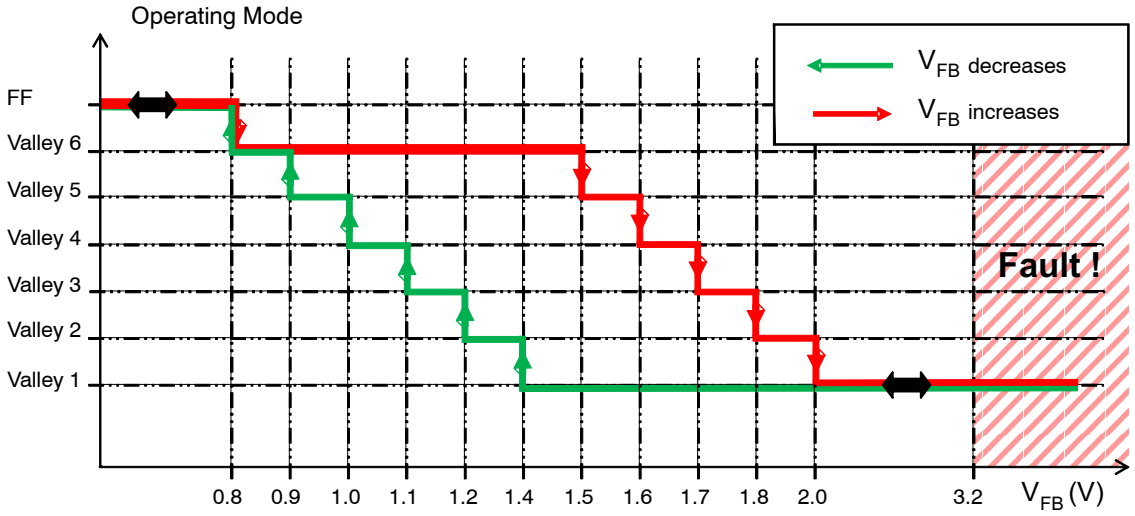



**Figure 16. Valley Lockout Threshold**

### Minimum Frequency Clamp and Skip Mode

As mentioned previously, the circuit prevents the switching frequency from dropping below $f_{MIN}$ (25 kHz typical). When the switching cycle would be longer than 40 μs, the circuit forces a new switching cycle. However, the $f_{MIN}$ clamp cannot generate a DRV pulse until the demagnetization is completed. In other words, it will not cause operation in CCM.

Since the NCP1345 forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled down to zero. Instead, the circuit starts skipping pulses when the FB voltage drops below the skip level, $V_{skip}$, and recovers operation when $V_{FB}$ exceeds $V_{skip}$ + $V_{skip(HYS)}$. This skip−mode method provides an efficient method of control during light loads.

*Quiet−Skip*

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer ($t_{quiet}$) that is activated during Quiet−Skip. The start of the next burst cycle is prevented until this timer has expired.

As the output power decreases, the switching frequency decreases. Once it hits 25 kHz, the skip−in threshold is reached and burst mode is entered – switching stops as soon as the current drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip−exit threshold, drive pulses will resume, but the controller remains in burst mode. At this point, a 1.25 ms timer, $t_{quiet}$, is started together with a count−to−3 counter. The next time the FB voltage drops below the skip−in threshold, drive pulses stop at the end of the current pulse as long as 3 drive pulses have been counted (if not, they do not stop until the end of the 3$^{rd}$ pulse). They are not allowed to start again until the timer expires, even if the skip−exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip−exit is reached after the timer expires, the drive pulses will wait for the skip−exit threshold.

This means that during no−load, there will be a minimum of 3 drive pulses, and the burst−cycle period will likely be much longer than 1.25 ms. This operation helps to improve efficiency at no−load conditions.

In order to exit burst mode, the FB voltage must rise higher than 1 V. If this occurs before $t_{quiet}$ expires, the drive pulses will resume immediately – i.e. the controller won't wait for the timer to expire. Figure 17 provides an example of how Quiet−Skip works.

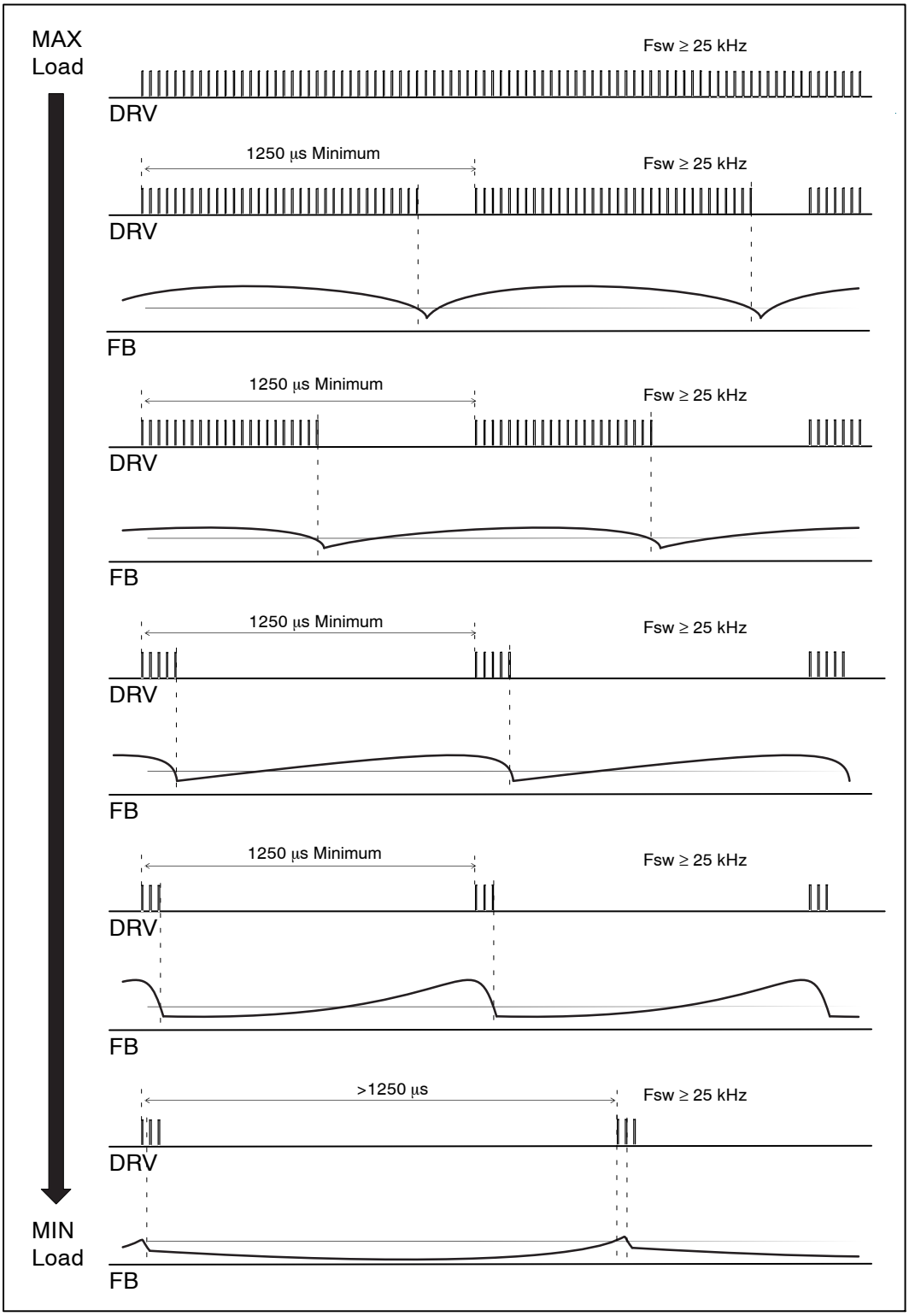



**Figure 17. Quiet−Skip Timing Diagram**

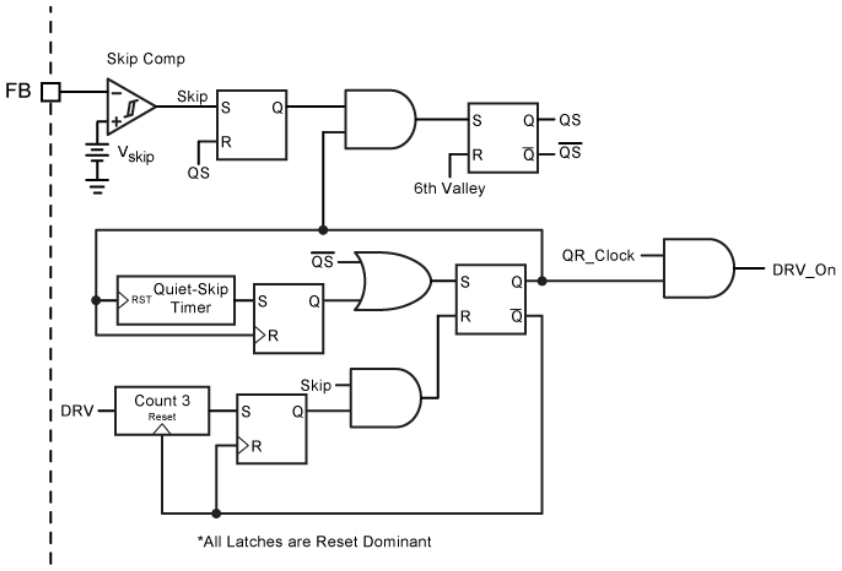



**Figure 18. Quiet−Skip Basic Implementation**

*Auto−Tuning Skip Mode*

In a typical flyback converter, skip mode is entered based on a specific output power. With variable output converters, this means that the output current in skip mode will be much higher at low output voltages. For example, a 60 W adapter that skips at 5 W will enter skip mode at 250 mA when the output is 20 V, but at 1 A when the output is 5 V. In order to prevent excess output ripple at low voltage, the skip threshold is automatically tuned to provide the optimum entry point for each output voltage.

The NCP1345 senses the output voltage via the ZCD pin during the demagnetization phase. It is timed such that the voltage is sensed right as the secondary current reaches zero, and the ZCD voltage begins to swing down, as shown in Figure 19. This ensures that the error from the output rectifier voltage drop is not included. The voltage is then scaled down by an external resistor divider. The scaling factor should be set such that the divider output is 2 V at the maximum nameplate output voltage.

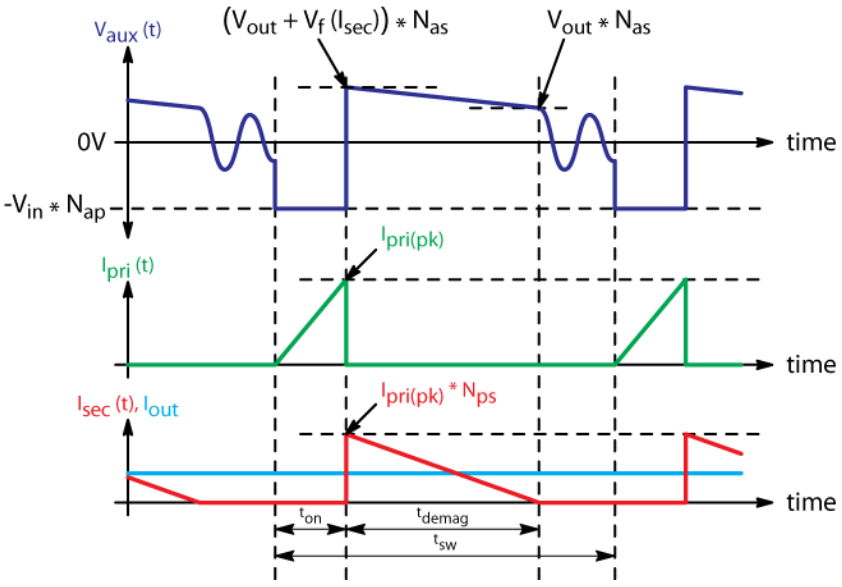



**Figure 19. Output Voltage Sensing Waveforms**

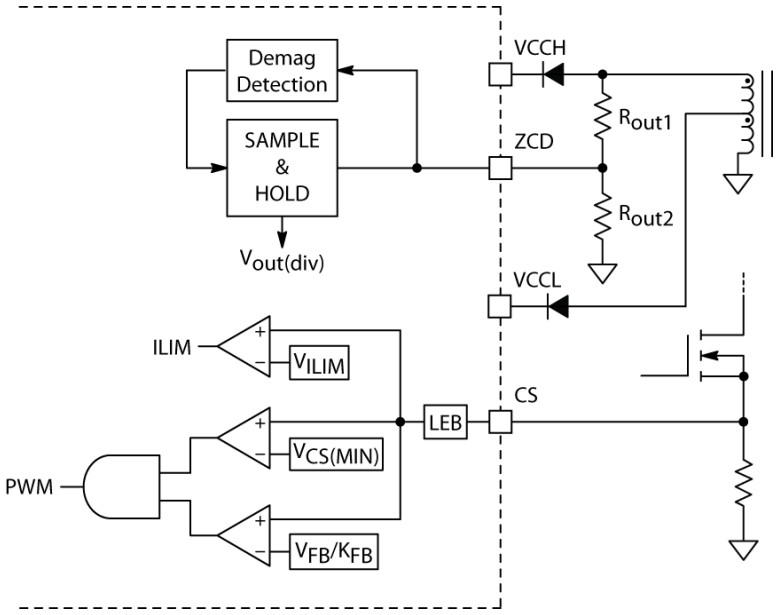



**Figure 20. Auto−Tuning Skip Circuit**

The minimum peak current threshold, $V_{CS(MIN)}$, is modulated based on the sensed output voltage such that

$$V_{CS(MIN)} = \frac{200\ mV}{\sqrt{\frac{V_{out(MAX)}}{V_{out}}}} \qquad \text{(eq. 2)}$$

Where:

- $V_{out(MAX)}$ is the maximum nameplate output voltage, and
- $V_{out}$ is the sensed output voltage

Since Equation 2 is non−linear, the output voltage is sensed at discreet intervals according to Table 7.

**Table 7. $V_{CSMIN}$ BINNING**

| Vout | $V_{ZCD(hi)}$ | BIN# | To | Vs Threshold | | | $V_{CSMIN}$ (mV) | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX |
| ≥20 | 9.75 | 17 | | | | | 180 | 200 | 220 |
| | | | 16to17 | 9 | 9.5 | 10 | | | |
| 19 | 9.25 | 16 | | | | | 175 | 195 | 215 |
| | | | 15to16 | 8.5 | 9 | 9.5 | | | |
| 18 | 8.75 | 15 | | | | | 170 | 190 | 210 |
| | | | 14to15 | 8 | 8.5 | 9 | | | |
| 17 | 8.25 | 14 | | | | | 165 | 185 | 205 |
| | | | 13to14 | 7.5 | 8 | 8.5 | | | |
| 16 | 7.75 | 13 | | | | | 160 | 180 | 200 |
| | | | 12to13 | 7 | 7.5 | 8 | | | |
| 15 | 7.25 | 12 | | | | | 155 | 175 | 195 |
| | | | 11to12 | 6.5 | 7 | 7.5 | | | |
| 14 | 6.75 | 11 | | | | | 145 | 165 | 185 |
| | | | 10to11 | 6 | 6.5 | 7 | | | |
| 13 | 6.25 | 10 | | | | | 141 | 160 | 179 |
| | | | 9to10 | 5.5 | 6 | 6.5 | | | |
| 12 | 5.75 | 9 | | | | | 136 | 155 | 174 |
| | | | 8to9 | 5 | 5.5 | 6 | | | |
| 11 | 5.25 | 8 | | | | | 131 | 150 | 169 |
| | | | 7to8 | 4.5 | 5 | 5.5 | | | |
| 10 | 4.75 | 7 | | | | | 121 | 140 | 159 |
| | | | 6to7 | 4 | 4.5 | 5 | | | |
| 9 | 4.25 | 6 | | | | | 116 | 135 | 154 |
| | | | 5to6 | 3.5 | 4 | 4.5 | | | |
| 8 | 3.75 | 5 | | | | | 106 | 125 | 144 |
| | | | 4to5 | 3 | 3.5 | 4 | | | |
| 7 | 3.25 | 4 | | | | | 102 | 120 | 138 |
| | | | 3to4 | 2.5 | 3 | 3.5 | | | |
| 6 | 2.75 | 3 | | | | | 92 | 110 | 128 |
| | | | 2to3 | 2 | 2.5 | 3 | | | |
| 5 | 2.25 | 2 | | | | | 82 | 100 | 118 |
| | | | 1to2 | 1.5 | 2 | 2.5 | | | |
| 4 | 1.75 | 1 | | | | | 72 | 90 | 108 |
| | | | 0to1 | 1.075 | 1.575 | 2.075 | | | |
| ≤3.3 | 1.4 | 0 | | | | | 63 | 80 | 97 |

## FAULT MANAGEMENT

The NCP1345 contains three separate fault modes. Depending on the type of fault, the device will either latch off, restart when the fault is removed, or resume operation after the auto−recovery timer expires.

### Latching Faults

Some faults will cause the NCP1345 to latch off. These include the abnormal OCP (AOCP), $V_{CC}$ OVP, and the external latch input. When the NCP1345 detects a latching fault, the driver is immediately disabled. The operation during a latching fault is identical to that of a non−latching fault except the controller will not attempt to restart at the next $V_{CC(on)}$, even if the fault is removed. In order to clear the latch and resume normal operation, $V_{CC}$ must first be allowed to drop below $V_{CC(reset)}$ or a line removal event must be detected. This operation is shown in Figure 21.

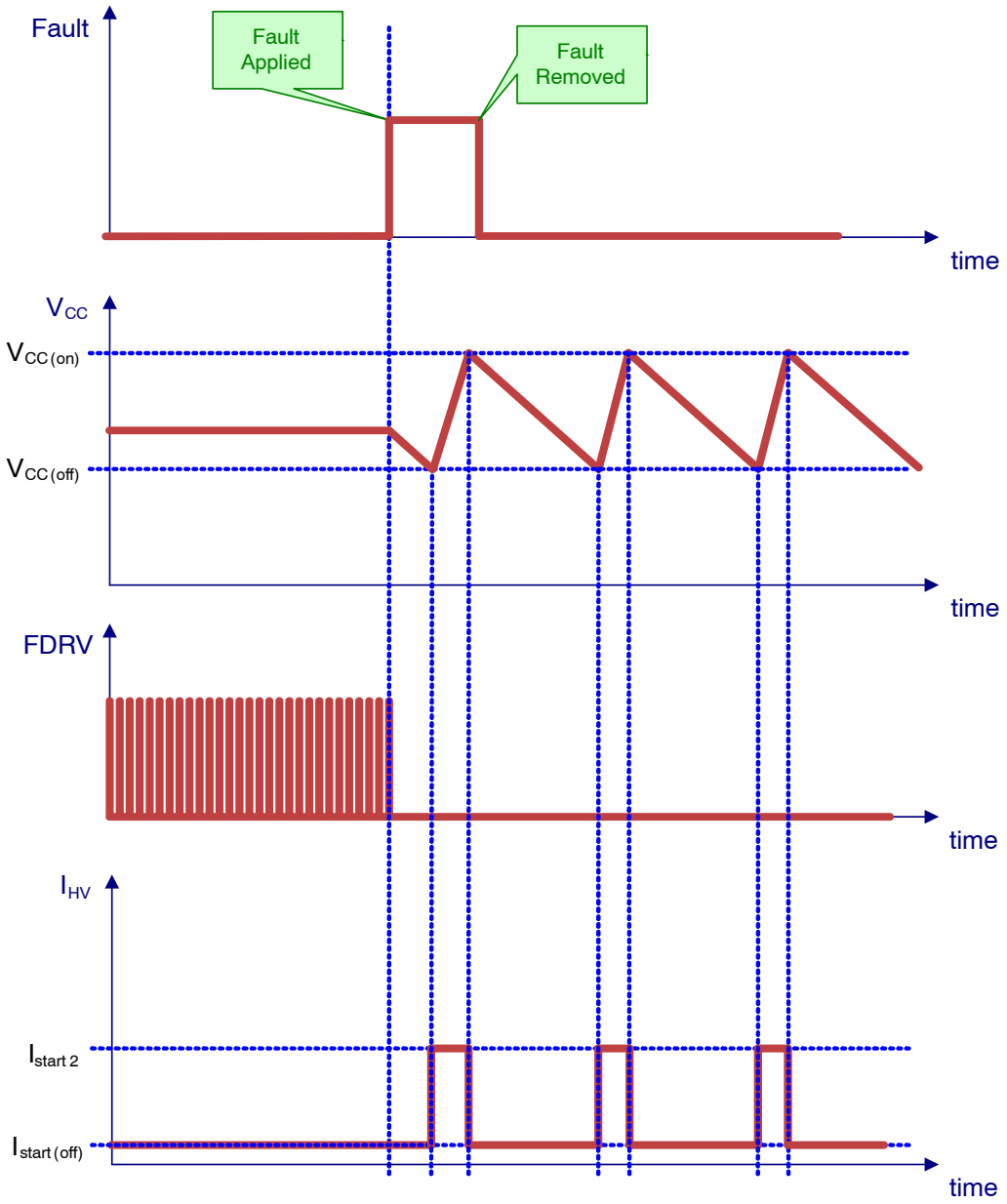



**Figure 21. Operation During Latching Fault**

### Non−Latching Faults

When the NCP1345 detects a non−latching fault (brownout or thermal shutdown), the drivers are disabled, and $V_{CC}$ falls towards $V_{CC(off)}$ due to the IC internal current consumption. Once $V_{CC}$ reaches $V_{CC(off)}$, the HV current source turns on and $C_{VCC}$ begins to charge towards $V_{CC(on)}$. When $V_{CC}$, reaches $V_{CC(on)}$, the cycle repeats until the fault is removed. Once the fault is removed, the NCP1345 is re−enabled when $V_{CC}$ reaches $V_{CC(on)}$ according to the initial power−on sequence, provided $V_{HV}$ is above $V_{BO(start)}$. This operation is shown in Figure 22. When $V_{HV}$ is reaches $V_{BO(start)}$, $V_{CC}$ immediately charges to $V_{CC(on)}$. If $V_{CC}$ is already above $V_{CC(on)}$ when the fault is removed, the controller will start immediately as long as $V_{HV}$ is above $V_{BO(start)}$.

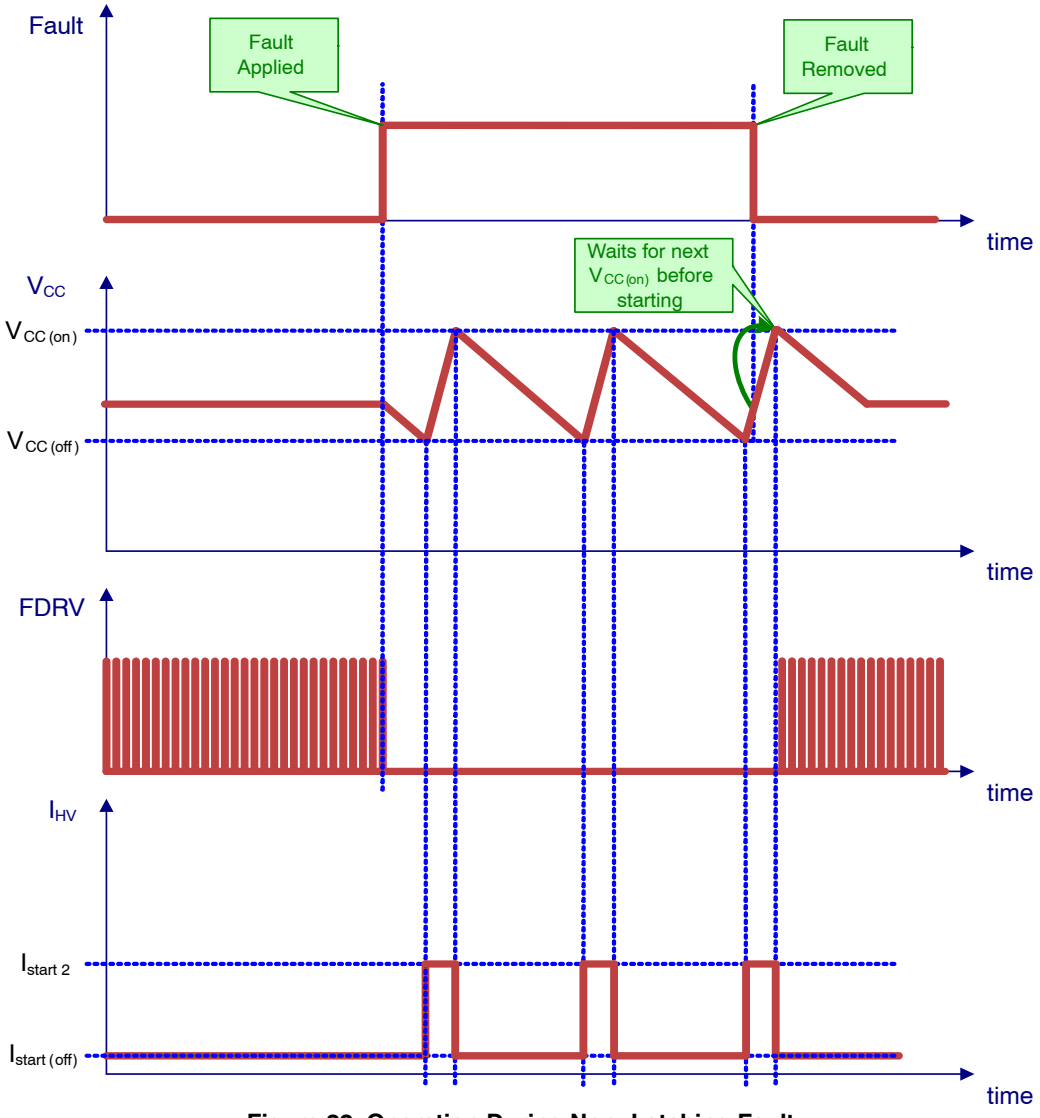



**Figure 22. Operation During Non−Latching Fault**

**Auto−recovery Timer Faults**

Some faults faults cause the NCP1345 auto−recovery timer to run. If an auto−recovery fault is detected, the gate drive is disabled and the auto−recovery timer, $t_{autorec}$ (typically 1.2 s), starts. While the auto−recovery timer is running, the HV current source turns on and off to maintain $V_{cc}$ between $V_{cc(off)}$ and $V_{cc(on)}$. Once the auto−recovery timer expires, the controller will attempt to start normally at the next $V_{CC(on)}$ provided $V_{HV}$ is above $V_{BO(start)}$. This operation is shown in Figure 23.

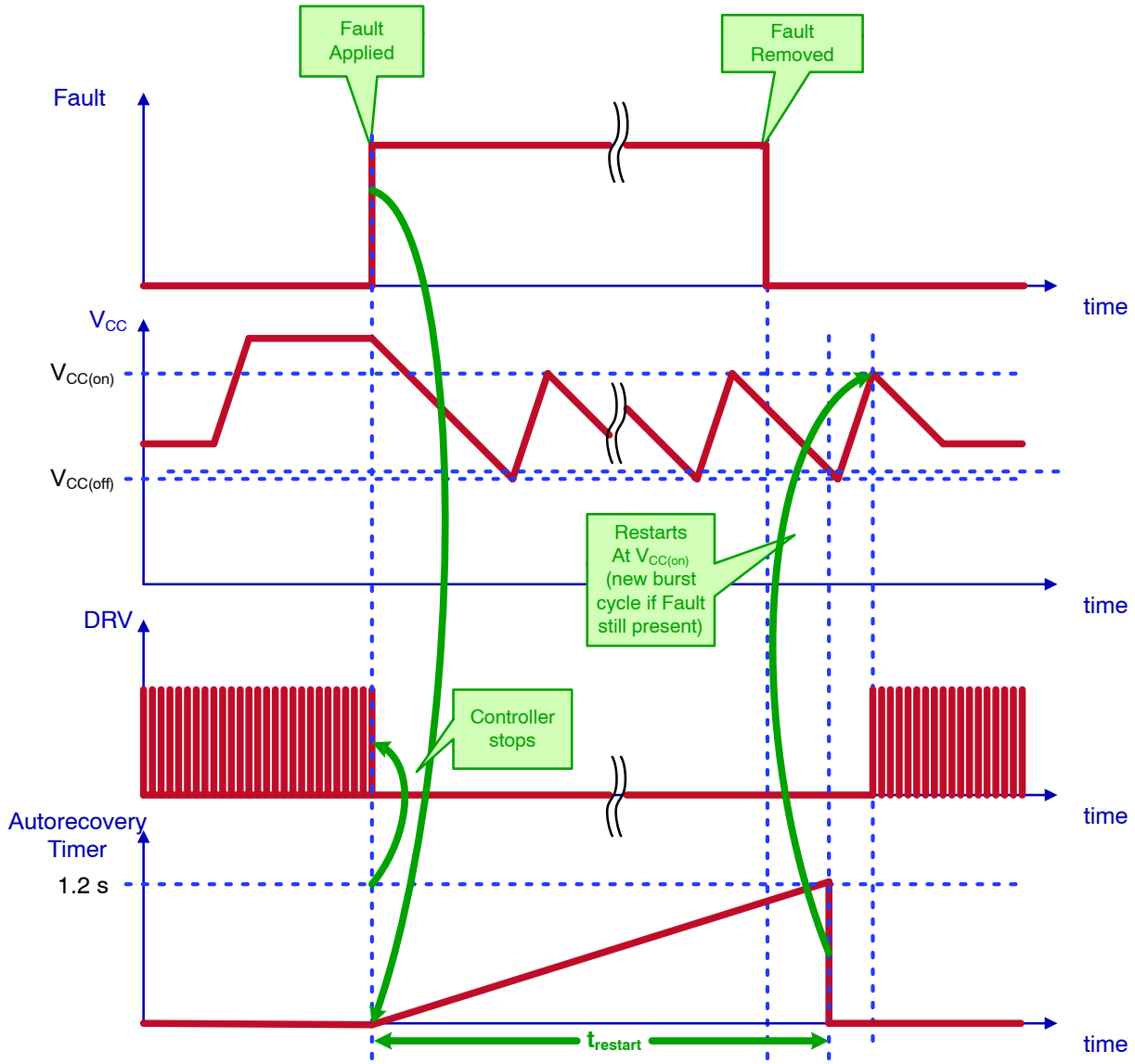



**Figure 23. Operation During Auto−Recovery Fault**

## PROTECTION FEATURES

### Brownout Protection

A timer is enabled once $V_{HV}$ drops below its disable threshold, $V_{BO(stop)}$ (typically 99 V). The controller is disabled if $V_{HV}$ doesn't exceed $V_{BO(stop)}$ before the brownout timer, $t_{BO}$ (typically 54 ms), expires. The timer is set long enough to ignore a two cycle dropout. The timer starts counting once $V_{HV}$ drops below $V_{BO(stop)}$.

Figure 24 shows the brownout detector waveforms during a brownout.

When a brownout is detected, the controller stops switching and enters non−latching fault mode (see Figure 22). The HV current source alternatively turns on and off to maintain $V_{CC}$ between $V_{CC(on)}$ and $V_{CC(off)}$ until the input voltage is back above $V_{BO(start)}$.

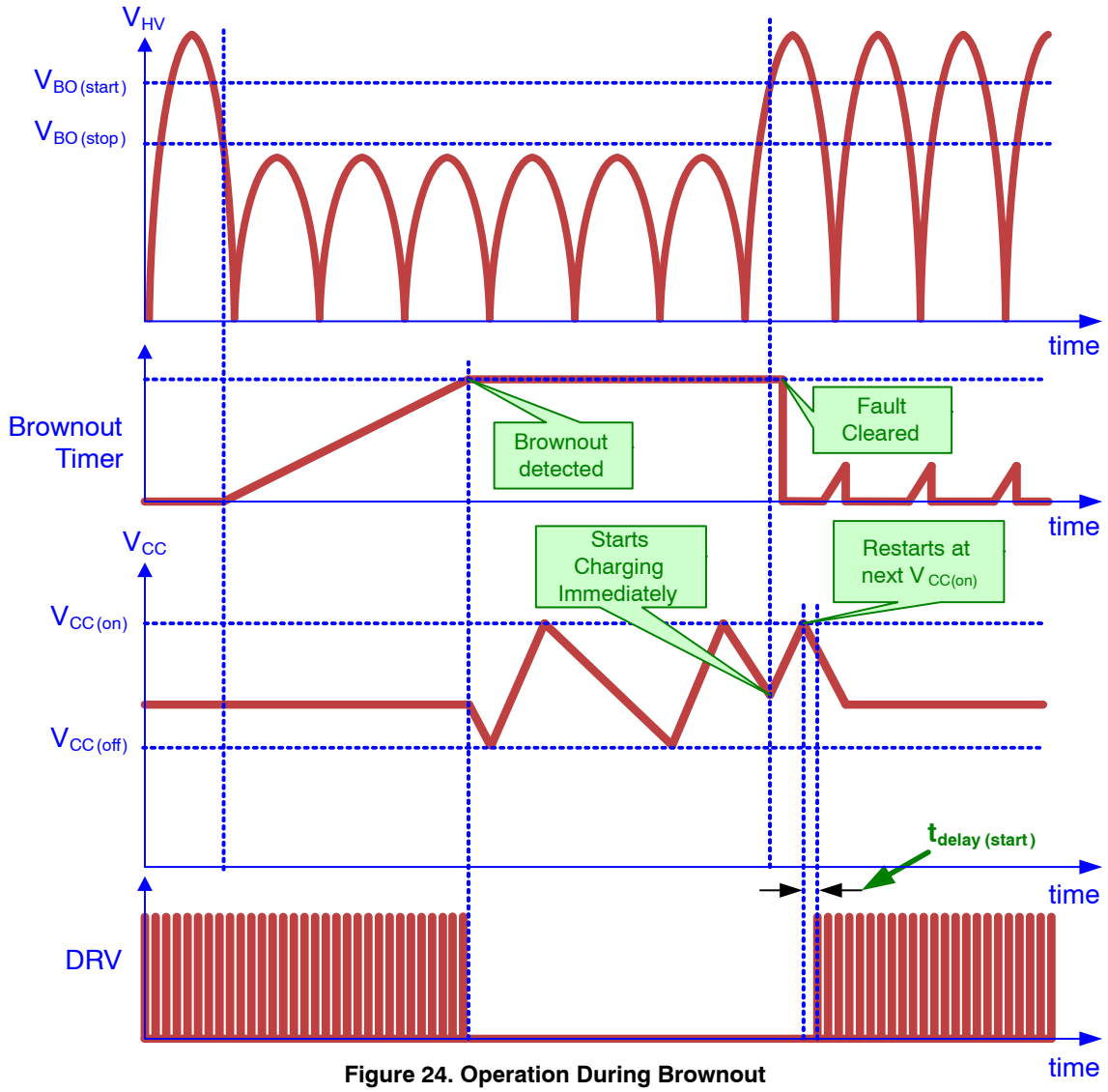



**Figure 24. Operation During Brownout**

### Line Removal and Input Filter Capacitor Discharge Circuitry

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and it is a major contributor of input power losses during light−load and no−load conditions.

The NCP1345 eliminates the need for external discharge resistors by integrating active input filter capacitor discharge circuitry. A novel approach is used to reconfigure the high voltage startup circuit to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

*Line Removal Detection*

The line removal is detected by digitally sampling the voltage present at the HV pin, and monitoring the magnitude of the slope using the circuit depicted in Figure 25.

A timer, $t_{line(removal)}$ (typically 100 ms), starts running when the slope magnitude of the input signal is below a minimum level. The timer is reset by the upslope detection reset timer $t_{HV(up)}$ (typically 14 ms) or the downslope detection reset timer $t_{HV(down)}$ (typically 1 ms).

Once the timer expires, a line removal condition is acknowledged initiating an HV discharge cycle, and disabling the controller. This operation is depicted in Figure 26.

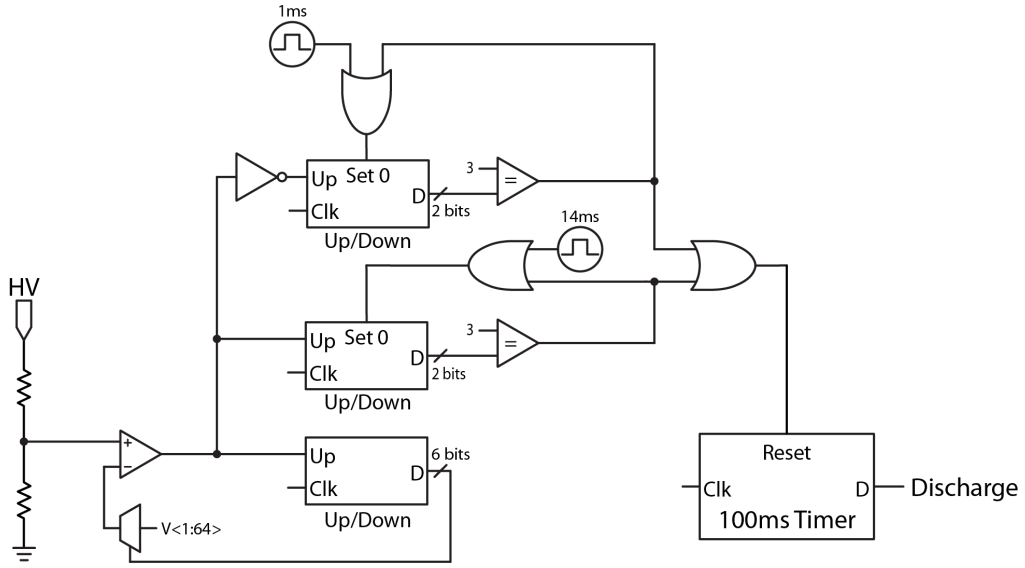



**Figure 25. Line Removal Detection Block Simplified Schematic**

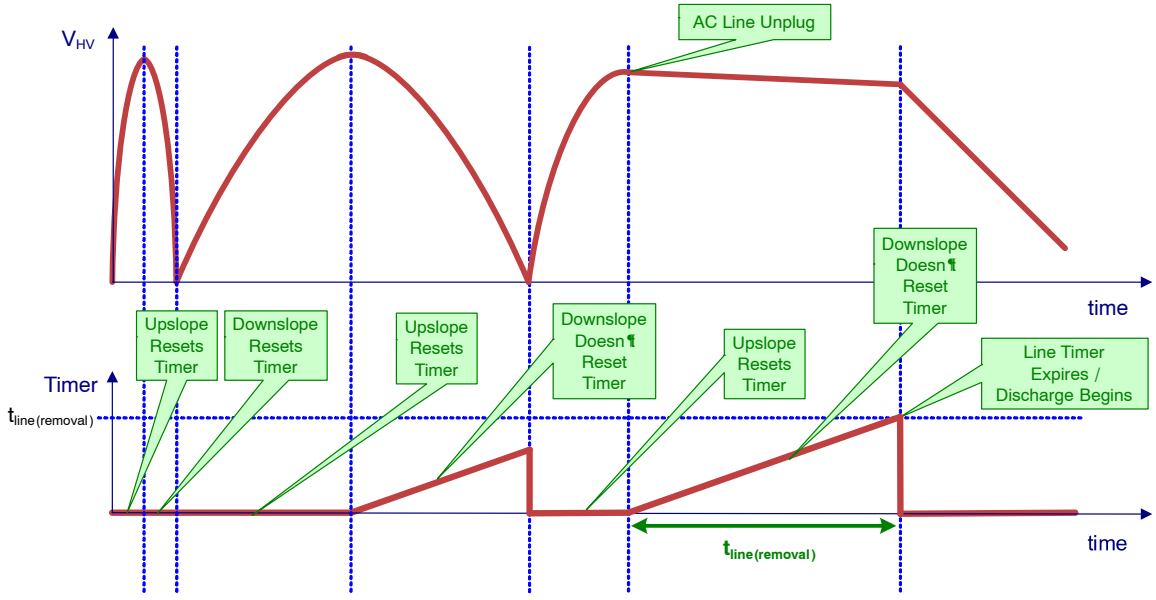



**Figure 26. Line Removal Detection Timing**

*Capacitor Discharge*

During the discharge phase, the discharge current source $I_{HV(disch)}$ (typically 2 mA) is activated. The current source $I_{HV(disch)}$ remains active and constant until $V_{HV}$ drops to $V_{HVdisch(MIN)}$ (typically 30 V). At this point, it begins to pinch off until the discharge phase completes when $V_{HV}$ drops to $V_{HV(disch)}$ (typically 18 V). Once the discharge phase completes, a new start−up cycle commences as normal. This circuit is shown in Figure 27, while the operation is depicted in Figure 28.

**It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to the bulk capacitor.**

In the event that line voltage is reapplied during a discharge phase, the circuit will simply continue to discharge until the line zero crossing occurs, at which point $V_{HV}$ will drop to $V_{HV(disch)}$ and a new start−up cycle will commence.

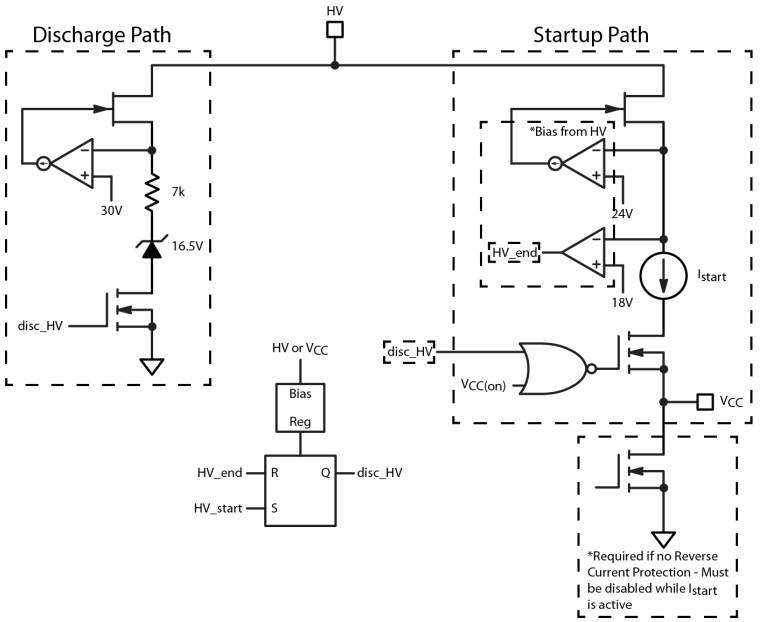



**Figure 27. Discharge Block Simplified Schematic**

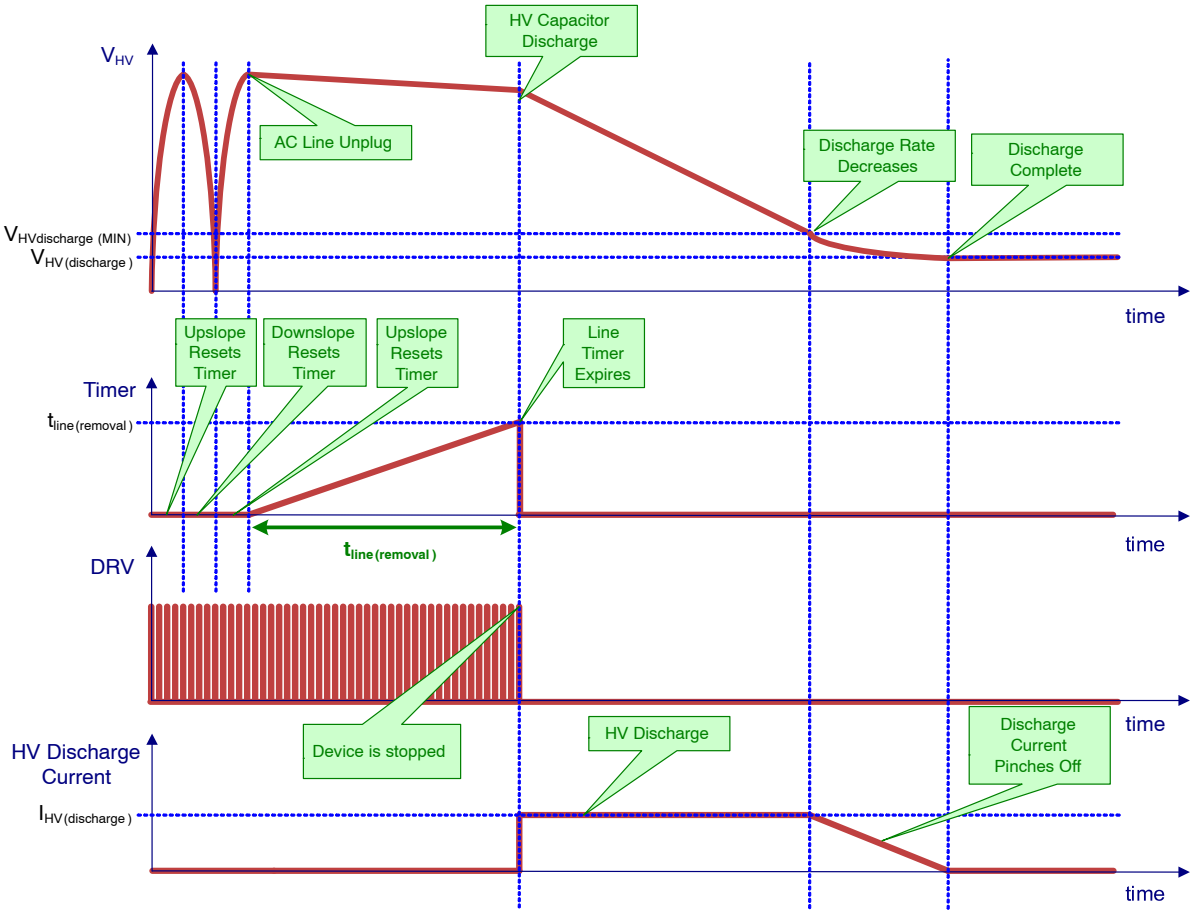



**Figure 28. HV Discharge Timing**

### Dedicated Fault Input

The NCP1345 includes a dedicated fault input accessible via the Fault pin. The controller can be latched by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$ (typically 3.0 V). The controller is disabled if the Fault pin voltage is pulled below the lower fault threshold, $V_{Fault(OTP_in)}$ (typically 0.4 V). The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 29 shows the architecture of the Fault input.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{delay(OVP)}$ and $t_{delay(OTP)}$, are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

*OVP*

An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$), i.e., approximately 1 mA.

The upper fault threshold is intended to be used for an overvoltage fault using a zener diode and a resistor in series from the auxiliary winding voltage. The controller is latched once $V_{Fault}$ exceeds $V_{Fault(OVP)}$.

Once the controller is latched, it follows the behavior of a latching fault according to Figure 21 and is only reset if $V_{CC}$ is reduced to $V_{CC(reset)}$, or X2 discharge is activated. In the typical application these conditions occur only if the ac voltage is removed from the system.

*OTP*

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source, $I_{Fault(OTP)}$ (typically 45.5 μA), generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP_in)}$.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{Fault(OTP)}$. This current source is enabled once $V_{CC}$ reaches $V_{CC(on)}$. A filter capacitor is typically connected between the Fault and GND pins. This will result in a delay before $V_{Fault}$ reaches its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during soft−start.

Options Bxxxx and Dxxxx E latch−off the controller after an overtemperature fault is detected according to Figure 21. In Options Axxxx and Cxxxx, the controller is re−enabled once the fault is removed such that $V_{Fault}$ increases above $V_{Fault(OTP_out)}$, the auto−recovery timer expires, and $V_{CC}$ reaches $V_{CC(on)}$ as shown in Figure 23.

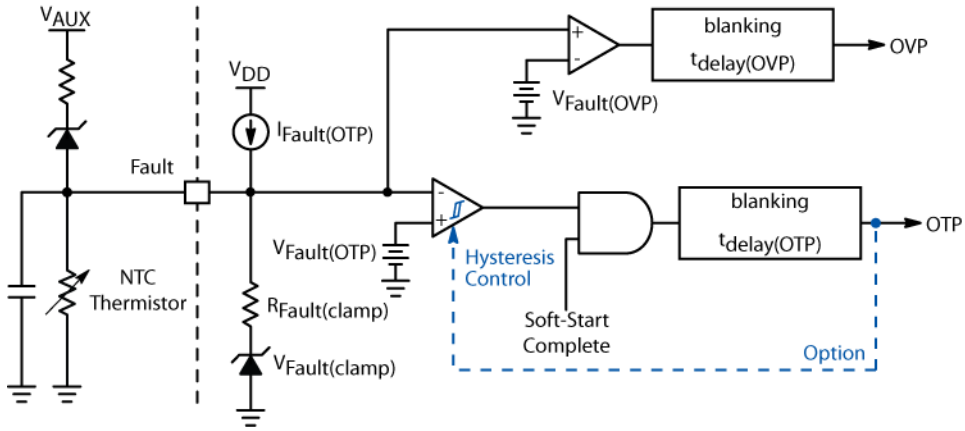



**Figure 29. Fault Pin Internal Schematic**

### Overpower Protection

The peak value of the AC line input voltage is sensed by the HV Pin, and internally scaled down to a smaller level for OPP. The OPP signal is then added to each of the comparators − ILIM1, CS(MIN), and Iout(limit).

The ZCD pin has 3 functions. The primary function is to detect the demagnetization of the transformer. The second function is to set the OPP gain via external resistor Ropp. During start−up, a 20 μA current is sourced from the ZCD pin to generate a voltage across the Ropp resistor. The voltage across the Ropp resistor determines the maximum possible OPP amount that will be added. The typical values of OPP vs. $R_{OPP}$ for given input voltages are shown in Figure 30.

The third function is to sense the output voltage during the drive off−time, and route it to the CS(MIN) comparator. During operation, an internal 1k resistor is connected in parallel with the Ropp resistor to create a 2:1 ratio for output voltage sensing. A current source provides error correction over the output voltage range. This is shown in Figure 31.




**Figure 30. OPP Voltage vs. $R_{OPP}$ for Different Input Voltages**

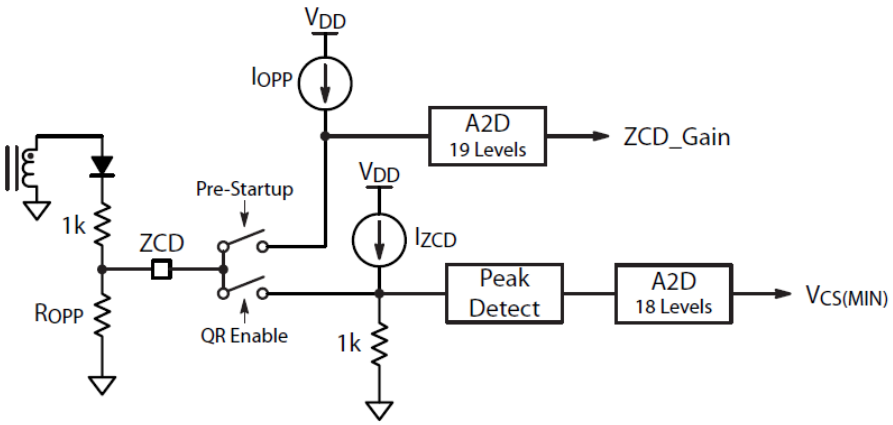



**Figure 31. OPP Programming Block**

### Overload Protection

The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The overload timer duration, $t_{OVLD}$, is typically 160 ms. When the overload timer expires, the controller detects an overload condition does one of the following:

- The controller latches off or
- Enters a safe, low duty−ratio auto−recovery mode.

Figure 32 shows the overload circuit schematic, while Figure 33 and Figure 34 show operating waveforms for latched and auto−recovery overload conditions.

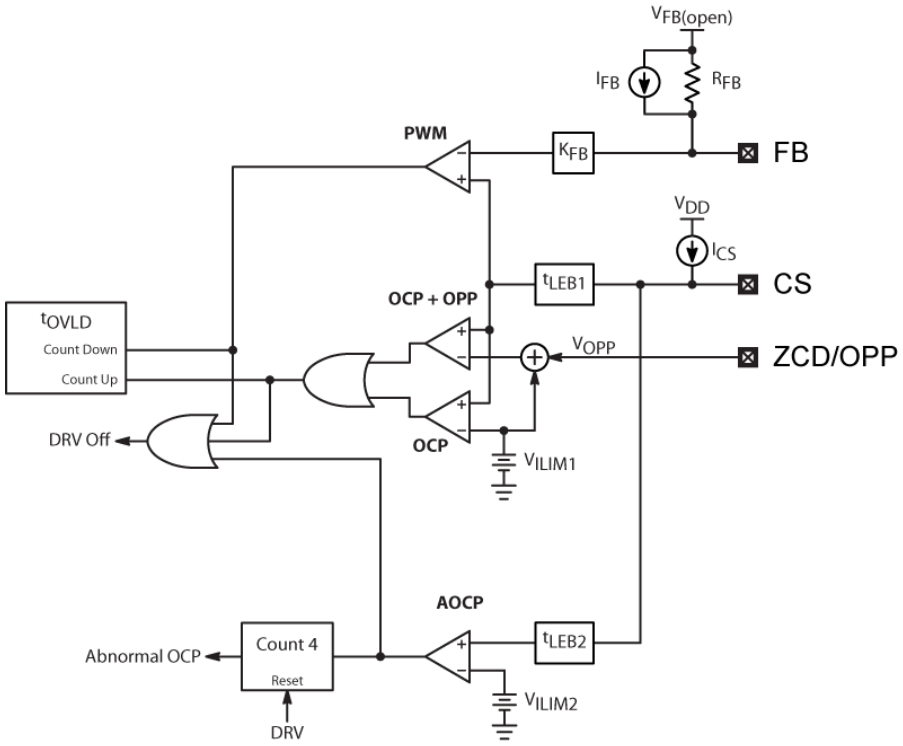



**Figure 32. Overload Circuitry**

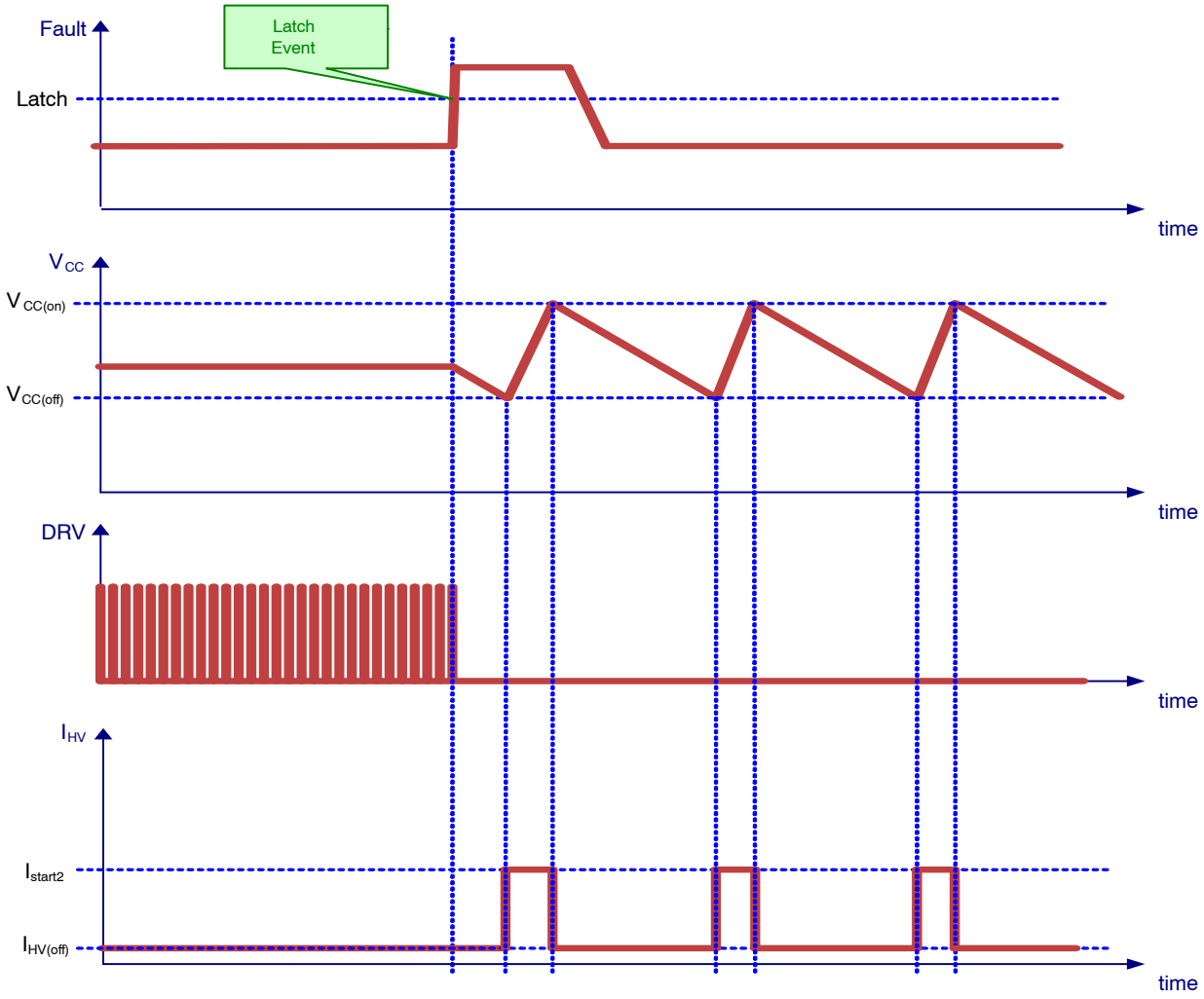



**Figure 33. Latched Overload Operation**

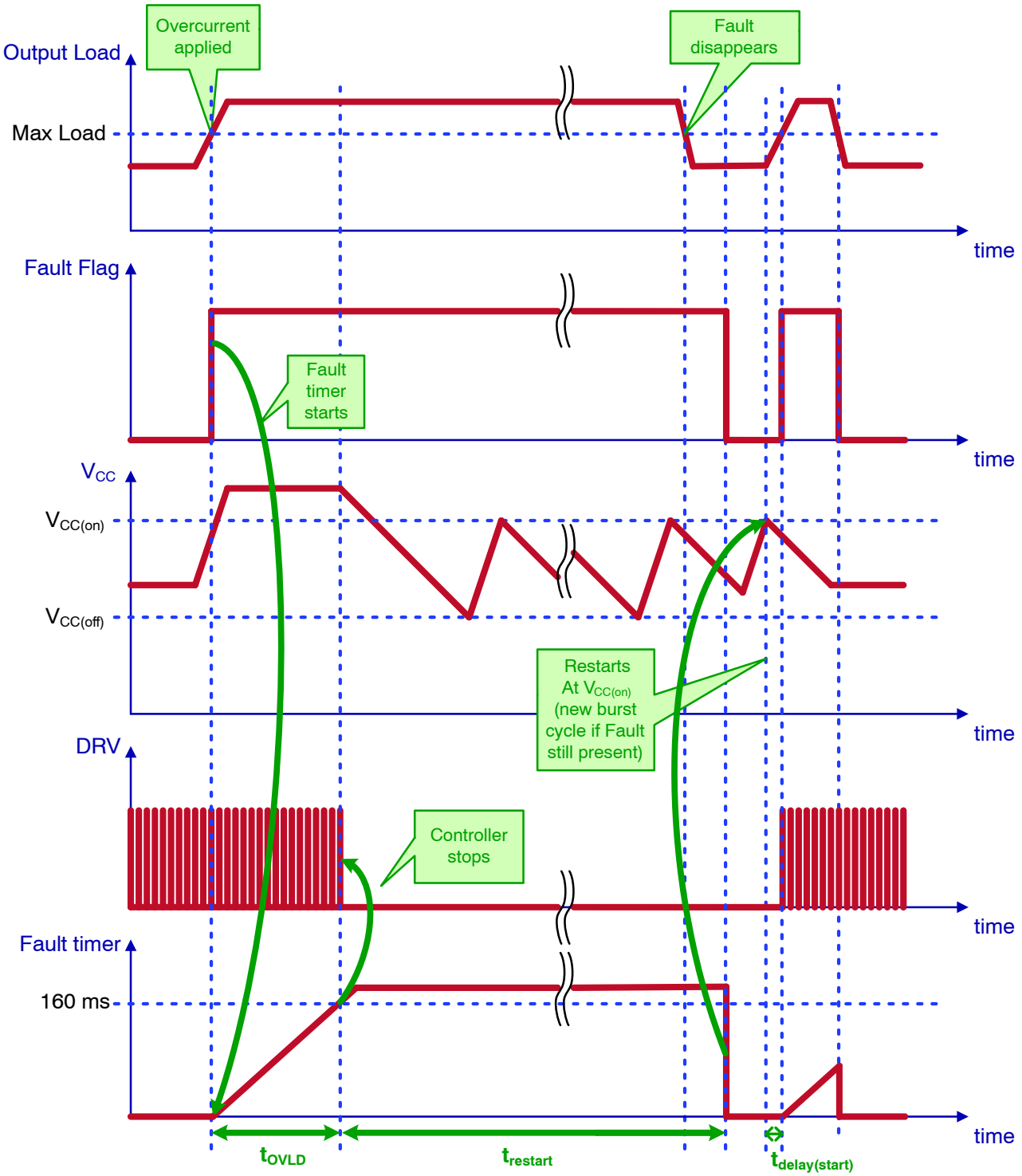



**Figure 34. Auto−Recovery Overload Operation**

**Output Current Limit**

Some regulations such as that for a Limited Power Source (LPS) require the output current and power to be limited during all conditions. In particular, LPS requires that the output power must be limited to 100 W, and the output current to 8 A after 5 seconds at all times, including during a single fault condition.

In order to maintain an output current limit of 8 A at low output voltages, the NCP1345 incorporates a special auto−tuning output current limit circuit.

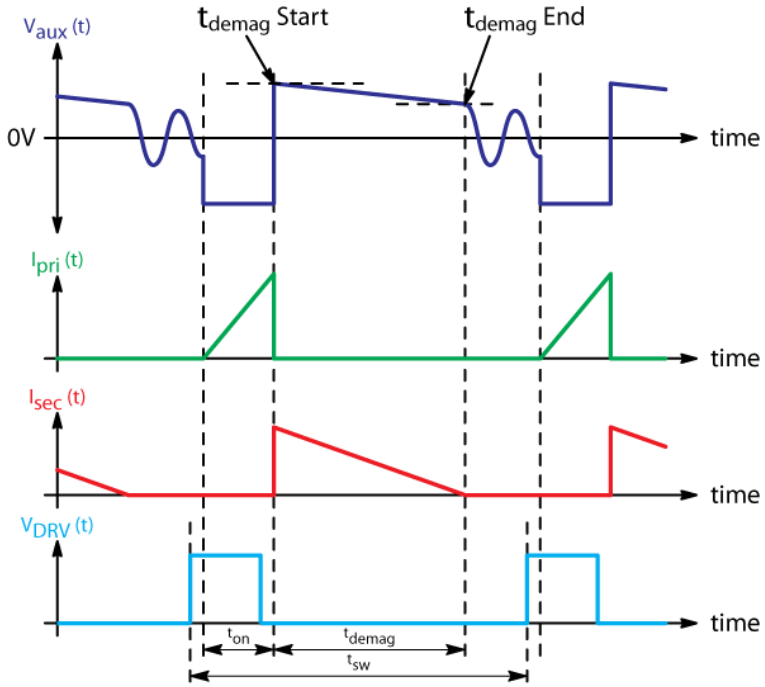



**Figure 35. Typical Flyback Current Waveforms**

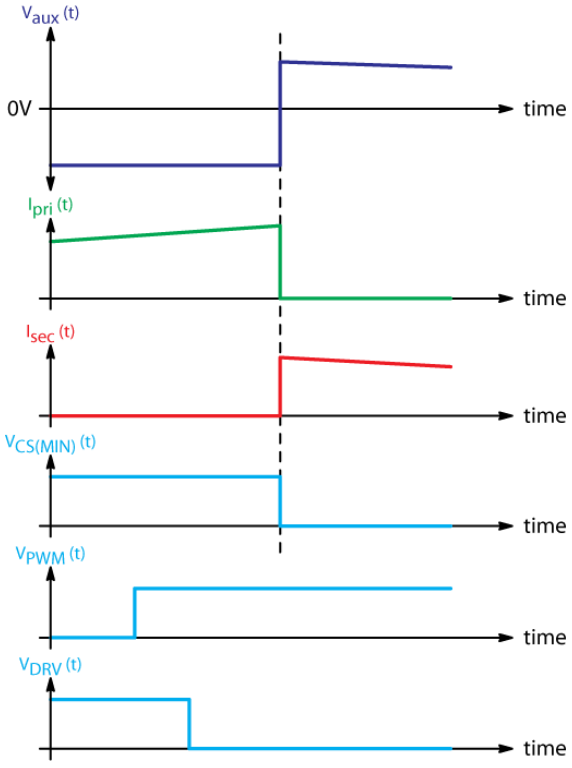



**Figure 36. Detailed View if Demagnetization Starting Point**

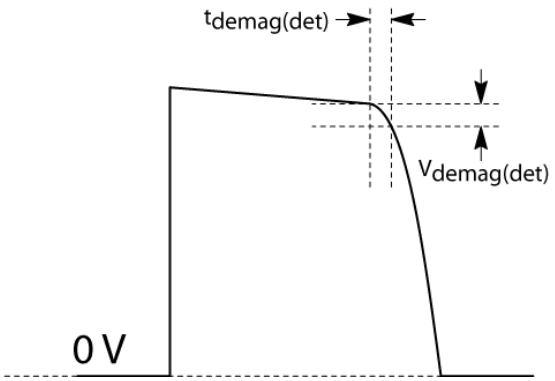



**Figure 37. Detailed View if Demagnetization Ending Point**

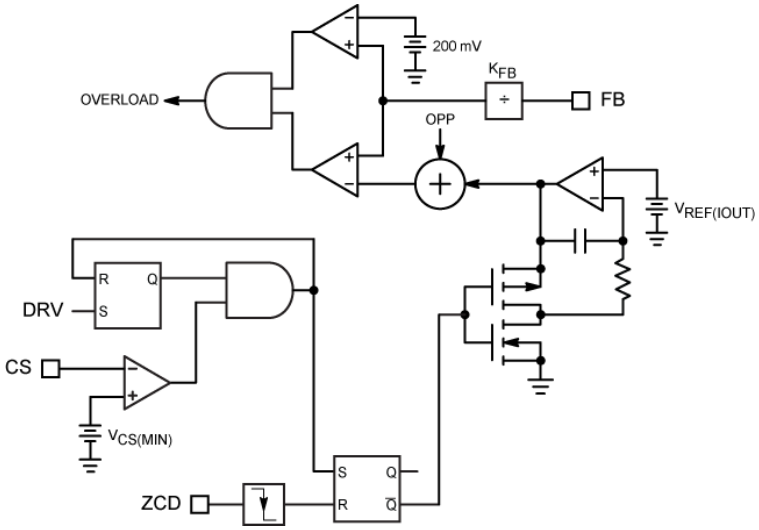



**Figure 38. Output Current Limit Schematic**

When measuring the demagnetization time, it is important to accurately sense the beginning and end of the demagnetization phase. The beginning of the demagnetization phase is not when the DRV signal goes low, but rather when the primary switch turns off. Thus, it is best to detect the demagnetization starting point by monitoring the CS Pin, and waiting for it to fall below the $V_{CS(MIN)}$ threshold. Figure 35 Typical Flyback Current Waveforms shows the beginning and ending point of the demagnetization phase, while Figure 36 shows a detailed view of the demagnetization starting point, including both internal and external propagation delays.

Figure 37 shows a detailed view of the demagnetization ending point. The ending point is when the ZCD Pin voltage suddenly drops the amount $V_{demag(det)}$, typically 150 mV. This also corresponds to the measurement point for detecting the output voltage. As shown in Figure 37, $t_{demag(det)}$ represents an error added to the measured demagnetization time. The amount of this error is directly proportional to $V_{demag(det)}$. Figure 38 depicts the implementation of the output current limiting circuit. When the OVERLOAD signal is high, the fault timer will run.

For the typical flyback converter waveforms shown in Figure 35, the output current is given by the following equation:

$$I_{out} = \frac{N_{ps}\, I_{p,pk}}{2} \frac{t_{demag}}{T_{sw}} \quad \text{(eq. 3)}$$

Where:

- $t_{demag}$ is the demagnetization time
- $N_{ps}$ is the primary to secondary turns ratio:

$$N_{ps} = \frac{N_p}{N_s} \quad \text{(eq. 4)}$$

- $I_{p,pk}$ is the primary peak inductor current

$$I_{p,pk} = \frac{V_{CS}}{R_{sense}} \quad \text{(eq. 5)}$$

Due to the internal divider ratio,

$$V_{CS} = \frac{V_{FB}}{4} \quad \text{(eq. 6)}$$

In order to maintain a constant output current limit, the controller creates a second feedback voltage,

$$V_{FB_Iout} = V_{REF} \frac{T_{sw}}{t_{demag}} \quad \text{(eq. 7)}$$

and the overload timer must run when

$$V_{CS} = V_{FB_Iout} \quad \text{(eq. 8)}$$

As $V_{CS}$ is not readily available, the controller compares the two feedback voltages and the overload timer runs when:

$$V_{FB} \geq 4V_{FB_Iout} \quad \text{(eq. 9)}$$

Thus, by combining equations (6), (8), (10), and (11) we obtain the output current limit equation:

$$I_{out_lim} = \frac{V_{REF} N_{ps}}{2R_{sense}} \quad \text{(eq. 10)}$$

In order to compensate for error due to propagation delays, the OPP signal is subtracted from $V_{FB_Iout}$, such that

$$V_{FB_Iout} = V_{REF} \frac{T_{sw}}{t_{demag}} - V_{OPP} \quad \text{(eq. 11)}$$

### Abnormal Overcurrent Protection (AOCP)

Under some severe fault conditions, like a winding short−circuit, the switch current can increase very rapidly during the on−time. The current sense signal significantly exceeds $V_{ILIM1}$, but because the current sense signal is blanked by the LEB circuit during the switch turn−on, the power switch current can become huge and cause severe system damage.

The NCP1345 protects against this fault by adding an additional comparator for Abnormal Overcurrent Fault detection. The current sense signal is blanked with a shorter LEB duration, $t_{LEB2}$, typically 125 ns, before applying it to the Abnormal Overcurrent Fault Comparator. The voltage threshold of the comparator, $V_{ILIM2}$, typically 1.2 V, is set 50 % higher than $V_{ILIM1}$, to avoid interference with normal operation. Four consecutive Abnormal Overcurrent faults cause the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Overcurrent Comparator.

### Current Sense Pin Failure Protection

A 1 μA (typically) pull−up current source, $I_{CS}$, pulls up the CS pin to disable the controller if the pin is left open. Additionally, the maximum on−time, $t_{on(MAX)}$ (32 μs typically), prevents the MOSFET from staying on permanently if the CS Pin is shorted to GND.

### Output Short Circuit Protection

During an output short−circuit, there is not enough voltage across the secondary winding to demagnetize the core. Due to the valley timeout feature of the controller, the flux level will quickly walk up until the core saturates. This can cause excessive stress on the primary MOSFET and secondary diode. This is not a problem for the NCP1345, however, because the valley timeout timer is disabled while the ZCD Pin voltage is above the arming threshold. Since the leakage energy is high enough to arm the ZCD trigger, the timeout timer is disabled and the next drive pulse is delayed until demagnetization occurs.

### $V_{CC}$ Overvoltage Protection

An additional comparator on the $V_{CC}$ pin monitors the $V_{CC}$ voltage. If $V_{CC}$ exceeds $V_{CC(OVP)}$, the gate drive is disabled and the NCP1345 follows the operation of a latching fault (see Figure 21).

### Output Overvoltage Protection

In addition to auto−tuning skip mode, the output voltage sensing includes an overvoltage protection circuit. In the event that the sensed output voltage exceeds $V_{out(OVP)}$ (typically 2.4 V) for 3 consecutive cycles, the controller is immediately latched off. This operation is depicted in Figure 39.

### Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the controller. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, $T_{SHDN}$ (typically 140°C). When a thermal shutdown fault is detected, the controller enters a non−latching fault mode as depicted in Figure 22. The controller restarts at the next $V_{CC(on)}$ once the junction temperature drops below below $T_{SHDN}$ by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

The thermal shutdown is also cleared if $V_{CC}$ drops below $V_{CC(reset)}$, or a line removal fault is detected. A new power up sequence commences at the next $V_{CC(on)}$ once all the faults are removed.

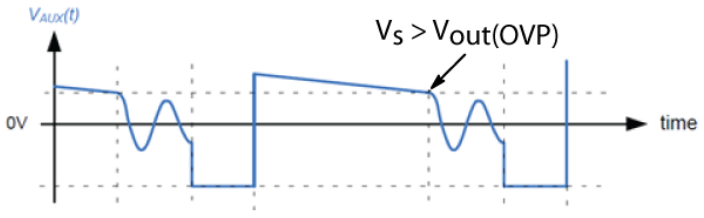



**Figure 39. Detailed View of Demagnetization Ending Point**

## TYPICAL CHARACTERISTICS

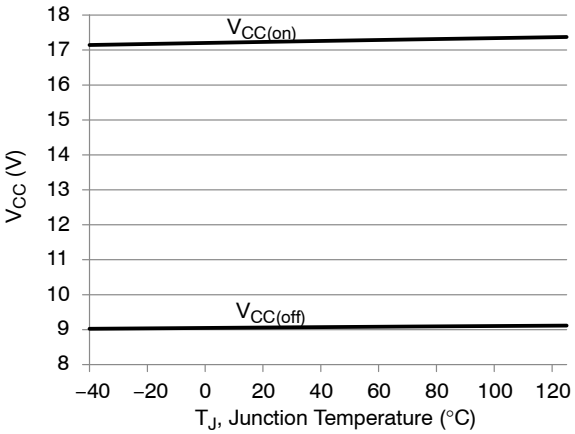



**Figure 40. $V_{CC(on/off)}$ vs. Temperature**

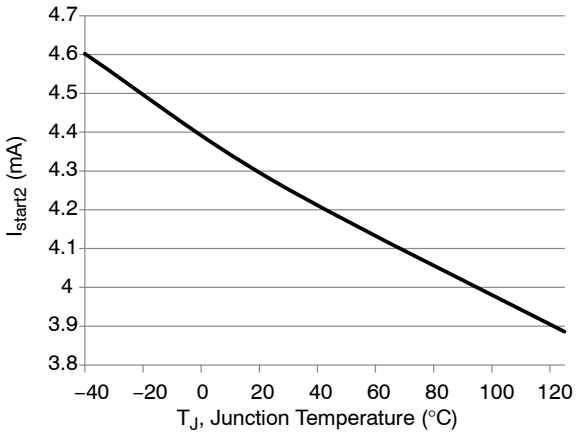



**Figure 41. $I_{start2}$ vs. Temperature**

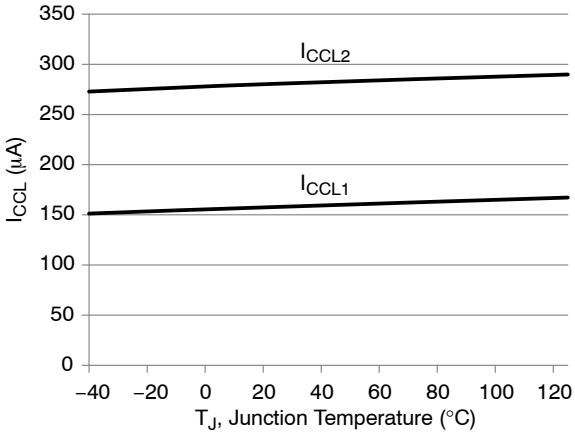



**Figure 42. $I_{CCL}$ vs. Temperature**

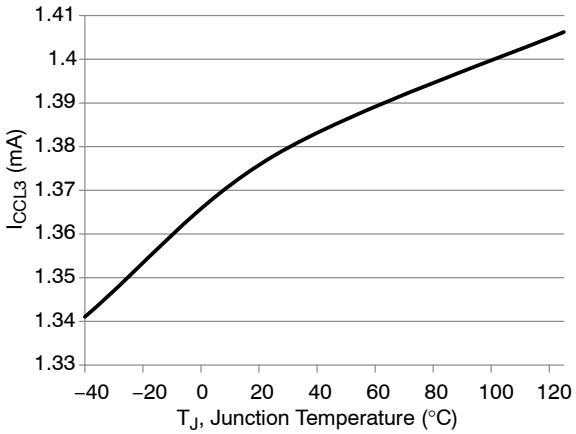



**Figure 43. $I_{CCL3}$ vs. Temperature**

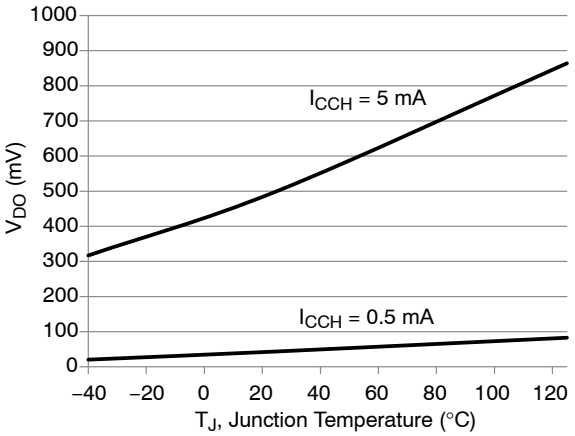



**Figure 44. $V_{DO}$ vs. Temperature**

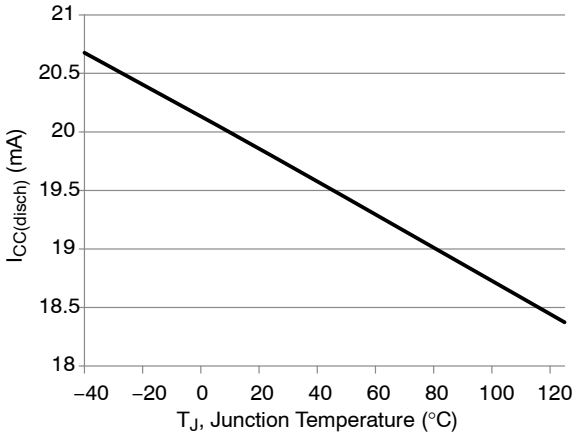



**Figure 45. $I_{CC(disch)}$ vs. Temperature**

## TYPICAL CHARACTERISTICS (CONTINUED)

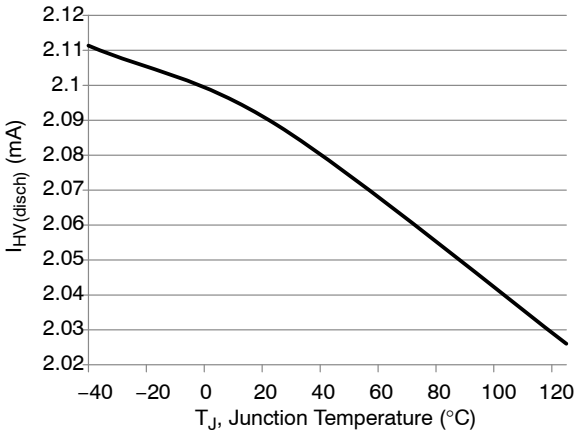



**Figure 46. $I_{HV(disch)}$ vs. Temperature**

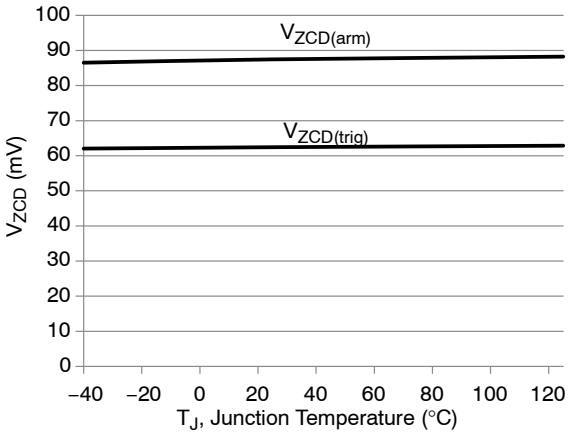



**Figure 47. $V_{ZCD(arm/trig)}$ vs. Temperature**

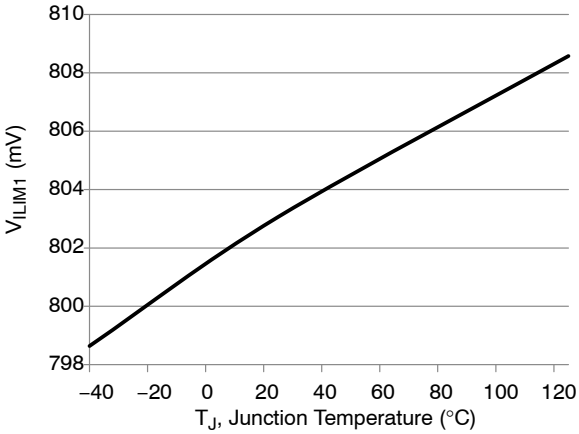



**Figure 48. $V_{ILIM1}$ vs. Temperature**

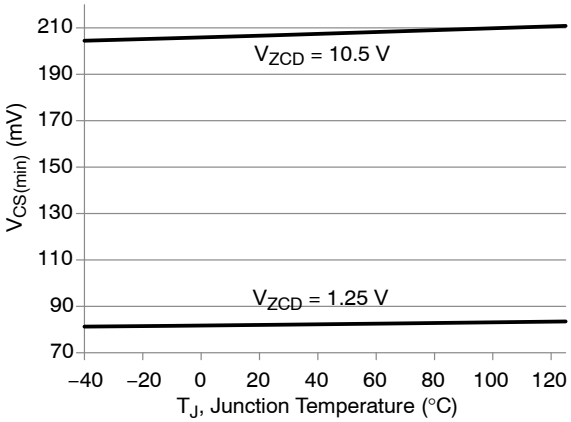



**Figure 49. $V_{CS(min)}$ vs. Temperature**

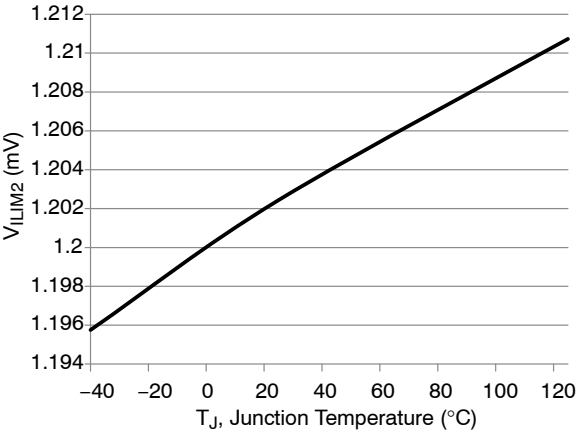



**Figure 50. $V_{ILIM2}$ vs. Temperature**

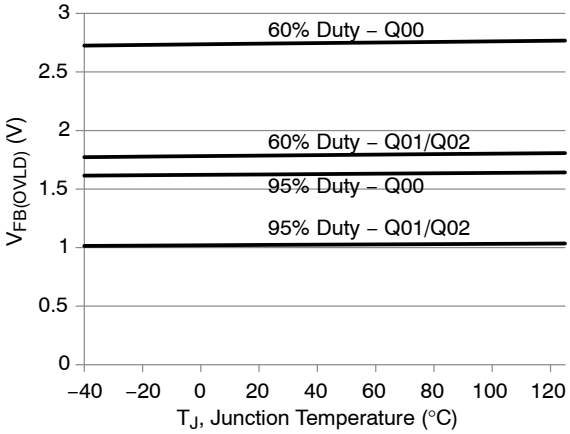



**Figure 51. $V_{FB(OVLD)}$ vs. Temperature**

## TYPICAL CHARACTERISTICS (CONTINUED)

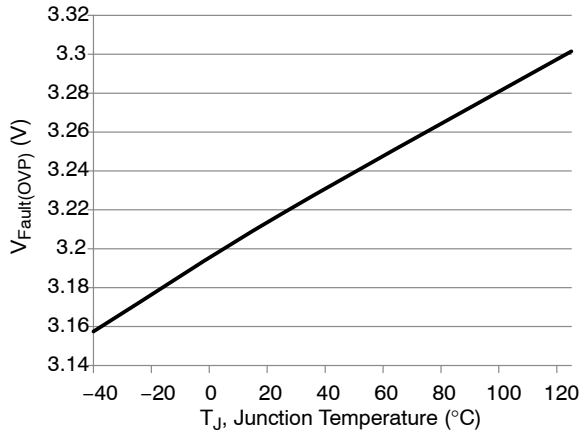



**Figure 52. $V_{Fault(OVP)}$ vs. Temperature**

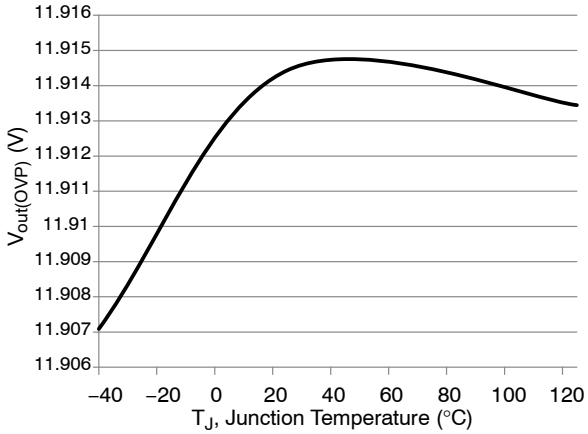



**Figure 53. $V_{out(OVP)}$ vs. Temperature**

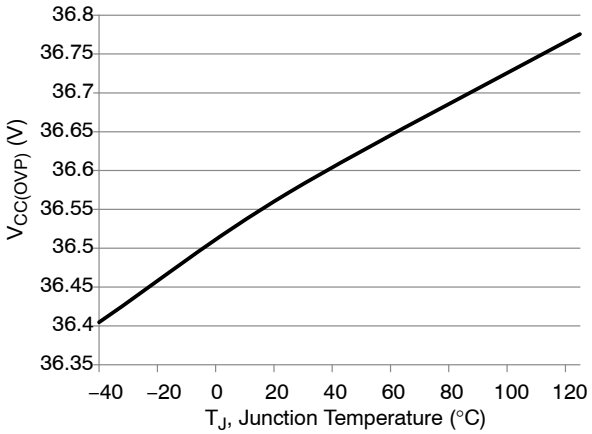



**Figure 54. $V_{CC(OVP)}$ vs. Temperature**

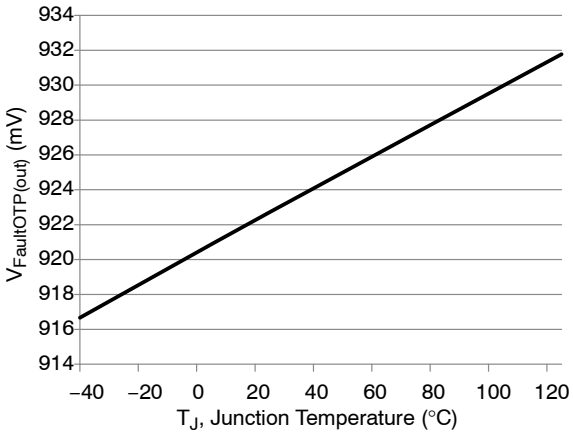



**Figure 55. $V_{FaultOTP(out)}$ vs. Temperature**

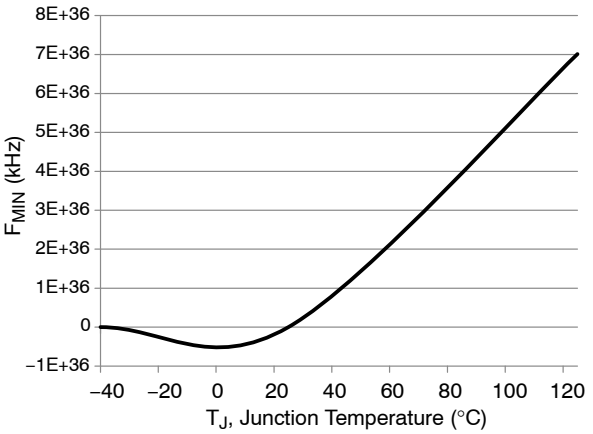



**Figure 56. $F_{MIN}$ vs. Temperature**

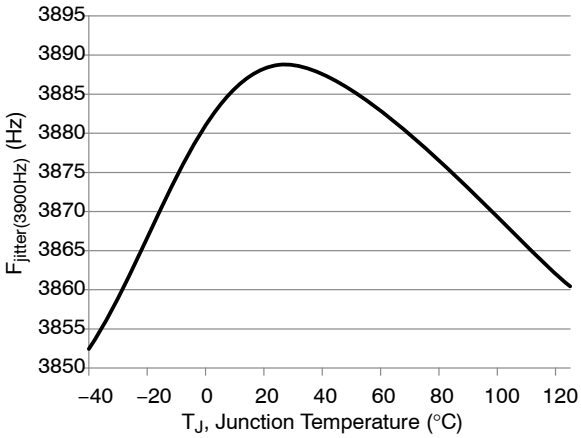



**Figure 57. $F_{jitter}$ vs. Temperature**

## TYPICAL CHARACTERISTICS (CONTINUED)

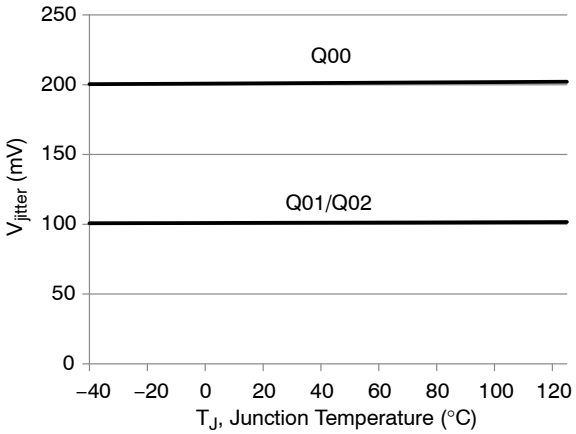



**Figure 58. $V_{jitter}$ vs. Temperature**

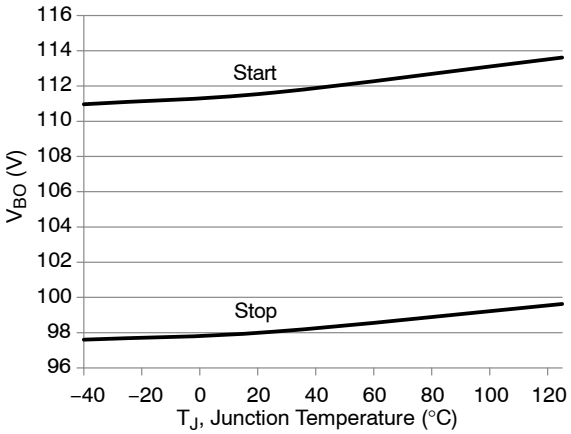



**Figure 59. $V_{BO}$ vs. Temperature**

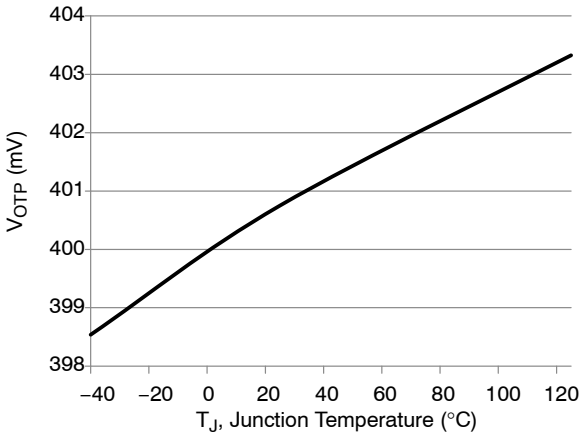


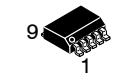

**Figure 60. $V_{OTP}$ vs. Temperature**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

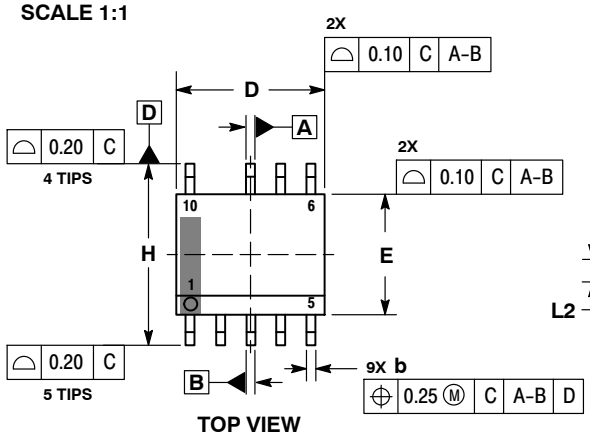
ON Semiconductor®

**SOIC−9 NB**
CASE 751BP
ISSUE A

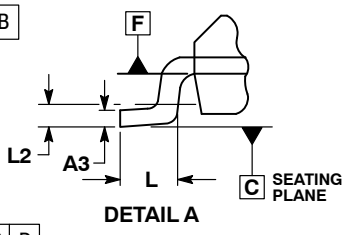
DATE 21 NOV 2011



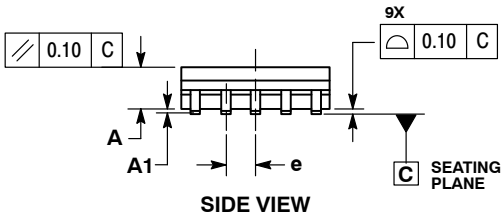

SCALE 1:1



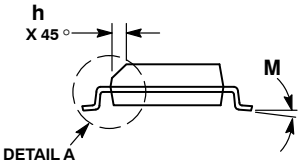

TOP VIEW




DETAIL A




SIDE VIEW

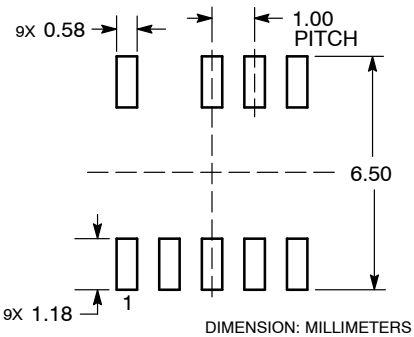



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.25 | 1.75 |
| A1 | 0.10 | 0.25 |
| A3 | 0.17 | 0.25 |
| b | 0.31 | 0.51 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.00 BSC | |
| H | 5.80 | 6.20 |
| h | 0.37 REF | |
| L | 0.40 | 1.27 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |

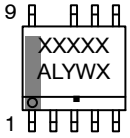
### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

| | | | |
|---|---|---|---|
| DOCUMENT NUMBER: | 98AON52301E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| DESCRIPTION: | SOIC−9 NB | | PAGE 1 OF 1 |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**onsemi**, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales