EVBUM2710/D

USB Type-C® Source Controller Supporting USB Power Delivery 3.0 w/PPS and a 4-Switch Buck Boost Controller Evaluation Board User's Manual

FUSB3307MX−PPS−GEVB (SOIC14 Package)

FUSB3307MPX−PPS−GEVB* (QFNW20 Package)

STR−FUSB3307MX−PPS−EVK* (SOIC14 with Strata Support)

STR−FUSB3307MPX−PPS−EVK* (QFNW20 with Strata Support)

Introduction

The FUSB3307 evaluation board (GEVB), or kit (EVK), is a complete platform to evaluate the Type−C interface detection and USB Power Delivery 3.0 solution the FUSB3307 provides. The EVB is designed for both stand−alone operation and connection to test equipment for specific testing requirements. Using a single DC power supply, the EVB functions as a source only port.

Description

The various FUSB3307 evaluation boards contain a USB Type−C source controller supporting USB Power Delivery (PD) 3.0 with PPS (Programmable Power Supply) based on USB PD 3.0 standards, as well as a 4−stage buck boost controller, delivering VBUS levels from 3.3 V to 21 V, and supporting nominal current loads up to 5 A.

The evaluation board has a VBAT connector for a DC power supply. It connects to the input switch of the NCV81599 DC to DC 4−Switch Buck Boost Controller. The FUSB3307 is used for CV/CC control by providing feedback compensation to the NCV81599 controller.

Charging voltages and currents are measured by detecting VFB and the current sensing resistor. The sensed voltage and current feed to the compensation logic and then controls the CATH pin for constant voltage (CV) or constant current (CC) control. A 5 mΩ VBUS load sense resistor is assembled on the EVB.

On the EVB, there are multiple test points for device validation. For example, VBUS and GND_SNS test points can be used for VBUS load testing.

Key Features

- Wide Input Voltage Range 4.5 V ~ 32 V
- Wide Output Voltage Range 3.3 V ~ 21 V
- Type−C r1.4 / USB PD 3.0 v1.2 Compliant
- USB−IF TID # 1430
- Type−C Source Only
- Detects Cable Marker Identity and offers 3 A or 5 A Power Objects
- VCONN Supply
- CV/CC Control with CATH Pin
- On Board 5 mΩ Rsense Resistor
- Over−Current/Short−Circuit Protection (OCP)
- Auto−tuning OCP for Low Output Voltages
- Over−Temperature Protection (OTP)
- Over− and Under−Voltage Protection (OVP/UVP)
- Cable Fault Detection
- External NFET for VBUS Control
- Easily Accessible Test Points for Rapid Evaluation and Performance Measurements

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EVAL BOARD USER'S MANUAL

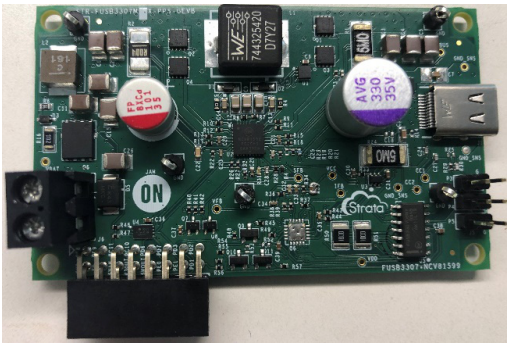


Figure 1. Evaluation Board Photo

*Not yet available

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Schematics for the Evaluation Board

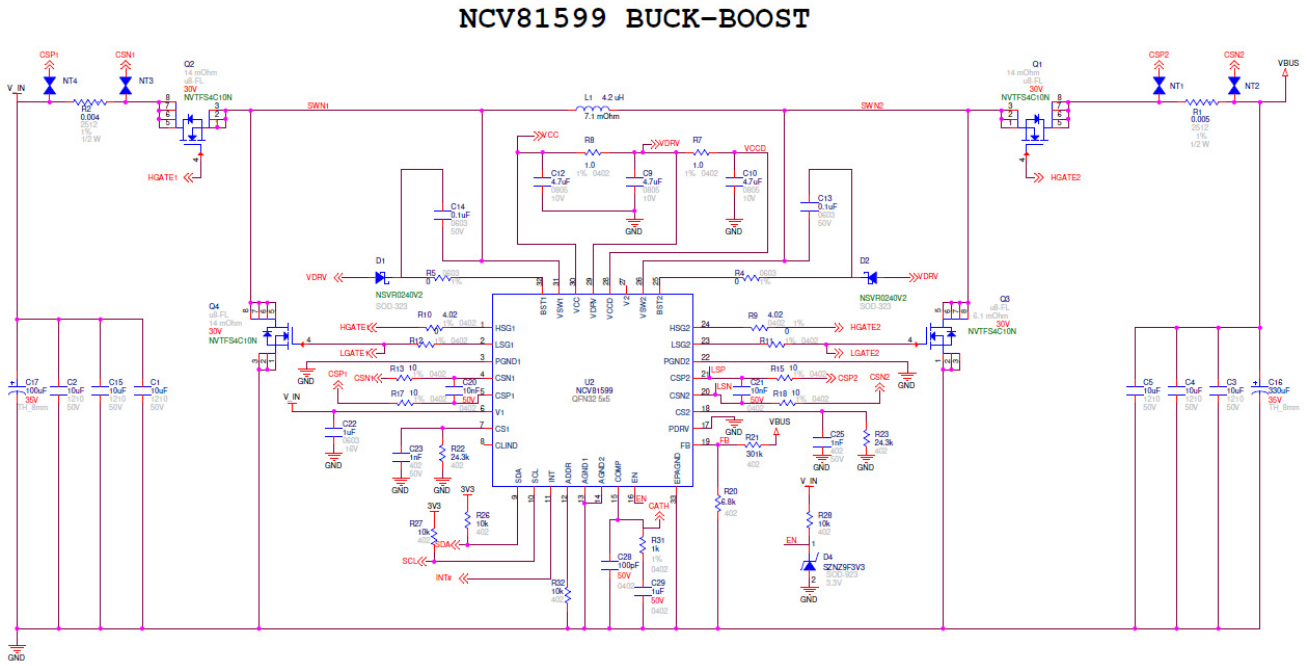


Figure 2. NCV81599 BUCK−BOOST Block

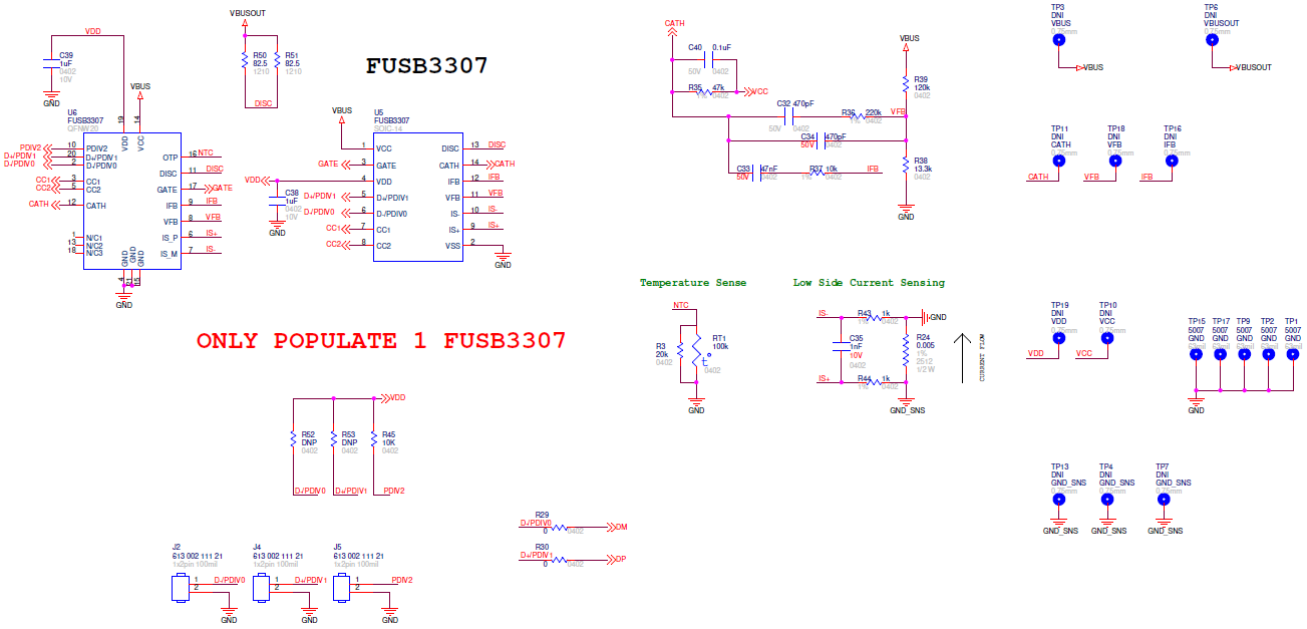


Figure 3. FISB3307, Feedback Components, and Testpoints

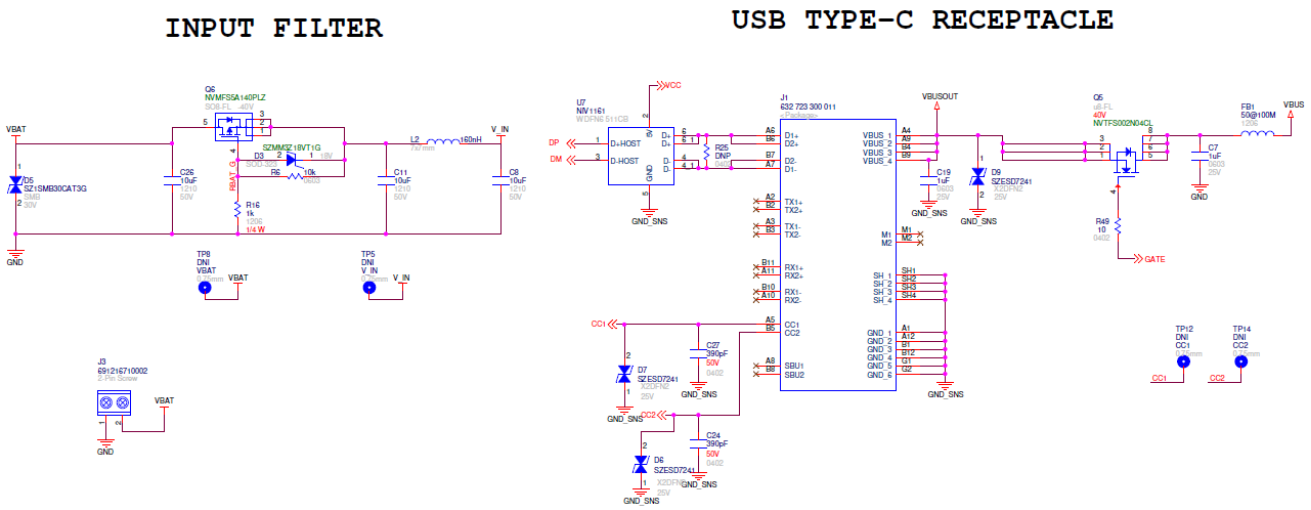


Figure 4. VBAT Input Filter and Type−C Receptacle

Evaluation Board Gerbers

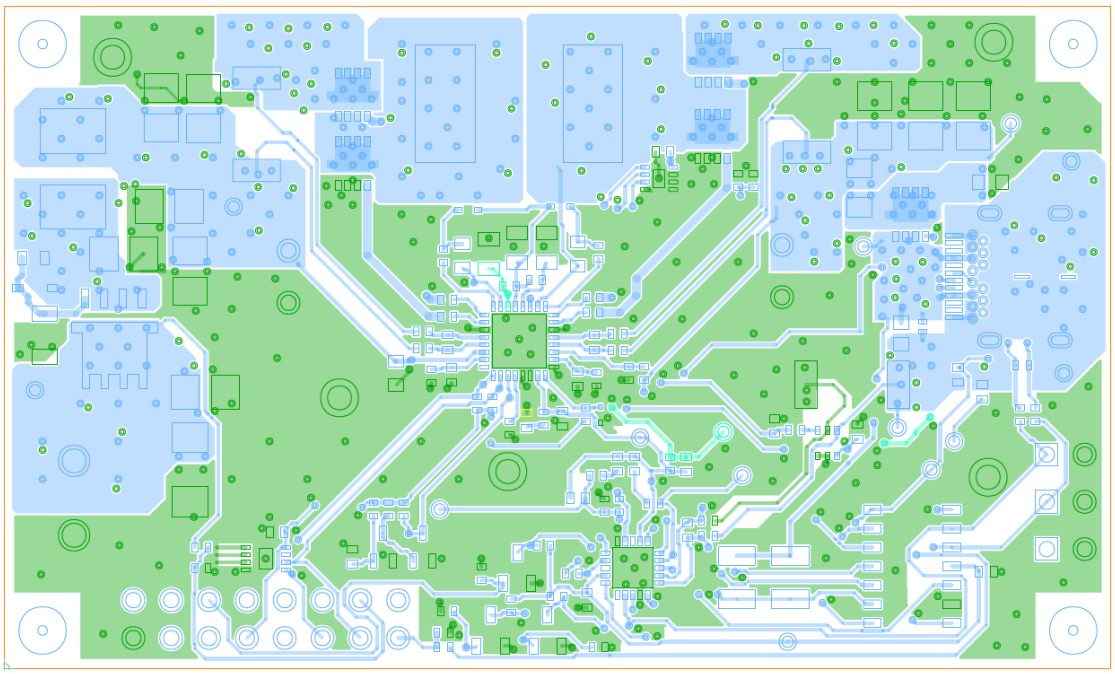


Figure 5. Top Layer

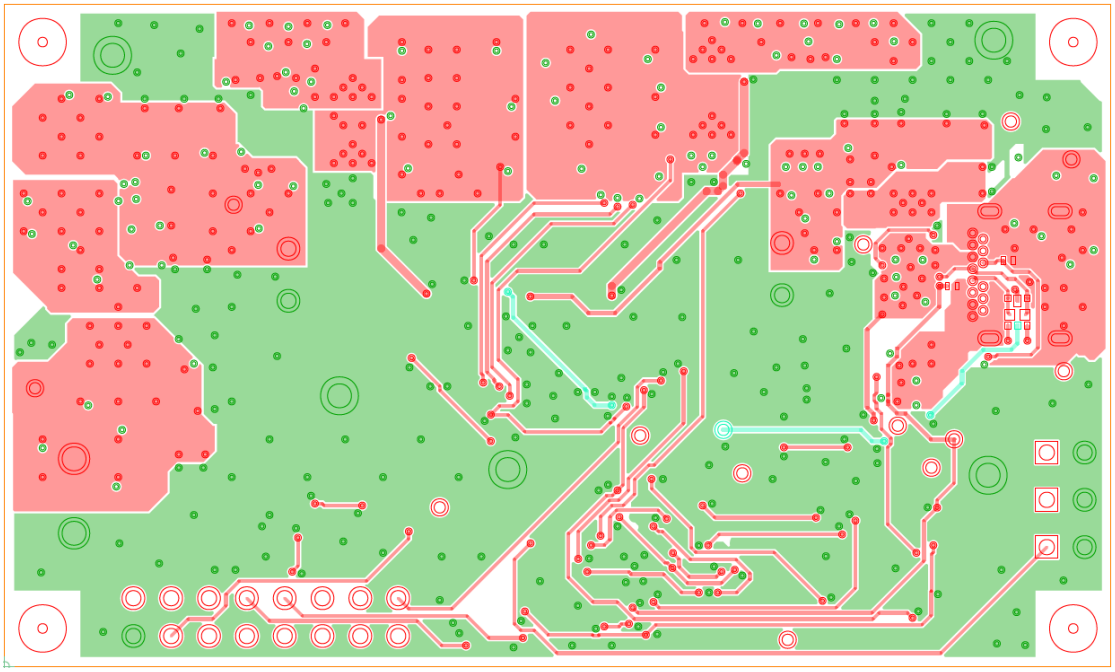


Figure 6. Bottom Layer

Descriptions for the Evaluation Board Test Points

VBAT

VBAT is the input DC voltage to power the evaluation board. It must be between 4.5 V and 32 V.

V_IN

V_IN is the same as VBAT after the input filter.

VCC

VCC on the evaluation board is VCC for the NCV81599. It is not the same as VCC for the FUSB3307. This is a constant 5V output from the NCV81599 when VBAT is applied.

VBUS

VBUS, which is also the same as VCC for the FUSB3307, is the device operating power from primary side. The default initial VCC of the FUSB3307 is 5 V (typical), with a valid range of 4.5 V to 5.5 V. The CATH pin is controlled to keep VCC in the valid range. The FUSB3307 VCC voltage sensing is used for OVP and UVP with an internal 1:9 resistor divider. The FUSB3307 VCC is also used for the FUSB3307 VCC current discharge function through an internal resistance, 22~25 Ω, when it's needed. After an explicit contract is established, the valid FUSB3307 VCC can be in the range of 3.3 V−5% (3.135 V) up to 21 V+5% (22.05 V) for the case of USB PD PPS contracts.

VDD

VDD is the internal 5 V regulator output from the FUSB3307, and an external 1 uF capacitor is required. The VDD is used for internal device power as well as VCONN supply when needed.

VBUSOUT

VBUSOUT is VBUS between the external NFET load switch and the Type−C receptacle and is also where a recommended external resistor, typically 39 Ω, is tied to the DISC pin for the VBUS discharge path. An internal path has 22 to 23 Ω in series with a switch.

GND

Evaluation board and device GND which is tied together with IS−. The IS− pin is tied to the FUSB3307 side of the current sense resistor. IS+ connects to ground sense return path, GND_SNS, from the Type−C receptacle.

GND_SNS

This is the return ground sense path from the Type−C receptacle. IS+ connects to this ground sense return path for sensing the sink load current.

IFB

This is a constant current amplifying signal. The voltage level on this point is the amplified current sense signal. This pin connects to the internal CC loop amplifier's non−inverting input terminal. Externally, the pin connects to the FUSB3307 VCC through a capacitor and resistor network, which contributes to the CATH pin current ramp.

VFB

This is the output voltage sensing voltage. This pin is for CV regulation, and connects to the internal CV loop amplifier non−inverting input terminal. Externally, it is tied to the output voltage resistor divider (1:10) on the evaluation board, where there is a 120 kΩ pull up to VCC and a 13.3 kΩ pull down to GND, creating the 1:10 divider.

SFB

The SFB test point is the CATH pin for the FUSB3307. CATH is the feedback signal to the primary controller. It connects to the comp pin of the NCV81599. CATH pin is open−drain output and controlled by CV/CC logic in the FUSB3307.

CC1, CC2

Configuration Channel 1 and 2, these pins are used to detect USB Type−C devices and to communicate using USB PD communication protocol when applicable. Also used for VCONN supply. For USB PD, the maximum capacitance is limited to 600 pF.

Descriptions of Other FUSB3307 Pins that do not have Test Points on the Evaluation Board

GATE

Gate drive signal to drive the gate of external NFET load switch. Using an internal charge pump, the external NFET gate is controlled using this pin. The source power of the charge pump is from FUSB3307 VCC.

IS+, IS−

Current sensing amplifier positive/negative terminals. IS+ is connected to the GND_SNS return path of the Type−C receptacle. IS− connects to the device GND pin. Charging current is calculated as: the voltage on IS+ is divided by Rsense (i.e. 5 mΩ) and then amplified 40 times, which will be actual sense current. The sense resistor needs to be 5 mΩ.

D−, D+

D−, D+ can be used for multiple purposes by the FUSB3307. The default programmed function is for BC1.2 functionality, used for signaling of BC1.2 host operation. Another option for these pins' function is for maximum power control: PDIV0 and PDIV1. This mode is controlled by programming (fuse trimmed during production). The QFNW package has a PDIV2 pin which can limit the total power by 50%. See the FUSB3307 datasheet for a full description of the PDIV0, PDIV1, and PDIV2 functionality.

Descriptions of Jumpers, Connectors on the Evaluation Board

P3, P4, and P5

If the FUSB3307 device mounted on the evaluation board is programmed to support PDIV0, PDIV1, or PDIV2, then the P3, P4, and P5 jumpers permit shorting any of the three PDIVn signals to GND. Leaving the jumper open allows the signal to be pulled up to VDD via R52, R53, or R45. Note that R52 and R53 are not populated by default, so if a custom FUSB3307 device is used with PDIV0, PDIV1 functionality, R52 and R53 need to also be populated with 10 kΩ resistors. See the FUSB3307 datasheet for a full description of the PDIV0, PDIV1, and PDIV2 functionality.

J3

This two pin connector is used for supplying VBAT and GND to the evaluation board.

J6

This 16 pin header is used for attaching the optional Strata controller daughter card to the evaluation board.

J1

The Type−C receptacle.

Descriptions of Key Features

VCC OVP (Over−Voltage Protection)

VCC voltage is measured by an ADC with $1/10^{th}$ VCC voltage. Since the VCC range is wide, between 3.3 V ~ 21 V, VCC OVP voltage threshold is defined in the datasheet as 121% of the PD contract voltage. There is a maximum OVP spec (23.8V Typ) which governs in general. So, in the case of a 5 V PD contract, the OVP trigger point is 6.05 V and so on for other PD contract voltages. For a 20 V PD contract, the OVP will be triggered by either the 121% (24.2 V) trigger point or the maximum OVP spec (23 V min / 23.8 V Typ / 24.8 V max).

Once an OVP Fault is triggered, VBUS will be shut off (external NFET off) and so the sink will be disconnected. Also, the CATH signal will drop to GND to recover VCC back to 5 V. There will be no PD Alert message transmitted to the sink device caused by the OVP Fault, which is different from OCP or OTP Faults. If an OTP or OCP Fault happens, there is a PD Alert message sent to the attached sink device.

When VBUS voltage is changing because of a PD contract change, the OVP is disabled during the transition time which is called OVP blanking time, typically 221 ms.

CC OVP (Over−Voltage Protection)

In the Type−C receptacle, there could be a chance to short between VBUS and either CC signal. The FUSB3307 has high voltage protection for this case. The threshold is 6.5 V Typ with 28 μs debounce.

VCC UVP (Under−Voltage Protection)

Like OVP, another protection is UVP which is the case when the VCC voltage drops blow the spec, which is 65% of contract voltage. For example, at VBUS of 5 V, the UVP trigger point is 3.25 V. There is the same blanking time of 221 ms during any VBUS voltage transition. Once UVP occurs, there is a PD Alert message sent to the sink device.

VCC OCP (Over−Current Protection)

The FUSB3307 senses the VBUS load current via a small Rsense resistor (5 milliohm) as described in the datasheet. The OCP fault is triggered at 120% of the maximum current for the requested Power Data Object (PDO) for fixed supplies only, typically 3.6A for a 3A maximum fixed supply current.

For PPS APDOs (Augmented Power Data Objects), Constant Current Limiting (CL) is used as specified in the USB PD specification where the voltage will drop to a low value based on keeping the current constant and equal to the requested PPS current. More details can be found in the FUSB3307 datasheet.

Once an OCP Fault is triggered, VBUS will be shut off (external NFET off) and so the sink will be disconnected. Also, the CATH signal will drop to GND to recover VCC back to 5V. There will be an OCP Fault happens, there is a PD Alert message sent to the attached sink device upon the FUSB3307 establishing an explicit contract with the sink device.

OTP (Over−Temperature Protection)

OTP is measured internally for the SOIC package. There are two different thresholds, 125C for a warning or 135C for a Fault. If the warning threshold is triggered longer then the OTP debounce time, typically 80 ms, a PD Alert message for the temperature warning will be sent to the sink. Once the Fault threshold is triggered, the FUSB3307 will disable the Type−C connection, shut off VBUS (external NFET off), and monitor the Fault. Once the Fault has been cleared, the FUSB3307 will wait a recovery time, typically 2 s, and then begin monitoring the CC lines for an attach. Upon re−establishing an explicit contract with the sink, a PD Alert message will be sent to let the sink know that the FUSB3307 previously experienced an OTP Fault.

The QFNW package also has an NTC pin to monitor the external temperature. In the case of the QFNW package, only the external temperature will trigger a PD Alert for a warning. The NTC pin is connected to an NTC resistor (100 kΩ ±1%, B25/50 = 4300k ±1%) in parallel with a 20 kΩ resistor to GND. But, either the internal temperature threshold or the external temperature threshold can cause an OTP Fault.

CATH feedback

The CATH pin is used to provide feedback to the circuit providing VCC/VBUS to the FUSB3307. Typically an

opto−coupler cathode on the secondary side is connected to the CATH pin to provide feedback signal to the primary side PWM controller. Alternatively, the CATH pin can be connected to the error amplifier output of a DC−DC regulator (often called the compensation pin) or with an inverting circuit to the DC−DC feedback (FB) pin. Once an explicit contract is established with the sink, this signal is used to control whatever VBUS voltage is required, from as little as 3.3 V to 21 V in the case of a USB PD PPS contract.

BMC Eye Diagram on CC1/CC2

The BMC eye diagram on CC, Figure 7 and Figure 8, is used to guarantee the signal level/quality is passing the mask that is defined by USB−IF PD specifications. The voltage range of the BMC signal is between −100 mV to 1.2 V but it can be higher and lower depending on GND shift due to load or noise interference on the signal path.

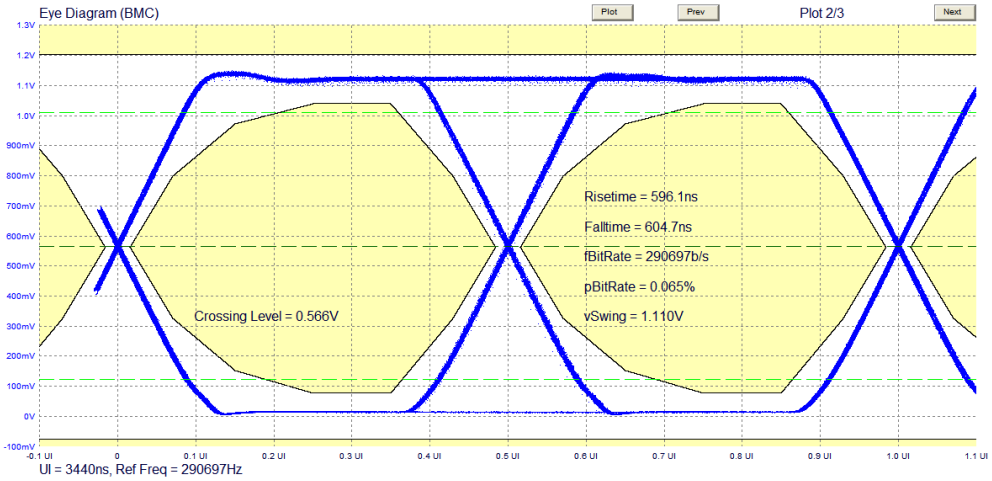


Figure 7. BMC Eye Diagram on CC1

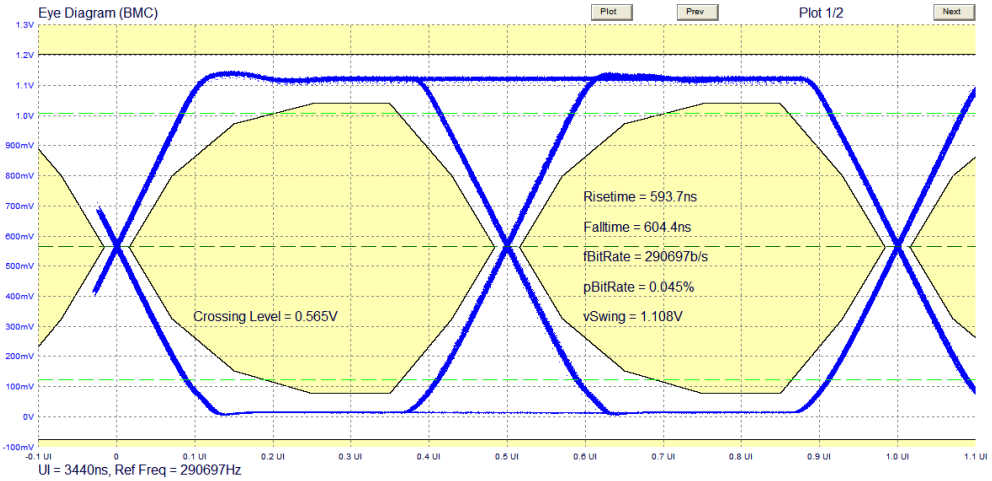


Figure 8. BMC Eye Diagram on CC2

60 W Efficiency

Figure 9 shows the efficiency curves for VBUS at 5 V, 9 V, 12 V, 15 V, and 20 V with load varying from 0.5 A to 3 A.

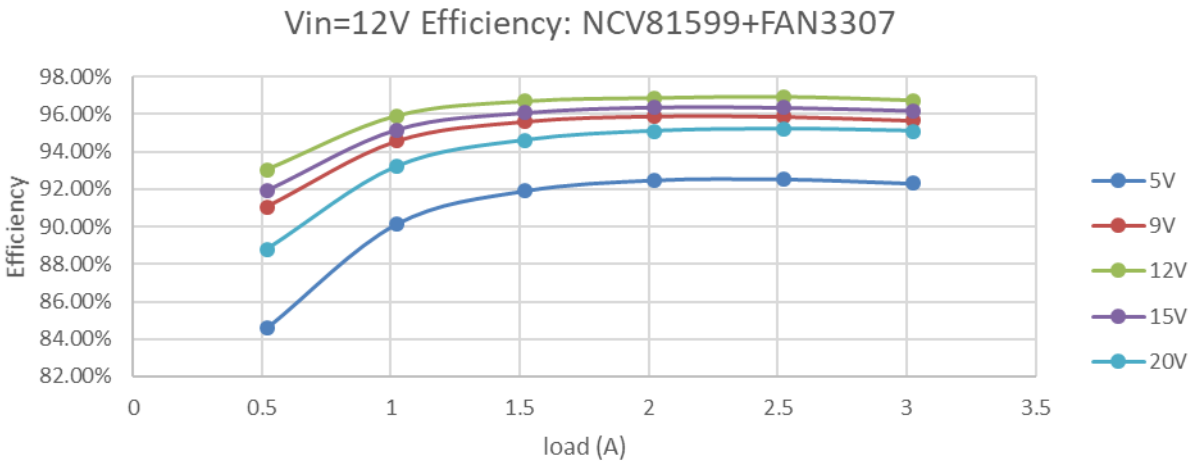


Figure 9. Efficiency Curves

Load Regulation

Figure 10 shows the load regulation curve for VBUS at 5 V with load varying from 0.5 A to 3 A. Figure 11 shows the 9 V curve.

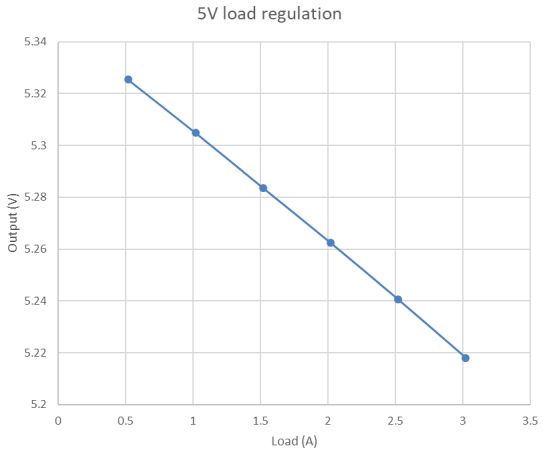


Figure 10. 5 V Regulation

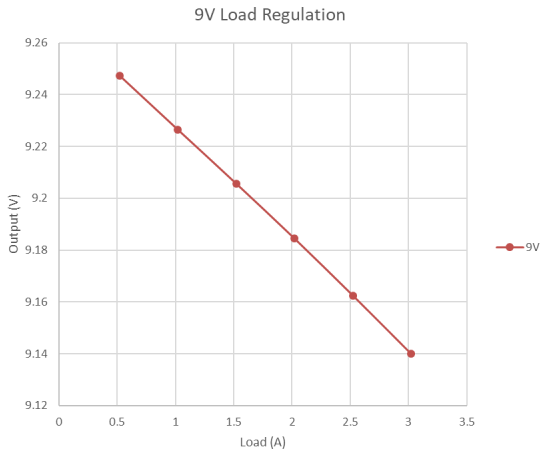


Figure 11. 9 V Regulation

Figure 12 shows the load regulation curve for VBUS at 12 V and Figure 13 shows the 15 V curve.

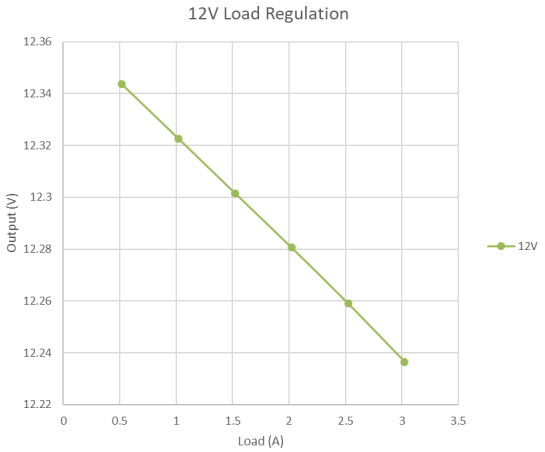


Figure 12. 12 V Regulation

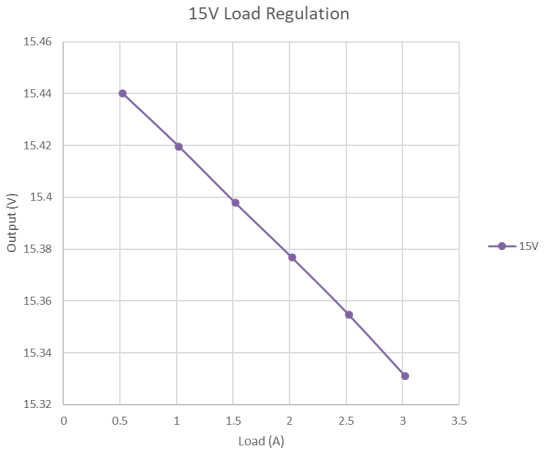


Figure 13. 15 V Regulation

Figure 14 shows the load regulation curve for VBUS at 20 V.



Figure 14. 20 V Regulation

Figure 15 shows the load regulation curves for each value of VBUS with load varying from 0.5 A to 3 A.

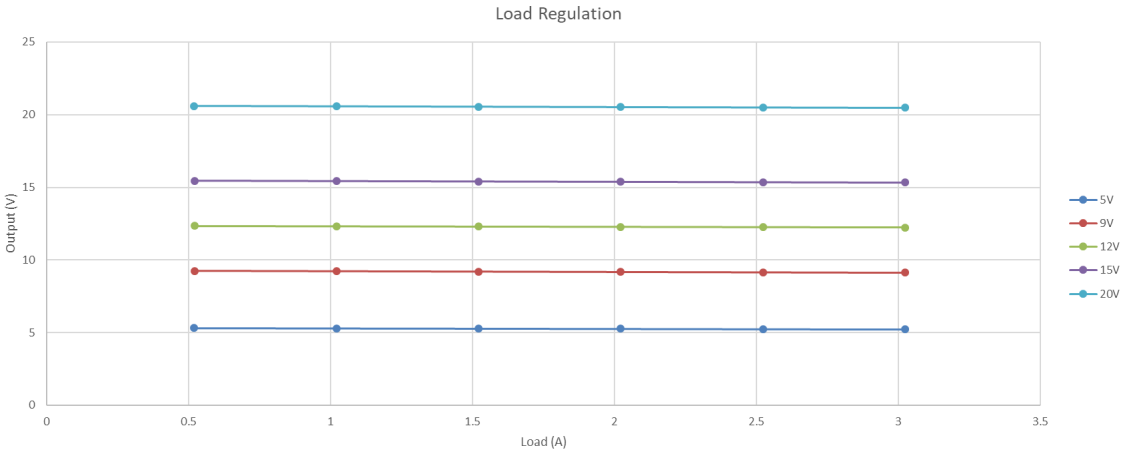


Figure 15. Regulation Curves

Voltage Transitions with No Load

Below are the waveforms of VBAT at 12 V and VBUS voltage changing from 5 V to 12 V and back to 5 V with no load. VBUS, SFB, and SWN1 waveforms are shown. VBUS change from 5 V to 12 V in Figure 16 and 12 V to 5 V in Figure 17.

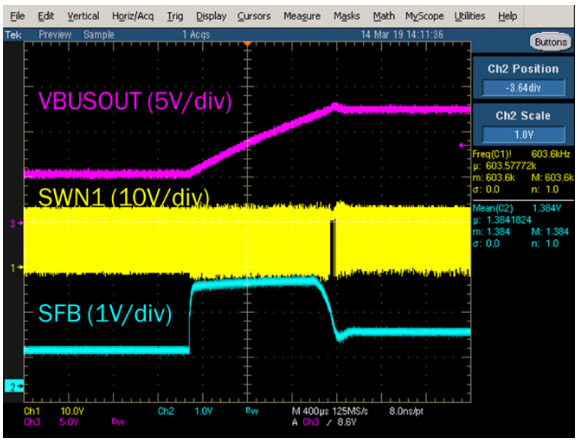


Figure 16. 5 V to 12 V Transition with No Load



Figure 17. 12 V to 5 V Transition with No Load

Below are the waveforms of VBAT at 12 V and VBUS voltage changing from 5 V to 15 V and back to 5 V with no load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 5 V to 15 V in Figure 18 and 15 V to 5 V in Figure 19.

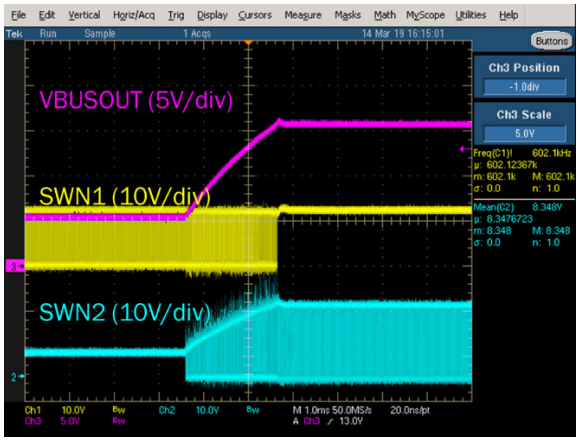


Figure 18. 5 V to 15 V Transition with No Load

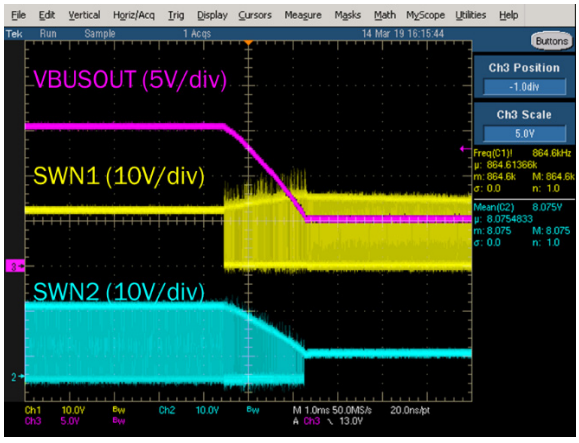


Figure 19. 15 V to 5 V Transition with No Load

Below are the waveforms of VBAT at 12 V and VBUS voltage changing from 5 V to 20 V and back to 5 V with no load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 5 V to 20 V in Figure 20 and 20 V to 5 V in Figure 21.

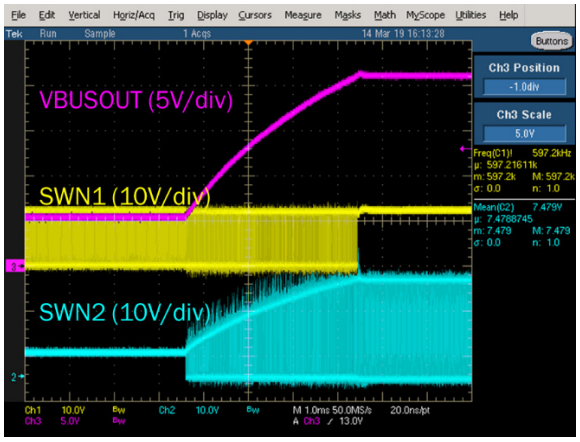


Figure 20. 5 V to 20 V Transition with No Load

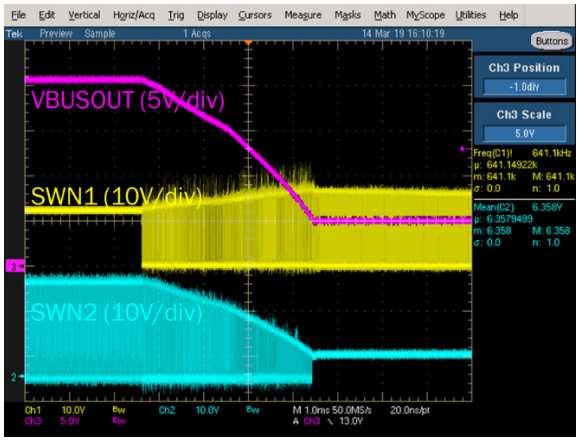


Figure 21. 20 V to 5 V Transition with No Load

Voltage Transitions with Load

Below are the waveforms of VBAT at 12 V and VBUS voltage changing from 20 V to 3.3 V with a 2.66 A load and back to 20 V with a 1 A load. VBUS, SWN1, and SWN2 waveforms are shown. VBUS change from 20 V to 3.3 V in Figure 22 and 3.3 V to 20 V in Figure 23.

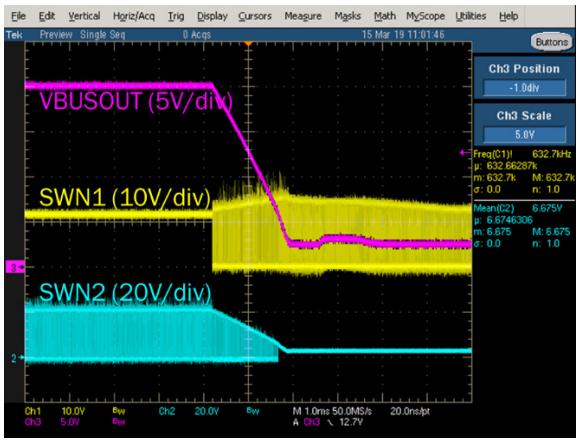


Figure 22. 20 V to 3.3 V Transition with 2.66 A Load

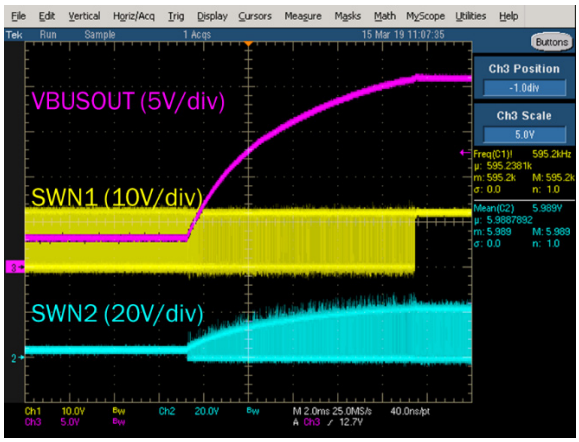


Figure 23. 3.3 V to 20 V Transition with 1 A Load

VBUSOUT Transient Load testing

Below are the waveforms with VBAT at 12 V and VBUSOUT with a 0 A load for 3 ms and then a 3 A load for 3 ms. t_{RISE} and t_{FALL} are 3 mA/µs. Transient waveforms for 5 V and 9 V are shown below in Figure 24 and Figure 25.



Figure 24. Transient Load on 5 V BUS



Figure 25. Transient Load on 9 V BUS

Transient waveforms for 12 V and 15 V are shown in Figure 26 and Figure 27.



Figure 26. Transient Load on 12 V BUS

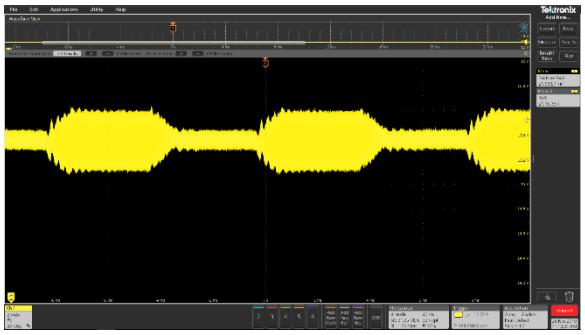


Figure 27. Transient Load on 15 V BUS

Transient waveform for 20 V is shown in Figure 28.

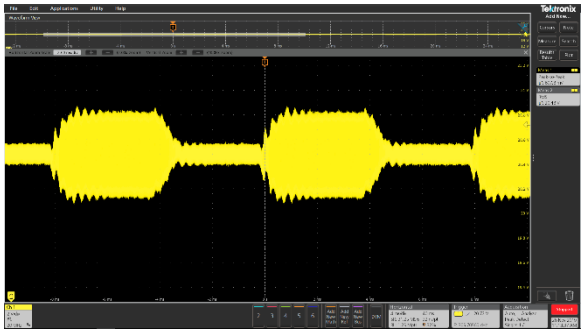


Figure 28. Transient Load on 20 V BUS

VBUSOUT Voltage Ripple with and without Load

Below are the waveforms with VBAT at 12 V and VBUSOUT voltage ripple for 5 V, with a 3 A load and no load. VBUSOUT waveforms are shown. Figure 29 is 5 V with 3 A load and Figure 30 is 5 V with no load.

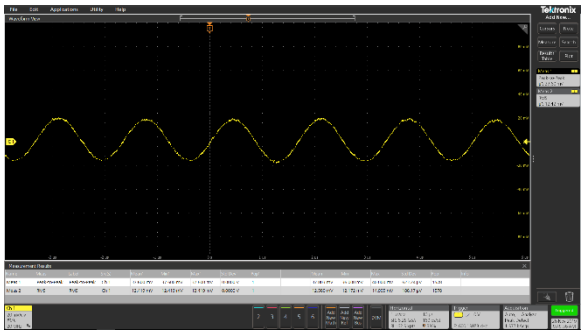


Figure 29. VBUSOUT Ripple for 5 V / 3 A

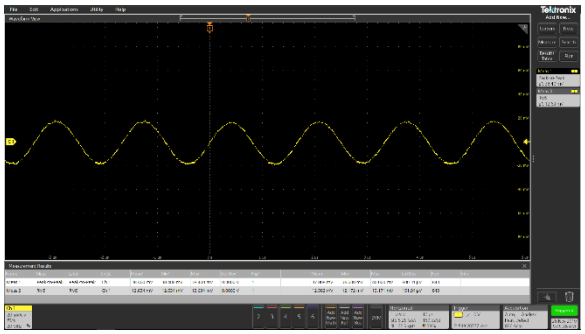


Figure 30. VBUSOUT Ripple for 5 V / 0 A

Below are the waveforms with VBAT at 12 V and VBUSOUT voltage ripple for 9 V, with a 3 A load and no load. VBUSOUT waveforms are shown. Figure 31 is 9 V with 3 A load and Figure 32 is 9 V with no load.

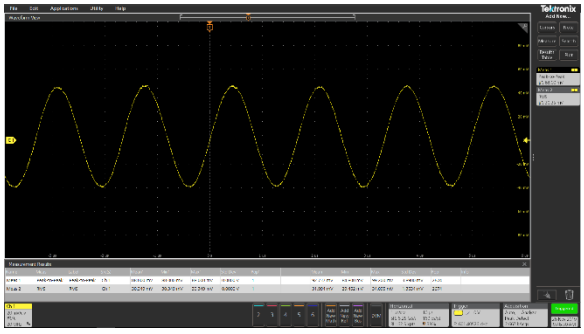


Figure 31. VBUSOUT Ripple for 9 V / 3 A

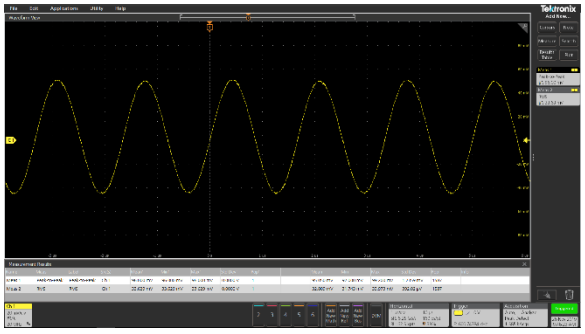


Figure 32. VBUSOUT Ripple for 9 V / 0 A

Below are the waveforms with VBAT at 12 V and VBUSOUT voltage ripple for 12 V, with a 3 A load and no load. VBUSOUT waveforms are shown. Figure 33 is 12 V with 3 A load and Figure 34 is 12 V with no load.

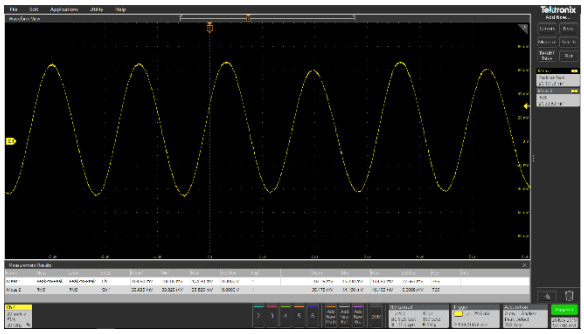


Figure 33. VBUSOUT Ripple for 12 V / 3 A

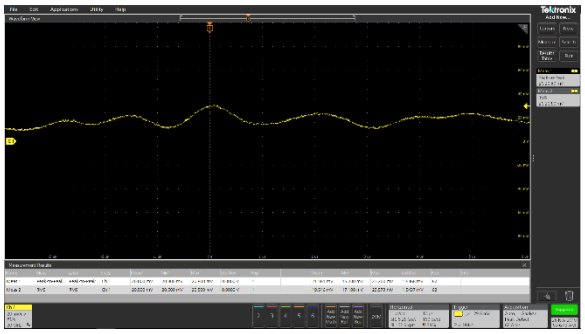


Figure 34. VBUSOUT Ripple for 12 V / 0 A

Below are the waveforms with VBAT at 12 V and VBUSOUT voltage ripple for 15 V, with a 3 A load and no load. VBUSOUT waveforms are shown. Figure 35 is 15 V with 3 A load and Figure 36 is 15 V with no load.

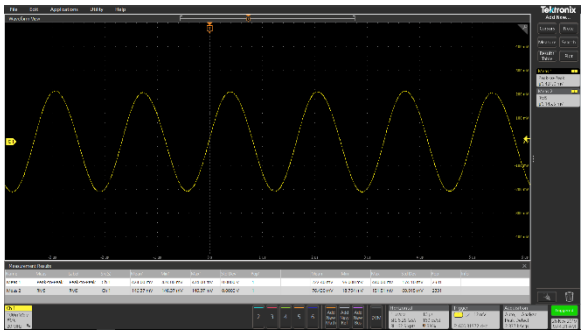


Figure 35. VBUSOUT Ripple for 15 V / 3 A

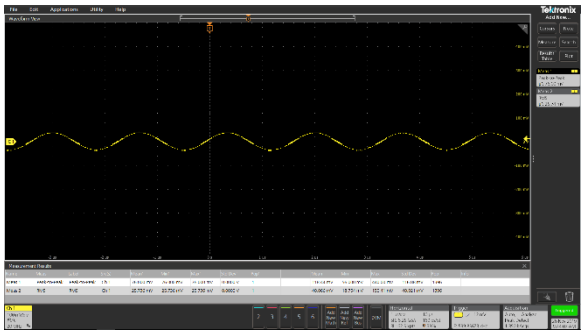


Figure 36. VBUSOUT Ripple for 15 V / 0 A

Below are the waveforms with VBAT at 12 V and VBUSOUT voltage ripple for 20 V, with a 3 A load and no load. VBUSOUT waveforms are shown. Figure 37 is 20 V with 3 A load and Figure 38 is 20 V with no load.

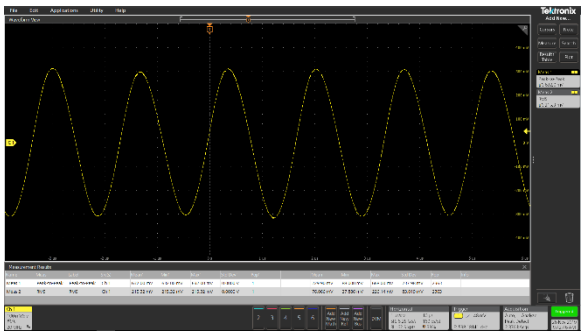


Figure 37. VBUSOUT Ripple for 20 V / 3 A

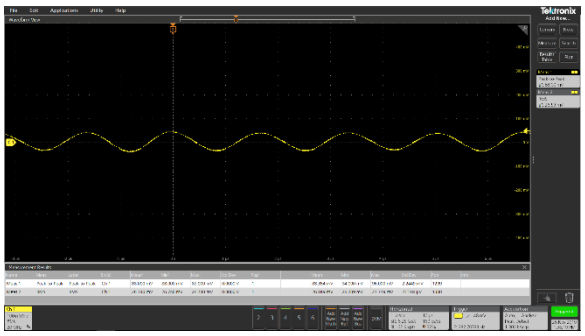


Figure 38. VBUSOUT Ripple for 20 V / 0 A

VBUS discharge

VBUS discharge occurs when the VBUS voltage transitions to a lower target voltage, such as 20 V down to 5 V, when there is a light load, less than 450 mA, or no load. If more of a load (tested 500 mA and 2 A) is present, there is no VBUS discharge during the transition as the load current itself discharges the VBUS. If a cable is unplugged (detach), there is VBUS discharge regardless of load presence unless VBUS is 5 V when the cable is unplugged.

When the cable is unplugged, there is another VBUS discharge with the GATE (NFET) off to discharge from 1 μF output capacitor. This applies even when VBUS was 5V previously.

The discharge timer is always the same at 210 ms, but, the discharge current is not consistent because it depends on the VBUS voltage when the internal discharge FET is turned on.

The waveform in Figure 39 is when VBUS changes from 20 V to 5 V and the waveform in Figure 40 is when the Type−C cable is unplugged. For both cases, there is a VBUS discharge because there was no load on this test. When the cable is unplugged, there is another discharge along with the VBUS shut off.

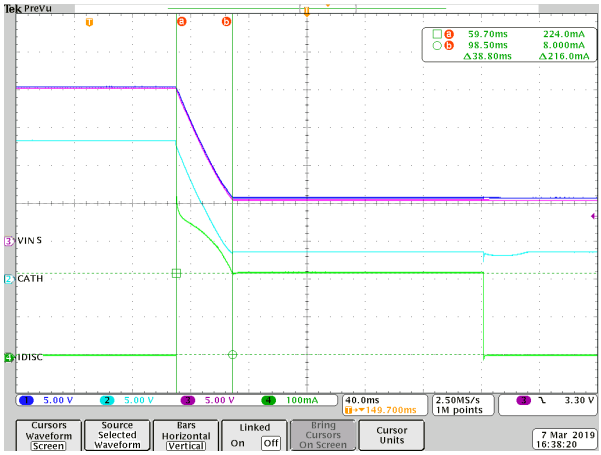


Figure 39. VBUS Discharge, from 20 V to 5 V, without a Load

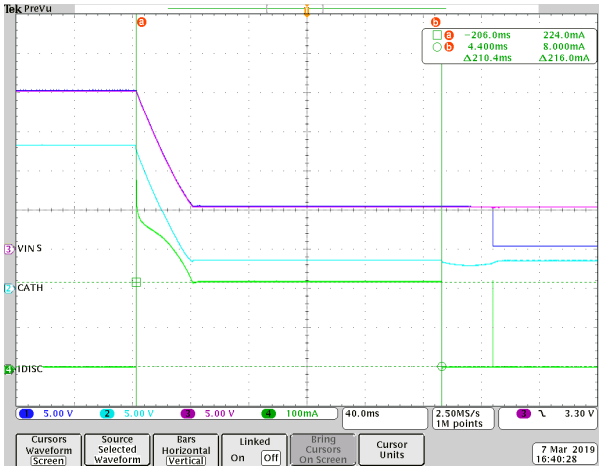


Figure 40. VBUS Discharge, from 20 V to 0 V, when Type−C Cable is Unplugged

Figure 41 is when VBUS changes from 20 V to 15 V without a load, and the Figure 42 waveform is the same voltage change, but, with a 500 mA load.

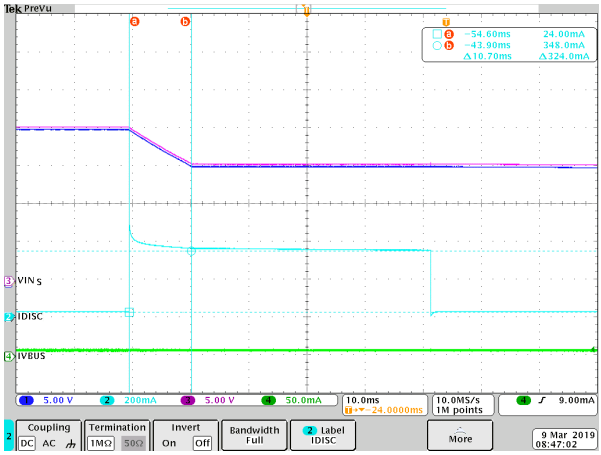


Figure 41. VBUS Discharge, from 20 V to 15 V, without a Load

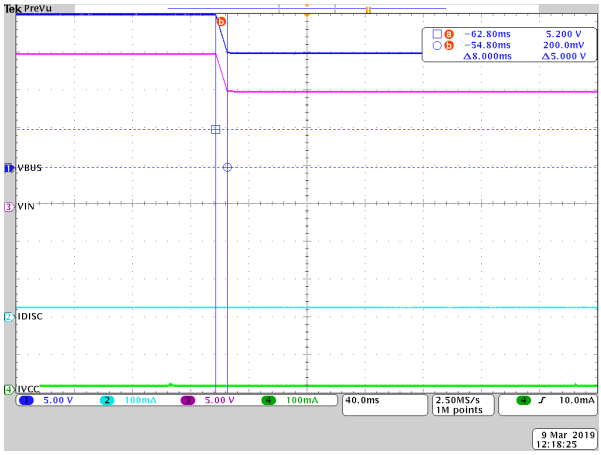


Figure 42. VBUS Discharge, from 20 V to 15 V, with a 500 mA Load

Figure 43 shows a waveform when VBUS changes from 20 V to 5 V without a load, Figure 44 shows a waveform with the same transition with a 500 mA load. If there is load above 250 mA, there is no VBUS discharge.

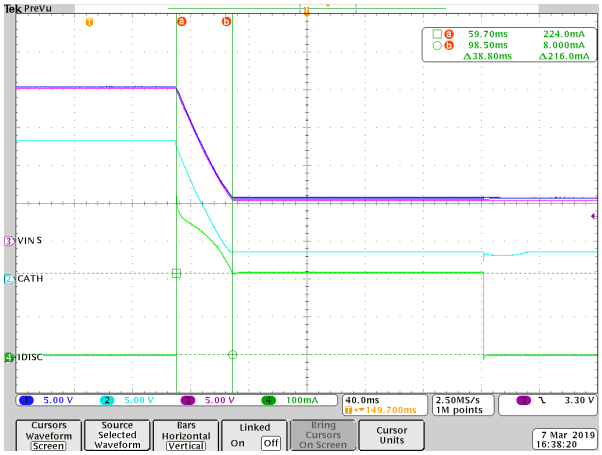


Figure 43. VBUS Discharge, from 20 V to 5 V, without a Load

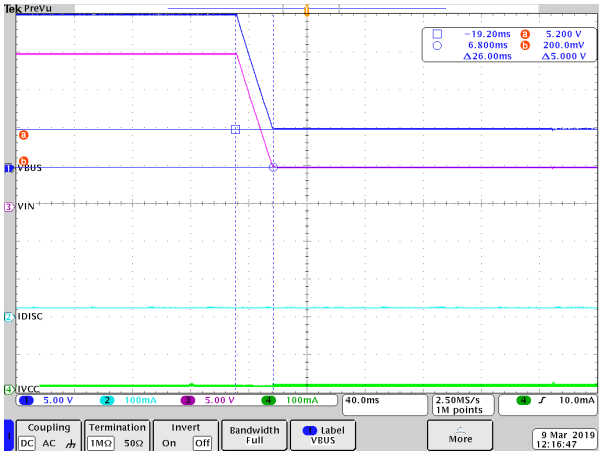


Figure 44. VBUS Discharge, from 20 V to 5 V, with a 500 mA Load

Figure 45 shows a waveform when VBUS changes from 20 V to 5 V with 2 A load and Figure 46 shows a waveform when VBUS changes from 20 V to 15 V with 2 A load as well. Due to the load, there is no VBUS discharge for either case.

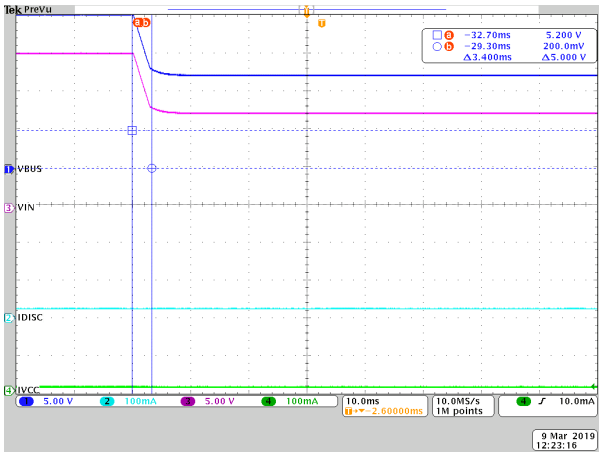


Figure 45. VBUS Discharge, from 20 V to 5 V, with a 2 A Load

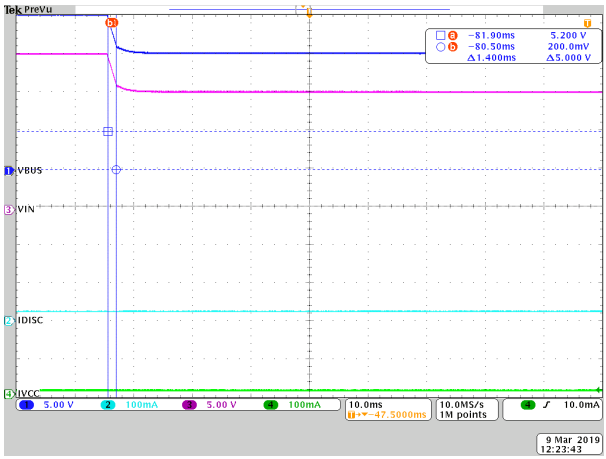


Figure 46. VBUS Discharge, from 20 V to 15 V, with a 2 A Load

VCC Discharge

VCC discharge occurs along with GATE off (external NFET off) for cases such as cable plug out or if a fault happens (OVP/OCP/OTP/UVP), so if cable is unplugged with VBUS at 9 V to 20 V, there will be both discharge on VBUS and VCC. VCC discharge occurs later than VBUS discharge. VCC discharge occurs after the NFET is open and after VBUS discharge is turned off, so the sink is not connected when VCC discharge occurs. VCC discharge timing is the same as VBUS discharge, 210 ms, but, the discharge current is constant because VCC discharge occurs when the VCC drops down to 5 V. The exception is VCC discharge at Fault, such as OCP, where VBUS discharge doesn't occur, so VCC voltage can be greater than 5 V, creating a larger VCC discharge current.

The waveform in Figure 47 is when the Type−C cable is unplugged with 5 V VBUS. As mentioned above, there is no VBUS discharge when the cable is unplugged at 5 V VBUS, but, there is VCC discharge. The waveform in Figure 48 is when the cable is unplugged at 9 V, VBUS discharge drops the VBUS voltage down to 5 V and then the external NFET opens followed by turning on VCC discharge.

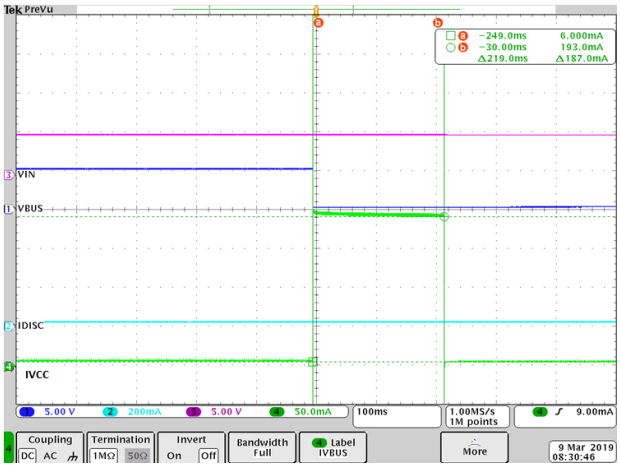


Figure 47. VCC Discharge, from 5 V, when Type−C Cable is Unplugged

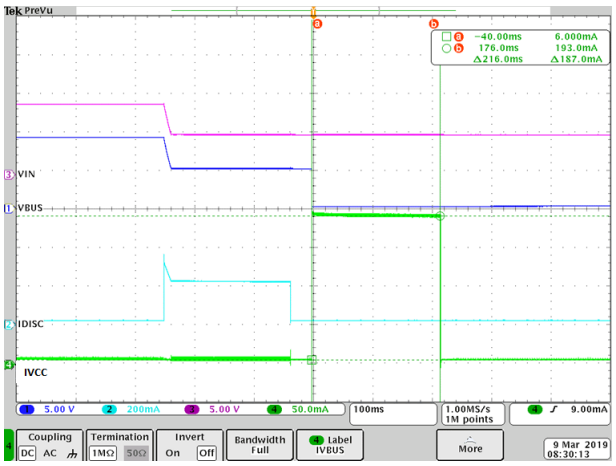


Figure 48. VCC Discharge, from 9 V, when Type−C Cable is Unplugged

The next 2 waveforms are the same, Figure 49 is a cable unplug at 15 V, and Figure 50 is a cable unplug at 20 V. Both VBUS and VCC discharges occur in series.

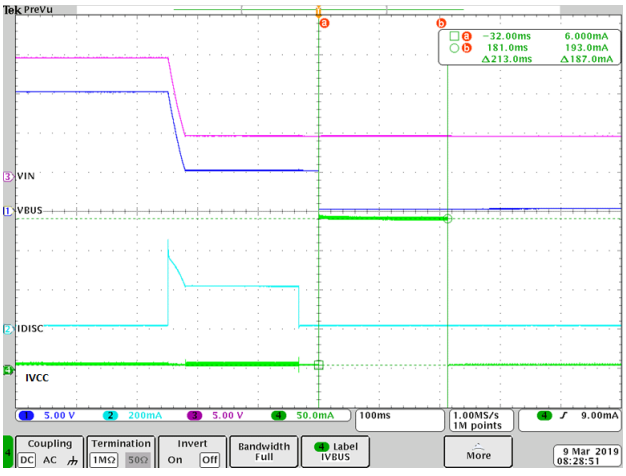


Figure 49. VCC Discharge, from 15 V, when Type−C Cable is Unplugged

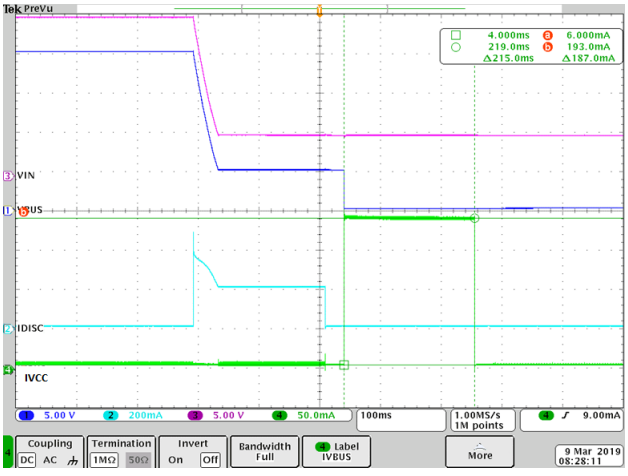


Figure 50. VCC Discharge, from 20 V, when Type−C Cable is Unplugged

BC1.2

The FUSB3307 supports BC1.2 (USB Battery Charging) along with proprietary charger support. Once a Type−C sink is attached, both D+/D− voltages increase to 2.75 V and stay at that voltage unless VDP (D+ voltage) or VDM (D− voltage) move above or below that threshold, then D+ and D− are shorted together so that a sink device having BC1.2 detection can detect the FUSB3307 as a DCP (Dedicated Charging Port). The waveform in Figure 51 shows D+/D− are the same voltage after attach.

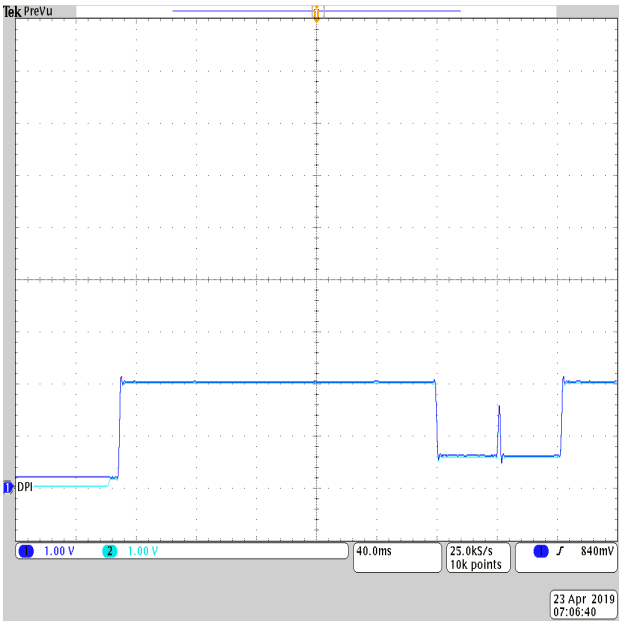


Figure 51. D+/D− Voltage after Attach

VCONN Supply

The FUSB3307 supports VCONN power to verify the cable type when sink is attached. It is enabled along with VBUS. But, VCONN is only supplied when the FUSB3307 is programmed (fuse trimmed during production) as 5 A (maximum VBUS current) capable and a cable marker IC is present in the Type−C cable. If the FUSB3307 is 3 A capable, VCONN is not enabled. If the FUSB3307 is programmed to support 5 A, VCONN is not always turned on. It is only turned on when there is Ra (1 kΩ) present on the non−communication CC channel (VCONN). In the 2 waveforms below, the waveform in Figure 52 shows a non−cable marker cable attach, while the waveform in Figure 53 shows a cable marker cable attach. There is no VCONN on the CC2 (the non−communication channel or VCONN) regardless of cable type because the FUSB3307 device used was only 3 A capable.

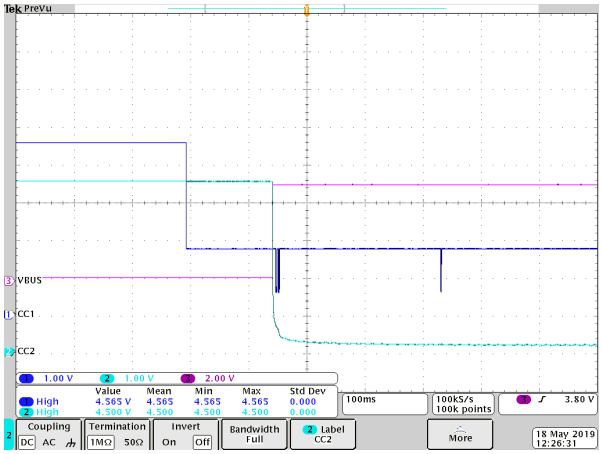


Figure 52. VCONN when Non−cable Marker Cable is Attached (FUSB3307 w/3A Support)

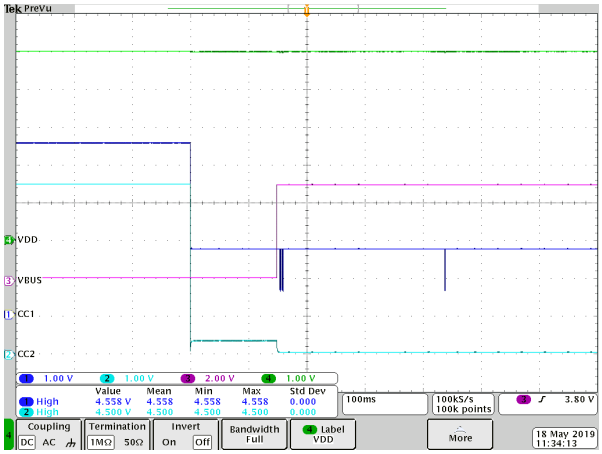


Figure 53. VCONN when Cable Marker Cable is Attached (FUSB3307 w/3A Support)

The two waveforms below are when the FUSB3307 is programmed to support 5 A. The waveform in Figure 54 is with a non−cable marker cable. If Ra is not present, VCONN gets turned off when Vbus is supplied. The waveform in Figure 55, where Ra is present (cable marker cable), VCONN is enabled on CC2 and valid until the cable ID is verified which takes about 50 ms.

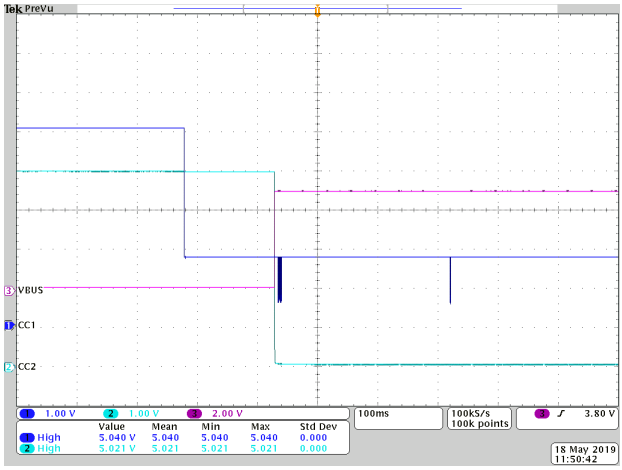


Figure 54. VCONN when Non−cable Marker Cable is Attached (FUSB3307 w/3A Support)

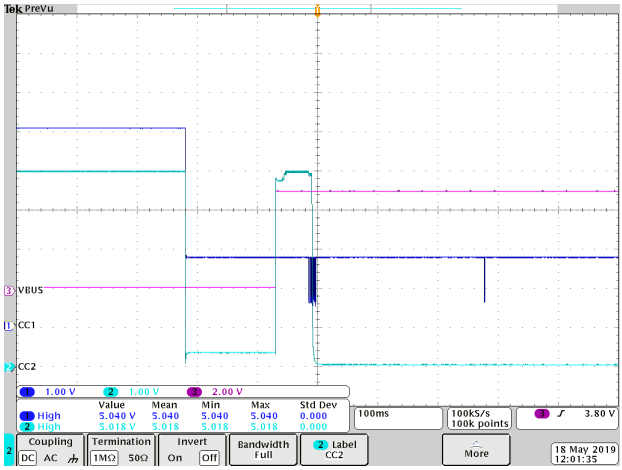
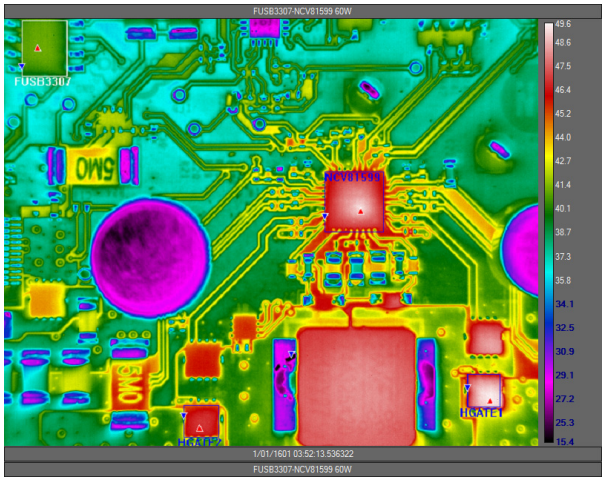


Figure 55. VCONN when Cable Marker Cable is Attached (FUSB3307 w/3A Support)

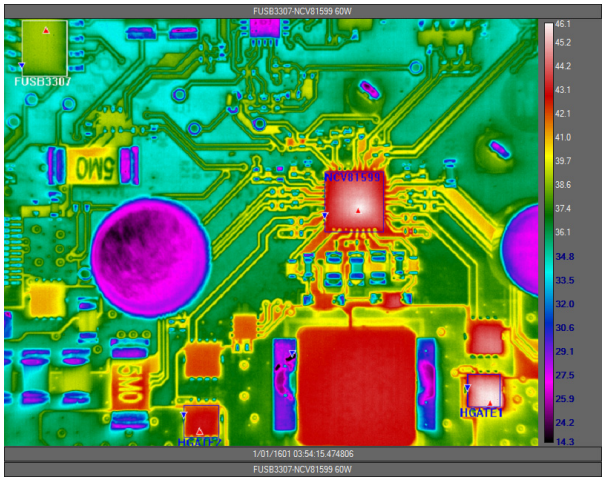
Thermal Measurements

Figure 56 shows the thermals for 15 W (5 V/3 A) and Figure 57 shows the thermals for 27 W (9 V/3 A).



15 W − 5 V/3 A	
Region	Max (°C)
FUSB3307	40
NCV81599	47
BUCK FET (HGATE1)	48
BOOST FET (HGATE2)	46

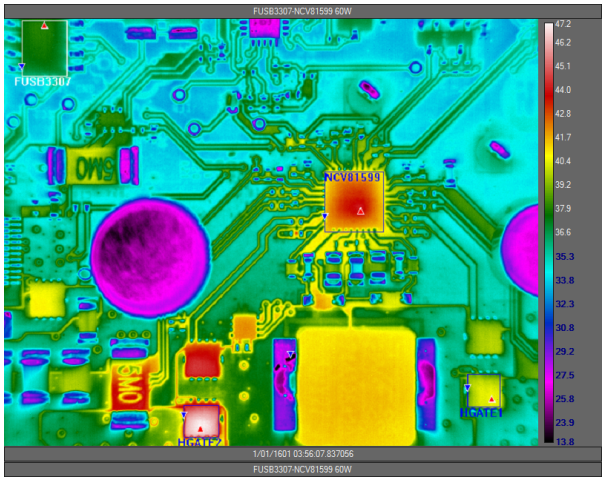
Figure 56. Thermal Image and Data for 15 W (5 V/3 A)



27 W − 9 V/3 A	
Region	Max (°C)
FUSB3307	38
NCV81599	44
BUCK FET (HGATE1)	45
BOOST FET (HGATE2)	42

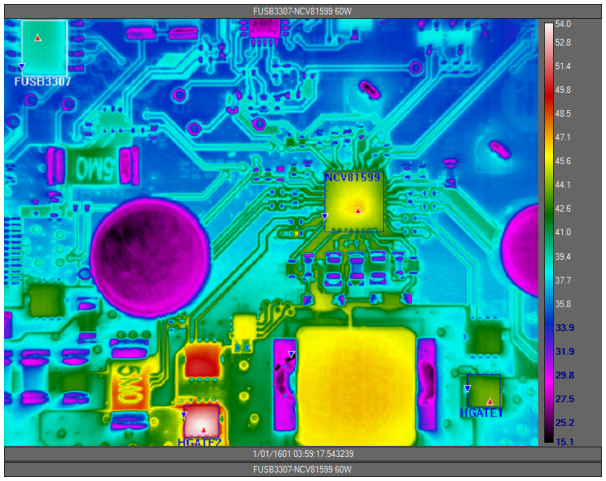
Figure 57. Thermal Image and Data for 27 W (9 V/3 A)

Figure 58 shows the thermals for 36 W (12 V/3 A) and Figure 59 shows the thermals for 45 W (15 V/3 A).



36 W − 12 V/3 A	
Region	Max (°C)
FUSB3307	37
NCV81599	42
BUCK FET (HGATE1)	40
BOOST FET (HGATE2)	46

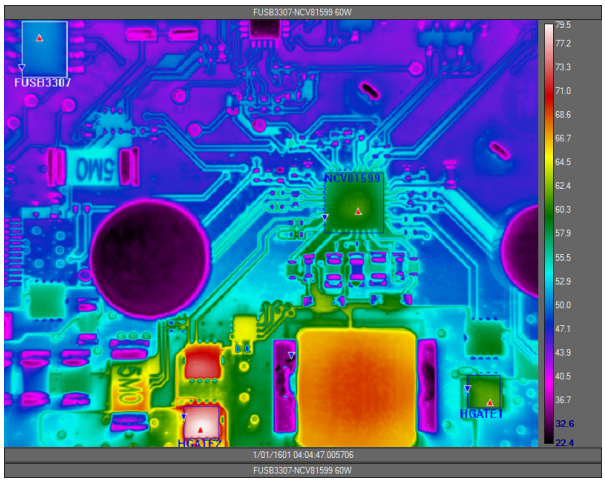
Figure 58. Thermal Image and Data for 36 W (12 V/3 A)



45 W − 15 V/3 A	
Region	Max (°C)
FUSB3307	39
NCV81599	45
BUCK FET (HGATE1)	43
BOOST FET (HGATE2)	52

Figure 59. Thermal Image and Data for 45 W (15 V/3 A)

Figure 60 shows the thermals for 60 W (20 V/3 A).



60 W − 20 V/3 A	
Region	Max (°C)
FUSB3307	49
NCV81599	58
BUCK FET (HGATE1)	60
BOOST FET (HGATE2)	76

Figure 60. Thermal Image and Data for 60 W (20 V/3 A)

USB−IF PD Compliance Testing Results

The FUSB3307D6MX passed testing for USB PD3.0 with PPS at the USB−IF PD Compliance Workshop #114 the week of June 10, 2019, using the STR−FUSB3307MX−PPS−GEVB. TID: 1430.

QuadraMAX − v0.8.7074

·**PASSED**

LeCroy − v3.81 build 836

·**PASSED**

GRL − SW v1.3.14.0 / FW v1.3.14.0.324

·**PASSED**

MQP − v6.06.08

·**PASSED**

USB2.0 Electricals

·**PASSED**

Type−C and PD IOP

- test against Google phone, Google laptop, and Macbook

·**PASSED**

Ellisys − v3.1.7095

·**PASSED**

BILL OF MATERIALS (BOM)

Table 1. BILL OF MATERIALS

Qty	Part Reference	Value	Package	Voltage	MFR	MFRPN	2nd Source-able?
9	C1 C2 C3 C4 C5 C8 C11 C15 C26	10uF	1210	50V	TDK	CGA6P3X7S1H106K250AE	Yes
4	C6 C31 C38 C39	1uF	0402	10V	Murata	GCM155C71A105KE38	Yes
2	C7 C19	1uF	0603	25V	Murata	GCM188R71E105KA64	Yes
3	C9 C10 C12	4.7uF	0805	10V	Murata	GCM21BC71A475KA73L	Yes
2	C13 C14	0.1uF	0603	50V	Murata	GCM188R71H104KA57D	Yes
1	C16	330uF	TH_8mm	35V	Illinois	337AVG035MGBJ	Yes
1	C17	100uF	TH_8mm	35V	Nichicon	RL81V101MDN1KX	Yes
2	C20 C21	10nF	0402	50V	Murata	GCM155R71H103KA55D	Yes
1	C22	1uF	0603	16V	Murata	GCM188R71C105KA64J	Yes
3	C23 C25 C35	1nF	402	50V	Murata	GCM155R71H102KA37D	Yes
2	C24 C27	390pF	0402	50V	Murata	GRM1555C1H391JA01D	Yes
1	C28	100pF	0402	50V	Murata	GRM1555C1H101GA01D	Yes
1	C29	1uF	0402	50V	Taiyo Yuden	UMK105CBJ105MV−F	Yes
1	C30	0.47uF	0402	35V	Murata	GRT155R6YA474KE01D	Yes
2	C32 C34	470pF	0402	50V	Murata	GCM155R71H471KA37D	Yes
1	C33	47nF	0402	50V	Murata	GRM155R71H473KE14D	Yes
2	C36 C37	1uF	0402	16V	Murata	GRM155C81C105KE11D	Yes
1	C40	100nF	0402	50V	Murata	GCM155R71H104ME02	Yes
2	D1 D2	NSVR0240V2	SOD−523	40V	ON Semiconductor	NSVR0240V2T1G	No
1	D3	SZMM3Z18VT1G	SOD−323	18V	ON Semiconductor	SZMM3Z18VT1G	No
1	D4	SZNZ9F3V3	SOD−923	3.3V	ON Semiconductor	NZ9F3V3T5G	No
1	D5	SZ1SMB30CAT3G	SMB	30V	Littelfuse	SZ1SMB30CAT3G	Yes
3	D6 D7 D9	SZESD7241	X2DFN2	25V	ON Semiconductor	SZESD7241N2T5G	No
1	FB1	50@100M	1206		Murata	BLM31SN500SZ1L	Yes
1	J1	632 723 300 011			Wurth Elektronik	632723300011	Yes
3	J2 J4 J5	613 002 111 21	1x2pin 100mil		Wurth Elektronik	61300211121	Yes
1	J3	691216710002	2−Pin Screw		Weidmuller	1716020000	Yes
1	J6	SGAP0	SGAP0		Wurth Elektronik	613016243121	Yes
1	L1	4.2 uH			Wurth Elektronik	744 325 420	No
1	L2	160nH	7x7mm		Coilcraft	XAL5030−161MEC	No
4	Q1 Q2 Q3 Q4	NVTFS4C10N	u8−FL	30V	ON Semiconductor	NVTFS4C10NWFTAG	No
1	Q5	NVTFS002N04CL	u8−FL	40V	ON Semiconductor	NVTFS002N04CLTAG	No
1	Q6	NVMFS5A140PLZ	SO8−FL	−40V	ON Semiconductor	NVMFS5A140PLZWFT1G	No
2	Q7 Q8	2V7002W	SOT−323	60V	ON Semiconductor	2V7002WT1G	No
3	Q9 Q10 Q11	2V7002L	SOT−23	60V	ON Semiconductor	2V7002LT1G	No
2	R1 R24	0.005	2512		Panasonic	ERJ−M1WSF5M0U	Yes
1	R2	0.004	2512		Panasonic	ERJ−M1WSF4M0U	Yes
1	R3	20k	0402		Yageo	RC0402FR−0720KL	Yes
6	R4 R5 R11 R12 R29 R30	0	0402		Yageo	RC0402JR−070RL	Yes
1	R6	10k	0603		Yageo	SR0603FR−7T10KL	Yes

Table 1. BILL OF MATERIALS (continued)

Qty	Part Reference	Value	Package	Voltage	MFR	MFRPN	2nd Source-able?
2	R7 R8	1.0	0402		Yageo	RC0402FR−071RL	Yes
2	R9 R10	4.02	0402		Vishay	CRCW04024R02FKEDC	Yes
5	R13 R15 R17 R18 R49	10	0402		Yageo	RC0402FR−0710RL	Yes
1	R16	1k	1206		Vishay	CRCW12061K00JNEA	Yes
1	R20	6.8k	0402		Yageo	RC0402FR−076K8L	Yes
1	R21	301k	0402		KOA Speer	RK73H1ETTP3013F	Yes
2	R22 R23	24.3k	0402		Yageo	RC0402FR−0724K3L	Yes
3	R25 R52 R53	DNP	0402			DNP	
10	R26 R27 R28 R32 R37 R42 R45 R48 R54 R57	10k	0402		Yageo	RC0402FR−0710KL	Yes
5	R31 R33 R43 R44 R47	1K	0402		Yageo	RC0402FR−071KL	Yes
1	R35	47k	0402		Yageo	RC0402FR−0747KL	Yes
1	R36	220k	0402		Yageo	RC0402FR−07220KL	Yes
1	R38	13.3k	0402		Yageo	RC0402FR−0713K3L	Yes
1	R39	120k	0402		Yageo	RC0402FR−07120KL	Yes
1	R40	34K	0402		Yageo	RC0402FR−0734KL	Yes
1	R41	100K	0402		Yageo	RC0402FR−07100KL	Yes
1	R46	9.09K	0402		Yageo	RC0402FR−079K09L	Yes
2	R50 R51	82.5	1210		Panasonic	ERJ−14NF82R5U	Yes
1	R55	24.9K	0402		Yageo	RC0402FR−0724K9L	Yes
1	R56	226K	0402		Yageo	RC0402FR−07226KL	Yes
1	RT1	100k	0402		Murata	NCP15WF104F03RC	Yes
5	TP1 TP2 TP9 TP15 TP17	5007	63mil		Keystone Electronics	5006	
1	U1	NCT375	DFN8 2x2mm		ON Semiconductor	NCT375MNR2G	No
1	U2	NCV81599	QFN32 5x5		ON Semiconductor	NCV81599MWTXG	No
1	U3	NCV213R	SC−70−6		ON Semiconductor	NCV213RSQT2G	No
1	U4	CAT24C512	UDFN−8		ON Semiconductor	CAT24C512HU5IGT3	No
1	U5	FUSB3307	SOIC−14		ON Semiconductor	FUSB3307D6MX	No
1	U6	DNP	QFNW20		ON Semiconductor	DNP	No
1	U7	NIV1161	WDFN6		ON Semiconductor	NIV1161MTTAG	No

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