NCT72

±1°C Temperature Monitor with Series Resistance Cancellation

The NCT72 is a dual-channel digital thermometer and undertemperature/overtemperature alarm, intended for use in PCs and thermal management systems. It is pin and register compatible with the NCT1008 but the NCT72 allows the user to pull the $\overline{\text{ALERT}}$ pin to 1.8 V without increasing the device Idd. A feature of the NCT72 is series resistance cancellation, where up to 1.5 kΩ (typical) of resistance in series with the temperature monitoring diode can be automatically cancelled from the temperature result, allowing noise filtering. The NCT72 has a configurable $\overline{\text{ALERT}}$ output and an extended, switchable temperature measurement range.

The NCT72 can measure the temperature of a remote thermal diode accurate to ±1°C and the ambient temperature accurate to ±3°C. The temperature measurement range defaults to 0°C to +127°C, compatible with the NCT1008, but it can be switched to a wider measurement range of −64°C to +191°C.

The NCT72 communicates over a 2-wire serial interface, compatible with system management bus (SMBus/I^{2}C) standards. The default SMBus/I^{2}C address of the NCT72 is 0x4C. An NCT72D is available with an SMBus/I^{2}C address of 0x4D. This is useful if more than one NCT72 is used on the same SMBus/I^{2}C.

An $\overline{\text{ALERT}}$ output signals when the on-chip or remote temperature is out of range. The $\overline{\text{THERM}}$ output is a comparator output that allows on/off control of a cooling fan. The $\overline{\text{ALERT}}$ output can be reconfigured as a second $\overline{\text{THERM}}$ output, if required.

Features

- On-chip and Remote Temperature Sensor
- 0.25°C Resolution/1°C Accuracy on Remote Channel
- 1°C Resolution/1°C Accuracy on Local Channel
- Series Resistance Cancellation Up to 1.5 kΩ
- Extended, Switchable Temperature Measurement Range 0°C to +127°C (Default) or –64°C to +191°C
- Pin and Register Compatible with NCT1008
- Remote $\overline{\text{THERM}}$ Limit of 108°C
- 2-wire SMBus/I^{2}C Serial Interface with SMBus Alert Support
- Programmable Over/Undertemperature Limits
- Offset Registers for System Calibration
- Up to Two Overtemperature Fail-safe $\overline{\text{THERM}}$ Outputs
- Small 8-lead DFN
- 240 μA Operating Current, 5 μA Standby Current
- Compatible with 1.8 V Logic
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

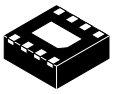
- Smart Phones
- Desktop and Notebook Computers
- Smart Batteries

ON Semiconductor®

www.onsemi.com

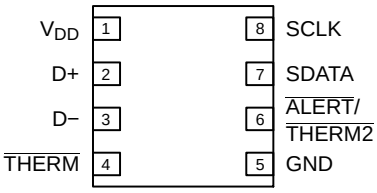


WDFN8
CASE 511AT



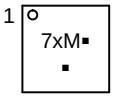
DFN8
CASE 506BJ

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAMS



WDFN8

7x = Device Code (Where x = C or D)
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)



DFN8

x = C or D
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

© Semiconductor Components Industries, LLC, 2012

- Automotive
- Embedded Systems

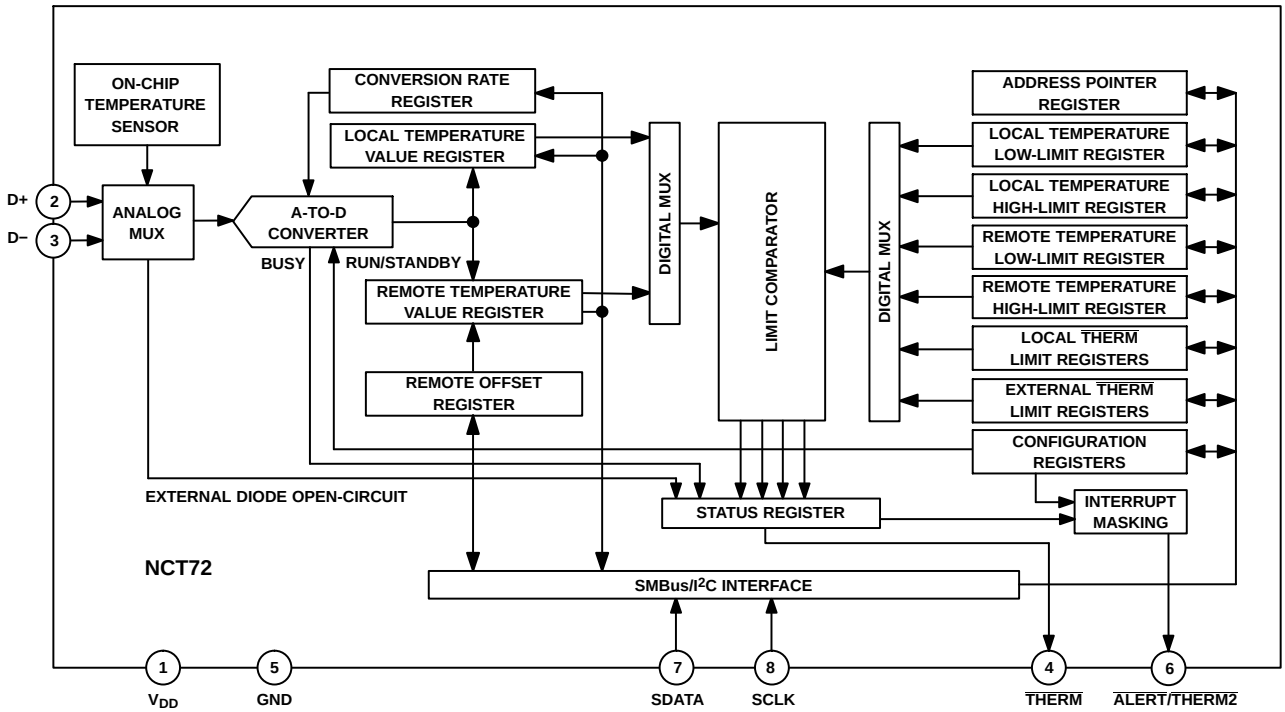


Figure 1. Functional Block Diagram

Table 1. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Supply, 2.8 V to 3.6 V.
2	D+	Positive Connection to Remote Temperature Sensor.
3	D−	Negative Connection to Remote Temperature Sensor.
4	$\overline{\text{THERM}}$	Open-drain Output. Can be used to turn a fan on/off or throttle a CPU clock in the event of an overtemperature condition. Requires pullup resistor.
5	GND	Supply Ground Connection.
6	$\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$	Open-drain Logic Output Used as Interrupt or SMBus $\overline{\text{ALERT}}$. This can also be configured as a second $\overline{\text{THERM}}$ output. Requires pullup resistor.
7	SDATA	Logic Input/Output, SMBus Serial Data. Open-drain Output. Requires pullup resistor.
8	SCLK	Logic Input, SMBus Serial Clock. Requires pullup resistor.

NOTE: The ground slug on 3x3 package can be left unconnected.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{DD}) to GND	−0.3, +3.6	V
D+	−0.3 to V_{DD} + 0.3	V
D− to GND	−0.3 to +0.6	V
SCLK, SDATA, $\overline{\text{ALERT}}$, $\overline{\text{THERM}}$	−0.3 to +3.6	V
Input Current, SDATA, $\overline{\text{THERM}}$	−1, +50	mA
Input Current, D−	±1	mA
ESD Rating, All Pins (Human Body Model)	1,500	V
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 3. THERMAL CHARACTERISTICS (Note 1)

Package Type	θ_{JA}	θ_{JC}	Unit
8-lead DFN	142	43.74	°C/W

1. θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. SMBus/I²C TIMING SPECIFICATIONS (Note 1)

Parameter	Limit at T_{MIN} and T_{MAX}	Unit	Description
f_{SCLK}	400	kHz max	−
t_{LOW}	1.3	μs min	Clock Low Period, between 10% Points
t_{HIGH}	0.6	μs min	Clock High Period, between 90% Points
t_R	300	ns max	Clock/Data Rise Time
t_F	300	ns max	Clock/Data Fall Time
$t_{SU;\ STA}$	600	ns min	Start Condition Setup Time
$t_{HD;\ STA}$ (Note 2)	600	ns min	Start Condition Hold Time
$t_{SU;\ DAT}$ (Note 3)	100	ns min	Data Setup Time
$t_{SU;\ STO}$ (Note 4)	600	ns min	Stop Condition Setup Time
t_{BUF}	1.3	μs min	Bus Free Time between Stop and Start Conditions

1. Guaranteed by design, but not production tested.
2. Time from 10% of SDATA to 90% of SCLK.
3. Time for 10% or 90% of SDATA to 10% of SCLK.
4. Time for 90% of SCLK to 10% of SDATA.

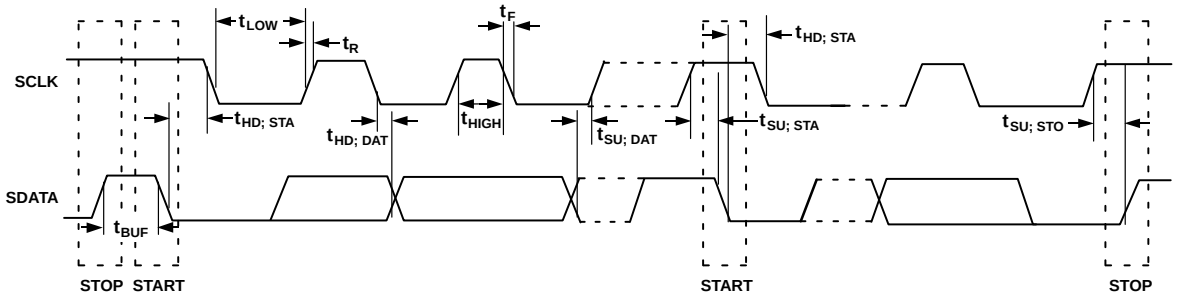


Figure 2. Serial Bus Timing

Table 5. ELECTRICAL CHARACTERISTICS (T_A = −40°C to +125°C, V_{DD} = 2.8 V to 3.6 V, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage, V_{DD}		2.8	3.30	3.6	V
Average Operating Supply Current, I_{DD}	0.0625 Conversions/Sec Rate (Note 1) Standby Mode	− −	240 5.0	350 30	μA
Undervoltage Lockout Threshold	V_{DD} Input, Disables ADC, Rising Edge	−	2.55	−	V
Power-on Reset Threshold		1.0	−	2.56	V
Temperature-to-digital Converter					
Local Sensor Accuracy 3.0 V to 3.6 V	0°C ≤ T_A ≤ +70°C 0°C ≤ T_A ≤ +85°C	− −	− −	±1.0 ±1.5	°C
Local Sensor Accuracy 2.8 V to 3.6 V	−20°C ≤ T_A ≤ +110°C	−	−	±2.5	°C
Resolution		−	1.0	−	°C
Remote Diode Sensor Accuracy 3.0 V to 3.6 V	0°C ≤ T_A ≤ +70°C, −55°C ≤ T_D (Note 2) ≤ +150°C 0°C ≤ T_A ≤ +85°C, −55°C ≤ T_D (Note 2) ≤ +150°C −40°C ≤ T_A ≤ +100°C, −55°C ≤ T_D (Note 2) ≤ +150°C	− − −	− − −	±1.0 ±1.5 ±2.5	°C
Remote Diode Sensor Accuracy 3.3 V	−20°C ≤ T_A ≤ +70°C, −55°C ≤ T_D ≤ +150°C	−	−	±1.0	°C
Remote Diode Sensor Accuracy 2.8 V to 3.6 V	0°C ≤ T_A ≤ +70°C, −20°C ≤ T_D ≤ +110°C −20°C ≤ T_A ≤ +110°C, T_D = +40°C	− −	− −	±1.5 ±2.25	°C
Resolution		−	0.25	−	°C
Remote Sensor Source Current	High Level (Note 3) Middle Level (Note 3) Low Level (Note 3)	− − −	220 82 13.5	− − −	μA
Conversion Time	From Stop Bit to Conversion Complete, One-shot Mode with Averaging Switched On	−	40	52	ms
	One-shot Mode with Averaging Off (That Is, Conversion Rate = 16-, 32-, or 64-conversions per Second)	−	6.0	8.0	ms
Maximum Series Resistance Cancelled	Resistance split evenly on both the D+ and D– inputs	−	1.5	−	kΩ
Open-drain Digital Outputs ($\overline{\text{THERM}}$, $\overline{\text{ALERT}}$/THERM2)					
Output Low Voltage, V_{OL}	I_{OUT} = −6.0 mA	−	−	0.4	V
High Level Output Leakage Current, I_{OH}	V_{OUT} = V_{DD}	−	0.1	1.0	μA
SMBus/I²C Interface (Note 3 and 4)					
Logic Input High Voltage, V_{IH} SCLK, SDATA		1.4	−	−	V
Logic Input Low Voltage, V_{IL} SCLK, SDATA		−	−	0.8	V
Hysteresis		−	500	−	mV
SDA Output Low Voltage, V_{OL}	I_{OUT} = −6.0 mA	−	−	0.4	V
Logic Input Current, I_{IH}, I_{IL}		−1.0	−	+1.0	μA
SMBus Input Capacitance, SCLK, SDATA		−	5.0	−	pF
SMBus Clock Frequency		−	−	400	kHz
SMBus Timeout (Note 5)	User Programmable	−	25	64	ms
SCLK Falling Edge to SDATA Valid Time	Master Clocking in Data	−	−	1.0	μs

1. See Table 9 for information on other conversion rates.
2. Guaranteed by characterization, but not production tested.
3. Guaranteed by design, but not production tested.
4. See SMBus/I²C Timing Specifications section for more information.
5. Disabled by default. Detailed procedures to enable it are in the Serial Bus Interface section of the datasheet.

TYPICAL PERFORMANCE CHARACTERISTICS

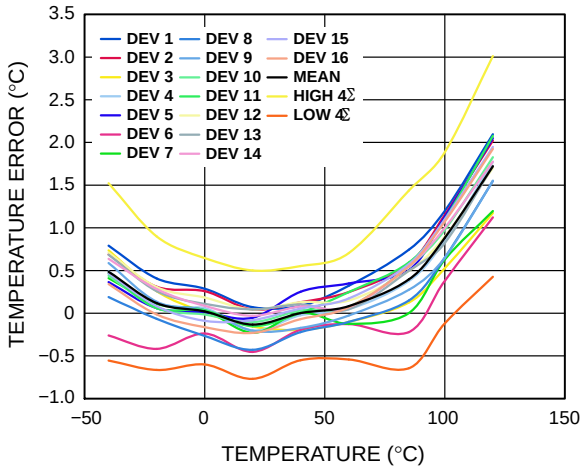


Figure 3. Local Temperature Error vs. Temperature

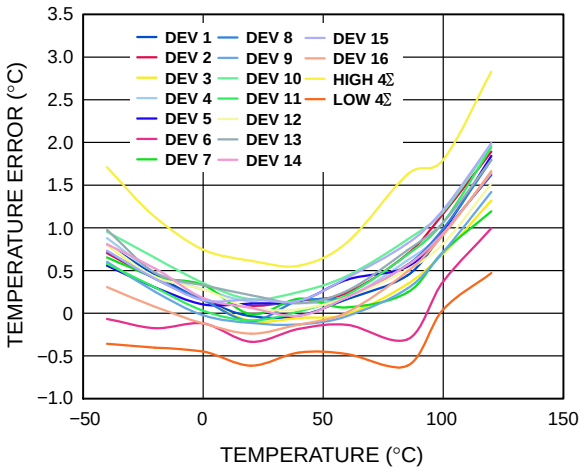


Figure 4. Remote Temperature Error vs. Actual Temperature

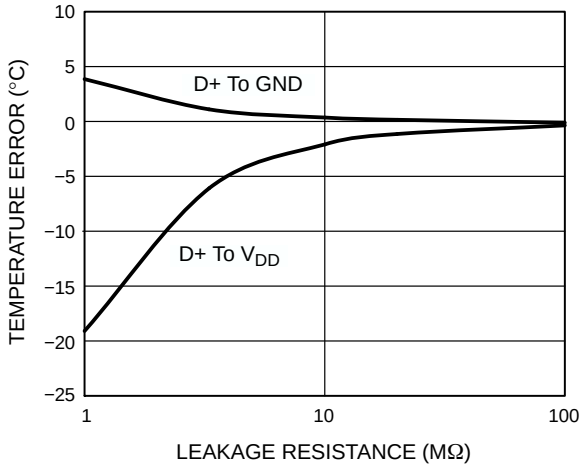


Figure 5. Temperature Error vs. D+/D− Leakage Resistance

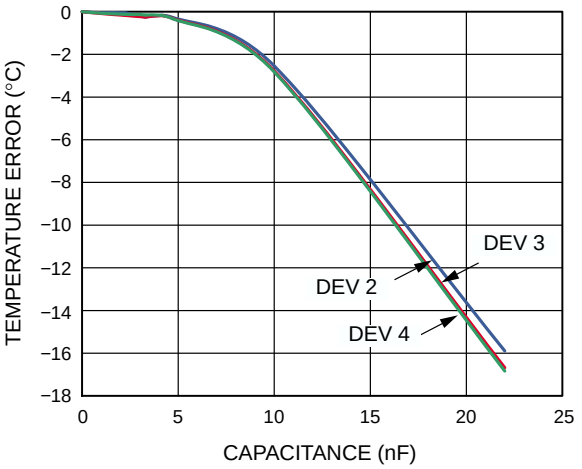


Figure 6. Temperature Error vs. D+/D− Capacitance

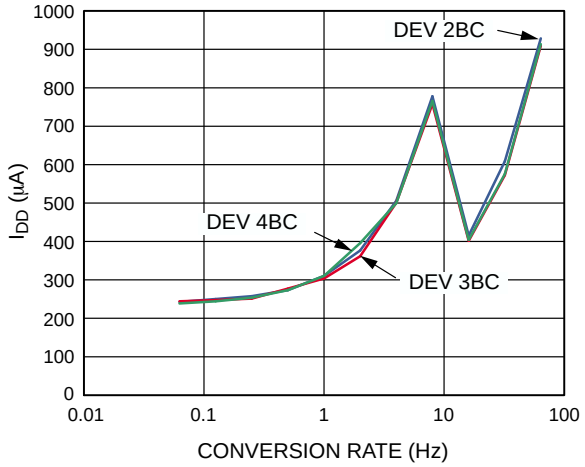


Figure 7. Operating Supply Current vs. Conversion Rate

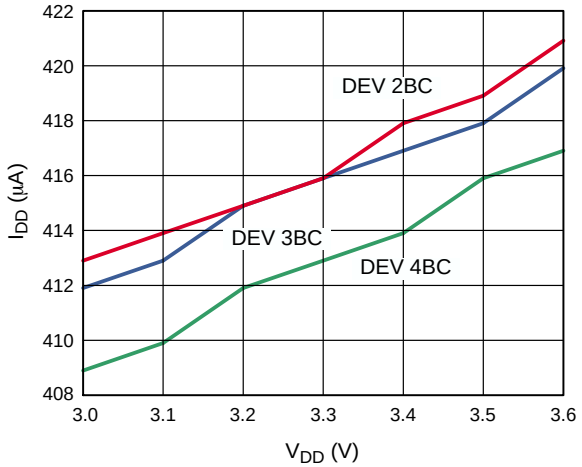


Figure 8. Operating Supply Current vs. Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

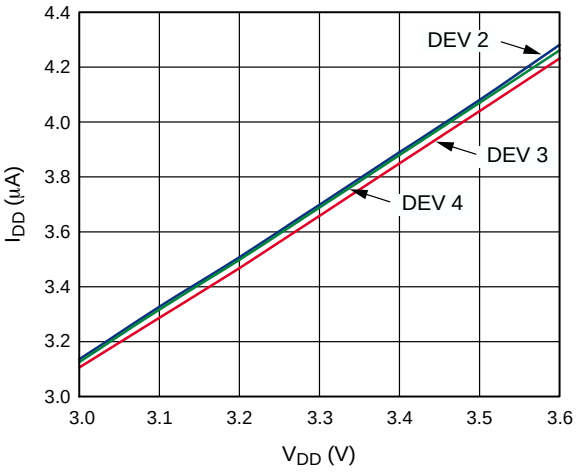


Figure 9. Standby Supply Current vs. Voltage

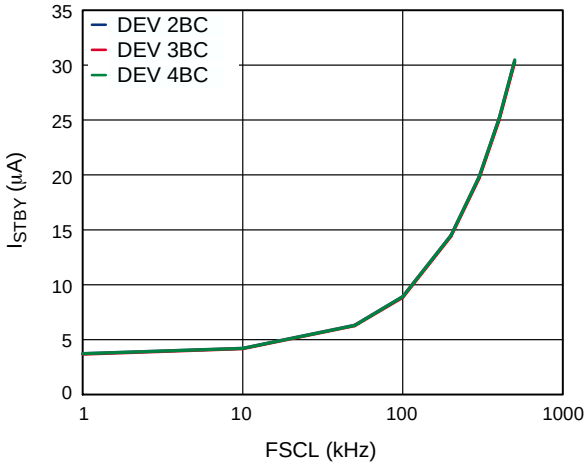


Figure 10. Standby Supply Current vs. Clock Frequency

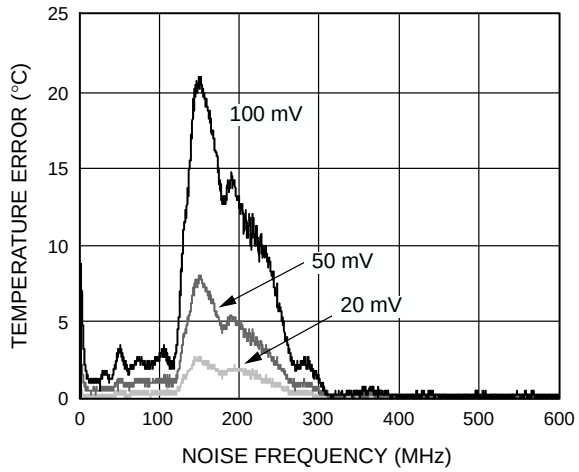


Figure 11. Temperature Error vs. Common-mode Noise Frequency

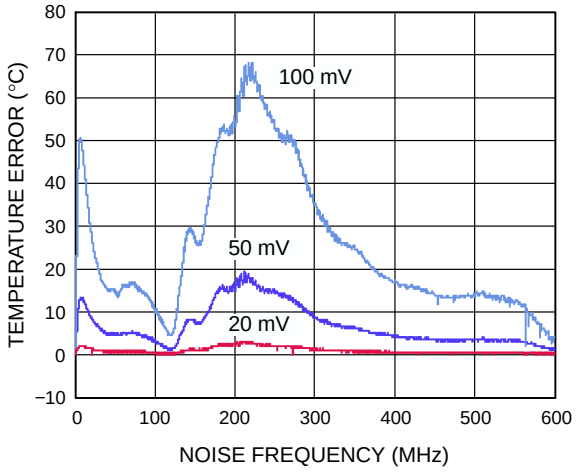


Figure 12. Temperature Error vs. Differential-mode Noise Frequency

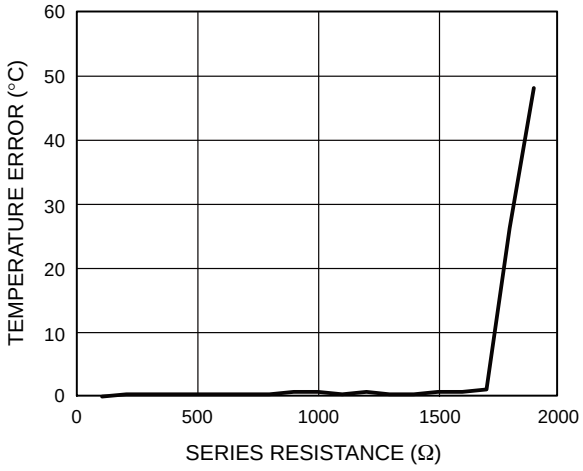


Figure 13. Temperature Error vs. Series Resistance

Theory of Operation

The NCT72 is a local and remote temperature sensor and over/under temperature alarm, with the added ability to automatically cancel the effect of 1.5 kΩ (typical) of resistance in series with the temperature monitoring diode. When the NCT72 is operating normally, the on-board ADC operates in a free running mode. The analog input multiplexer alternately selects either the on-chip temperature sensor to measure its local temperature or the remote temperature sensor. The ADC digitizes these signals and the results are stored in the local and remote temperature value registers.

The local and remote measurement results are compared with the corresponding high, low, and $\overline{\text{THERM}}$ temperature limits, stored in eight on-chip registers. Out-of-limit comparisons generate flags that are stored in the status register. A result that exceeds the high temperature limit or the low temperature limit causes the $\overline{\text{ALERT}}$ output to assert. The $\overline{\text{ALERT}}$ output also asserts if an external diode fault is detected. Exceeding the $\overline{\text{THERM}}$ temperature limits causes the $\overline{\text{THERM}}$ output to assert low. The $\overline{\text{ALERT}}$ output can be reprogrammed as a second $\overline{\text{THERM}}$ output.

The limit registers are programmed and the device controlled and configured via the serial SMBus. The contents of any register are also read back via the SMBus.

Control and configuration functions consist of switching the device between normal operation and standby mode, selecting the temperature measurement range, masking or enabling the $\overline{\text{ALERT}}$ output, switching Pin 6 between $\overline{\text{ALERT}}$ and $\overline{\text{THERM2}}$, and selecting the conversion rate.

Series Resistance Cancellation

Parasitic resistance to the D+ and D− inputs to the NCT72, seen in series with the remote diode, is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per ohm of parasitic resistance in series with the remote diode.

The NCT72 automatically cancels the effect of this series resistance on the temperature reading, giving a more accurate result, without the need for user characterization of this resistance. The NCT72 is designed to automatically cancel typically up to 1.5 kΩ of resistance. By using an advanced temperature measurement method, this process is transparent to the user. This feature permits resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the section on Noise Filtering for more details.

Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

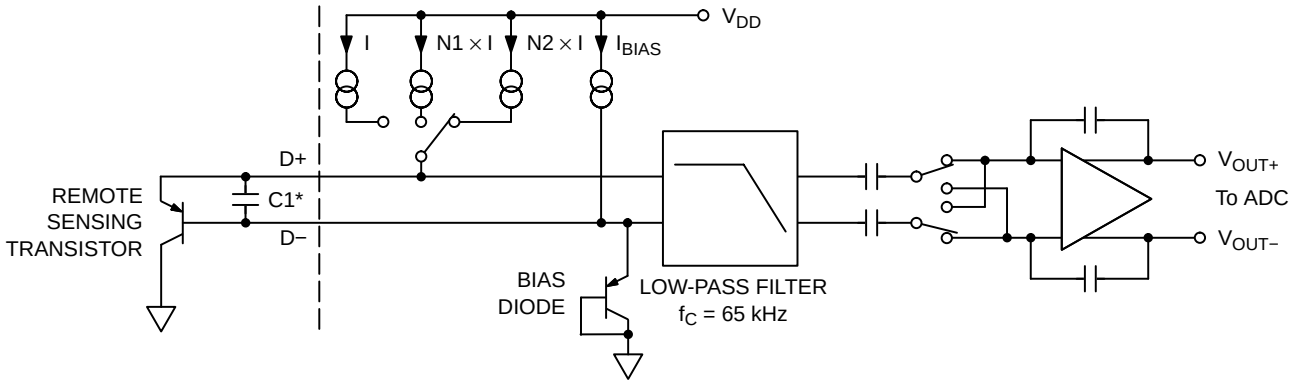
The technique used in the NCT72 measures the change in V_{BE} when the device operates at three different currents. Previous devices used only two operating currents, but it is the use of a third current that allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 14 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it can equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded but is linked to the base. To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D− input. C1 may be added as a noise filter (a recommended maximum value of 1,000 pF). However, a better option in noisy environments is to add a filter, as described in the Noise Filtering section. See the Layout Considerations section for more information on C1.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. As shown in Figure 14, $N1 \times I$ and $N2 \times I$ are different multiples of the current, I. The currents through the temperature diode are switched between I and $N1 \times I$, giving ΔV_{BE1}; and then between I and $N2 \times I$, giving ΔV_{BE2}. The temperature is then calculated using the two ΔV_{BE} measurements. This method also cancels the effect of any series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then to a chopper-stabilized amplifier. This amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage producing a temperature measurement. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles for low conversion rates. At rates of 16-, 32-, and 64-conversions/second, no digital averaging occurs.

Signal conditioning and measurement of the internal temperature sensor are performed in the same manner.



*CAPACITOR C1 IS OPTIONAL. IT IS ONLY NECESSARY IN NOISY ENVIRONMENTS. C1 = 1,000 pF MAX.

Figure 14. Input Signal Conditioning

Temperature Measurement Results

The results of the local and remote temperature measurements are stored in the local and remote temperature value registers and compared with limits programmed into the local and remote high and low limit registers.

The local temperature value is in Register 0x00 and has a resolution of 1°C. The external temperature value is stored in two registers, with the upper byte in Register 0x01 and the lower byte in Register 0x10. Only the two MSBs in the external temperature low byte are used giving the external temperature measurement a resolution of 0.25°C. Table 6 lists the data format for the external temperature low byte.

Table 6. EXTENDED TEMPERATURE RESOLUTION (REMOTE TEMPERATURE LOW BYTE)

Extended Resolution	Remote Temperature Low Byte
0.00°C	0 000 0000
0.25°C	0 100 0000
0.50°C	1 000 0000
0.75°C	1 100 0000

When reading the full external temperature value, read the LSB first. This causes the MSB to be locked (that is, the ADC does not write to it) until it is read. This feature ensures that the results read back from the two registers come from the same measurement.

Temperature Measurement Range

The temperature measurement range for both internal and external measurements is, by default, 0°C to +127°C. However, the NCT72 can be operated using an extended temperature range. The extended measurement range is −64°C to +191°C. Therefore, the NCT72 can be used to measure the full temperature range of an external diode, from −55°C to +150°C.

The extended temperature range is selected by setting Bit 2 of the configuration register to 1. The temperature range is 0°C to 127°C when Bit 2 equals 0. A valid result is available in the next measurement cycle after changing the temperature range.

In extended temperature mode, the upper and lower temperature that can be measured by the NCT72 is limited by the remote diode selection. The temperature registers can have values from −64°C to +191°C. However, most temperature sensing diodes have a maximum temperature range of −55°C to +150°C. Above +150°C, they may lose their semiconductor characteristics and approximate conductors instead. This results in a diode short. In this case, a read of the temperature result register gives the last good temperature measurement. Therefore, the temperature measurement on the external channel may not be accurate for temperatures that are outside the operating range of the remote sensor.

It should be noted that although both local and remote temperature measurements can be made while the part is in extended temperature mode, the NCT72 itself should not be exposed to temperatures greater than those specified in the absolute maximum ratings section. Further, the device is only guaranteed to operate as specified at ambient temperatures from −40°C to +120°C.

Temperature Data Format

The NCT72 has two temperature data formats. When the temperature measurement range is from 0°C to 127°C (default), the temperature data format for both internal and external temperature results is binary. When the measurement range is in extended mode, an offset binary data format is used for both internal and external results. Temperature values are offset by 64°C in the offset binary data format. Examples of temperatures in both data formats are shown in Table 7.

Table 7. TEMPERATURE DATA FORMAT (TEMPERATURE HIGH BYTE)

Temperature	Binary	Offset Binary (Note 1)
–55°C	0 000 0000 (Note 2)	0 000 1001
0°C	0 000 0000	0 100 0000
+1°C	0 000 0001	0 100 0001
+10°C	0 000 1010	0 100 1010
+25°C	0 001 1001	0 101 1001
+50°C	0 011 0010	0 111 0010
+75°C	0 100 1011	1 000 1011
+100°C	0 110 0100	1 010 0100
+125°C	0 111 1101	1 011 1101
+127°C	0 111 1111	1 011 1111
+150°C	0 111 1111 (Note 3)	1 101 0110

1. Offset binary scale temperature values are offset by 64°C.
2. Binary scale temperature measurement returns 0°C for all temperatures < 0°C.
3. Binary scale temperature measurement returns 127°C for all temperatures > 127°C.

The user can switch between measurement ranges at any time. Switching the range likewise switches the data format. The next temperature result following the switching is reported back to the register in the new format. However, the contents of the limit registers do not change. It is up to the user to ensure that when the data format changes, the limit registers are reprogrammed as necessary. More information on this is found in the Limit Registers section.

NCT72 Registers

The NCT72 contains 22, 8-bit registers in total. These registers store the results of remote and local temperature measurements, high and low temperature limits, and configure and control the device. See the Address Pointer Register section through the Consecutive $\overline{\text{ALERT}}$ Register section of this data sheet for more information on the NCT72 registers. Additional details are shown in Table 8 through Table 12. The entire register map is available in Table 13.

Address Pointer Register

The address pointer register itself does not have, nor does it require, an address because the first byte of every write operation is automatically written to this register. The data in this first byte always contains the address of another register on the NCT72 that is stored in the address pointer register. It is to this register address that the second byte of a write operation is written, or to which a subsequent read operation is performed.

The power-on default value of the address pointer register is 0x00. Therefore, if a read operation is performed immediately after power-on, without first writing to the address pointer, the value of the local temperature is returned because its register address is 0x00.

Temperature Value Registers

The NCT72 has three registers to store the results of local and remote temperature measurements. These registers can only be written to by the ADC and can be read by the user over the SMBus/I^2C. The local temperature value register is at Address 0x00.

The external temperature value high byte register is at Address 0x01, with the low byte register at Address 0x10. The power-on default for all three registers is 0x00.

Configuration Register

The configuration register is Address 0x03 at read and Address 0x09 at write. Its power-on default is 0x00. Only four bits of the configuration register are used. Bit 0, Bit 1, Bit 3, and Bit 4 are reserved; the user does not write to them.

Bit 7 of the configuration register masks the $\overline{\text{ALERT}}$ output. If Bit 7 is 0, the $\overline{\text{ALERT}}$ output is enabled. This is the power-on default. If Bit 7 is set to 1, the $\overline{\text{ALERT}}$ output is disabled. This applies only if Pin 6 is configured as $\overline{\text{ALERT}}$. If Pin 6 is configured as $\overline{\text{THERM2}}$, then the value of Bit 7 has no effect.

If Bit 6 is set to 0, which is power-on default, the device is in operating mode with ADC converting. If Bit 6 is set to 1, the device is in standby mode and the ADC does not convert. The SMBus does, however, remain active in standby mode; therefore, values can be read from or written to the NCT72 via the SMBus. The $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ outputs are also active in standby mode. Changes made to the registers in standby mode that affect the $\overline{\text{THERM}}$ or $\overline{\text{ALERT}}$ outputs cause these signals to be updated.

Bit 5 determines the configuration of Pin 6 on the NCT72. If Bit 5 is 0 (default), then Pin 6 is configured as an $\overline{\text{ALERT}}$ output. If Bit 5 is 1, then Pin 6 is configured as a $\overline{\text{THERM2}}$ output. Bit 7, the $\overline{\text{ALERT}}$ mask bit, is only active when Pin 6 is configured as an $\overline{\text{ALERT}}$ output. If Pin 6 is set up as a $\overline{\text{THERM2}}$ output, then Bit 7 has no effect.

Bit 2 sets the temperature measurement range. If Bit 2 is 0 (default value), the temperature measurement range is set between 0°C to +127°C. Setting Bit 2 to 1 sets the measurement range to the extended temperature range (−64°C to +191°C).

Table 8. CONFIGURATION REGISTER BIT ASSIGNMENTS

Bit	Name	Function	Power-on Default
7	MASK1	0 = $\overline{\text{ALERT}}$ Enabled 1 = $\overline{\text{ALERT}}$ Masked	0
6	RUN/STOP	0 = Run 1 = Standby	0
5	$\overline{\text{ALERT}}$/ $\overline{\text{THERM2}}$	0 = $\overline{\text{ALERT}}$ 1 = $\overline{\text{THERM2}}$	0
4, 3	Reserved		0
2	Temperature Range Select	0 = 0°C to 127°C 1 = Extended Range	0
1, 0	Reserved		0

Conversion Rate Register

The conversion rate register is Address 0x04 at read and Address 0x0A at write. The lowest four bits of this register are used to program the conversion rate by dividing the internal oscillator clock by 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024 to give conversion times from 15.5 ms (Code 0x0A) to 16 seconds (Code 0x00). For example, a conversion rate of eight conversions per second means that beginning at 125 ms intervals, the device performs a conversion on the internal and the external temperature channels.

The conversion rate register can be written to and read back over the SMBus/I^2C. The higher four bits of this register are unused and must be set to 0. The default value of this register is 0x08, giving a rate of 16 conversions per second. Use of slower conversion times greatly reduces the device power consumption.

Table 9. CONVERSION RATE REGISTER CODES

Code	Conversion/Second	Time
0x00	0.0625	16 s
0x01	0.125	8 s
0x02	0.25	4 s
0x03	0.5	2 s
0x04	1	1 s
0x05	2	500 ms
0x06	4	250 ms
0x07	8	125 ms
0x08	16	62.5 ms
0x09	32	31.25 ms
0x0A	64	15.5 ms
0x0B to 0xFF	Reserved	–

Limit Registers

The NCT72 has eight limit registers: high, low, and $\overline{\text{THERM}}$ temperature limits for both local and remote temperature measurements. The remote temperature high and low limits span two registers each, to contain an upper and lower byte for each limit. There is also a $\overline{\text{THERM}}$ hysteresis register. All limit registers can be written to, and read back over, the SMBus. See Table 13 for details of the limit register addresses and their power-on default values.

When Pin 6 is configured as an $\overline{\text{ALERT}}$ output, the high limit registers perform a > comparison, while the low limit registers perform a ≤ comparison. For example, if the high limit register is programmed with 80°C, then measuring 81°C results in an out-of-limit condition, setting a flag in the status register. If the low limit register is programmed with 0°C, measuring 0°C or lower results in an out-of-limit condition.

Exceeding either the local or remote $\overline{\text{THERM}}$ limit asserts $\overline{\text{THERM}}$ low. When Pin 6 is configured as $\overline{\text{THERM2}}$, exceeding either the local or remote high limit asserts $\overline{\text{THERM2}}$ low. A default hysteresis value of 10°C is provided that applies to both $\overline{\text{THERM}}$ channels. This hysteresis value can be reprogrammed to any value after powerup (Register Address 0x21).

It is important to remember that the temperature limits data format is the same as the temperature measurement data format. Therefore, if the temperature measurement uses default binary, then the temperature limits also use the binary scale. If the temperature measurement scale is switched, however, the temperature limits do not automatically switch. The user must reprogram the limit registers to the desired value in the correct data format. For example, if the remote low limit is set at 10°C with the default binary scale, the limit register value is 0000 1010b. If the scale is switched to offset binary, the value in the low temperature limit register needs to be reprogrammed to 0100 1010b.

Status Register

The status register is a read-only register at Address 0x02. It contains status information for the NCT72.

When Bit 7 of the status register is high, it indicates that the ADC is busy converting. The other bits in this register flag the out-of-limit temperature measurements (Bit 6 to Bit 3, and Bit 1 to Bit 0) and the remote sensor open circuit (Bit 2).

If Pin 6 is configured as an $\overline{\text{ALERT}}$ output, the following applies: If the local temperature measurement exceeds its limits, Bit 6 (high limit) or Bit 5 (low limit) of the status register asserts to flag this condition. If the remote temperature measurement exceeds its limits, then Bit 4 (high limit) or Bit 3 (low limit) asserts. Bit 2 asserts to flag an open circuit condition on the remote sensor. These five flags are NOR'ed together, so if any of them is high, the $\overline{\text{ALERT}}$ interrupt latch is set and the $\overline{\text{ALERT}}$ output goes low.

Reading the status register clears the five flags, Bit 6 to Bit 2, provided the error conditions causing the flags to be set have gone away. A flag bit can be reset only if the corresponding value register contains an in-limit measurement or if the sensor is good.

The $\overline{\text{ALERT}}$ interrupt latch is not reset by reading the status register. It resets when the $\overline{\text{ALERT}}$ output has been serviced by the master reading the device address, provided the error condition has gone away and the status register flag bits are reset.

When Flag 1 and/or Flag 0 are set, the $\overline{\text{THERM}}$ output goes low to indicate that the temperature measurements are outside the programmed limits. The $\overline{\text{THERM}}$ output does not need to be reset, unlike the $\overline{\text{ALERT}}$ output. Once the measurements are within the limits, the corresponding status register bits are automatically reset and the $\overline{\text{THERM}}$ output goes high. The user may add hysteresis by programming Register 0x21. The $\overline{\text{THERM}}$ output is reset only when the temperature falls to limit value minus the hysteresis value.

When Pin 6 is configured as $\overline{\text{THERM2}}$, only the high temperature limits are relevant. If Flag 6 and/or Flag 4 are

set, the $\overline{\text{THERM2}}$ output goes low to indicate that the temperature measurements are outside the programmed limits. Flag 5 and Flag 3 have no effect on $\overline{\text{THERM2}}$. The behavior of $\overline{\text{THERM2}}$ is otherwise the same as $\overline{\text{THERM}}$.

Table 10. STATUS REGISTER BIT ASSIGNMENTS

Bit	Name	Function
7	BUSY	1 when ADC Is Converting
6	LHIGH (Note 1)	1 when Local High Temperature Limit is Tripped
5	LLOW (Note 1)	1 when Local Low Temperature Limit is Tripped
4	RHIGH (Note 1)	1 when Remote High Temperature Limit is Tripped
3	RLOW (Note 1)	1 when Remote Low Temperature Limit is Tripped
2	OPEN (Note 1)	1 when Remote Sensor is an Open Circuit
1	RTHRM	1 when Remote $\overline{\text{THERM}}$ Limit is Tripped
0	LTHRM	1 when Local $\overline{\text{THERM}}$ Limit is Tripped

1. These flags stay high until the status register is read or they are reset by POR unless Pin 6 is configured as $\overline{\text{THERM2}}$. Then, only Bit 2 remains high until the status register is read or is reset by POR.

Offset Register

Offset errors can be introduced into the remote temperature measurement by clock noise or when the thermal diode is located away from the hot spot. To achieve the specified accuracy on this channel, these offsets must be removed.

The offset value is stored as a 10-bit, twos complement value in Register 0x11 (high byte) and Register 0x12 (low byte, left justified). Only the upper two bits of Register 0x12 are used. The MSB of Register 0x11 is the sign bit. The minimum, programmable offset is −128°C, and the maximum is +127.75°C. The value in the offset register is added to, or subtracted from, the measured value of the remote temperature.

The offset register powers up with a default value of 0°C and has no effect unless the user writes a different value to it.

Table 11. SAMPLE OFFSET REGISTER CODES

Offset Value	0x11	0x12
−128°C	1000 0000	00 00 0000
−4°C	1111 1100	00 00 0000
−1°C	1111 1111	00 000000
−0.25°C	1111 1111	10 00 0000
0°C	0000 0000	00 00 0000
+0.25°C	0000 0000	01 00 0000
+1°C	0000 0001	00 00 0000
+4°C	0000 0100	00 00 0000
+127.75°C	0111 1111	11 00 0000

One-shot Register

The one-shot register is used to initiate a conversion and comparison cycle when the NCT72 is in standby mode, after which the device returns to standby. Writing to the one-shot register address (0x0F) causes the NCT72 to perform a conversion and comparison on both the internal and the external temperature channels. This is not a data register as such, and it is the write operation to Address 0x0F that causes the one-shot conversion. The data written to this address is irrelevant and is not stored.

Consecutive $\overline{\text{ALERT}}$ Register

The value written to this register determines how many out-of-limit measurements must occur before an $\overline{\text{ALERT}}$ is generated. The default value is that one out-of-limit measurement generates an $\overline{\text{ALERT}}$. The maximum value that can be chosen is 4. The purpose of this register is to allow the user to perform some filtering of the output. This is particularly useful at the fastest three conversion rates, where no averaging takes place. This register is at Address 0x22.

Table 12. CONSECUTIVE $\overline{\text{ALERT}}$ REGISTER CODES

Register Value	Number of Out-of-limit Measurements Required
yxxx 000x	1
yxxx 001x	2
yxxx 011x	3
yxxx 111x	4

NOTE: x = don't care bits, and y = SMBus timeout bit. Default = 0. See SMBus section for more information.

Table 13. LIST OF REGISTERS

Read Address (Hex)	Write Address (Hex)	Name	Power-on Default
Not Applicable	Not Applicable	Address Pointer	Undefined
00	Not Applicable	Local Temperature Value	0000 0000 (0x00)
01	Not Applicable	External Temperature Value High Byte	0000 0000 (0x00)
02	Not Applicable	Status	Undefined
03	09	Configuration	0000 0000 (0x00)
04	0A	Conversion Rate	0000 1000 (0x08)
05	0B	Local Temperature High Limit	0101 0101 (0x55) (85°C)
06	0C	Local Temperature Low Limit	0000 0000 (0x00) (0°C)
07	0D	External Temperature High Limit High Byte	0101 0101 (0x55) (85°C)
08	0E	External Temperature Low Limit High Byte	0000 0000 (0x00) (0°C)
Not Applicable	0F (Note 1)	One-shot	
10	Not Applicable	External Temperature Value Low Byte	0000 0000
11	11	External Temperature Offset High Byte	0000 0000
12	12	External Temperature Offset Low Byte	0000 0000
13	13	External Temperature High Limit Low Byte	0000 0000
14	14	External Temperature Low Limit Low Byte	0000 0000
19	19	External $\overline{\text{THERM}}$ Limit	0110 1100 (0x6C) (108°C)
20	20	Local $\overline{\text{THERM}}$ Limit	0101 0101 (0x55) (85°C)
21	21	$\overline{\text{THERM}}$ Hysteresis	0000 1010 (0x0A) (10°C)
22	22	Consecutive $\overline{\text{ALERT}}$	0000 0001 (0x01)
FE	Not Applicable	Manufacturer ID	0100 0001 (0x41)

1. Writing to Address 0x0F causes the NCT72 to perform a single measurement. It is not a data register, and it does not matter what data is written to it.

Serial Bus Interface

Control of the NCT72 is carried out via the serial bus. The NCT72 is connected to this bus as a slave device, under the control of a master device.

The NCT72 has an SMBus/I^{2}C timeout feature. When this is enabled, the SMBus/I^{2}C times out after typically 25 ms of no activity. However, this feature is not enabled by default. Bit 7 of the consecutive alert register (Address = 0x22) should be set to enable it.

Addressing the Device

In general, every SMBus/I^{2}C device has a 7-bit device address, except for some devices that have extended 10-bit addresses. When the master device sends a device address over the bus, the slave device with that address responds. The NCT72 is available with one device address, 0x4C (1001 100b). An NCT72D is also available.

The NCT72D has an SMBus/I^{2}C address of 0x4D (1001 101b). This is to allow two NCT72 devices on the same bus, or if the default address conflicts with an existing device on the SMBus/I^{2}C. The serial bus protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on SDATA, the serial data line, while SCLK, the serial clock line, remains high. This indicates that an address/data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{\text{W}}$ bit, which determines the direction of the data transfer, that is, whether data is written to, or read from, the slave device. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{\text{W}}$ bit is a 0, the master writes to the slave device. If the R/$\overline{\text{W}}$ bit is a 1, the master reads from the slave device.
2. Data is sent over the serial bus in a sequence of nine clock pulses, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, since a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master takes the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition.
Any number of bytes of data are transferable over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. For the NCT72, write operations contain either one or two bytes, while read operations contain one byte.

To write data to one of the device data registers, or to read data from it, the address pointer register must be set so that the correct data register is addressed. The first byte of a write operation always contains a valid address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This procedure is illustrated in Figure 15. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

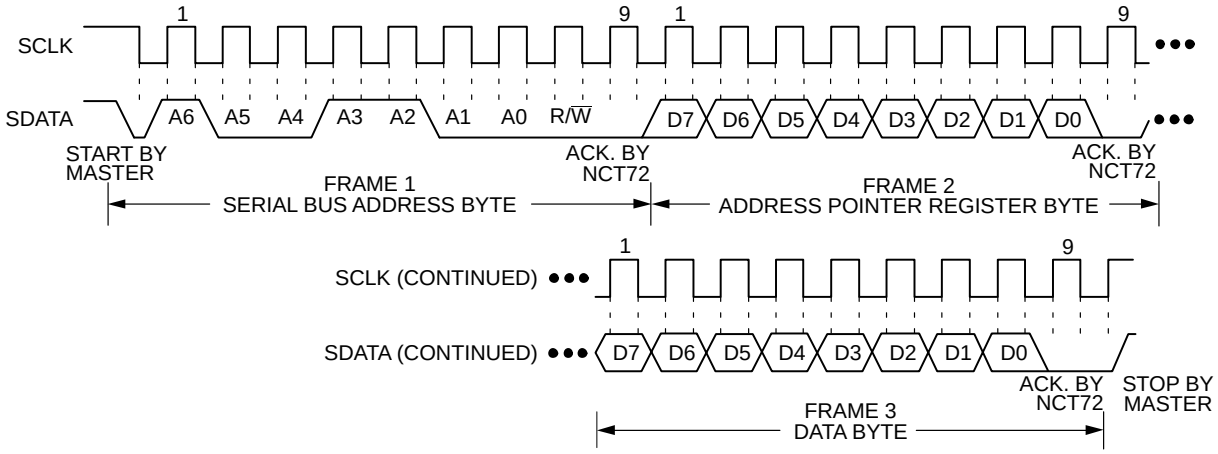


Figure 15. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

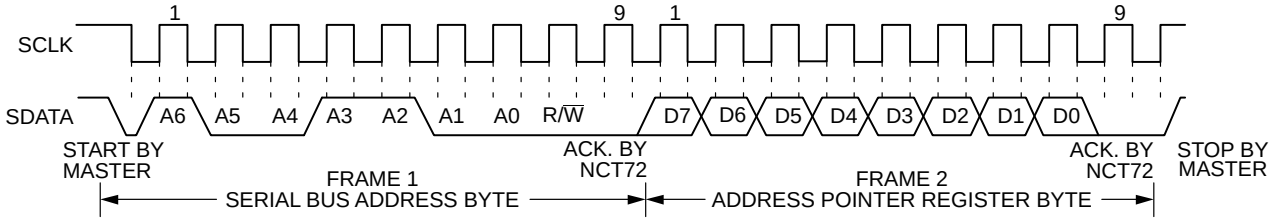


Figure 16. Writing to the Address Pointer Register Only

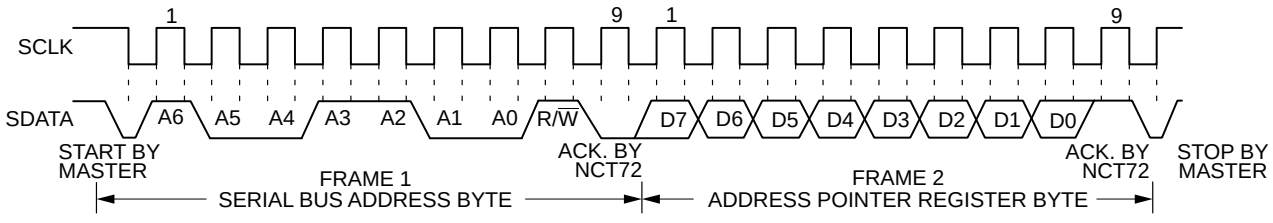


Figure 17. Reading Data from a Previously Selected Register

When reading data from a register there are two possibilities.

- If the address pointer register value of the NCT72 is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by writing to the NCT72 as before, but only the data byte containing the register read address is sent, because data is not to be written to the register see Figure 16.
  A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register see Figure 17.
- If the address pointer register is known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register and the bus transaction shown in Figure 16 can be omitted.

NOTES: It is possible to read a data byte from a data register without first writing to the address pointer register. However, if the address pointer register is already at the correct value, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

Some of the registers have different addresses for read and write operations. The write address of a register must be written to the address pointer if data is to be written to that register, but it may not be possible to read data from that address. The read address of a register must be written to the address pointer before data can be read from that register.

$\overline{\text{ALERT}}$ Output

This is applicable when Pin 6 is configured as an $\overline{\text{ALERT}}$ output. The $\overline{\text{ALERT}}$ output goes low whenever an out-of-limit measurement is detected, or if the remote temperature sensor is open circuit. It is an open-drain output and requires a pullup resistor to V_{DD}. Several $\overline{\text{ALERT}}$ outputs can be wire-OR'ed together, so that the common line goes low if one or more of the $\overline{\text{ALERT}}$ outputs goes low.

The $\overline{\text{ALERT}}$ output can be used as an interrupt signal to a processor, or as an $\overline{\text{SMBALERT}}$. Slave devices on the SMBus cannot normally signal to the bus master that they want to talk, but the $\overline{\text{SMBALERT}}$ function allows them to do so.

One or more $\overline{\text{ALERT}}$ outputs can be connected to a common $\overline{\text{SMBALERT}}$ line that is connected to the master. When the $\overline{\text{SMBALERT}}$ line is pulled low by one of the devices, the following procedure occurs (see Figure 18):

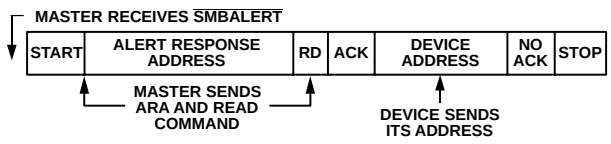


Figure 18. Use of $\overline{\text{SMBALERT}}$

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. Master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{ALERT}}$ output is low responds to the alert response address and the master reads its device address. As the device address is seven bits, an LSB of 1 is added. The address of the device is now known and it can be interrogated in the usual way.
4. If more than one device's $\overline{\text{ALERT}}$ output is low, the one with the lowest device address takes priority, in accordance with normal SMBus arbitration.

Once the NCT72 has responded to the alert response address, it resets its $\overline{\text{ALERT}}$ output, provided that the error condition that caused the $\overline{\text{ALERT}}$ no longer exists. If the $\overline{\text{SMBALERT}}$ line remains low, the master sends the ARA again, and so on until all devices whose $\overline{\text{ALERT}}$ outputs were low have responded.

Low Power Standby Mode

The NCT72 can be put into low power standby mode by setting Bit 6 of the configuration register. When Bit 6 is low, the NCT72 operates normally. When Bit 6 is high, the ADC is inhibited, and any conversion in progress is terminated without writing the result to the corresponding value register. However, the SMBus is still enabled. Power consumption in the standby mode is reduced to 5 μA if there is no SMBus activity, or 30 μA if there are clock and data signals on the bus.

When the device is in standby mode, it is possible to initiate a one-shot conversion of both channels by writing to the one-shot register (Address 0x0F), after which the device returns to standby. It does not matter what is written to the one-shot register, all data written to it is ignored. It is also possible to write new values to the limit register while in standby mode. If the values stored in the temperature value registers are outside the new limits, an $\overline{\text{ALERT}}$ is generated, even though the NCT72 is still in standby.

1.8 V Logic Operation

The NCT72 is 1.8 V logic compatible; this means that the communication lines (SDA and SCL) $\overline{\text{ALERT}}$/$\overline{\text{THERM2}}$ and $\overline{\text{THERM}}$ can be pulled up to a 1.8 V supply while still remaining within the device Idd spec.

Sensor Fault Detection

At its D+ input, the NCT72 contains internal sensor fault detection circuitry. This circuit can detect situations where an external remote diode is either not connected or incorrectly connected to the NCT72. A simple voltage comparator trips if the voltage at D+ exceeds V_{DD} − 1.0 V (typical), signifying an open circuit between D+ and D−. The output of this comparator is checked when a conversion is initiated. Bit 2 of the status register (open flag) is set if a

fault is detected. If the $\overline{\text{ALERT}}$ pin is enabled, setting this flag causes $\overline{\text{ALERT}}$ to assert low.

If the user does not wish to use an external sensor with the NCT72, tie the D+ and D− inputs together to prevent continuous setting of the open flag.

The NCT72 Interrupt System

The NCT72 has two interrupt outputs, $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$. Both have different functions and behavior. $\overline{\text{ALERT}}$ is maskable and responds to violations of software programmed temperature limits or an open-circuit fault on the external diode. $\overline{\text{THERM}}$ is intended as a fail-safe interrupt output that cannot be masked.

If the external or local temperature exceeds the programmed high temperature limits, or equals or exceeds the low temperature limits, the $\overline{\text{ALERT}}$ output is asserted low. An open-circuit fault on the external diode also causes $\overline{\text{ALERT}}$ to assert. $\overline{\text{ALERT}}$ is reset when serviced by a master reading its device address, provided the error condition has gone away and the status register has been reset.

The $\overline{\text{THERM}}$ output asserts low if the external or local temperature exceeds the programmed $\overline{\text{THERM}}$ limits. $\overline{\text{THERM}}$ temperature limits should normally be equal to or greater than the high temperature limits. $\overline{\text{THERM}}$ is reset automatically when the temperature falls back within the $\overline{\text{THERM}}$ limit. A hysteresis value can be programmed; in which case, $\overline{\text{THERM}}$ resets when the temperature falls to the limit value minus the hysteresis value. This applies to both local and remote measurement channels. The power-on hysteresis default value is 10°C, but this can be reprogrammed to any value after powerup.

The hysteresis loop on the $\overline{\text{THERM}}$ outputs is useful when $\overline{\text{THERM}}$ is used, for example, as an on/off controller for a fan. The user's system can be set up so that when $\overline{\text{THERM}}$ asserts, a fan is switched on to cool the system. When $\overline{\text{THERM}}$ goes high again, the fan can be switched off. Programming a hysteresis value protects from fan jitter, where the temperature hovers around the $\overline{\text{THERM}}$ limit, and the fan is constantly switched.

Table 14. $\overline{\text{THERM}}$ HYSTERESIS

$\overline{\text{THERM}}$ Hysteresis	Binary Representation
0°C	0 000 0000
1°C	0 000 0001
10°C	0 000 1010

Figure 19 shows how the $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ outputs operate. The $\overline{\text{ALERT}}$ output can be used as a $\overline{\text{SMBALERT}}$ to signal to the host via the SMBus that the temperature has risen. The user can use the $\overline{\text{THERM}}$ output to turn on a fan to cool the system, if the temperature continues to increase. This method ensures that there is a fail-safe mechanism to cool the system, without the need for host intervention.

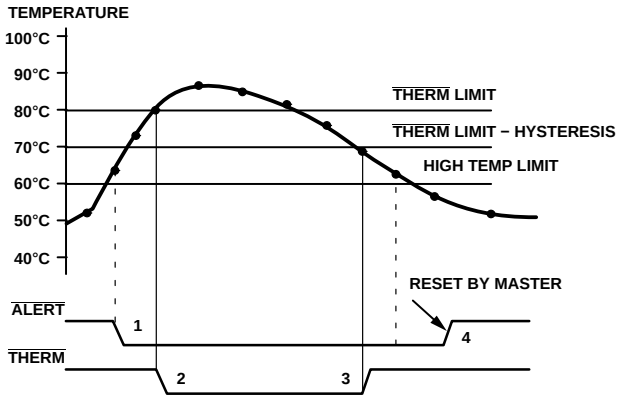


Figure 19. Operation of the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Interrupts

- If the measured temperature exceeds the high temperature limit, the $\overline{\text{ALERT}}$ output asserts low.
- If the temperature continues to increase and exceeds the $\overline{\text{THERM}}$ limit, the $\overline{\text{THERM}}$ output asserts low. This can be used to throttle the CPU clock or switch on a fan.
- The $\overline{\text{THERM}}$ output deasserts (goes high) when the temperature falls to $\overline{\text{THERM}}$ limit minus hysteresis. In , the default hysteresis value of 10°C is shown.
- The $\overline{\text{ALERT}}$ output deasserts only when the temperature has fallen below the high temperature limit, and the master has read the device address and cleared the status register.
- Pin 6 on the NCT72 can be configured as either an $\overline{\text{ALERT}}$ output or as an additional $\overline{\text{THERM}}$ output.
- $\overline{\text{THERM2}}$ asserts low when the temperature exceeds the programmed local and/or remote high temperature limits. It is reset in the same manner as $\overline{\text{THERM}}$ and is not maskable.
- The programmed hysteresis value also applies to $\overline{\text{THERM2}}$.

Figure 20 shows how $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ operate together to implement two methods of cooling the system. In this example, the $\overline{\text{THERM2}}$ limits are set lower than the $\overline{\text{THERM}}$ limits. The $\overline{\text{THERM2}}$ output is used to turn on a fan. If the temperature continues to rise and exceeds the $\overline{\text{THERM}}$ limits, the $\overline{\text{THERM}}$ output provides additional cooling by throttling the CPU.

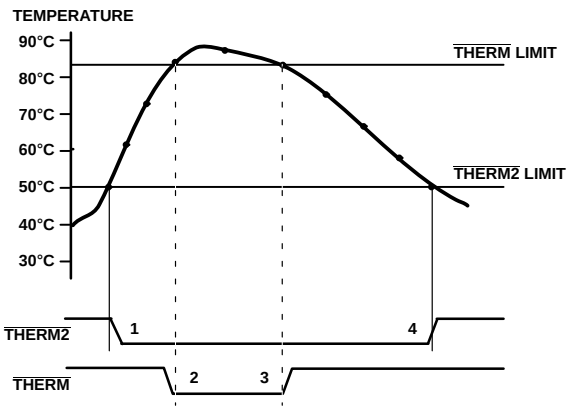


Figure 20. Operation of the $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ Interrupts

- When the $\overline{\text{THERM2}}$ limit is exceeded, the $\overline{\text{THERM2}}$ signal asserts low.
- If the temperature continues to increase and exceeds the $\overline{\text{THERM}}$ limit, the $\overline{\text{THERM}}$ output asserts low.
- The $\overline{\text{THERM}}$ output deasserts (goes high) when the temperature falls to $\overline{\text{THERM}}$ limit minus hysteresis. In Figure 20, there is no hysteresis value shown.
- As the system cools further, and the temperature falls below the $\overline{\text{THERM2}}$ limit, the $\overline{\text{THERM2}}$ signal resets. Again, no hysteresis value is shown for $\overline{\text{THERM2}}$.

Both the external and internal temperature measurements cause $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ to operate as described.

Application Information

Noise Filtering

For temperature sensors operating in noisy environments, the industry standard practice was to place a capacitor across the D+ and D− pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF. Although this capacitor reduces the noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The NCT72 has a major advantage over other devices when it comes to eliminating the effects of noise on the external sensor. The series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the part. The effect of any filter resistance seen in series with the remote sensor is automatically cancelled from the temperature result.

The construction of a filter allows the NCT72 and the remote temperature sensor to operate in noisy environments. Figure 21 shows a low-pass R-C-R filter, where R = 100 Ω and C = 1 nF. This filtering reduces both common-mode and differential noise.

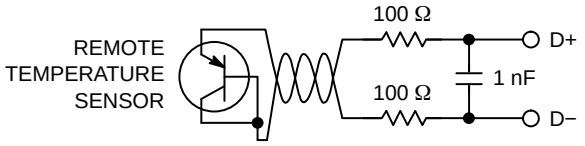


Figure 21. Filter between Remote Sensor and NCT72 Factors Affecting Diode Accuracy

Remote Sensing Diode

The NCT72 is designed to work with substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types are either PNP or NPN transistors connected as diodes (base-shorted to collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter to D+.

To reduce the error due to variations in both substrate and discrete transistors, consider several factors:

- The ideality factor, nF, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The NCT72 is trimmed for an nF value of 1.008. The following equation may be used to calculate the error introduced at a temperature, T (°C), when using a transistor whose nF does not equal 1.008. Consult the processor data sheet for the nF values.

  $$\Delta T = (nF - 1.008)/1.008 \times (273.15\ \text{Kelvin} + T)$$

  To factor this in, the user writes the ΔT value to the offset register. It is then automatically added to, or subtracted from, the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the NCT72, I_{HIGH}, is 220 μA and the low level current, I_{LOW}, is 13.5 μA. If the NCT72 current levels do not match the current levels specified by the CPU manufacturer, it may become necessary to remove an offset. The CPU data sheet should advise whether this offset needs to be removed and how to calculate it. This offset is programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the NCT72, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 6 μA, at the highest operating temperature
- Base-emitter voltage less than 0.95 V at 100 μA, at the lowest operating temperature

- Base resistance less than 100 Ω
- Small variation in h_{FE} (50 to 150) that indicates tight control of V_{BE} characteristics

Transistors, such as the 2N3904, 2N3906, or equivalents in SOT−23 packages are suitable devices to use.

Thermal Inertia and Self-heating

Accuracy depends on the temperature of the remote sensing diode and/or the internal temperature sensor being at the same temperature as that being measured. Many factors can affect this. Ideally, place the sensor in good thermal contact with the part of the system being measured. If it is not, the thermal inertia caused by the sensor's mass causes a lag in the response of the sensor to a temperature change. In the case of the remote sensor, this should not be a problem since it is either a substrate transistor in the processor or a small package device, such as the SOT−23, placed in close proximity to it.

The on-chip sensor, however, is often remote from the processor and only monitors the general ambient temperature around the package. How accurately the temperature of the board and/or the forced airflow reflects the temperature to be measured dictates the accuracy of the measurement. Self-heating due to the power dissipated in the NCT72 or the remote sensor causes the chip temperature of the device or remote sensor to rise above ambient. However, the current forced through the remote sensor is so small that self-heating is negligible. In the case of the NCT72, the worst-case condition occurs when the device is converting at 64 conversions per second while sinking the maximum current of 1 mA at the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ output. In this case, the total power dissipation in the device is about 4.5 mW. The thermal resistance, θ_{JA}, of the 8-lead DFN is approximately 142°C/W.

Layout Considerations

Digital boards can be electrically noisy environments, and the NCT72 is measuring very small voltages from the remote sensor, so care must be taken to minimize noise induced at the sensor inputs. Take the following precautions:

- Place the NCT72 as close as possible to the remote sensing diode. Provided that the worst noise sources, that is, clock generators, data/address buses, and CRTs are avoided, this distance can be 4 inches to 8 inches.
- Route the D+ and D– tracks close together, in parallel, with grounded guard tracks on each side. To minimize inductance and reduce noise pickup, a 5 mil track width and spacing is recommended. Provide a ground plane under the tracks, if possible.



Figure 22. Typical Arrangement of Signal Tracks

- Try to minimize the number of copper/solder joints that can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− path and at the same temperature.
- Thermocouple effects should not be a major problem as 1°C corresponds to about 200 mV, and thermocouple voltages are about 3 mV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.
- Place a 0.1 μF bypass capacitor close to the V_{DD} pin. In extremely noisy environments, place an input filter capacitor across D+ and D− close to the NCT72. This capacitance can effect the temperature measurement, so ensure that any capacitance seen at D+ and D− is, at maximum, 1,000 pF. This maximum value includes the filter capacitance, plus any cable or stray capacitance between the pins and the sensor diode.
- If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. A total of 6 feet to 12 feet is needed.
  For really long distances (up to 100 feet), use a shielded twisted pair, such as the Belden No. 8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND close to the NCT72. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable or filter capacitance can affect the measurement. When using long cables, the filter capacitance can be reduced or removed.

Application Circuit

Figure 23 shows a typical application circuit for the NCT72, using a discrete sensor transistor connected via a shielded, twisted pair cable. The pullups on SCLK, SDATA, and $\overline{\text{ALERT}}$ are required only if they are not provided elsewhere in the system.

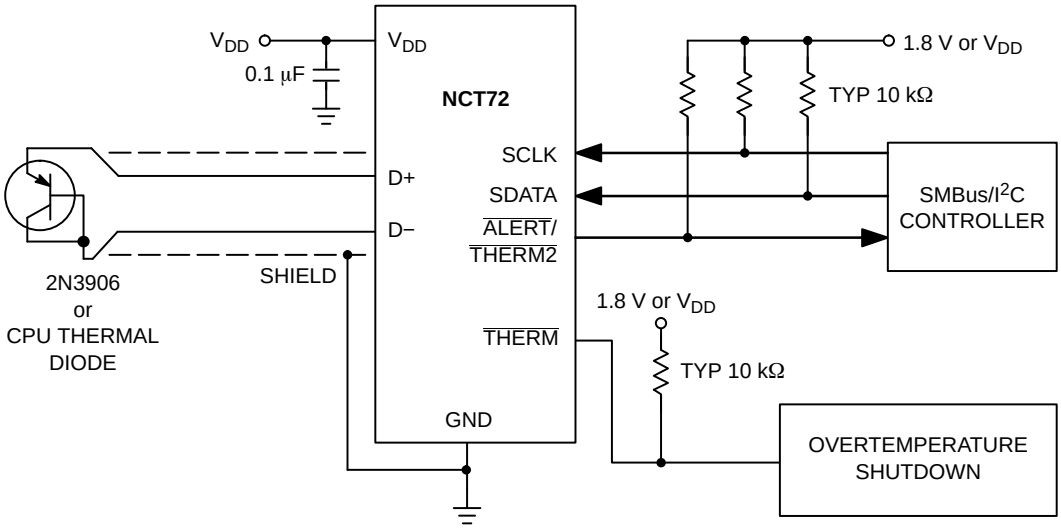


Figure 23. Typical Application Circuit

Table 15. ORDERING INFORMATION

Device Order Number*	Package Description	Package Option	Marking	SMBus Address	Shipping†
NCT72CMTR2G	8-lead WDFN, 2x2	MT	C	0x4C	3,000 Tape & Reel
NCT72DMTR2G	8-lead WDFN, 2x2	MT	D	0x4D	3,000 Tape & Reel
NCT72CMNR2G	8-lead DFN, 3x3	MN	C	0x4C	3,000 Tape & Reel
NCT72DMNR2G	8-lead DFN, 3x3	MN	D	0x4D	3,000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The “G’’ suffix indicates Pb-Free package available.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

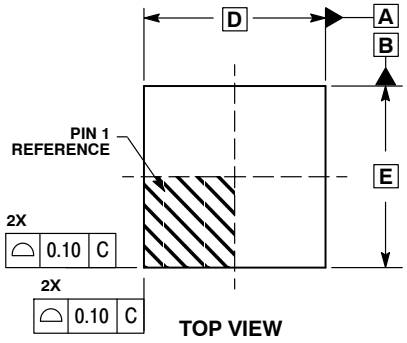
ON Semiconductor®

DFN8 3x3, 0.5P
CASE 506BJ−01
ISSUE O

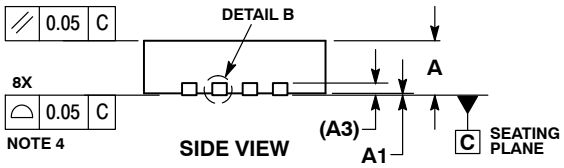
DATE 08 NOV 2007



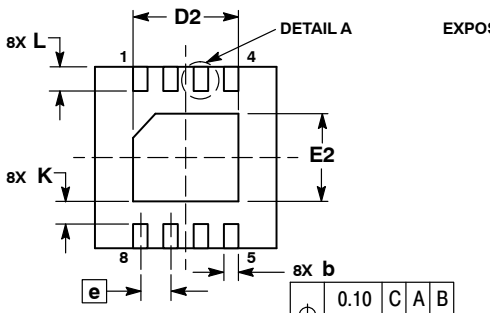
SCALE 2:1



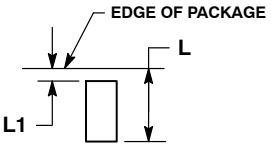
TOP VIEW



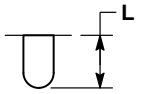
SIDE VIEW



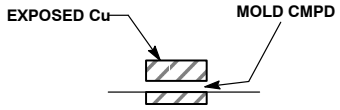
BOTTOM VIEW



DETAIL A
OPTIONAL
CONSTRUCTION



DETAIL A
OPTIONAL
CONSTRUCTION



DETAIL B
OPTIONAL
CONSTRUCTION

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.64	1.84
E	3.00 BSC	
E2	1.35	1.55
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	0.00	0.03

GENERIC MARKING DIAGRAM*

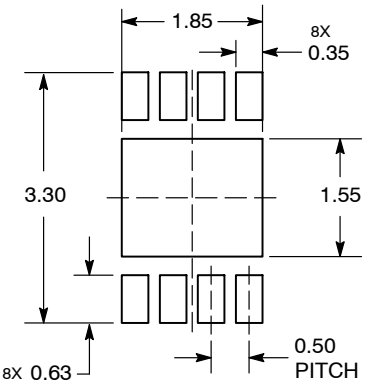


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON25786D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFN8 3X3, 0.5P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

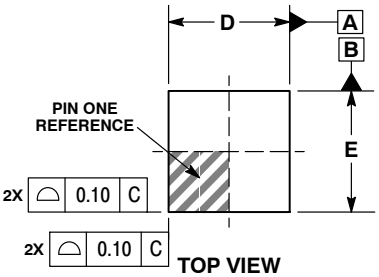
ON Semiconductor®



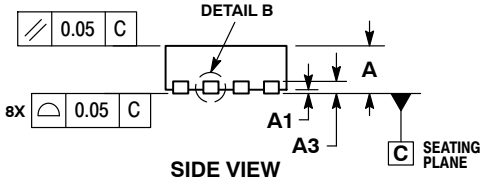
SCALE 4:1

WDFN8 2x2, 0.5P
CASE 511AT−01
ISSUE O

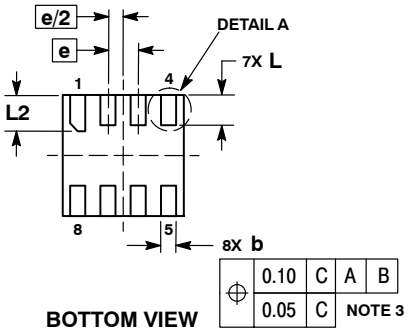
DATE 26 FEB 2010



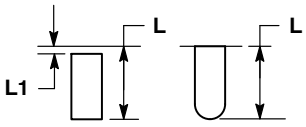
TOP VIEW



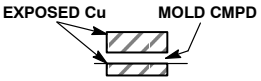
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

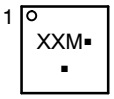


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

GENERIC MARKING DIAGRAM*

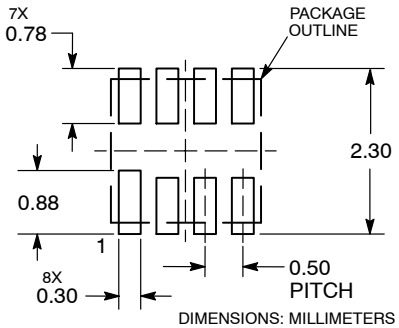


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON48654E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**WDFN8, 2X2, 0.5 P**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales