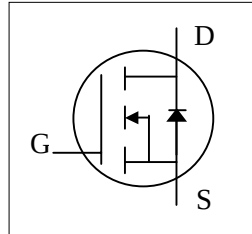


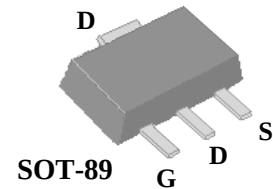
- ▼ Lower Gate Charge
- ▼ Capable of 2.5V Gate Drive
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant



BV_{DSS}	20V
$R_{DS(ON)}$	50m Ω
I_D	4A

Description

XP9452 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.



Absolute Maximum Ratings@ $T_J=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 16	V
$I_D@T_A=25^\circ\text{C}$	Drain Current, $V_{GS} @ 4.5V^3$	4	A
$I_D@T_A=70^\circ\text{C}$	Drain Current, $V_{GS} @ 4.5V^3$	2.5	A
I_{DM}	Pulsed Drain Current ¹	12	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	1.25	W
	Linear Derating Factor	0.01	W/ $^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	100	$^\circ\text{C}/\text{W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.03	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =4A	-	-	38	mΩ
		V _{GS} =4.5V, I _D =4A	-	-	50	mΩ
		V _{GS} =2.5V, I _D =3A	-	-	80	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	0.5	-	1.5	V
g _{fs}	Forward Transconductance ²	V _{DS} =5V, I _D =3A	-	10	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =70°C)	V _{DS} =16V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ±16V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =4A	-	6	10	nC
Q _{gs}	Gate-Source Charge	V _{DS} =16V	-	1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	2	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	8	-	ns
t _r	Rise Time	I _D =1A	-	9	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	13	-	ns
t _f	Fall Time	V _{GS} =5V	-	3	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	360	570	pF
C _{oss}	Output Capacitance	V _{DS} =20V	-	80	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	65	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =1A, V _{GS} =0V	-	-	1.3	V
t _{rr}	Reverse Recovery Time ²	I _S =4A, V _{GS} =0V,	-	18	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	10	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mount on FR4 board, t ≤ 10s.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

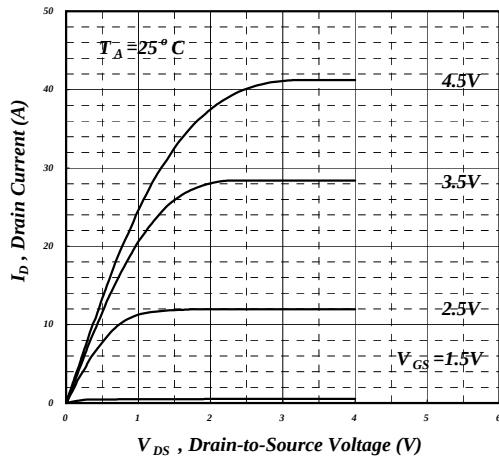


Fig 1. Typical Output Characteristics

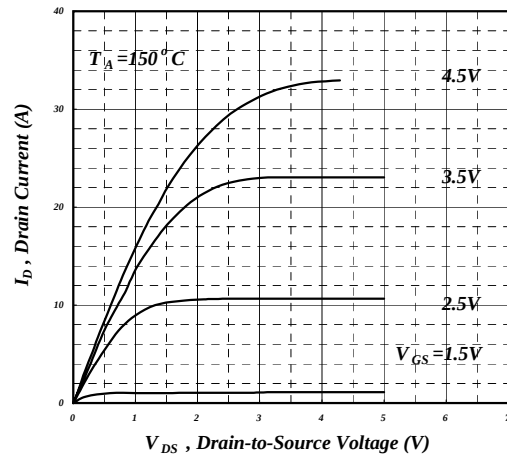


Fig 2. Typical Output Characteristics

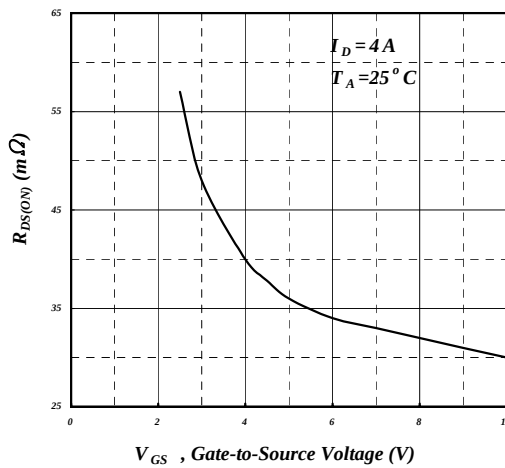
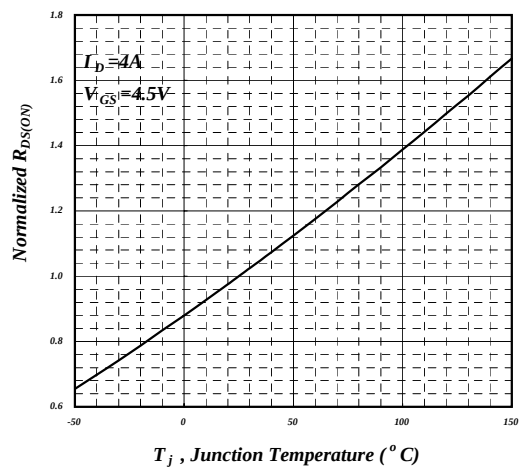
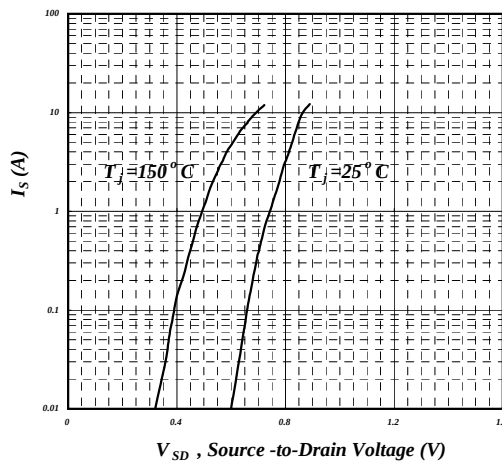


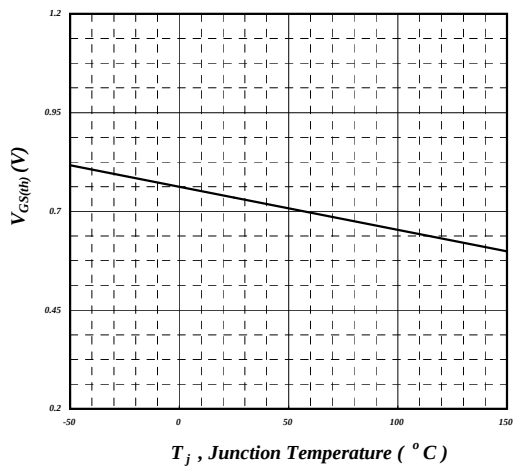
Fig 3. On-Resistance v.s. Gate Voltage



**Fig 4. Normalized On-Resistance
v.s. Junction Temperature**



**Fig 5. Forward Characteristic of
Reverse Diode**



**Fig 6. Gate Threshold Voltage v.s.
Junction Temperature**

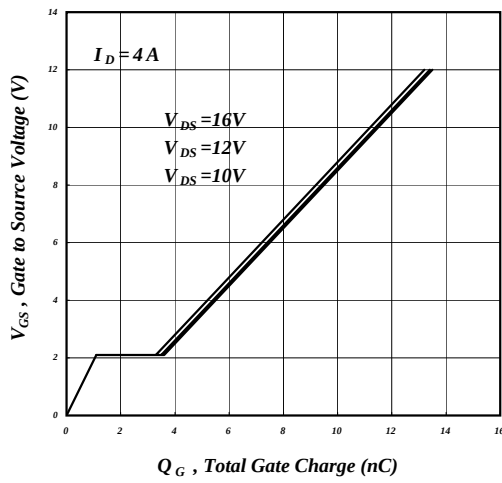


Fig 7. Gate Charge Characteristics

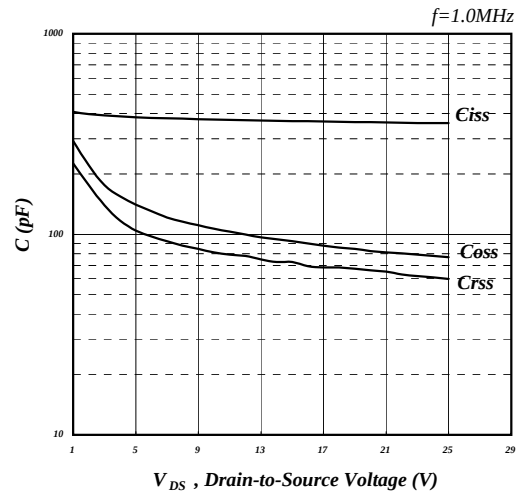


Fig 8. Typical Capacitance Characteristics

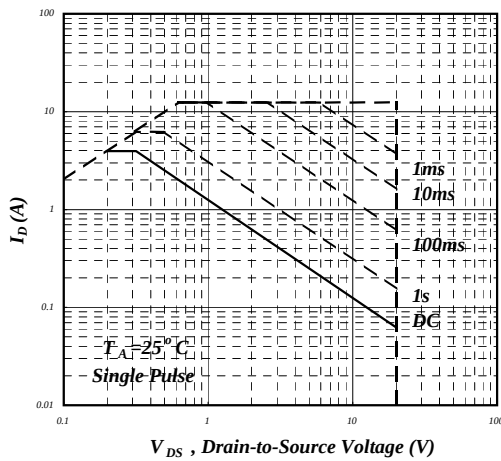


Fig 9. Maximum Safe Operating Area

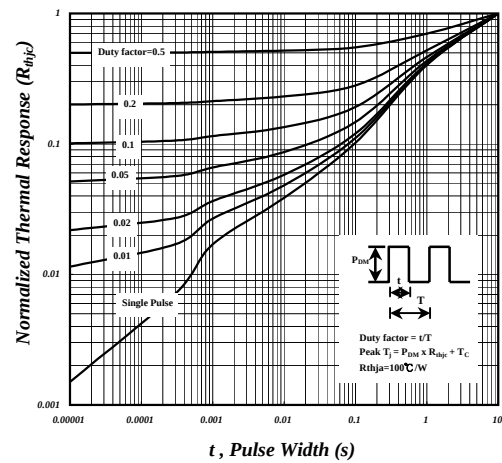


Fig 10. Effective Transient Thermal Impedance

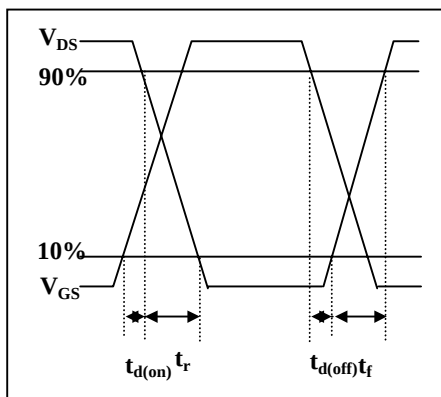


Fig 11. Switching Time Waveform

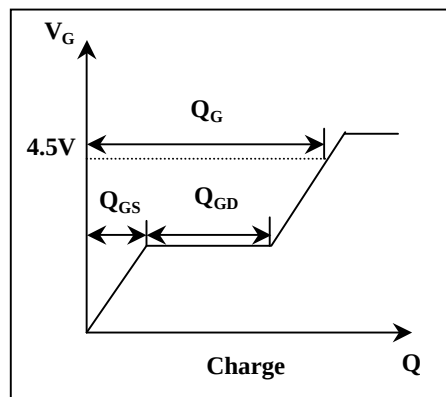
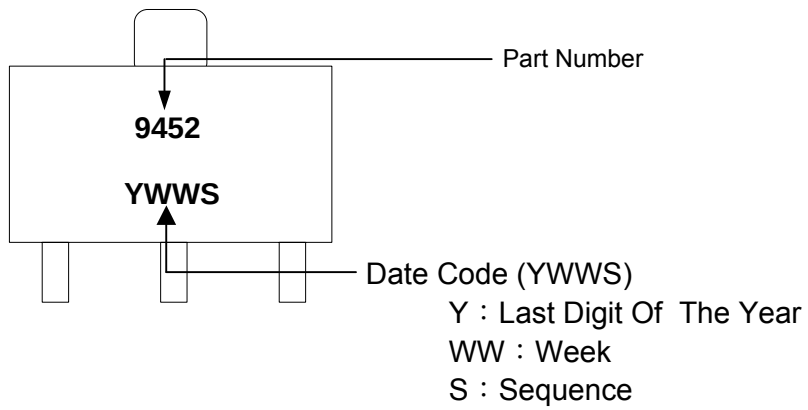
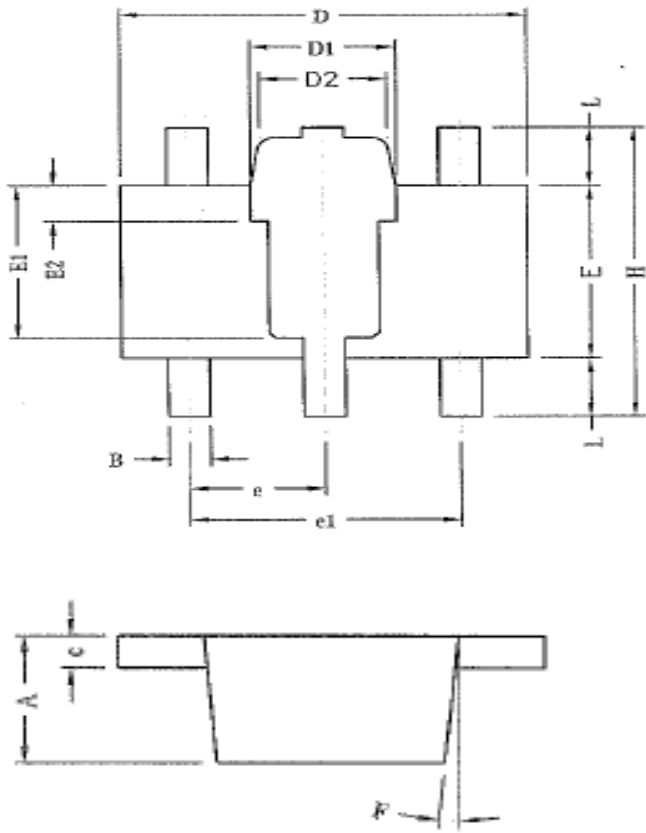


Fig 12. Gate Charge Waveform

MARKING INFORMATION

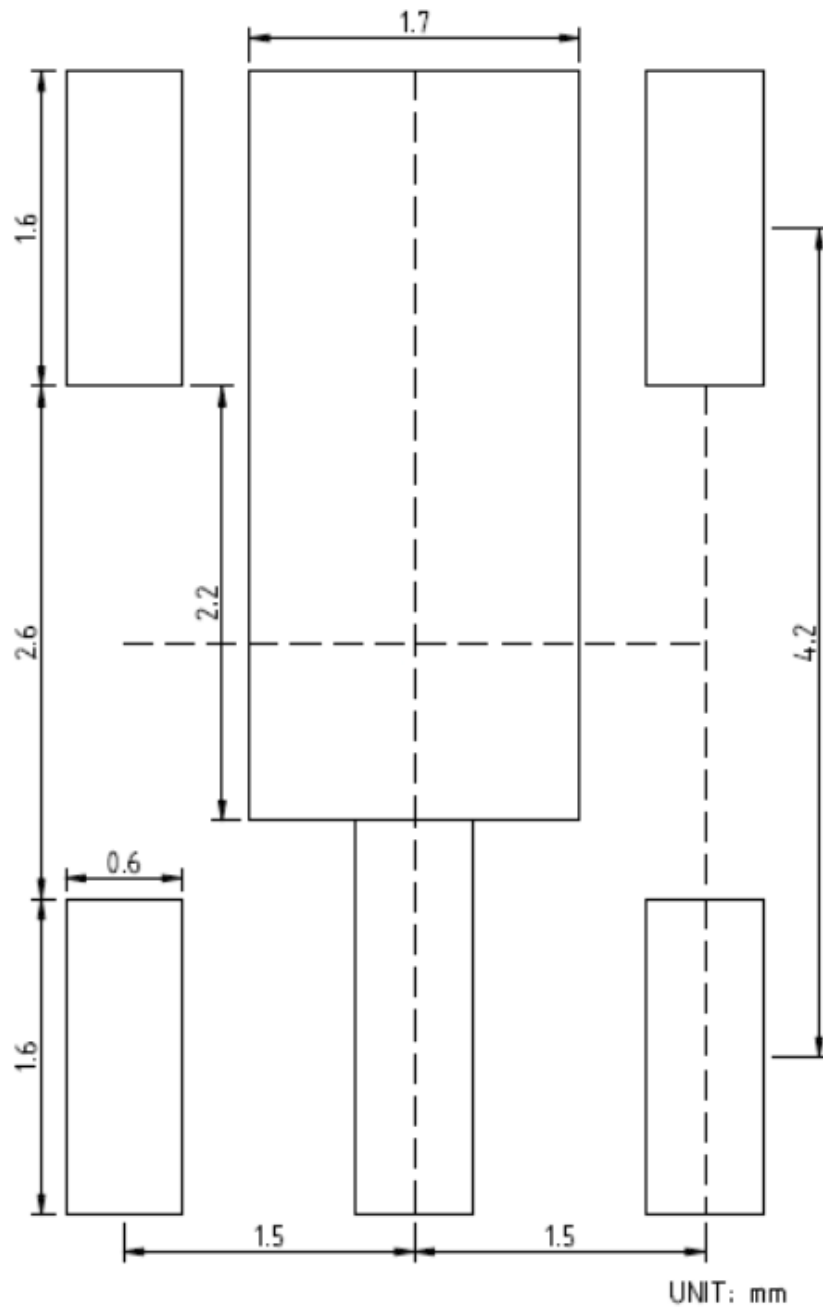
Package Outline & Packing : SOT-89-5L



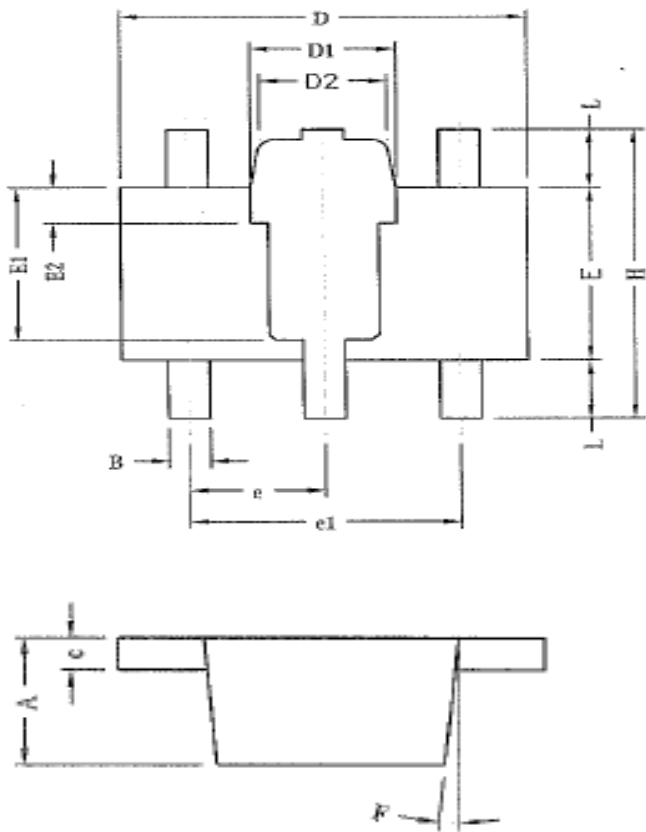
SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.40	1.50	1.60
B	0.50	0.51	0.52
c	0.35	0.38	0.41
D	4.40	4.50	4.60
D1	1.50	1.60	1.70
D2	1.30	1.40	1.50
E	2.40	2.50	2.60
E1	2.2 REF		
E2	0.52 REF		
e	1.50 REF		
e1	3.00 REF		
F	5° REF		
H	4.05	4.15	4.25
L	0.8	—	

- 1.All Dimensions Are in Millimeters.
2.Dimension Does Not Include Mold Protrusions.

SOT-89-5L FOOTPRINT :



Package Outline & Packing : SOT-89-5L



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.40	1.50	1.60
B	0.50	0.51	0.52
c	0.35	0.38	0.41
D	4.40	4.50	4.60
D1	1.50	1.60	1.70
D2	1.30	1.40	1.50
E	2.40	2.50	2.60
E1	2.2 REF		
E2	0.52 REF		
e	1.50 REF		
e1	3.00 REF		
F	5° REF		
H	4.05	4.15	4.25
L	0.8	—	

- 1.All Dimensions Are in Millimeters.
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SOT-89-5L FOOTPRINT :

