

MOSFET - Power, N-Channel, SUPERFET® III, FAST

650 V, 49 A, 50 mΩ

NTBL050N65S3H

Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFAST III FAST MOSFET series helps minimize various power systems and improve system efficiency. The TOLL package offers improved thermal performance and excellent switching performance thanks to Kelvin Source configuration and lower parasitic source inductance. TOLL offers Moisture Sensitivity Level 1 (MSL 1).

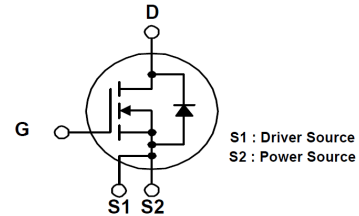
Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 40\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 98\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 909\text{ pF}$)
- 100% Avalanche Tested
- Kelvin Source Configuration and Low Parasitic Source Inductance
- MSL1 Qualified
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

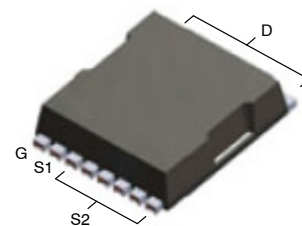
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	50 mΩ @ 10 V	49 A

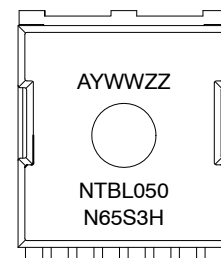


N-Channel MOSFET



H-PSOF8L
CASE 100DC

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code
NTBL050N65S3H	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTBL050N65S3H

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	± 30	V
		AC ($f > 1\text{ Hz}$)	± 30	V
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	49	A
		Continuous ($T_C = 100^\circ\text{C}$)	31	
I_{DM}	Drain Current	Pulsed (Note 1)	132	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		491	mJ
I_{AS}	Avalanche Current (Note 2)		6.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		3.05	mJ
dv/dt	MOSFET dv/dt		120	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	305	W
		Derate Above 25°C	2.44	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2. $I_{AS} = 6.8\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.

3. $I_{SD} \leq 24.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Steady State	0.41	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Steady State (Note 4)	43	

4. Device on 1 in², 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
NTBL050N65S3H	NTBL050N65S3H	H-PSOF8L	13" mm	24 mm	2000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NTBL050N65S3H

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	–	0.63	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	1.0	μA
		V _{DS} = 520 V, T _C = 125°C	–	3.21	–	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 4.8 mA	2.4	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 24.5 A	–	42.5	50	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 24.5 A	–	52	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	4880	–	pF
C _{oss}	Output Capacitance		–	70	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	909	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	128	–	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 24.5 A, V _{GS} = 10 V (Note 5)	–	98	–	nC
Q _{gs}	Gate to Source Gate Charge		–	24	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	25	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.6	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 24.5 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 5)	–	32	–	ns
t _r	Turn-On Rise Time		–	9.5	–	ns
t _{d(off)}	Turn-Off Delay Time		–	96	–	ns
t _f	Turn-Off Fall Time		–	2.6	–	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current		–	–	49	A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	132	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 24.5 A	–	–	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 24.5 A, dI _F /dt = 100 A/μs	–	442	–	ns
Q _{rr}	Reverse Recovery Charge		–	8.8	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

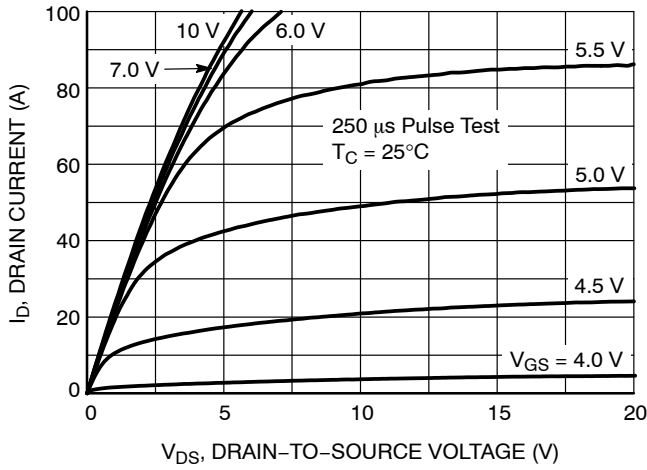


Figure 1. On-Region Characteristics

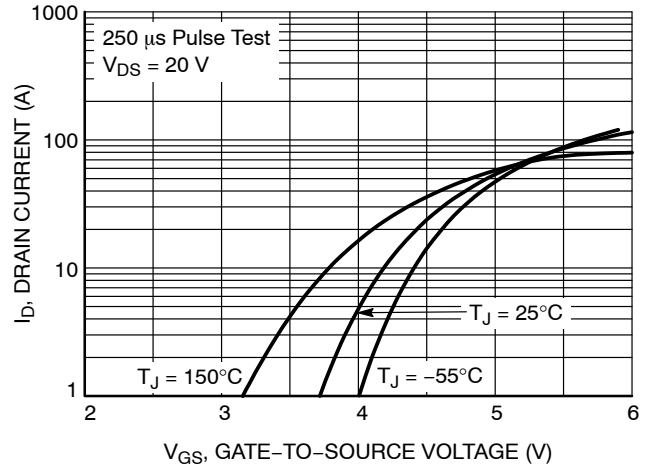


Figure 2. Transfer Characteristics

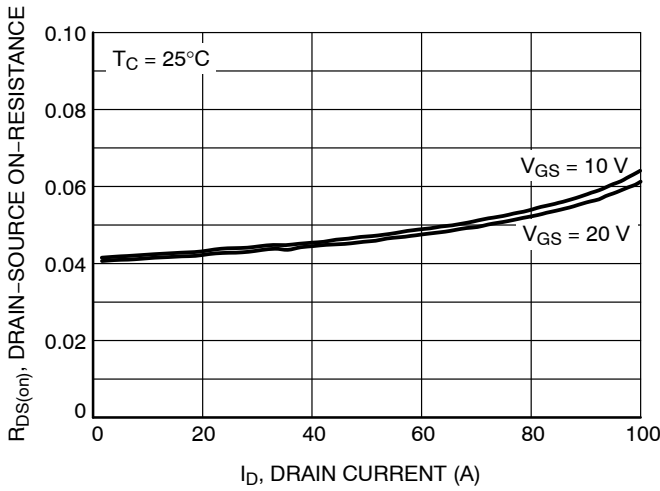


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

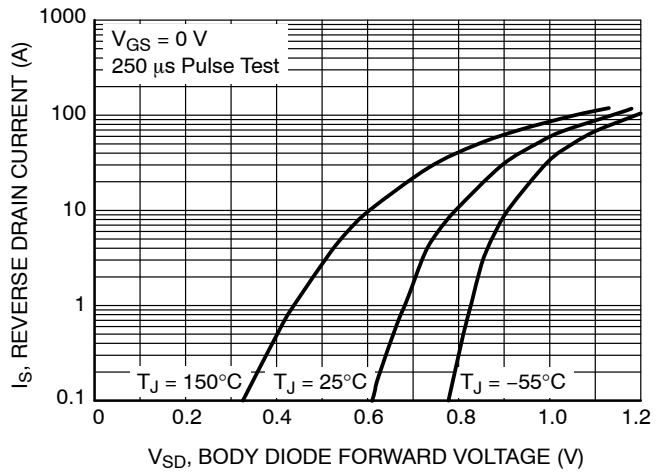


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

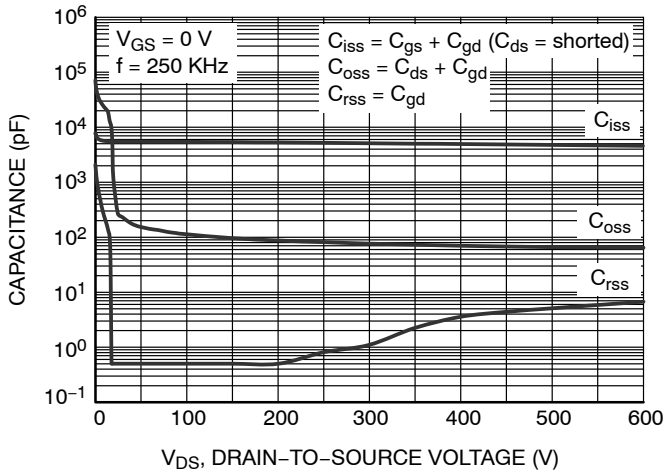


Figure 5. Capacitance Characteristics

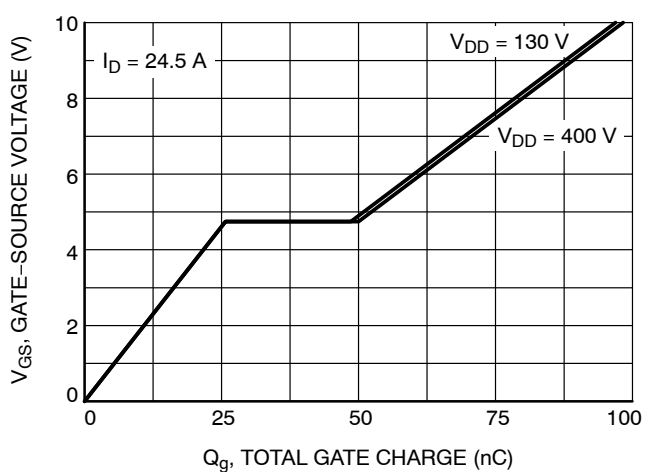


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

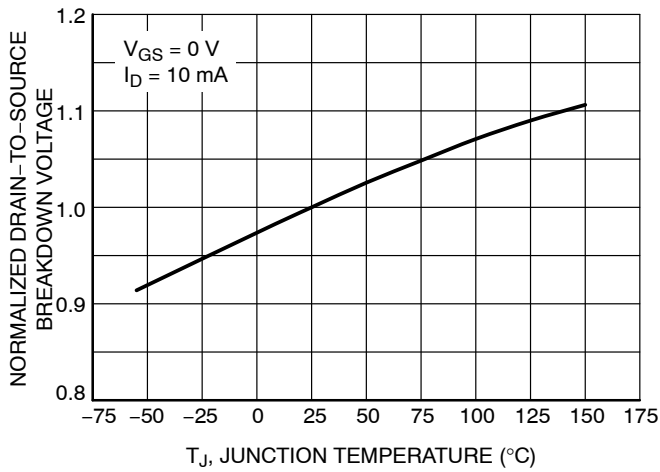


Figure 7. Breakdown Voltage Variation vs. Temperature

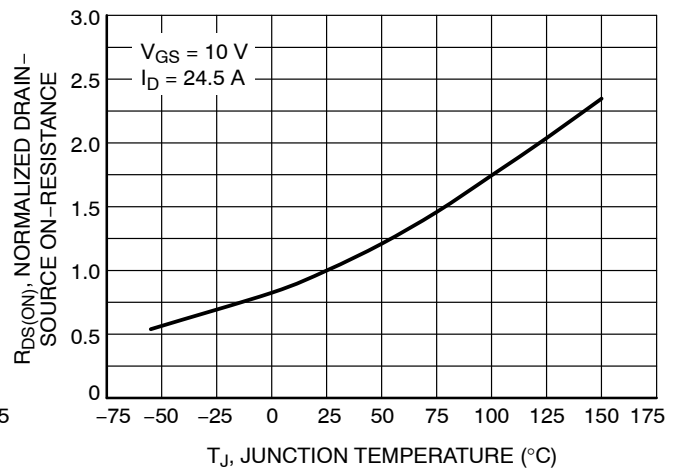


Figure 8. On-Resistance Variation vs. Temperature

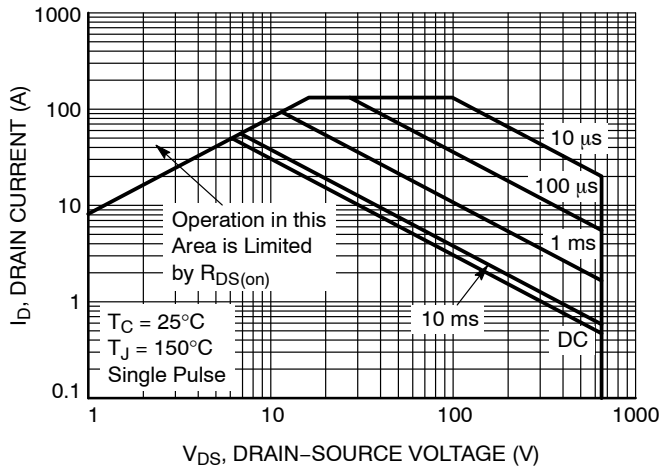


Figure 9. Maximum Safe Operating Area

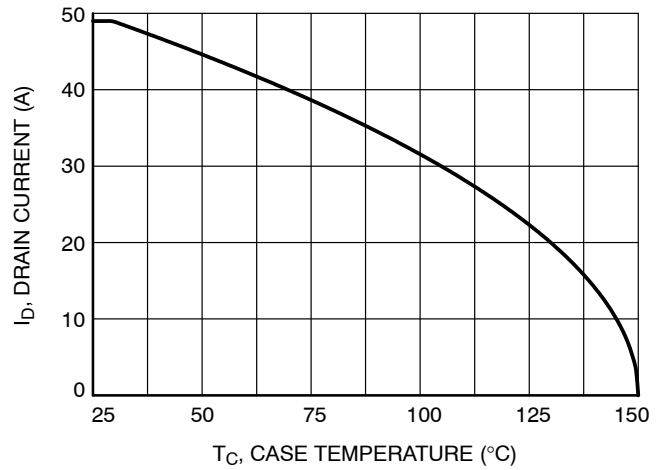


Figure 10. Maximum Drain Current vs. Case Temperature

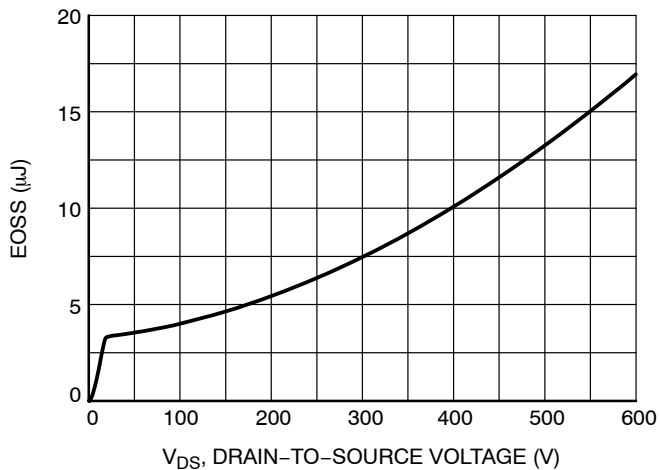


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

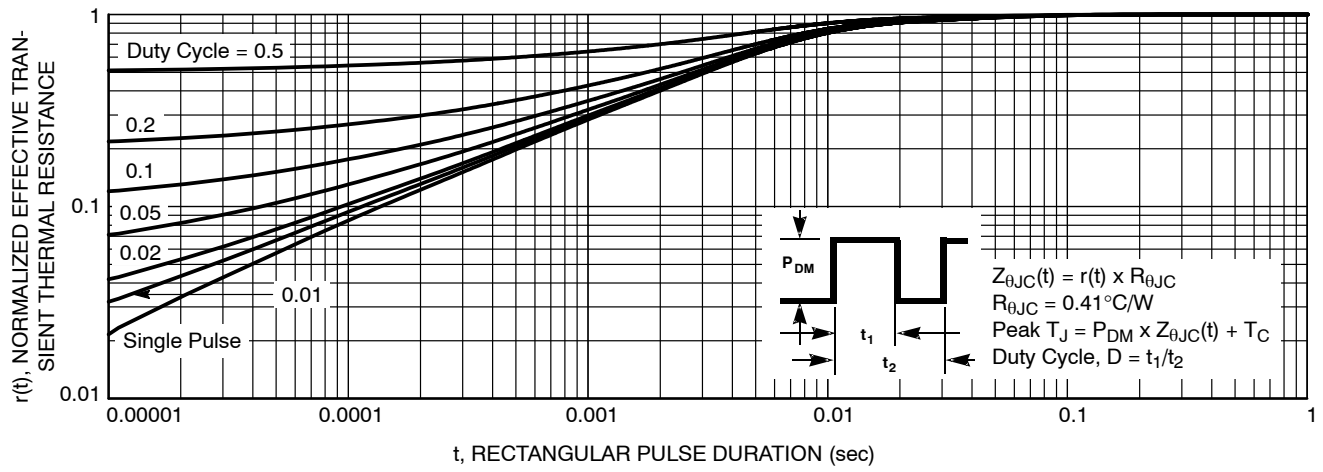


Figure 12. Transient Thermal Impedance

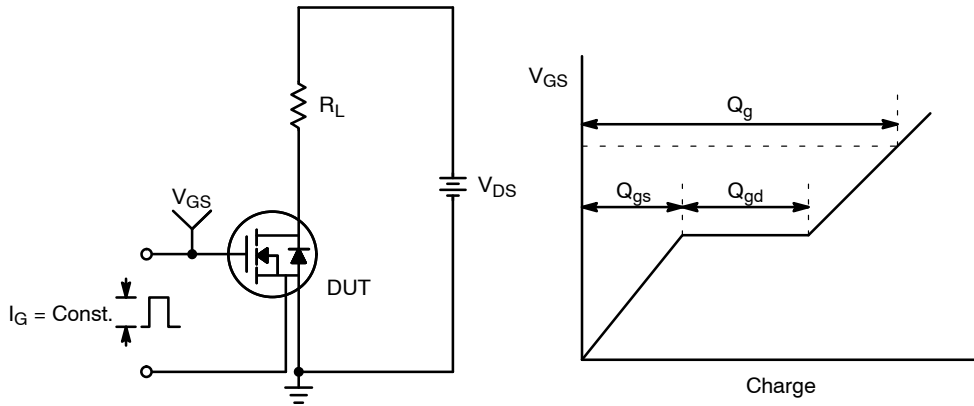


Figure 13. Gate Charge Test Circuit & Waveform

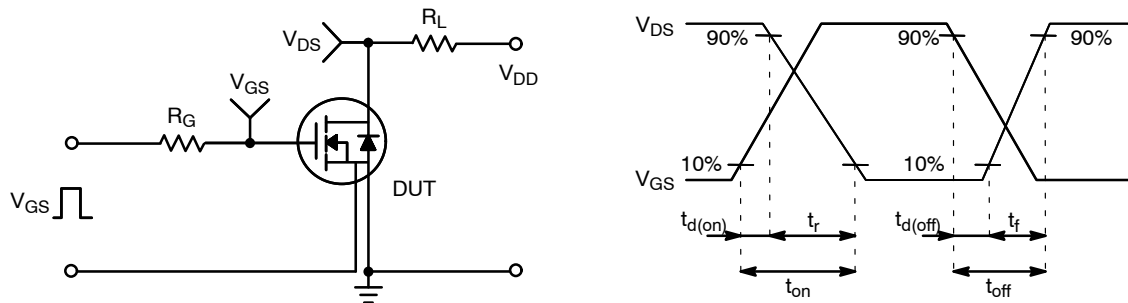


Figure 14. Resistive Switching Test Circuit & Waveforms

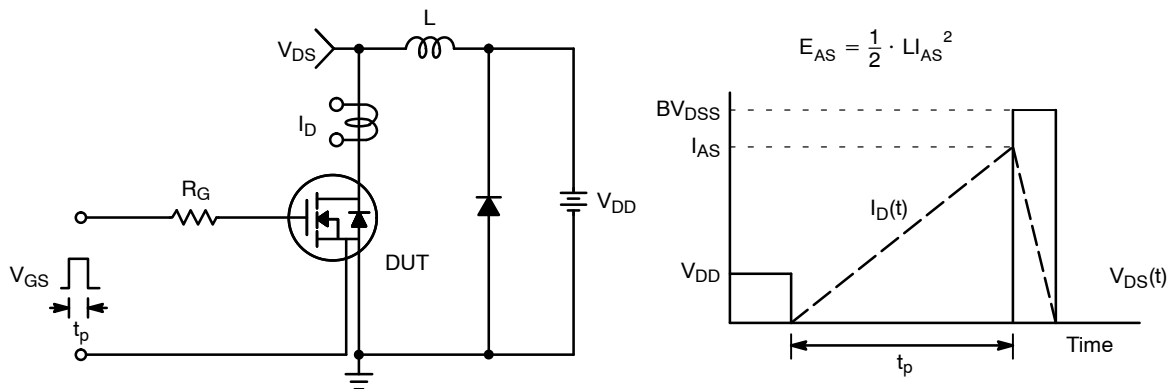


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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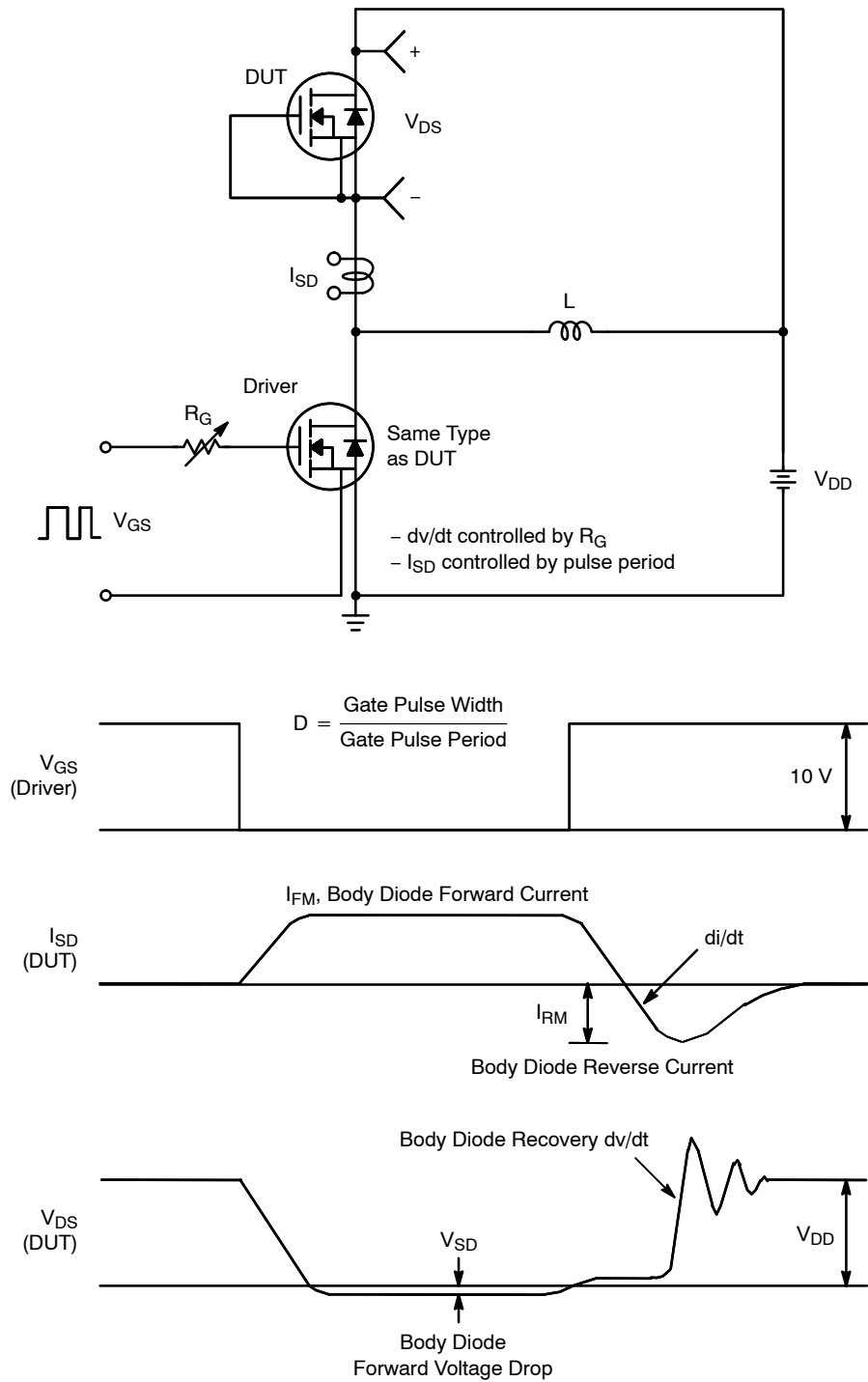
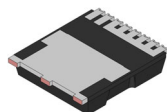


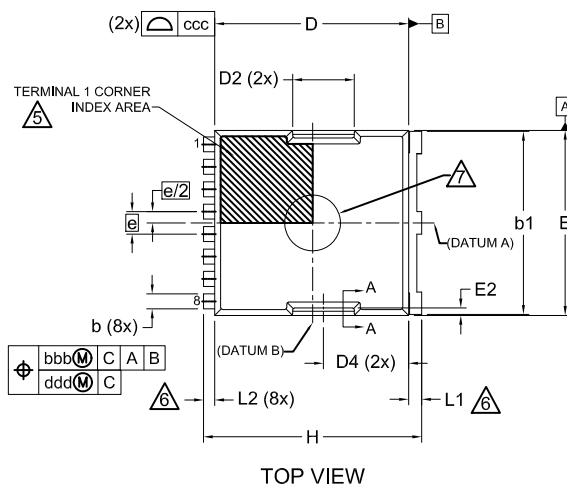
Figure 16. Peak Diode Recovery $d v/dt$ Test Circuit & Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

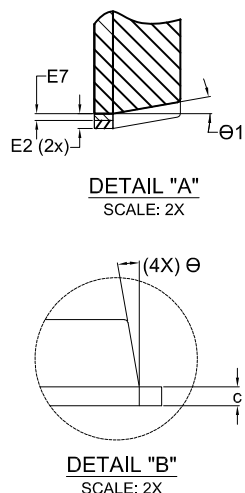


H-PSOF8L 9.90x10.38x2.30, 1.20P CASE 100DC ISSUE B

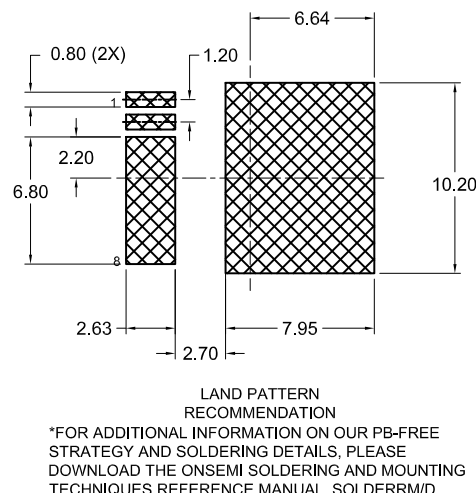
DATE 30 APR 2024



TOP VIEW

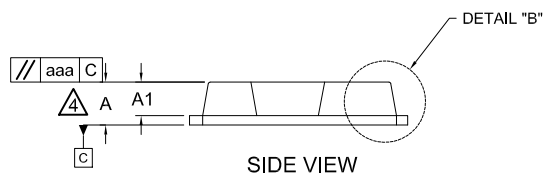


DETAIL "B"
SCALE: 2X

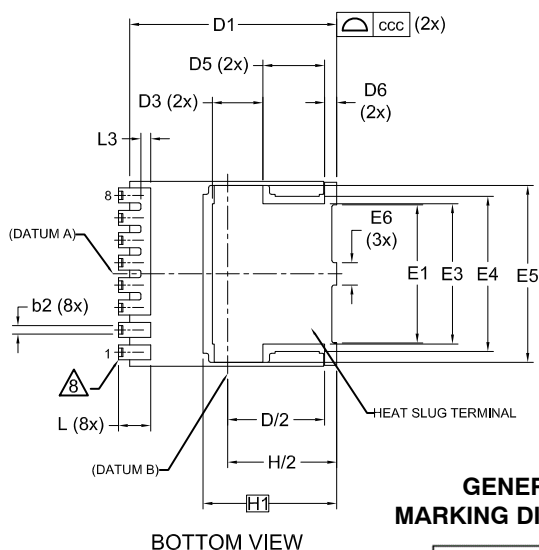


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.



SIDE VIEW



BOTTOM VIEW

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.47
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
theta	10° REF		
theta 1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	H-PSOF8L 9.90x10.38x2.30, 1.20P	PAGE 1 OF 1

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