FDBL0630N150

MOSFET – N-Channel, POWERTRENCH®

150 V, 169 A, 6.3 mΩ

Features

- Typ $r_{DS(on)}$ = 5 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typ $Q_{g(tot)}$ = 70 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- This Device is Pb−Free and is RoHS Compliant

Applications

- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch

MAXIMUM RATINGS (T_J = 25°C, unless otherwise specified)

Symbol	Parameter	Ratings	Unit
VDSS	Drain to Source Voltage	150	V
VGS	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous (V_{GS} = 10 V) (Note 1) T_C = 25°C	169	A
	Pulsed Drain Current T_C = 25°C	See Figure 4	
EAS	Single Pulse Avalanche Energy (Note 2)	502	mJ
P_D	Power Dissipation	500	W
	Derate above 25°C	3.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	0.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	43	°C/W

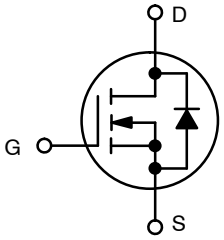
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by junction temperature.
2. Starting T_J = 25°C, L = 0.24 mH, I_{AS} = 64 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

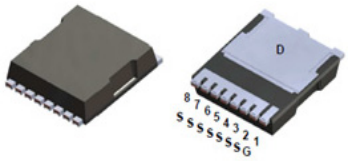
ON Semiconductor®

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V_{DSS}	$r_{DS(ON)}$ MAX	I_D MAX
150 V	6.3 mΩ @ 10 V	169 A



MOSFET — N−Channel



H−PSOF8L 11.68x9.80
CASE 100CU

MARKING DIAGRAM



$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Date Code
&K = Lot Run Traceability Code
FDBL0630N150 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		150	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 150 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
			T_J = 175°C (Note 4)	–	–	1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	2.8	4.0	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = 80 A, V_{GS} = 10 V	T_J = 25°C	–	5	6.3	mΩ
			T_J = 175°C (Note 4)	–	14	17.5	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 75V, V_{GS} = 0V, f = 1 MHz		–	5805	–	pF
C_{oss}	Output Capacitance			–	536	–	pF
C_{rss}	Reverse Transfer Capacitance			–	16	–	pF
R_g	Gate Resistance	f = 1 MHz		–	2.2	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V, V_{DD} = 75 V, I_D = 80 A		–	70	90	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 75 V, I_D = 80 A		–	10.5	13	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 75 V, I_D = 80 A		–	32.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 75 V, I_D = 80 A		–	10	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 75 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	80	ns
$t_{d(on)}$	Turn−On Delay Time			–	39	–	ns
t_r	Rise Time			–	30	–	ns
$t_{d(off)}$	Turn−Off Delay Time			–	70	–	ns
t_f	Fall Time			–	23	–	ns
t_{off}	Turn−Off Time			–	–	130	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
T_{rr}	Reverse Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 120 V		–	108	125	ns
Q_{rr}	Reverse Recovery Charge			–	323	467	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

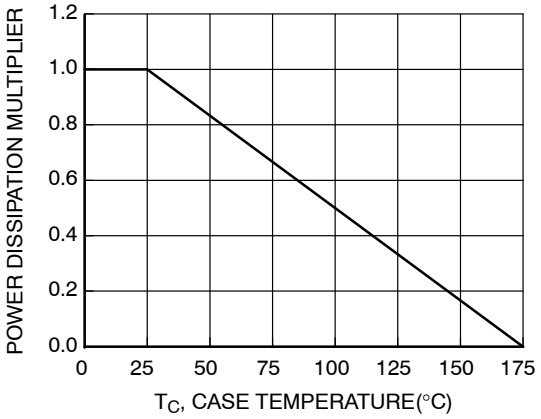


Figure 1. Normalized Power Dissipation vs. Case Temperature

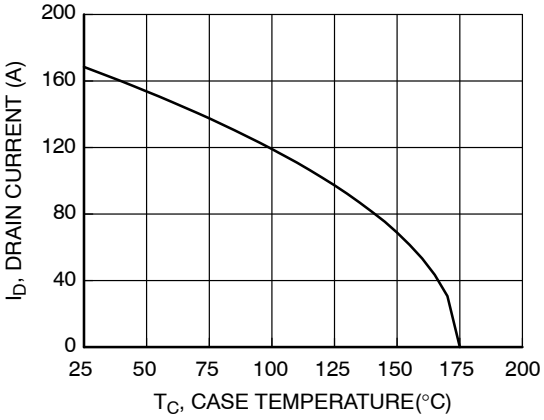


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

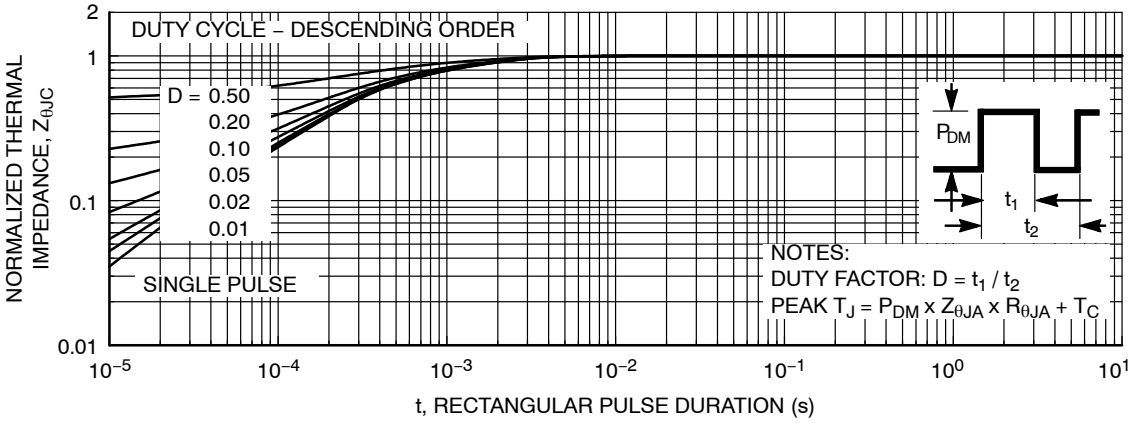


Figure 3. Normalized Maximum Transient Thermal Impedance

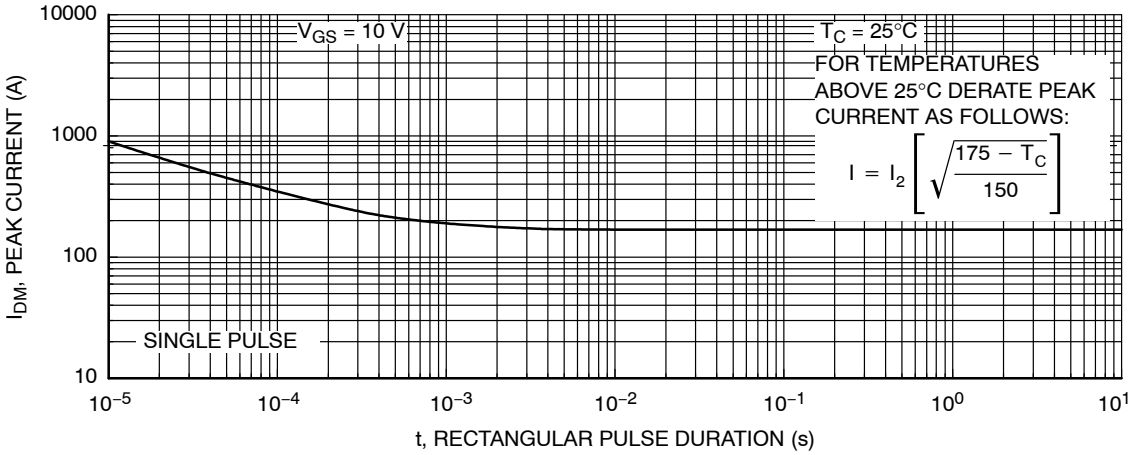


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

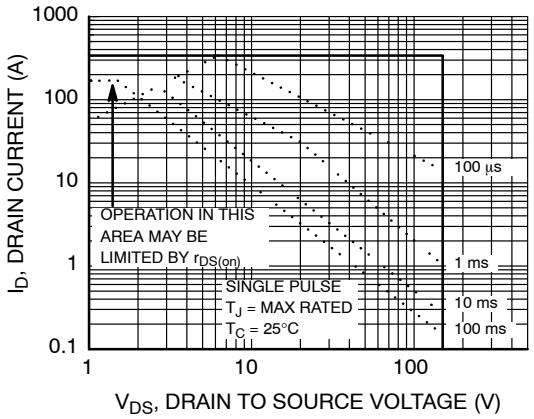
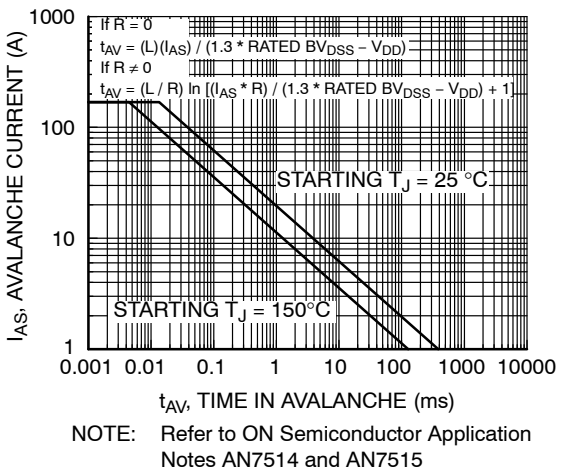


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

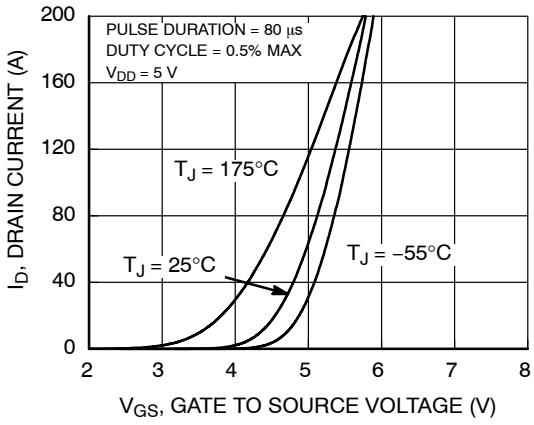


Figure 7. Transfer Characteristics

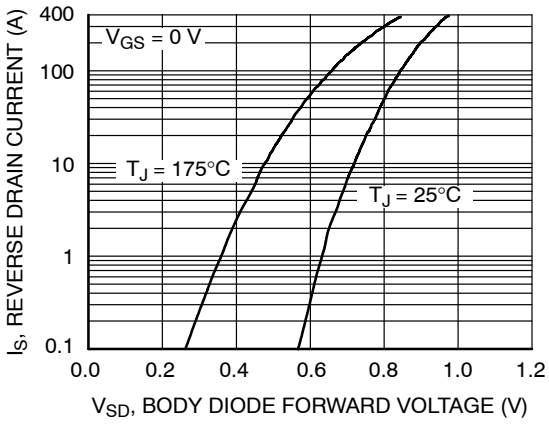


Figure 8. Forward Diode Characteristics

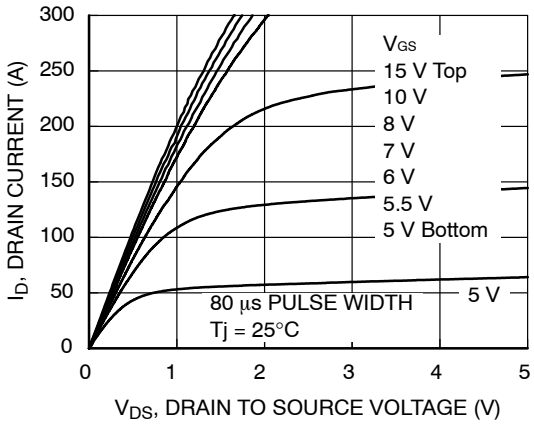


Figure 9. Saturation Characteristics

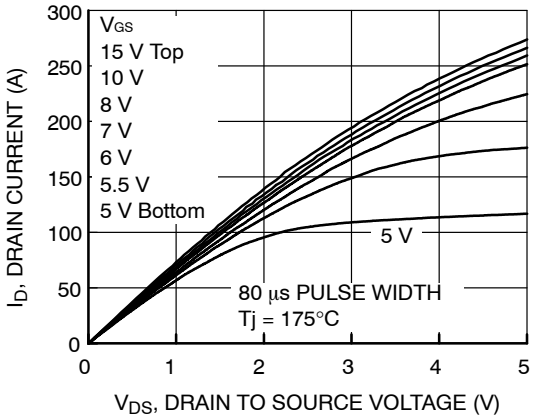


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

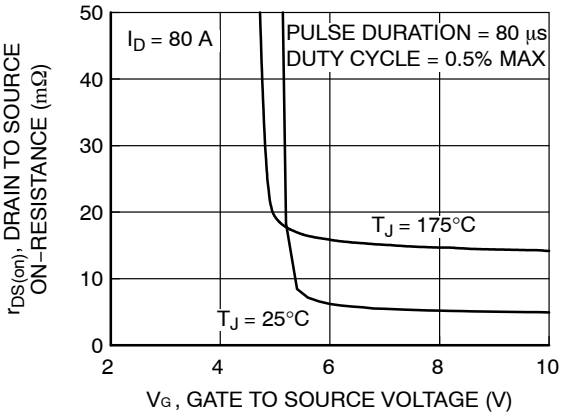


Figure 11. Rdson vs. Gate Voltage

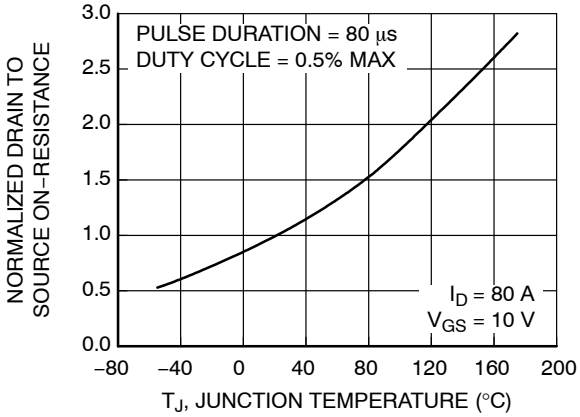


Figure 12. Normalized Rdson vs. Junction Temperature

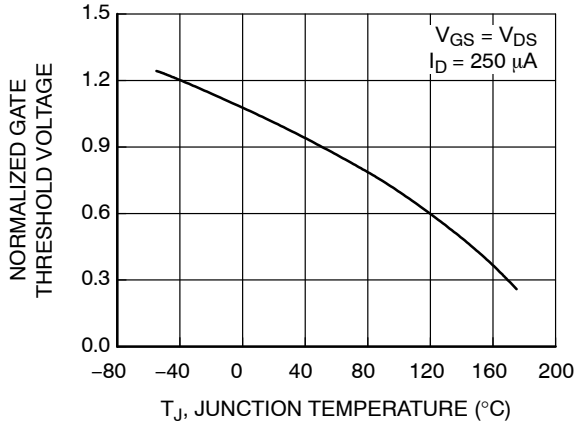


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

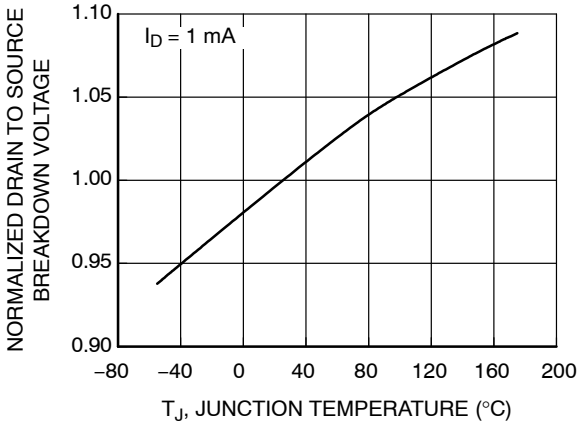


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

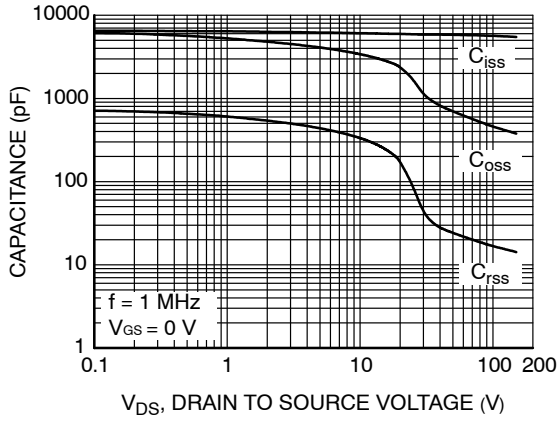


Figure 15. Capacitance vs Drain to Source Voltage

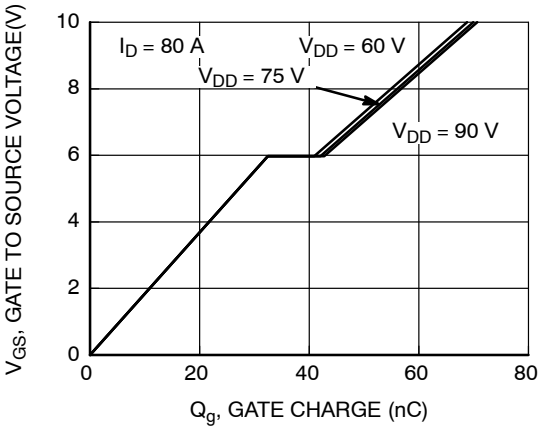


Figure 16. Gate Charge vs Gate to Source Voltage

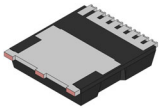
ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDBL0630N150	FDBL0630N150	H−PSOF8L 11.68x9.80 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

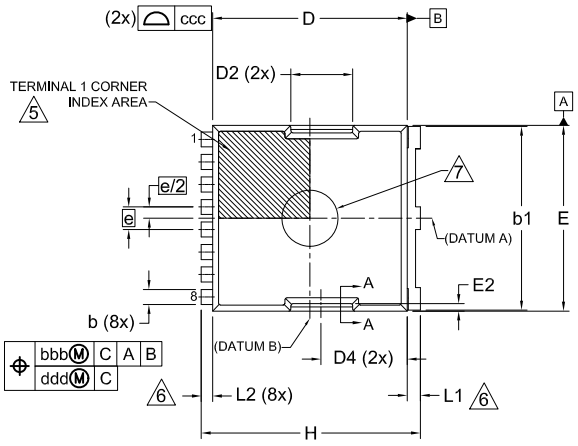
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

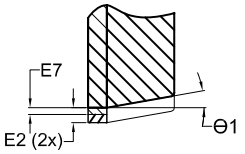


H−PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE D

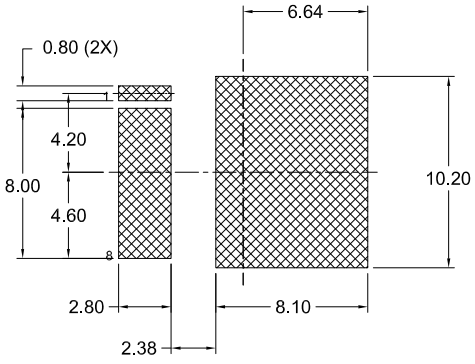
DATE 25 APRIL 2024



TOP VIEW

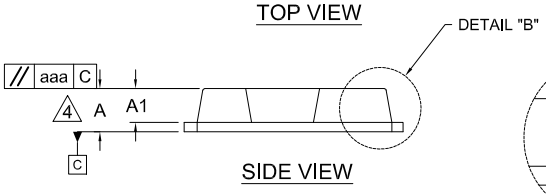


DETAIL "A"
SCALE: 2X

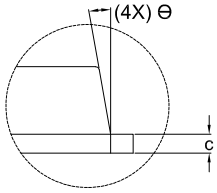


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

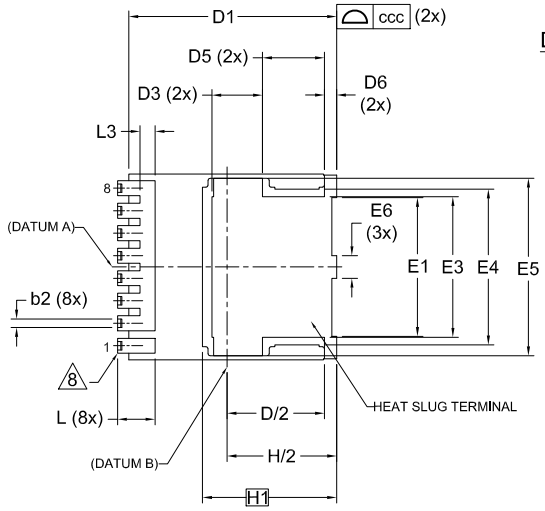


SIDE VIEW



DETAIL "B"
SCALE: 2X

NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g.,EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1,L1,L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

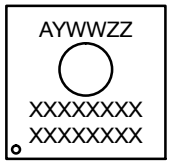


BOTTOM VIEW

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.47
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13813G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**H−PSOF8L 11.68x9.80x2.30, 1.20P**	**PAGE 1 OF 1**

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