

DESCRIPTION

The MP8020 is an IEEE 802.3af/at/bt-compliant, Power over Ethernet (PoE), powered device (PD). The device supports all the functions of IEEE 802.3af/at/bt, including detection, 5-event classification, input current (I_{IN}) control, and an internal 100V hot-swap MOSFET.

The MP8020 provides configurable inrush current limiting during start-up and operation current limiting when the internal MOSFET is fully turned on. The GATE1 driver supports the use of an external low on resistance ($R_{DS(ON)}$) MOSFET for high-power design. A high power good (PG) signal enables the use of a downstream DC/DC converter. The MP8020 also provides automatic maintain power signature functionality under light loads.

An auxiliary power input detector (AUX) and GATE2 driver provide a smooth power switch from the power-sourcing equipment (PSE) to an auxiliary wall adapter with low power loss. The MP8020 also features a built-in detection resistor, thermal protection, and a wide input under-voltage lockout (UVLO) hysteresis.

The MP8020 is available in a QFN-18 (3mmx5mm) package.

FEATURES

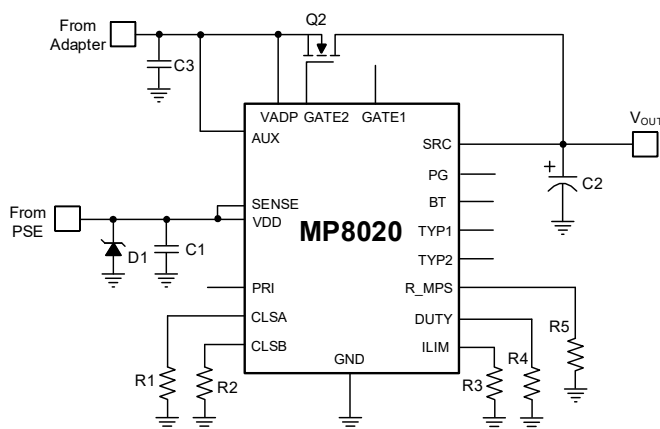
- Compliant with 802.3af/at/bt Specifications
- Internal Detection Resistor
- Supports Up to 71.3W Powered Device (PD) Operation
- Internal Hot-Swap MOSFET for $\leq 51W$ Design
- External MOSFET with GATE1 for $>51W$ Design
- Auxiliary Power Supply from $>8.8V$ Adapter
- GATE2 N-Channel MOSFET Driver for Adapter Supply
- Configurable Current Limit
- Automatic Maintain Power Signature
- PG and Allocated Power Type Indicators
- $150^{\circ}C$ Over-Temperature Protection (OTP)
- Available in a QFN-18 (3mmx5mm) Package

APPLICATIONS

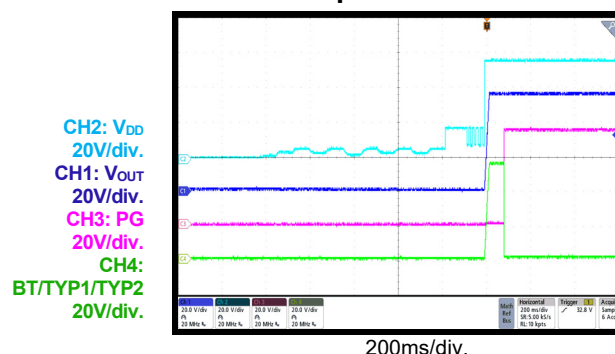
- IEEE 802.3 af/at/bt-Compliant Devices
- Security Cameras
- Video and VoIP Phones
- WLAN Access Points
- Internet of Things (IoT) Devices
- Pico Base Stations

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TYPICAL APPLICATION



PSE Start-Up



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP8020GQV*	QFN-18(3mmx5mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP8020GQV-Z).

TOP MARKING

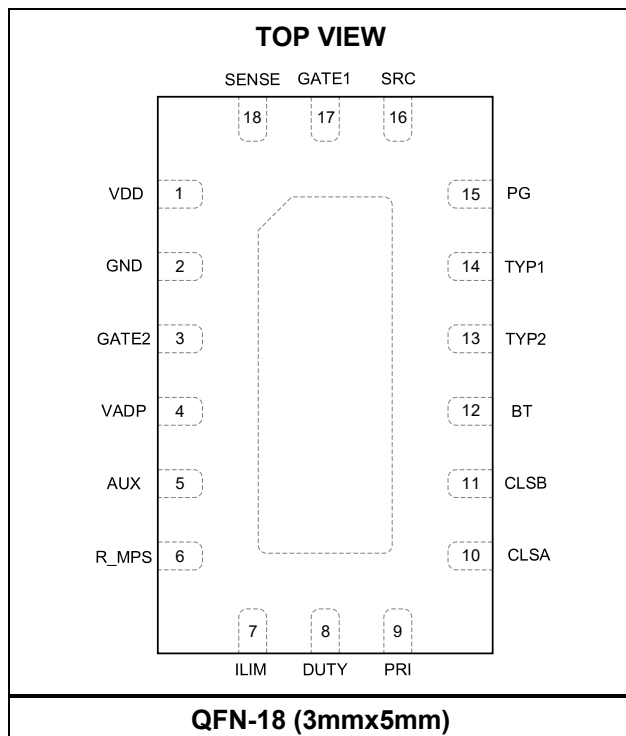
MPYW

8020

LLL

MP: MPS prefix
Y: Year code
W: Week code
8020: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	VDD	Positive power supply terminal from the Power over Ethernet (PoE) input power rail.
2	GND	Negative power supply terminal.
3	GATE2	External N-channel MOSFET GATE driver for the adapter power supply.
4	VADP	Positive power supply terminal from the adapter.
5	AUX	Adapter power input detector pin. The AUX pin configures the adapter's auxiliary power under-voltage lockout (UVLO) voltage. Pull down AUX internally to GND via a resistor. If this pin is not used, pull it to GND externally.
6	R_MPS	Automatic maintain power signature load resistor connection. The R_MPS pin generates a 24V output pulse when the maintain power signature function is triggered.
7	ILIM	Internal hot-swap MOSFET current limit configuration. See the Hot-Swap MOSFET and Current Limit section on page 17 for more details.
8	DUTY	Automatic maintain power signature output duty setting pin. See the Automatic Maintain Power Signature section on page 19 for more details.
9	PRI	Power-sourcing equipment (PSE) power and adapter power priority setting pin. Pull up this pin internally to the internal 5V power source via a resistor. If PRI is low, then the PSE power source has a higher priority.
10	CLSA	Power class signature pin. CLSA is used during the first two class events.
11	CLSB	Power class signature pin. CLSB is used during the third class event and all subsequent class events.
12	BT	PSE type indicator. BT is an open-drain output.
13	TYP2	Allocated PSE power type indicator. TYP2 is an open-drain output.
14	TYP1	Allocated PSE power type indicator. TYP1 is an open-drain output.
15	PG	Power good (PG) indicator. PG is an open-drain output. Pull this pin active high.
16	SRC	Hot-swap MOSFET source pin. SRC is the power output from both the internal and external hot-swap MOSFETs.
17	GATE1	External, parallel N-channel MOSFET GATE driver for the PSE power supply.
18	SENSE	External MOSFET current-sense pin. If not used, connect this pin to VDD.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

VDD, SENSE, SRC, TYP1, TYP2, PG, AUX, VADP, BT	-0.3V to +100V
R_MPS	-0.3V to +30V
GATE1 to SRC	-0.3V to +6.5V
GATE2 to VADP	-0.3V to +6.5V
SENSE to VDD	-6.5V to +0.3V
All other pins	-0.3V to +6.5V
PG, TYP1, TYP2, BT sinking current.....	5mA
Continuous power dissipation (T _A = 25°C) ⁽²⁾	2.7W ⁽⁴⁾
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to +150°C

Recommended Operating Conditions ⁽³⁾

PSE supply voltage (V _{DD}).....	0V to 57V
Adapter supply voltage (V _{ADP}).....	0V to 57V
PG, TYP1, TYP2, BT max sink current.....	3mA
Operating junction temp (T _J)....	-40°C to +125°C

Thermal Resistance

 θ_{JA}
 θ_{JC}

QFN-18 (3mmx5mm)

EV8020-QV-00A ⁽⁴⁾ 46 7°C/W

JESD51-7 ⁽⁵⁾ 47 7°C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on the EV8020-QV-00A, a 1oz, 2-layer (63mmx63mm) PCB.
- 5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

$V_{DD} = 54V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁶⁾, typical values are tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V_{DET-ON}	V_{DD} rising		1	1.4	V
Detection off	$V_{DET-OFF}$	V_{DD} rising	10.1	11		V
Bias current	I_{BIAS}	$V_{DD} = 10.1V$, not in mark event, measure I_{SUPPLY}			12	μA
Detection resistance	R_{DET}	V_{DD} from 1.5V to 10.1V, calculate with $\Delta V / \Delta I$	24.1	25	26.1	k Ω
Classification						
Classification stability time		Stable output voltage (V_{OUT}) from V_{CL-ON} to CLSA or CLSB		0.4	1	ms
CLSA and CLSB class voltage (V_{CLASS}) output voltage	V_{CLSA}	$13V < V_{DD} < 21V$, $1mA < I_{CLASS} < 44mA$	1.11	1.16	1.21	V
	V_{CLSB}					
Classification current for CLSA and CLSB	I_{CLASS}	Measure input current, $13 \leq V_{DD} \leq 21V$, guaranteed by V_{CLSA} and V_{CLSB}				mA
		$R_{CLASS} = 578\Omega$, $13 \leq V_{DD} \leq 21V$	1.8	2	2.4	
		$R_{CLASS} = 110\Omega$, $13 \leq V_{DD} \leq 21V$	9.9	10.55	11.3	
		$R_{CLASS} = 62\Omega$, $13 \leq V_{DD} \leq 21V$	17.7	18.7	19.8	
		$R_{CLASS} = 41.2\Omega$, $13 \leq V_{DD} \leq 21V$	26.6	28.15	29.7	
		$R_{CLASS} = 28.7\Omega$, $13 \leq V_{DD} \leq 21V$	38.2	40.4	42.6	
Long first class event	t_{LCE}	Determine type 3 and type 4 PoE from trigger V_{CL-ON}	76	81.5	87	ms
Classification lower threshold	V_{CL-ON}	Regulator turns on, V_{DD} rising	12	12.5	13	V
Classification lower threshold hysteresis	$V_{CL-L-HYS}$	Low threshold hysteresis	1.3	1.5	1.7	V
Classification upper threshold	V_{CL-OFF}	Regulator turns off, V_{DD} rising	21	22	23	V
Classification upper threshold hysteresis	$V_{CL-H-HYS}$	High threshold hysteresis		0.5		V
Mark event reset threshold	V_{MARK-L}		4.5	5	5.5	V
Max mark event voltage	V_{MARK-H}		10.5	11	11.5	V
Mark event current	I_{MARK}		0.5	1.1	2	mA
Mark event resistance	R_{MARK}	2-point measurement at 5.5V and 10.1V, calculate with $\Delta V / \Delta I$			12	k Ω
IC supply current during classification	$I_{IN-CLASS}$	$V_{DD} = 17.5V$, float CLSA and CLSB		180	300	μA
Class leakage current	$I_{LEAKAGE}$	$V_{CLSA} = V_{CLSB} = 0V$, $V_{DD} = 57V$, test both CLSA and CLSB			1	μA

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 54V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁶⁾, typical values are tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Under-Voltage Lockout (UVLO)						
V_{DD} turn-on threshold	V_{DD_R}	V_{DD} rising	37	38.5	40	V
V_{DD} turn-off threshold	V_{DD_F}	V_{DD} falling	30	31.5	33	V
V_{DD} UVLO hysteresis	V_{DD_HYS}		5	7		V
IC supply current during operation	I_{IN}	No load and no R_{MPS} resistor		1	1.5	mA
Input leakage current		$V_{DD} = 29.5V$		150	250	μA
Hot-Swap MOSFET and Current Limit						
Internal MOSFET on resistance	$R_{DS(ON)}$	$I_{SRC} = 500mA$		0.35		Ω
Leakage current	I_{SRC-LK}	$V_{DD} = 57V$, $V_{SRC} = 0V$, AUX = high, PRI = high		1	15	μA
ILIM detection period				270		μs
ILIM detection current			130	165	180	μA
ILIM voltage threshold		0.9A setting voltage range			0.8	V
		1.6A setting voltage range	1		2.2	V
Internal MOSFET current limit	I_{LIMIT}	V_{SRC} drops from V_{DD} , $V_{DD} - V_{SRC} = 1V$				
		ILIM = 0V	0.75	0.9	1.05	A
		Connect ILIM to GND via a 7.15k Ω resistor	1.4	1.6	1.8	A
Internal MOSFET inrush limit	I_{INRUSH}	V_{SRC} ramps up from low to high, $V_{DD} - V_{SRC} = 1V$				
		ILIM = 0V	70	130	190	mA
		Connect ILIM to GND via a 7.15k Ω resistor	170	230	290	mA
Inrush current termination	I_{TERM}	V_{SRC} rising, I_{TERM} / I_{INRUSH}		75%		I_{INRUSH}
Inrush to operation mode delay	t_{DELAY}		80	90	100	ms
Current foldback threshold		V_{SRC} falling, $V_{DD} - V_{SRC}$	8.2	10	11.8	V
Foldback deglitch time ⁽⁷⁾		V_{SRC} falling to inrush current foldback		1		ms
GATE1 source current		$V_{GATE1} - V_{SRC} = 4V$		10		μA
GATE1 sink current		$V_{GATE1} - V_{SRC} = 4V$		30		μA
GATE1 max driving voltage				6		V
External MOSFET current limit		$V_{DD} - V_{SENSE}$	22	26	30	mV
SENSE leakage current		$V_{SENSE} = V_{DD} = 54V$			0.1	μA
PG, BT, TYP1, TYP2						
Output low voltage		$I_{SINK} = 1mA$		0.2	0.4	V
Leakage current		Logic = high, connect to 57V			1	μA

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 54V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁶⁾, typical values are tested at $T_J = 25^{\circ}C$, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maintain Power Signature						
Automatic maintain power signature current enable threshold	$I_{PORT-MPS}$	Load current drops		36		mA
Automatic maintain power signature current threshold hysteresis		Load current rises to disable the maintain power signature current again		10		mA
R_MPS output voltage		1mA to 20mA	23	24	25	V
Type 1 and type 2 power sourcing equipment (PSE), R_MPS output duty cycle		Duty		37		%
		On period	75	85	95	ms
		Off period	115	140	165	ms
Type 3 and type 4 PSE, R_MPS output duty cycle with DUTY short to GND		Duty		6		%
		On period	14	16	18	ms
		Off period	210	250	290	ms
Type 3 and type 4 PSE, R_MPS output duty cycle with DUTY to GND via a 7.15kΩ resistor		Duty		11.5		%
		On period	26	31	36	ms
		Off period	200	235	270	ms
Type 3 and type 4 PSE, R_MPS output duty cycle with DUTY floating		Duty		17		%
		On period	39	45	52	ms
		Off period	190	221	260	ms
External MOSFET voltage drop control threshold		$V_{DS} = V_{SENSE} - V_{SRC}$		26		mV
DUTY detection current			130	165	180	μA
DUTY detection period				130		μs
DUTY voltage threshold		6% duty setting voltage range			0.8	V
		11.5% duty setting voltage range	1		2.2	V
		17% duty setting voltage range	2.5			V
Adapter Supply						
V _{ADP} UVLO rising threshold	ADP _{UV-R}		7.8	8.3	8.8	V
V _{ADP} UVLO falling threshold	ADP _{UV-F}		6.5	7	7.5	V
AUX high threshold voltage	V _{AUX-H}		1.92	2	2.08	V
AUX threshold hysteresis	V _{AUX-HYS}			0.15		V
AUX leakage current		V _{AUX} = 2V		1		μA
		V _{AUX} = 57V		2.5		μA
GATE2 source current		V _{GATE2} - V _{ADP} = 4V		20		μA
GATE2 sink current		V _{GATE2} - V _{ADP} = 4V	200			μA
GATE2 max driving voltage		GATE2 to V _{ADP}		6		V
GATE2 turn-on threshold		V _{ADP} - V _{SRC} voltage after adapter supply is enabled	0		0.45	V

ELECTRICAL CHARACTERISTICS *(continued)*

$V_{DD} = 54V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ⁽⁶⁾, typical values are tested at $T_J = 25^{\circ}C$, unless otherwise noted.

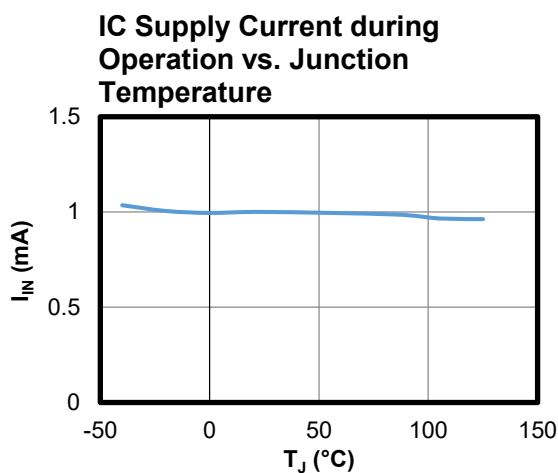
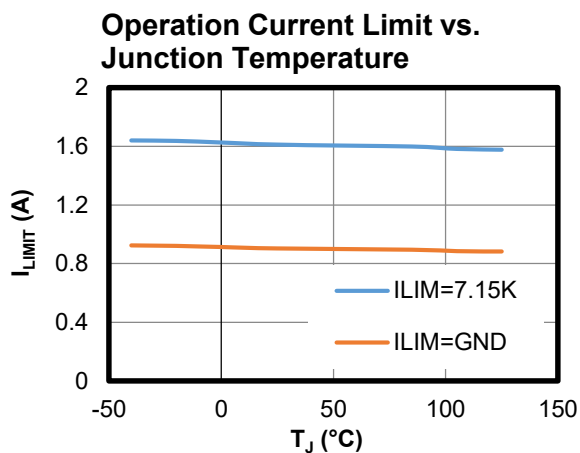
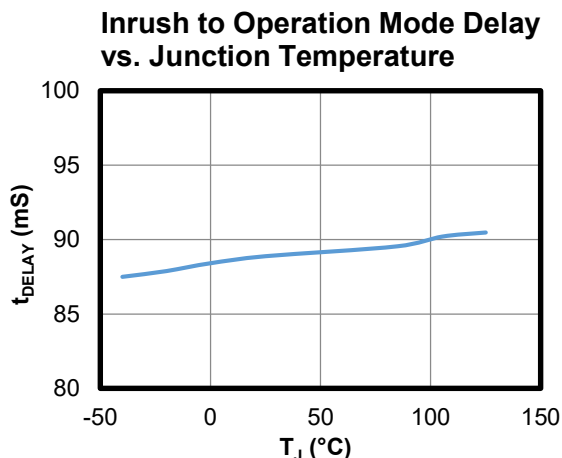
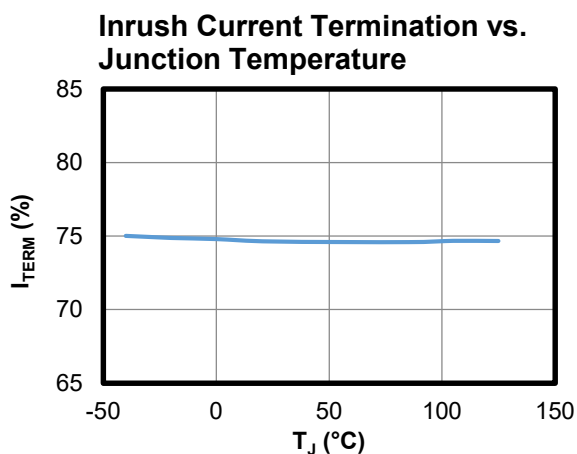
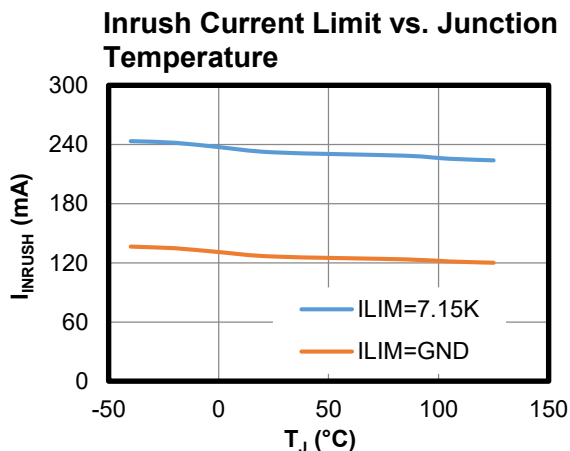
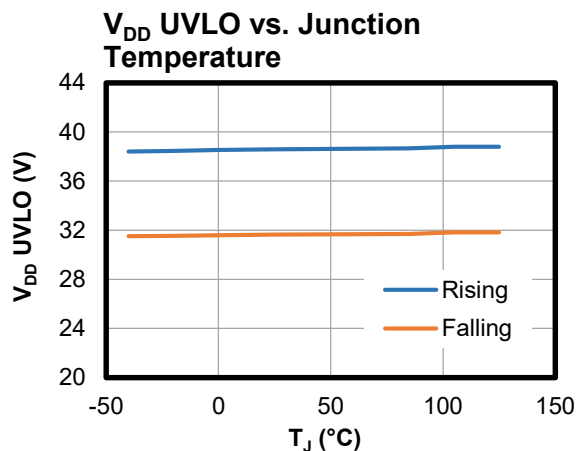
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Priority						
PRI input high voltage			2			V
PRI input low voltage					0.4	V
PRI internal pull up resistor		Pull up to internal 5V V_{CC}		1		m Ω
Thermal Shutdown						
Thermal shutdown temperature	T_{SD}			150		$^{\circ}C$
Thermal shutdown hysteresis	T_{HYS}			20		$^{\circ}C$

Notes:

- 6) Guaranteed by over-temperature correlation. Not tested in production.
7) Guaranteed by characterization. Not tested in production.

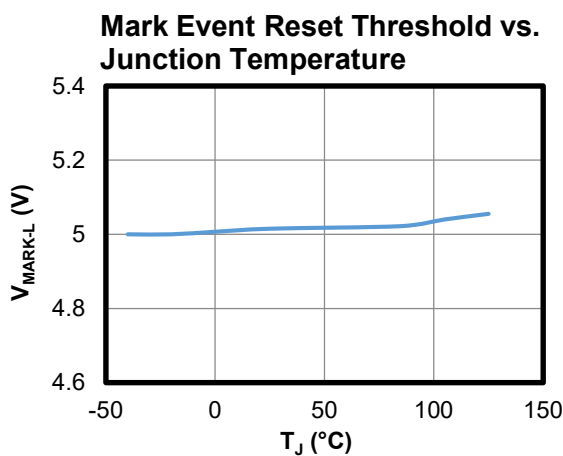
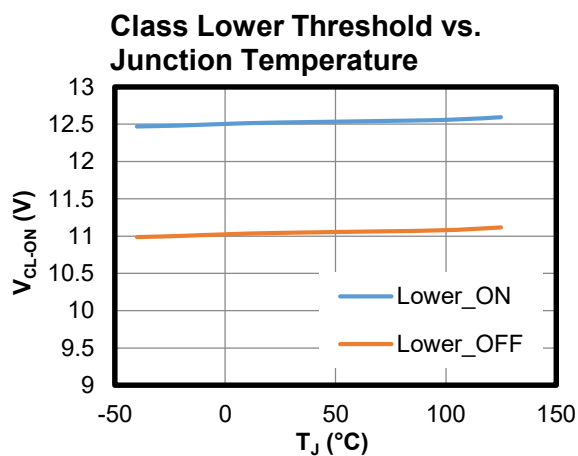
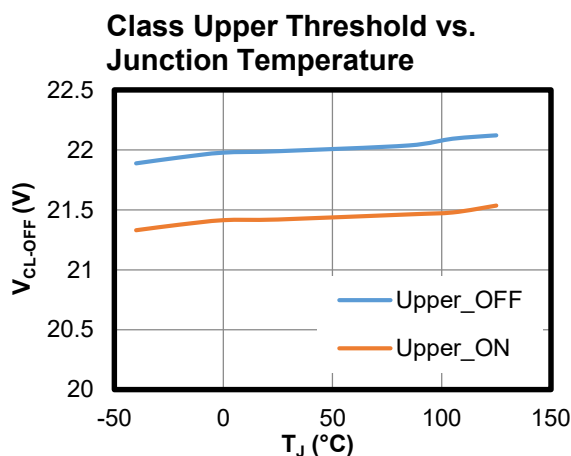
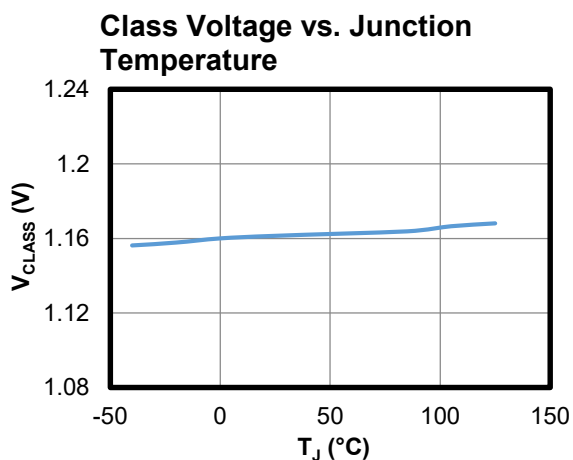
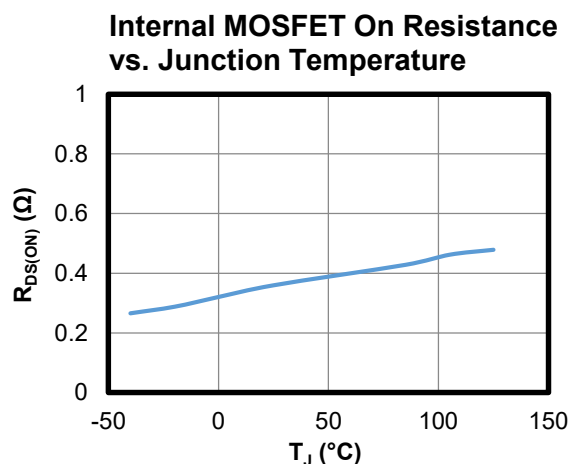
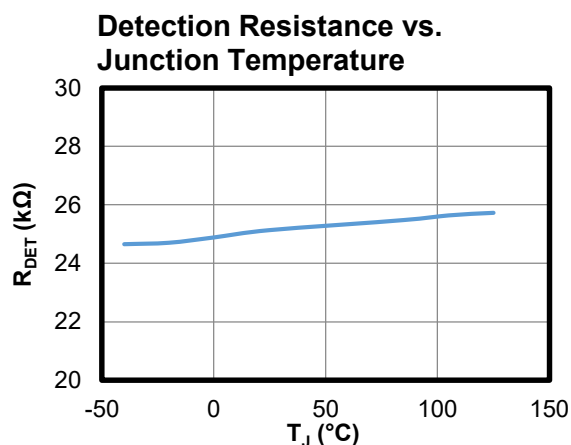
TYPICAL CHARACTERISTICS

$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.



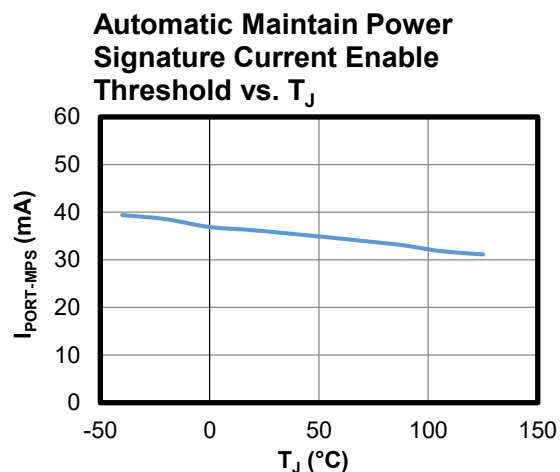
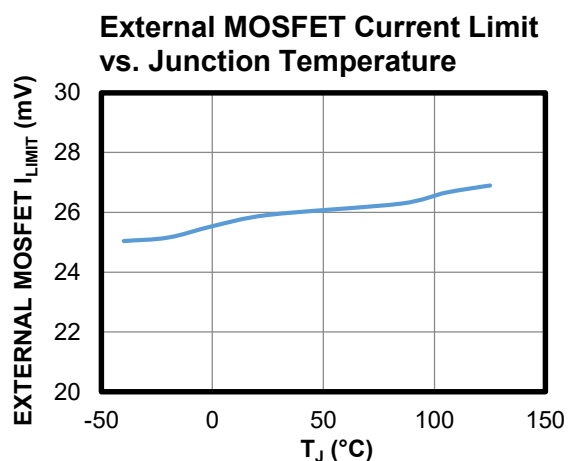
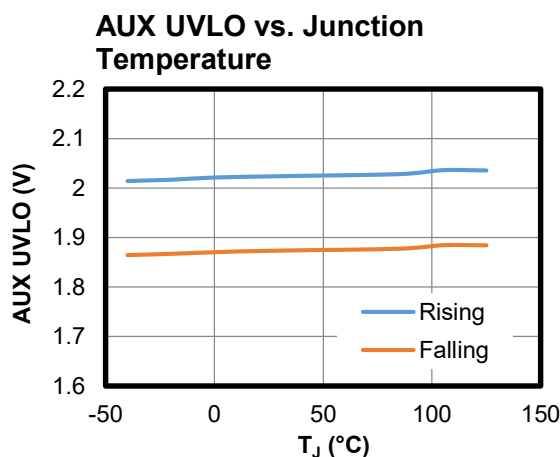
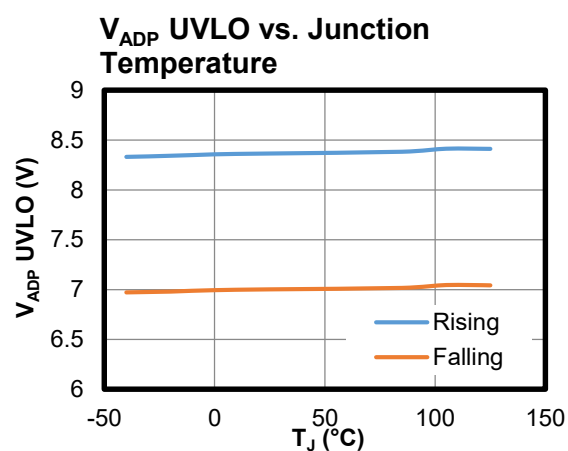
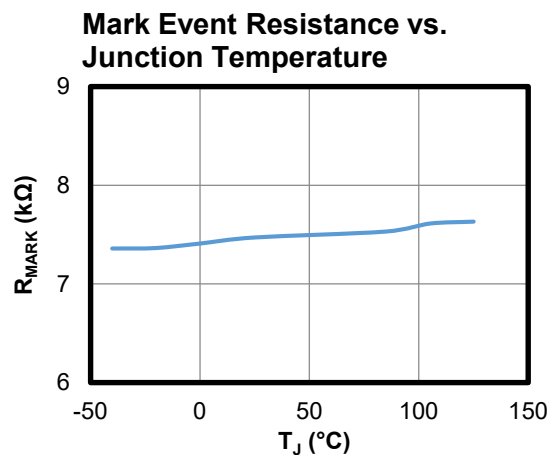
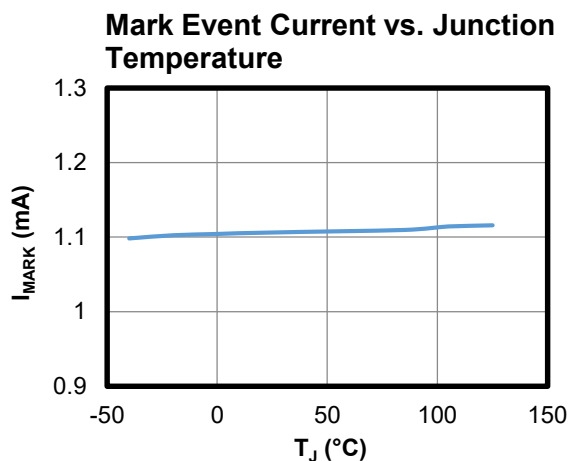
TYPICAL CHARACTERISTICS *(continued)*

$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.



TYPICAL CHARACTERISTICS *(continued)*

$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.



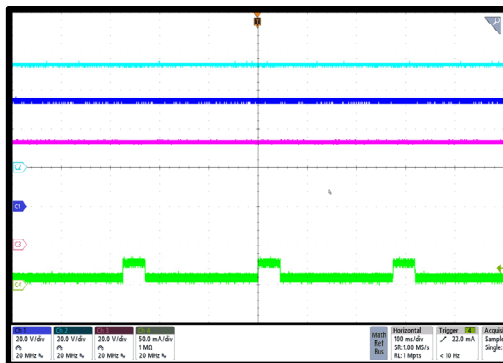
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Steady State

$I_{OUT} = 0A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
50mA/div.

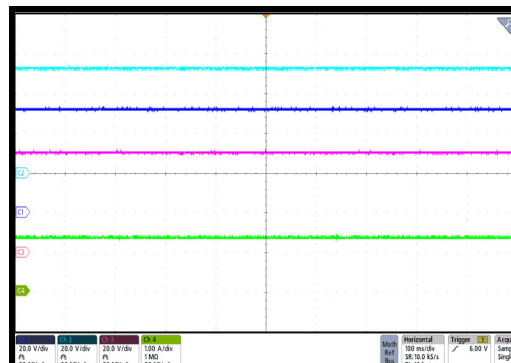


100ms/div.

Steady State

$I_{OUT} = 1.35A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
1A/div.

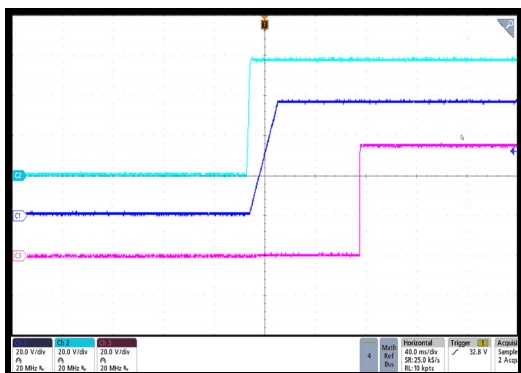


100ms/div.

Start-Up through VDD

$I_{OUT} = 0A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.

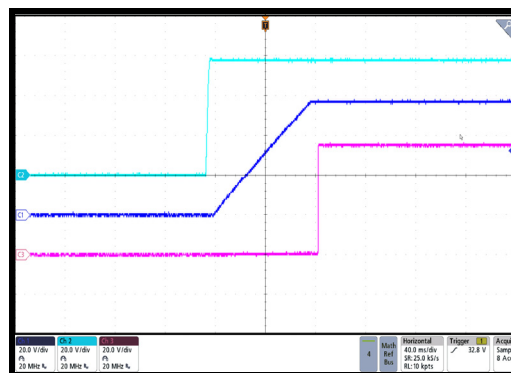


40ms/div.

Start-Up through VDD

$I_{OUT} = 0.1A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.

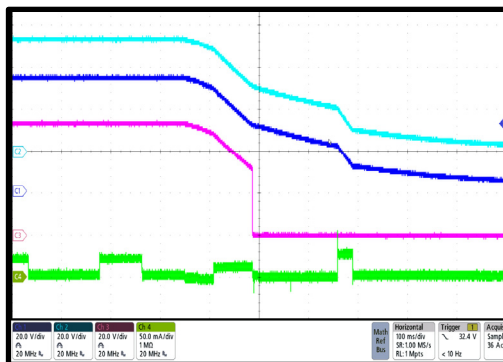


40ms/div.

Shutdown through VDD

$I_{OUT} = 0A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
50mA/div.

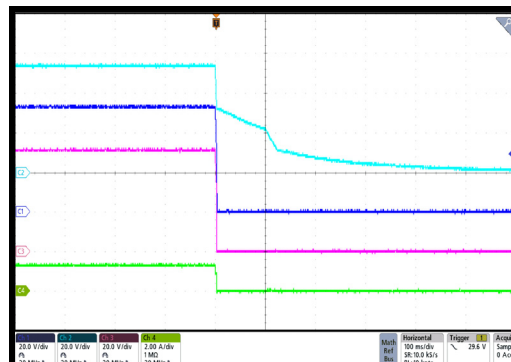


100ms/div.

Shutdown through VDD

$I_{OUT} = 1.35A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
2A/div.



100ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

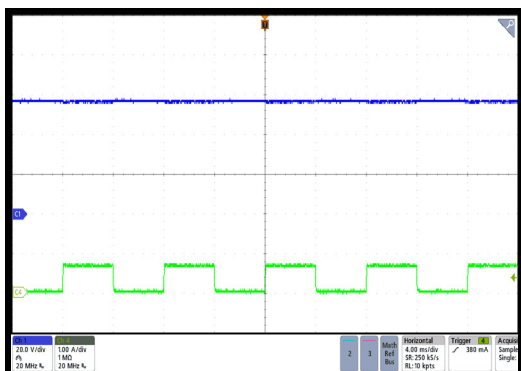
$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Load Transient

$I_{OUT} = 0A$ to $0.675A$, $I_{RAMP} = 50mA/\mu s$

CH1: V_{OUT}
20V/div.

CH4: I_{OUT}
1A/div.



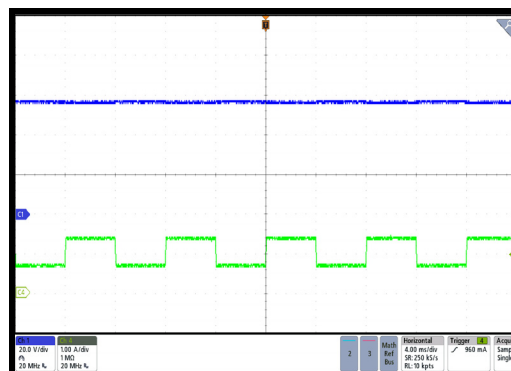
4ms/div.

Load Transient

$I_{OUT} = 0.675A$ to $1.35A$, $I_{RAMP} = 50mA/\mu s$

CH1: V_{OUT}
20V/div.

CH4: I_{OUT}
1A/div.

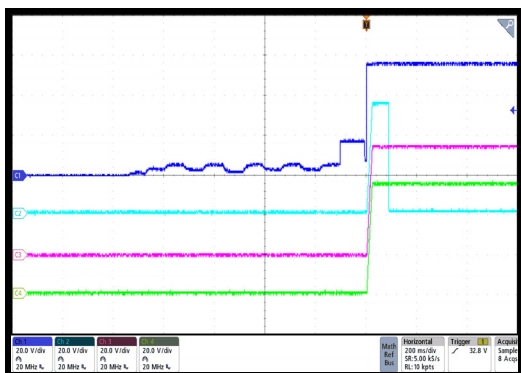


4ms/div.

PSE Start-Up

Class 1

CH1: V_{DD}
20V/div.
CH2: BT
20V/div.
CH3: TYP1
20V/div.
CH4: TYP2
20V/div.

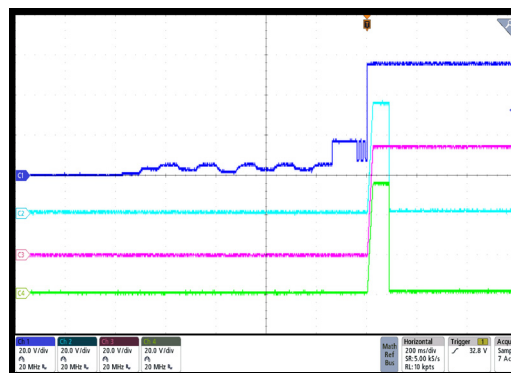


200ms/div.

PSE Start-Up

Class 4

CH1: V_{DD}
20V/div.
CH2: BT
20V/div.
CH3: TYP1
20V/div.
CH4: TYP2
20V/div.

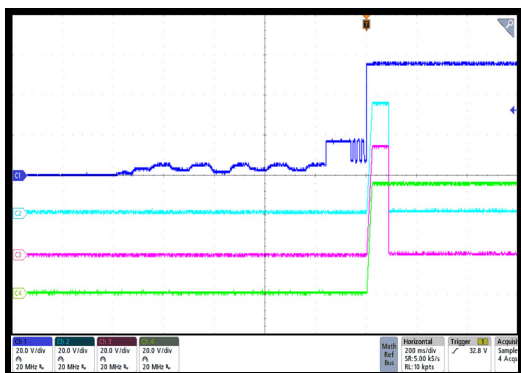


200ms/div.

PSE Start-Up

Class 6

CH1: V_{DD}
20V/div.
CH2: BT
20V/div.
CH3: TYP1
20V/div.
CH4: TYP2
20V/div.

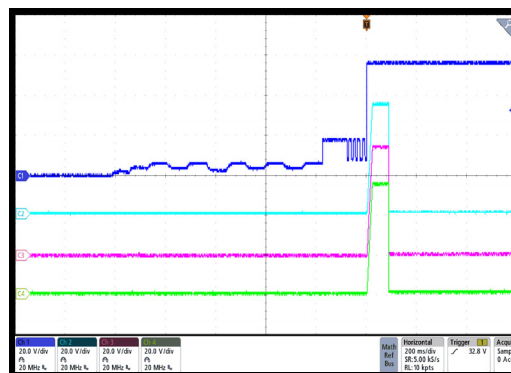


200ms/div.

PSE Start-Up

Class 8

CH1: V_{DD}
20V/div.
CH2: BT
20V/div.
CH3: TYP1
20V/div.
CH4: TYP2
20V/div.



200ms/div.

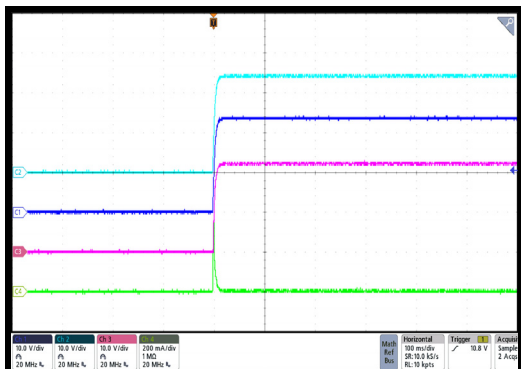
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} = 54V$, $V_{ADP} = 24V$, $T_A = 25^{\circ}C$, unless otherwise noted.

Adapter Start-Up

$I_{OUT} = 0A$

CH2: V_{ADP}
10V/div.
CH1: V_{OUT}
10V/div.
CH3: PG
10V/div.
CH4: I_{VADP}
200mA/div.

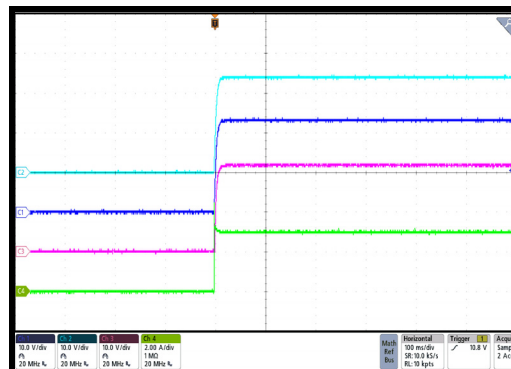


100ms/div.

Adapter Start-Up

$I_{OUT} = 3A$

CH2: V_{ADP}
10V/div.
CH1: V_{OUT}
10V/div.
CH3: PG
10V/div.
CH4: I_{VADP}
2A/div.

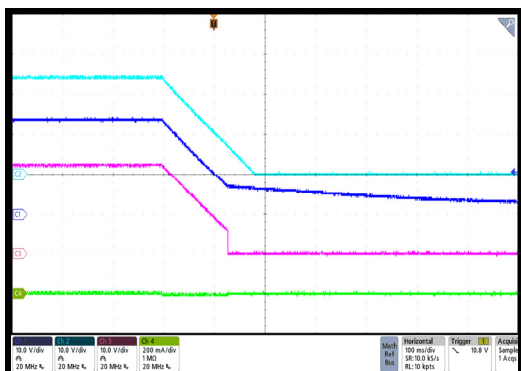


100ms/div.

Adapter Shutdown

$I_{OUT} = 0A$

CH2: V_{ADP}
10V/div.
CH1: V_{OUT}
10V/div.
CH3: PG
10V/div.
CH4: I_{VADP}
200mA/div.

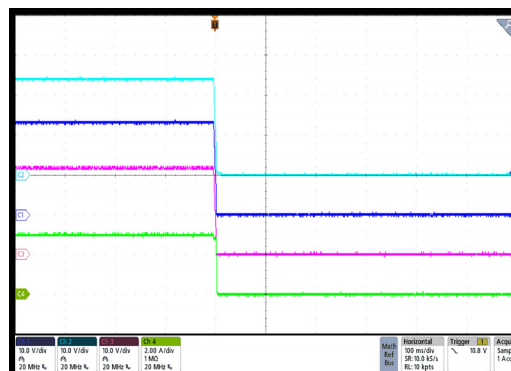


100ms/div.

Adapter Shutdown

$I_{OUT} = 3A$

CH2: V_{ADP}
10V/div.
CH1: V_{OUT}
10V/div.
CH3: PG
10V/div.
CH4: I_{VADP}
2A/div.

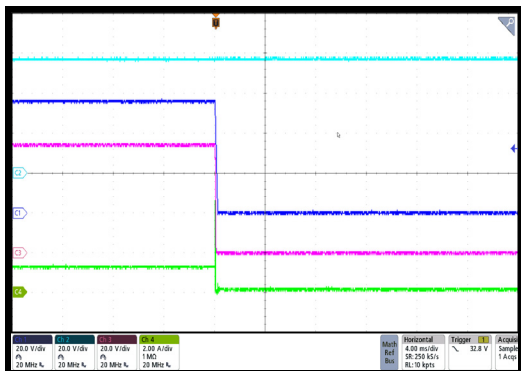


100ms/div.

SCP Entry

$I_{OUT} = 1.35A$ to short

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
2A/div.

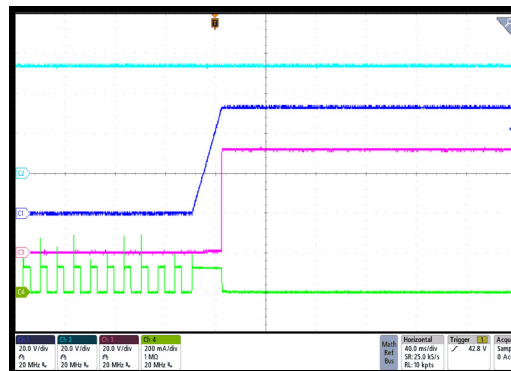


4ms/div.

SCP Recovery

$I_{OUT} = \text{short to } 0A$

CH2: V_{DD}
20V/div.
CH1: V_{OUT}
20V/div.
CH3: PG
20V/div.
CH4: I_{VDD}
200mA/div.



40ms/div.

FUNCTIONAL BLOCK DIAGRAM

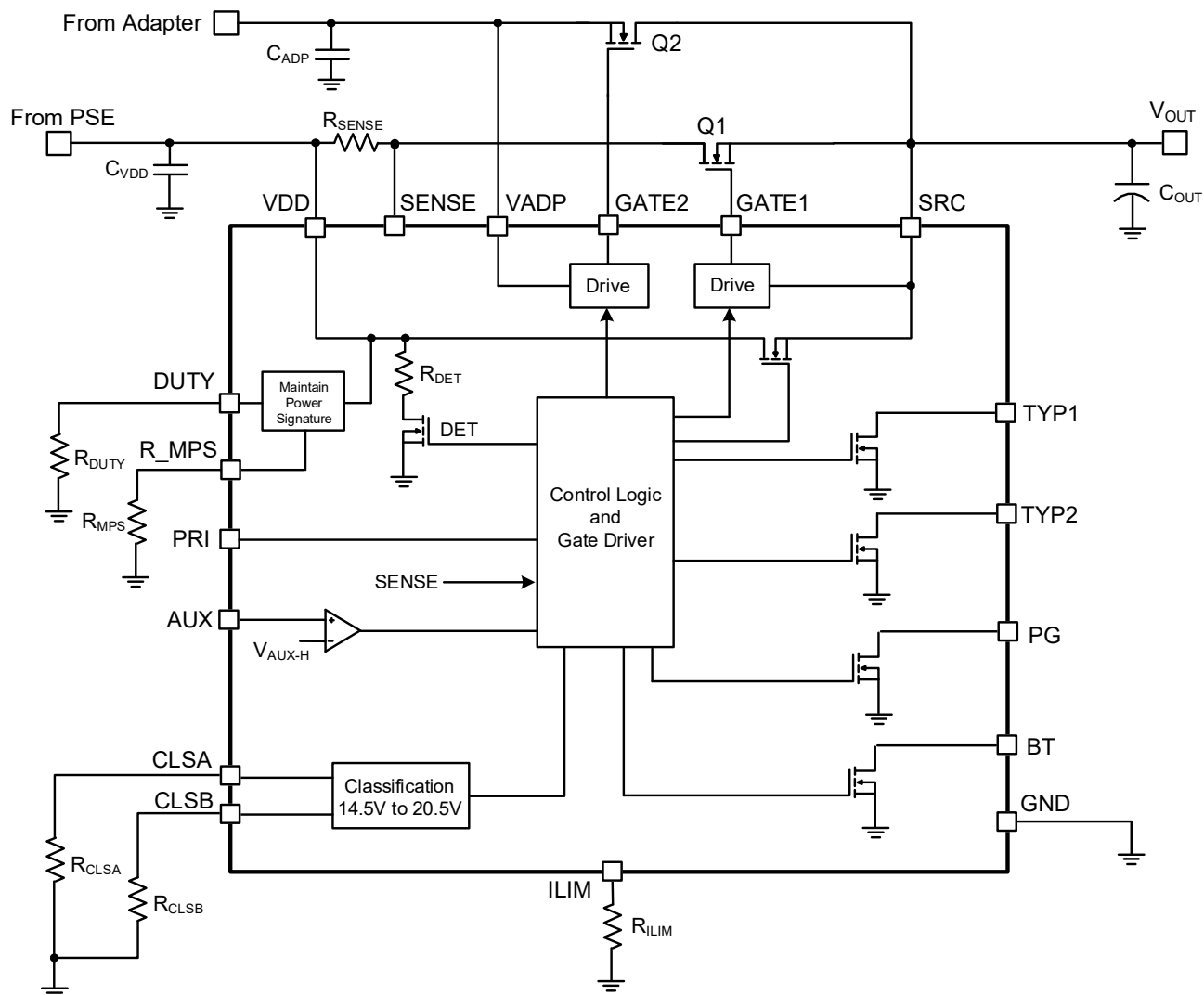


Figure 1: Functional Block Diagram

OPERATION

The MP8020 is an IEEE802.3af/at/bt-compliant, Power over Ethernet (PoE), powered device (PD). The device includes all the functions of IEEE 802.3af/at/bt, including detection, classification, input current (I_{IN}) control, a 100V hot-swap MOSFET, and automatic maintain power signature functionality.

Detection

The MP8020 integrates an internal detection resistor. When the power-sourcing equipment

(PSE) applies two safe voltages between 2.7V and 10.1V to the MP8020, the MP8020 typically shows a 25k Ω resistance between the VDD and GND pins.

Classification

The PSE distributes power to the PDs based on the classification results. Classification mode is active between 14.5V and 20.5V. The MP8020 presents different currents in classification mode (see Table 1).

Table 1: Different Classification Power Rating and Setting with the MP8020

PD Class	Power Rating (W)	Class Cycle with Max Power	CLSA Signature	CLSB Signature	CLSA Resistor	CLSB Resistor
0	0.44 to 12.95	1	0	0	578	578
1	0.44 to 3.84	1	1	1	110	110
2	3.84 to 6.49	1	2	2	62	62
3	6.49 to 12.95	1	3	3	41.2	41.2
4	12.95 to 25.5	2, 3	4	4	28.7	28.7
5	25.5 to 40	4	4	0	28.7	578
6	40 to 51	4	4	1	28.7	110
7	51 to 62	5	4	2	28.7	62
8	62 to 71.3	5	4	3	28.7	41.2

IEEE802.3bt supports an 8-level class power rating, with up to 5 classification cycle operations. These classification cycles have the below functions:

- All PSEs perform one cycle classification for the class 0, class 1, class 2, and class 3 PDs.
- Type 2 PSEs perform 2-cycle classification if a class 4 signature is detected during the first class cycle.
- Type 3 and type 4 PSEs start their third cycle classification if a class 4 signature is detected during the first and second class-cycle. Based on the third cycle classification result, the Type 3 and Type 4 PSEs follow one of the operations listed below:
 - If the third classification result is a class 4 signature, classification stops and there is a class 4 PD.
 - If the third classification results in a class 0 or class 1 signature, the devices continue to the fourth cycle classification.

- If the third classification result is class 2 or class 3 signature, the type 4 PSE performs a fourth and fifth cycle classification.

The MP8020 performs a class signature signal with the CLSA pin during the first and second class cycles. The device performs a class signature signal with the CLSB pin in the remaining class cycles, unless V_{DD} drops to the mark event reset threshold.

Both CLSA and CLSB use the same output voltage (V_{OUT}) for classification. The maximum output current (I_{OUT}) is limited for self-protection.

Under-Voltage Lockout (UVLO) and the Power Supply Voltage

The MP8020 integrates one under-voltage lockout (UVLO) circuit with a large hysteresis. The UVLO block ensures that the MP8020 starts up when V_{DD} exceeds 40V and shuts down when V_{DD} drops below 30V.

The MP8020 also has an inrush current limit function during start-up. This current is about 1/7 of the steady state current limit, which is configured by the ILIM pin.

Hot-Swap MOSFET and Current Limit

The MP8020 integrates one 100V MOSFET for output disconnect.

When the PD voltage is powered by the PSE and V_{DD} exceeds the UVLO turn-on threshold, the hot-swap MOSFET starts passing a limited current (I_{INRUSH}) to charge the downstream DC/DC converter's input bulk capacitor. The inrush current limit function works until I_{INRUSH} drops below 75% of the inrush current limit, and then the current limit changes to the normal current limit threshold.

To meet different power ratings, the MP8020 supports current limit configuration via the ILIM pin. The ILIM pin sources a current after V_{DD} reaches the UVLO threshold. This current detects the configured current limit level. Table 2 shows the ILIM configurations.

Table 2: ILIM Configurations

ILIM to GND Resistance (kΩ)			Current Limit (A)
Min	Typ	Max	
0	0	1.4	0.9
5.76	7.15	9.09	1.6

The GATE1 pin can drive one external N-channel MOSFET, which is connected in parallel with the internal 0.35Ω MOSFET. GATE1 turns on the external MOSFET after a delay time (t_{DELAY} , 90ms) completes. If $V_{DD} - V_{SRC}$ exceeds 10V after t_{DELAY} , then over-current protection (OCP) is triggered and GATE1 does not turn on. If V_{SRC} is below V_{DD} by less than 10V, GATE1 turns on to charge the bulk capacitor. The MP8020 turns off the external MOSFET under light-load conditions.

The internal MOSFET and external MOSFET have different current limit control loops. The internal MOSFET current limit is configured by the ILIM pin, while the external MOSFET current limit is configured by a resistor (R_{SENSE}) between the VDD and SENSE pins. To reduce additional power loss and cost, the external MOSFET current limit can be disabled by removing R_{SENSE} (connecting the SENSE pin to the VDD pin). It is typically recommended for R_{SENSE} to be 18mΩ. When an external 18mΩ R_{SENSE} is used, it is recommended to connect the ILIM pin to GND for the lowest total current limit.

Figure 2 shows the internal and external MOSFET start-up sequence.

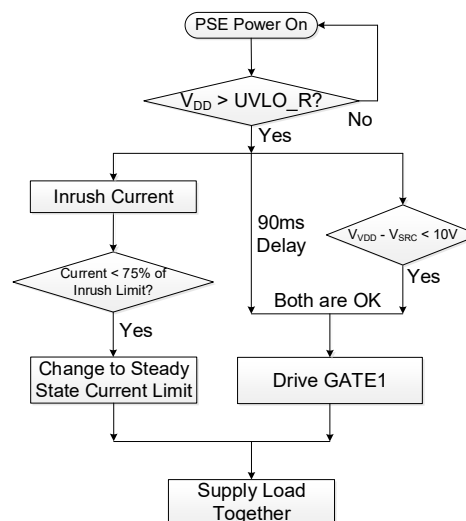


Figure 2: Internal MOSFET and External MOSFET Start-Up Sequence

The internal and external MOSFETs have fast-off current protection in the event of short-circuit protection (SCP) being triggered. If this occurs, GATE1 turns off, the internal MOSFET recovers if $V_{DD} - V_{SRC} < 10V$.

If an overload event occurs when both the internal MOSFET and external MOSFET are connected, the current limit function can work in one of several ways:

- If the internal MOSFET triggers a current limit first, then the internal current is limited and additional current goes through the external MOSFET. If the external MOSFET also triggers the current limit, then the external MOSFET pulls GATE1 low and V_{SRC} drops. If $V_{DD} - V_{SRC}$ exceeds 10V for 1ms, then the external MOSFET turns off and the internal MOSFET current limit switches to the inrush limit threshold. At the same time, PG pulls low to disable the downstream DC/DC converter, then begins a new start-up cycle with the inrush current limit. During this over-current (OC) condition, PG recovers without a 90ms delay after the inrush completes.
- If the external MOSFET triggers the current limit first, GATE1 pulls low, additional current goes through the internal MOSFET, and then triggers the internal current limit. After both current limits are triggered and

the device enters current foldback mode (reaches the inrush current limit), V_{SRC} drops. At the same time, PG is pulled low.

- If the internal MOSFET or external MOSFET triggers the fast-off current limit, the MP8020 quickly turns off the related MOSFET and then restarts with a delay.

Power Good (PG) and Delay

The MP8020 has one PG output to enable the downstream DC/DC converter after the inrush period finishes and the PSE is ready to provide high power. PG is an open-drain output with a voltage rating up to 100V.

PG goes to a high-impedance (Hi-Z) state when the device meets all of the following conditions:

- The device has changed to the steady current limit, which means that the inrush period is complete.
- The 90ms delay (t_{DELAY}) from UVLO has completed.
- A wall power adapter is detected on AUX, and V_{ADP} exceeds the UVLO threshold (see Figure 3).

The PG signal resets when the V_{DD} UVLO turn-off threshold (V_{DD_F}) is triggered, over-temperature protection (OTP) occurs, or if $V_{DD} - V_{SRC} > 10V$ for more than 1ms. The 90ms timer only works after V_{DD} UVLO is triggered.

PSE and Allocated Power Indicators

IEEE802.3bt supports 4 different PSE power supplies. The BT, TYP1, and TYP2 pins indicate the PSE-allocated power type. Table 3 on page 19 shows the detailed power level indicators. Note that the indicator only displays high when it is in logic high and pulled up to a high voltage via an external pull-up resistor.

The TYP1, TYP2, and BT signals are active after a t_{DELAY} of 90ms (same as the PG signal). The outputs become inactive (high-impedance) when V_{DD} falls below its UVLO threshold, or if OTP is triggered. The BT, TYP1, and TYP2 signals are latched in the MP8020 after start-up and do not reset until V_{DD} drops to the mark event reset threshold.

If an adapter is detected, the TYP1 and TYP2 pins go low and BT goes high.

Table 4 on page 19 shows some power demotion cases.

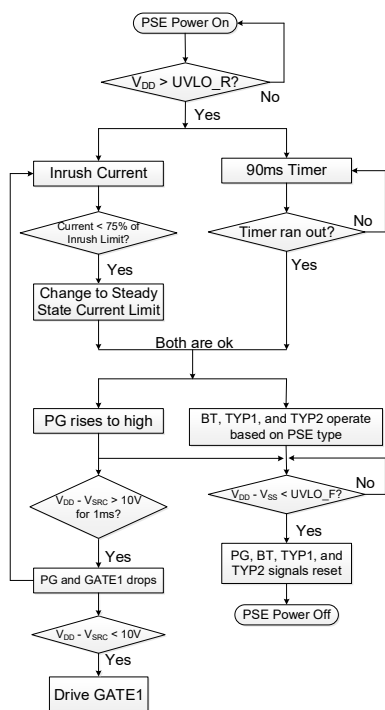


Figure 3: PG Logic

Table 3: PSE and Allocated Power Indicator

PSE Type	PD Class	PSE Allocated Power	Number of Class Cycles	BT	TYP1	TYP2
Type 1 Type 2	Class 0 Class 1 Class 2 Class 3	12.95W 3.84W 6.49W 12.95W	1	High	High	High
Type 2	Class 4	25.5W	2	High	High	Low
Type 3 Type 4	Class 0 Class 1 Class 2 Class 3	12.95W 3.84W 6.49W 12.95W	1	Low	High	High
	Class 4	25.5W	2, 3	Low	High	Low
	Class 5 Class 6	40W 51W	4	Low	Low	High
Type 4	Class 7 Class 8	62W 71.3W	5	Low	Low	Low

Table 4: Power Demotion Cases

PSE Type	PD Class	PSE Allocated Power	Number of Class Cycles	BT	TYP1	TYP2
Type 2	Class 4	12.95W	1	High	High	High
Type 3 Type 4	Classes 4~8	12.95W	1	Low	High	High
Type 3 Type 4	Classes 5~8	25.5W	2, 3	Low	High	Low
Type 3 Type 4	Classes 7~8	51W	4	Low	Low	High

Automatic Maintain Power Signature

To maintain the PSE power supply, the MP8020 supports automatic maintain power signature, and the current is configured by a resistor on the R_MPS pin.

The MP8020 also has one DUTY pin to configure the R_MPS pin's voltage duty cycle, which can compensate the effects of the long cable and bulk bus capacitors. After V_{DD} reaches the UVLO rising threshold, the DUTY pin sources one pulse current to detect the maintain power signature function duty cycle setting. Table 5 shows the DUTY pin's configuration options. Once V_{DD} falls to the VDD UVLO falling threshold, the DUTY signal resets.

Table 5: DUTY Configurations

DUTY to GND Resistance (k Ω)			R_MPS Duty Cycle (%)
Min	Typ	Max	
0	0	1.4	6
5.76	7.15	9.09	11.5
17.4	Float	Float	17

With type 1 and type 2 PSE inputs, the MP8020 generates a voltage on the R_MPS pin with a fixed 37% duty cycle.

Wall Adapter Power Supply

For applications where an auxiliary power source such as a wall adapter is used to power the device, the MP8020 features wall power adapter detection. Once the adapter voltage (V_{ADP}) exceeds about 8.3V, the MP8020 enables wall adapter detection.

The resistor divider connected from VADP to AUX detects the adapter status. Once the AUX voltage exceeds the internal reference voltage, the MP8020 switches the power source from the PSE to the adapter if the adapter has higher priority.

GATE2 drives the external N-channel MOSFET and provides a smooth switch between the PSE and auxiliary wall adapter with less power loss than a traditional diode input. After the adapter supply is enabled, the PG signal is high, the TYP1 and TYP2 pins output low, and the BT pin remains high.

When PRI is high, pull AUX high to disable the DET, CLS, and maintain power signature functions. When PRI is low, pulling AUX high cannot disable DET, CLS, and maintain power signature functions.

If an adapter is available, the PG signal is pulled high under all conditions. If the adapter has a higher priority and replaces the PSE power supply, then BT, TYP1, and TYP2 are updated once the AUX and ADP_UV signals are working. If the PSE has a higher priority and replaces the adapter supply, then the MP8020 changes the BT, TYP1, and TYP2 statuses to Hi-Z once PSE UVLO occurs. The statuses change to indicate the PSE power type after inrush is complete and the 90ms delay has finished.

Power Priority

The adapter is available when both AUX and V_{ADP} exceed the threshold. The MP8020 can source a current from the adapter or PSE if both the adapter and PSE are connected. This is determined by the PRI and AUX pin settings.

The PRI pin is internally pulled up to the internal VCC. If the PRI pin is floating (the adapter has higher priority) and $V_{ADP/AUX}$ exceed their thresholds, the MP8020 disables the PSE power supply, and enables the adapter power source. If AUX is below its falling threshold, then the PSE supplies power to the output even when PRI is floating.

If the PRI pin is connected to GND, the PSE has the higher priority. Regardless of the AUX

signal, the PSE outputs power unless V_{DD} is below UVLO.

If the PSE has a higher priority and the adapter is connected before PSE plug-in, a reverse blocking MOSFET must be added to reverse block the power from the adapter during PoE detection and classification (see Figure 4). At the same time, the output downstream DC/DC converter should lower the power rating so that the inrush current charges the MP8020's output capacitor (C_{OUT}) quickly. If C_{OUT} is not charged quickly, then the current limit is triggered and the device fails to start up.

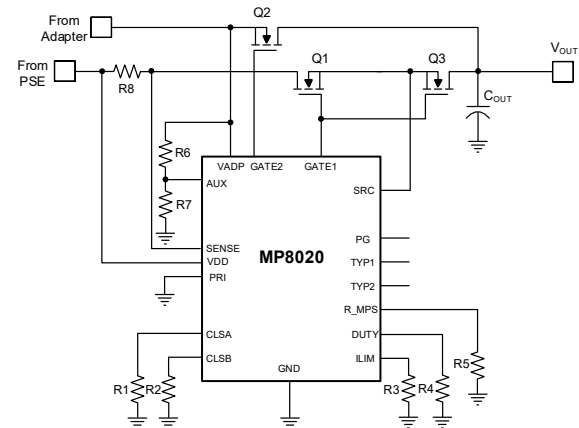


Figure 4: Reverse Block Solution

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds 150°C, the IC shuts down. Once the die temperature drops to 20°C, the device resumes normal operation.

APPLICATION INFORMATION

Selecting a TVS Diode

To limit the input transient voltage within the absolute maximum ratings, a TVS diode should be placed across the rectified voltage (between VDD and GND). For general indoor applications, it is recommended to use an SMAJ58A diode, or one with an equivalent protection voltage. Outdoor transient levels and special applications typically require additional protection.

Selecting an Input Capacitor

A 0.05μF to 0.12μF input bypass capacitor must be placed from VDD to GND for IEEE 802.3bt standard specifications. A 0.1μF, 100V ceramic capacitor is typically used.

Selecting the Classification Resistors (R_{CLSA} and R_{CLSB})

Connect a resistor from CLSA and CLSB to GND to configure the classification current according to the IEEE 802.3bt standard. The assigned class power should correspond to the maximum average power drawn by the PD during operation. To select R_{CLSA} and R_{CLSB} , see Table 1 on page 16.

Wall Power Adapter Detection Circuit

The MP8020 features wall power adapter detection. Once V_{DD} (between VADP and GND) exceeds about 8.3V, the MP8020 enables wall adapter detection. At this point, the resistor divider from the VADP to AUX pin can configure the threshold to switch from the PSE to an adapter.

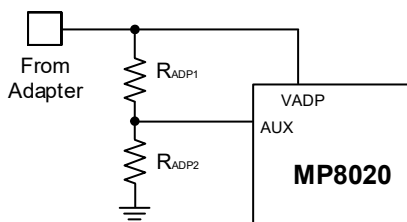


Figure 5: Wall Adapter Threshold Setting

PG Pin Setting

The PG pin is an active high, open-drain output that requires an external pull-up resistor. The PG pin's maximum sink current should be limited below 3mA. It is recommended to connect a 20kΩ to 100kΩ pull-up resistor from SRC to PG. Connect PG to the downstream

DC/DC converter's EN pin to enable the DC/DC converter.

PG goes to a high-impedance state if all of the following conditions are met:

- The steady current limit changes, which means the inrush period is complete.
- t_{DELAY} of 90ms from UVLO is complete.
- The wall power adapter is detected on AUX, and V_{ADP} exceeds the UVLO threshold.

BT, TYP1, and TYP2 Indicator Connection

The BT, TYP1, and TYP2 pins are open-drain outputs that indicate the PSE type or the presence of a wall adapter. Optocouplers can interface these pins to circuitry on the converter's secondary side. Figure 6 shows the optocoupler interface design for the BT, TYP1, and TYP2 signals.

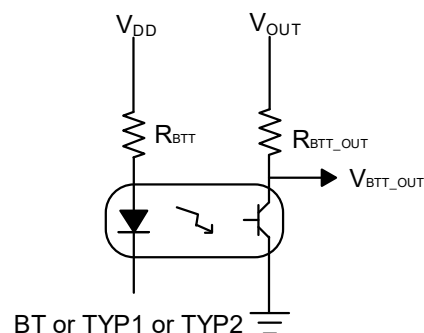


Figure 6: BT, TYP1, and TYP2 Interface

Where BT, TYP1, and TYP2 should have maximum sink currents of 3mA, and R_{BTT} should exceed 20kΩ to match the maximum 57V input.

When lighting an LED from VDD to BT/TYP1/TYP2 to indicate the PSE type, the resistance can be higher to match the LED's maximum current and reduce power loss.

Configurable Current Limit

After V_{DD} exceeds the UVLO threshold, the ILIM pin sources a current that detects the configurable current limit. By connecting ILIM to GND via a resistor (or shorting ILIM to GND), the MP8020's current limit can be configured to 1.6A or 0.9A (see Table 2 on page 17).

The MP8020 also has an inrush current limit function after start-up, which is about 1/7 of the steady state current limit.

Selecting the PoE Power MOSFET

The MP8020 internal hot-swap MOSFET has a maximum 1.6A current limit. For type 1, 2, and 3 PDs ($\leq 51\text{W}$), the internal hot-swap MOSFET is sufficient. For type 4 PDs ($> 51\text{W}$), an external MOSFET must be placed in parallel with the internal hot-swap MOSFET. The GATE1 pin can drive one external N-channel MOSFET. The MOSFET should be selected to meet the following specifications:

- The voltage rating should be at least 100V for high-voltage surge environments.
- The on resistance ($R_{DS(ON)}$) should be below 200m Ω for power dissipation and for light-load shutdown functions. A 100m Ω $R_{DS(ON)}$ is typically recommended.
- The gate charge (Q_G) should be as small as possible to provide faster response times under overload conditions. It is typically recommended for Q_G to be below 15nC ($V_{GATE} = 4.5\text{V}$).
- The gate threshold voltage should be below 4V to fully drive the GATE1 and GATE2 voltages.

SENSE Pin Setting

The external parallel MOSFET current limit is configured by a resistor (R_{SENSE}) between the VDD and SENSE pins. It is typically recommended for R_{SENSE} to be 18m Ω . The total current limit (I_{IN_LIM}) can be calculated using Equation (1):

$$I_{IN_LIM} = I_{INNER} + \frac{26\text{mV}}{R_{SENSE}} \quad (1)$$

Where I_{IN_LIM} is the PD current limit, and I_{INNER} is the MP8020 internal hot-swap MOSFET current limit.

When the external MOSFET is connected, it is recommended to set I_{INNER} to 0.9A.

Selecting the Adapter MOSFET

The GATE2 pin is designed to drive one external N-channel MOSFET for the adapter supply. Select the adapter MOSFET using the same guidelines as the PoE power MOSFET.

Design Example

Table 6 shows a design example following the application guidelines for the specifications below.

Table 6: Design Example

V _{DD}	Class Level	V _{ADP}
54V	Class 8	24V

For the detailed application schematic, see Figure 8 on page 24. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 12. For more device applications, refer to the related evaluation board datasheet.

PCB Layout Guidelines

Efficient PCB layout is critical. Poor layout may result in reduced performance, resistive loss, and system instability. To ensure an optimal layout design, refer to Figure 7 and follow the guidelines below:

1. Ensure that all power connections are as short as possible with wide traces.
2. Place the current-sense resistor (R8) as close to the VDD pin as possible.
3. Use a Kelvin connection between the SENSE pin and R8 for an accurate current limit.
4. Place the PoE input capacitor as close to the VDD pin as possible.
5. Place the adapter's input capacitor as close to the VADP pin as possible.
6. Place the SRC capacitor as close to the SRC pin as possible.

7. Place a wide copper plane and vias under the MP8020, PoE power MOSFET, and adapter MOSFET to improve thermal performance.

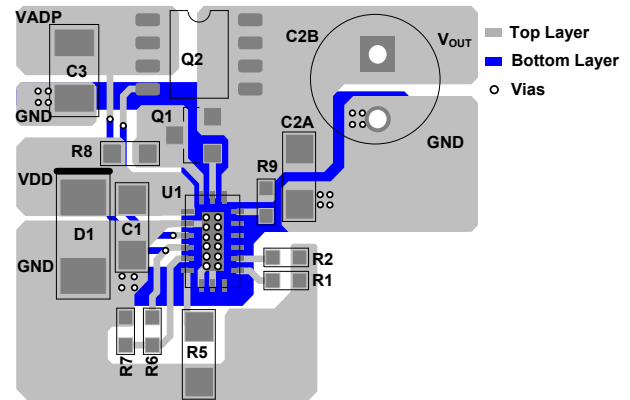


Figure 7: Recommended PCB Layout ⁽⁸⁾

Note:

- 8) Figure 7 is based on the Typical Application Circuit (see Figure 8 on page 24).

TYPICAL APPLICATION CIRCUIT

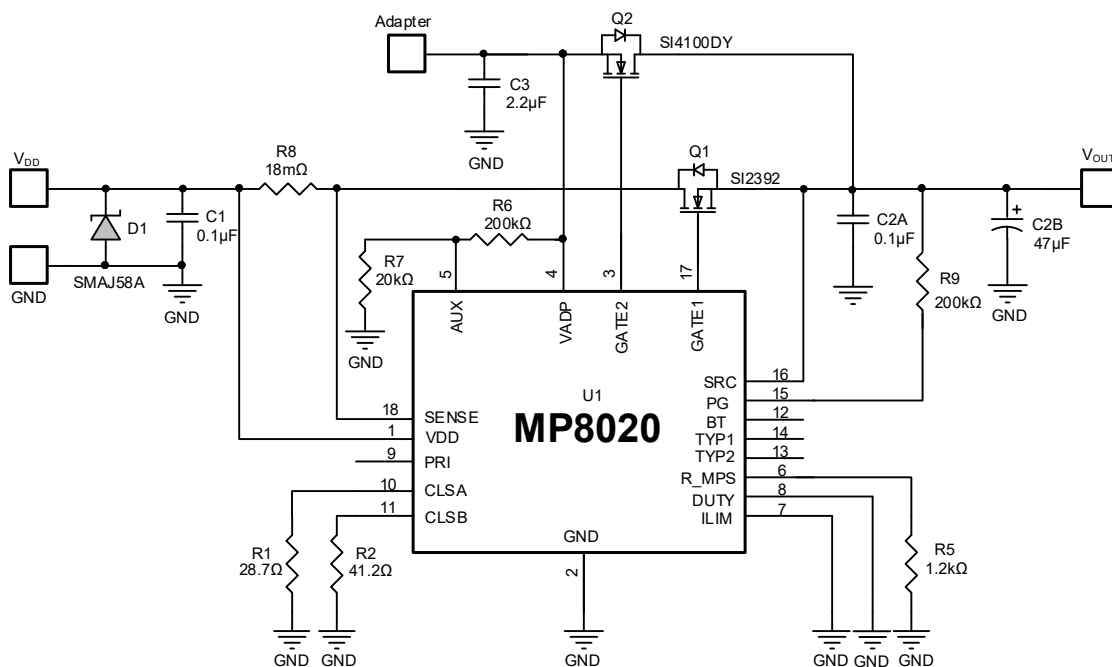
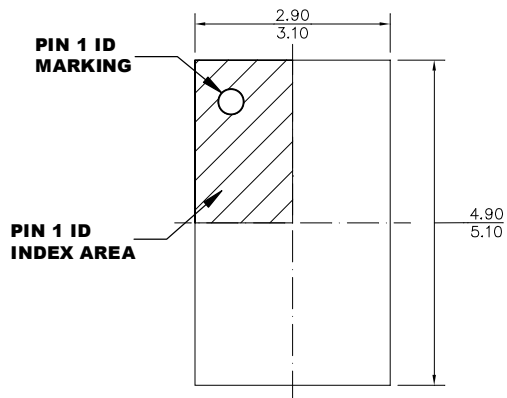


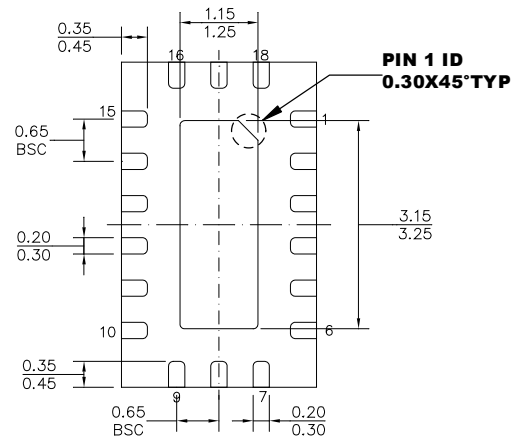
Figure 8: Class-8 PD Solution with PSE and Adapter Supplies

PACKAGE INFORMATION

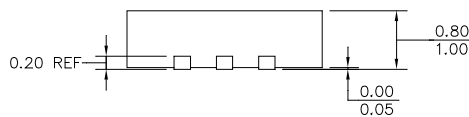
QFN-18 (3mmx5mm)



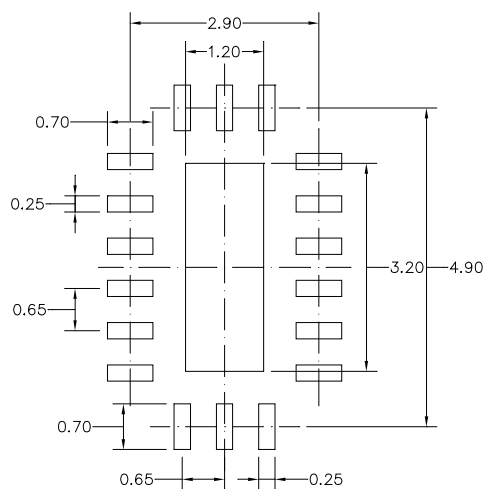
TOP VIEW



BOTTOM VIEW



SIDE VIEW

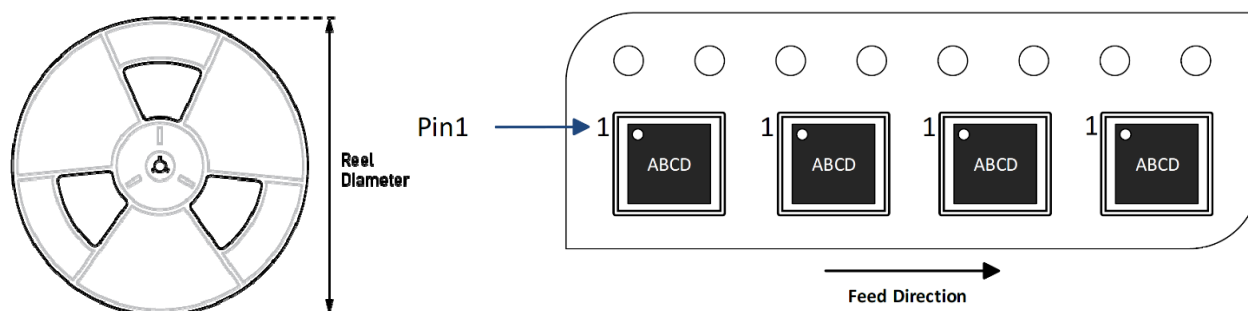


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8020GQV-Z	QFN-18 (3mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/17/2022	Initial Release	-

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