MP5031

USB PD Port Controller with Five Configurable PDOs and Load-Shedding

DESCRIPTION

The MP5031 is a USB power delivery (PD) controller that is compatible with USB Type-C 2.0 and USB PD 3.0 specifications. The MP5031 is designed for downward-facing port (DFP) applications, such as USB PD charging ports.

The MP5031's backward compatibility supports dedicated charging port (DCP) schemes for Quick Charge 3.0 (QC3.0), Huawei Fast Charge Protocol (FCP), BC1.2, Apple divider 3 mode, and 1.2V/1.2V mode without outside user interaction. It also supports BC1.2 charging data port (CDP) handshaking. The I^2C interface and GPIO pins provide communication with an external power converter.

The MP5031 supports up to 100W of PD power. It can also support a programmable power supply (PPS). The power data object (PDO) list and charging protocols can be flexibly configured via the I^2C. The I^2C also selects the slave devices and protection mode.

The two NTC pins monitor abnormal temperature rises, such as a temperature rise on the Type-C receptacle or the PCB board. The power-sharing function supports smart power budget management between two USB PD ports. If a car battery voltage is low, then the PDO capacity is reduced. The high-voltage I/O pins support short-circuit protection (SCP) for the DC/DC converter (i.e. battery short protection and V_{BUS} short protection).

The MP5031 is available in a QFN-20 (4mmx4mm) package with wettable flanks.

FEATURES

- 4.6V to 5.5V VCC Supply Voltage Range
- 3.3V to 21V Bus Voltage (V_{BUS}) Range
- Integrated Physical Layer for Biphase Mark Code (BMC)
- Integrated Protocol Layer
- Integrated Policy Engine
- Supports One Type-C Downward-Facing Port (DFP) with USB PD 3.0 and a Programmable Power Supply (PPS)
- Supports Dedicated Charging Port (DCP) Schemes for BC1.2, Apple Divider 3 Mode, and 1.2V/1.2V Mode
- Supports Quick Charge 3.0 (QC3.0) and Huawei Fast Charge Protocol (FCP)
- Low 100µA Standby Quiescent Current (I_Q)
- V_{BUS} Isolation N-Channel MOSFET Driver
- EN Off Timer Up to 120 Minutes
- I^2C Master/Slave Interface and Interrupt Function
- Load-Shedding with Thermal Sense and Low Battery Detection
- High-Voltage Pins: CC1, CC2, DP, and DM
- Integrated High-Voltage V_{CONN} Power MOSFET
- 60W/100W USB-IF PPS Certified
- Available in a QFN-20 (4mmx4mm) Package with Wettable Flanks

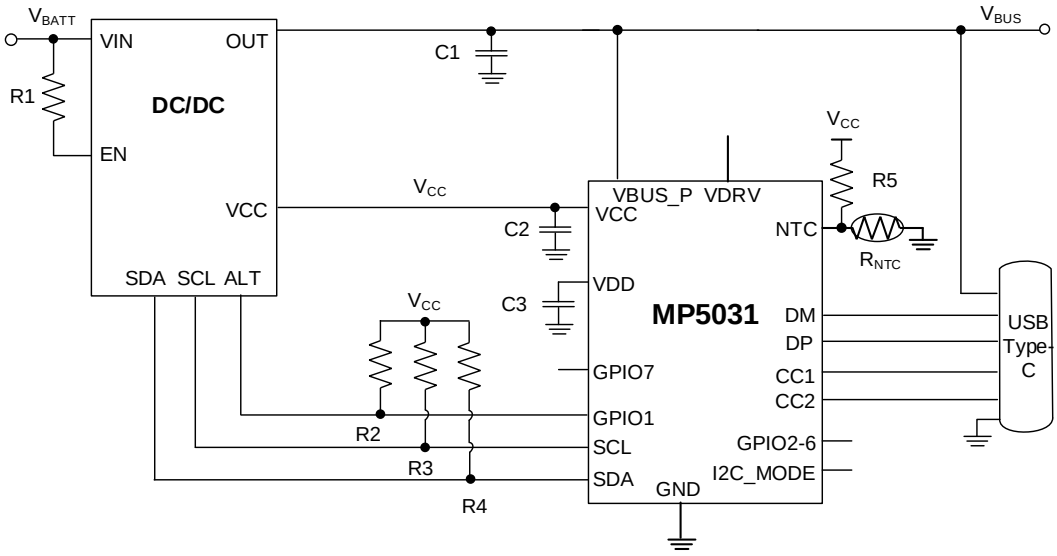
APPLICATIONS

- USB Power Delivery (PD) Charging Ports
- Car Chargers
- Multi-Port Wall Chargers

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MP5031GRE-00A3	QFN-20 (4mmx4mm)	See Below	1
MP5031GRE-xxxx**			
EVKT-MP5031	-	-	-

* For Tape & Reel, add suffix -Z (e.g. MP5031GRE-xxxx-Z).

** “xxxx” is the configuration code identifier for the register setting stored in the OTP. Each “x” can be a hexadecimal value between 0 and F.

TOP MARKING

MPSYWW
MP5031
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP5031: Part number
LLLLLL: Lot number
E: Wettable lead flank

EVKT-MP5031 EVALUATION KIT

EVKT-MP5031 kit contents (items listed below can be ordered separately):

#	Part Number	Item	Quantity
1	EVL5031-4247-RE-00A	MP5031 + MP4247 evaluation board	1
2	EVKT-USBI2C-02 bag	Includes USB to I²C communication interface, one USB cable, and one ribbon cable	1
3	MP5031GRE-00A3	IC with default configuration	2
4	MP4247GQV-0002	IC with default configuration	2

Order directly from MonolithicPower.com or our distributors.

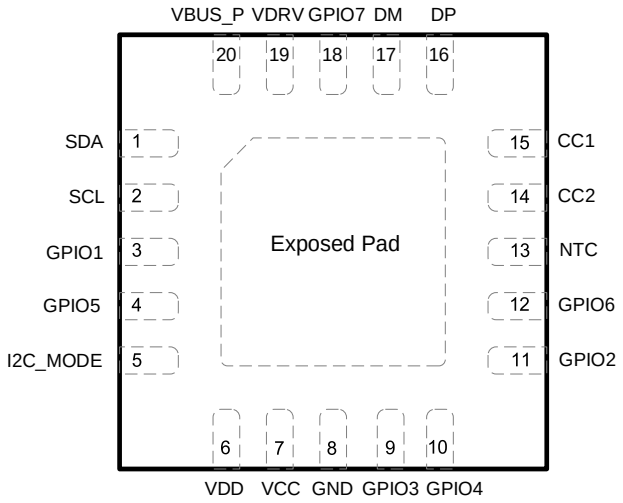


Figure 1: EVKT-MP5031 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE REFERENCE

TOP VIEW



QFN-20 (4mmx4mm)
with Exposed Pad and Wettable Flank

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	SDA	I/O	**I²C data line.**
2	SCL	I/O	**I²C clock signal input.** If the MP5031 is selected as the I²C master, then the SCL pin is an output pin.
3	GPIO1	I/O	**General-purpose I/O 1.** The GPIO1 pin is a low-voltage pin that supports 5.5V operation. For more information on GPIO1's configurable functions, see the CTL3 register description on page 34.
4	GPIO5	I/O	**General-purpose I/O 5.** The GPIO5 pin can be configured via the I²C. For more information on GPIO5's configurable functions, see the CTL4 register description on page 35.
5	I2C_ MODE	Input	**I²C operation mode setting.** Float or pull the I2C_MODE pin low to set the MP5031 as the master. Pull I2C_MODE high to set the MP5031 as the slave. If the MP5031 is in slave mode, then the GPIO5 and GPIO6 slave functions are disabled. The SDA and SCL pins are the I²C slave entrance. I2C_MODE has a 1MΩ internal pull-down resistor.
6	VDD	Output	**1.8V internal LDO output.** Decouple the VDD pin with a 0.47µF capacitor.
7	VCC	Input	**5V power supply for the internal circuitry.** The MP5031 operates from a 4.5V to 5.5V input voltage (V_{IN}). A 4.7µF ceramic capacitor (C_{IN}) is required to supply power to the internal circuitry (including V_{CONN}).
8	GND	N/A	**Ground.**
9	GPIO3	I/O	**General-purpose I/O 3.** The GPIO3 pin is a low-voltage pin that supports 5.5V operation and has an internal ESD Zener diode. GPIO3 can be configured via the I²C. For more information on GPIO3's configurable functions, see the CTL3 register description on page 33.
10	GPIO4	I/O	**General-purpose I/O 4.** The GPIO4 pin can be configured via the I²C. For more information on GPIO4's configurable functions, see the CTL3 register description on page 33.
11	GPIO2	I/O	**General-purpose I/O 2.** The GPIO2 pin is a low-voltage pin that can be configured via the I²C. For more information on GPIO2's configurable functions, see the CTL3 register description on page 33.
12	GPIO6	I/O	**General-purpose I/O 6.** The GPIO6 pin can be configured via the I²C. For more information on GPIO6's configurable functions, see the CTL4 register description on page 35.
13	NTC	Input	**External temperature-sense pin.** The NTC pin sets the negative temperature coefficient (NTC) behavior. For more information on the NTC settings, see the CTL4 register description on page 34.
14	CC2	I/O	**Configuration channel.** The CC2 pin detects, configures, and manages the connections across a USB Type-C cable.
15	CC1	I/O	**Configuration channel.** The CC1 pin detects, configures, and manages the connections across a USB Type-C cable.
16	DP	I/O	**D+ data line to USB connector.** The DP pin is an input and output used for handshaking with portable devices.
17	DM	I/O	**D- data line to USB connector.** The DM pin is an input and output used for handshaking with portable devices.
18	GPIO7	I/O	**General purpose I/O 7.** The GPIO7 pin is a low-voltage pin that can be configured via the I²C. For more information on GPIO7's configurable functions, see the CTL4 register description on page 34.
19	VDRV	Output	**External N-channel MOSFET gate driver signal.** If the sink is attached, then the VDRV pin turns the external N-channel MOSFET on, and power flows from the DC/DC output to the sink. If the sink is detached, VDRV turns the external N-channel MOSFET off to isolate the power path.
20	VBUS_P	Input	**Bus voltage (V_{BUS}) sensing and discharge pin.**
Exposed pad	N/A	N/A	**Exposed pad.** Connect the exposed pad to GND.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

VBUS_P .....-0.3V (-5V for <10ns) to +24V
VDRV .....VBUS_P + 5V
VDD..... -0.3V to +3V
DM, DP, CC1, CC2.....
……-0.3V (-5V for <10ns) to +24V
GPIO4, GPIO6, NTC ..... -0.3V to +5.5V
All other pins..... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-20 (4mmx4mm).....2.1W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (3)

Power supply to VCC..... 5V/25mA
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (4mmx4mm) ..... 60 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Standby supply current	I_{STB}	VCC current, not attached		100		µA
On supply current	I_{ON}	CC1 to GND with 5.1kΩ R_D (as defined by the USB Type-C Cable and Connector Specification, Revision 2.0, which can be downloaded from the official USB website)		3.5	4.5	mA
Thermal shutdown (5)	T_{SD}			150		°C
Thermal hysteresis (5)	T_{SD_HYS}			20		°C
VDD regulator	V_{DD}		1.7	1.8	1.9	V
VDD load regulation	V_{DD_REG}	I_{DD} = 5mA		3		%
VCC under-voltage lockout (UVLO) rising threshold	$V_{CC_UVLO_RISING}$		4	4.3	4.6	V
VCC UVLO threshold hysteresis	$V_{CC_UVLO_HYS}$			350		mV
VBUS_P UVLO falling threshold	V_{BUS_UVLO}	VBUS_UV_THD = 0b	2.79	2.97	3.15	V
GPIO7						
Discharge output high	V_{DIS_HIGH}	Discharge turns on, 50kΩ load		4.4		V
Discharge output low	V_{DIS_LOW}			3.3		kΩ
Adjustable sink current	I_{ADJ}	GPIO3_ISENS+ = 1.5V	1	2	3	µA
EN_OUT_MID voltage	$V_{EN_OUT_MID}$	100kΩ, pull-up resistor to 12V	0.8	1	1.2	V
EN_OUT_HIGH voltage	$V_{EN_OUT_HIGH}$	Open drain, 100kΩ, pull-up resistor to VCC	4.5			V
EN_OUT_LOW voltage	$V_{EN_OUT_LOW}$				0.4	V
GPIO5 and GPIO6						
VBUS_UV_FIXPDO falling threshold	$V_{BUS_UV_FIXPDO}$	V_{BUS} = 5V	0.91	0.96	1.01	V
PWM current (I_{PWM}) duty cycle	I_{PWM_DUTY}	4.7kΩ, pull-up resistor to VCC, 3A power data object (PDO)		50		%
SYNC_OUT1 frequency	f_{SYNC_OUT1}	4.7kΩ, pull-up resistor to VCC		450		kHz
SYNC_OUT2 frequency	f_{SYNC_OUT2}	4.7kΩ, pull-up resistor to VCC		450		kHz
I^2C_SLV_SDA/SCL frequency	$f_{I2C_SLV_SDA/SCL}$	4.7kΩ, pull-up resistor to VCC		400		kHz
VSEL2 output low	V_{SEL2_LOW}	100kΩ to VCC			0.4	V
GPIO4, GPIO3						
EN UVLO rising threshold	$V_{EN_UVLO_RISING}$		1.33	1.43	1.53	V
EN UVLO falling hysteresis voltage	$V_{EN_UVLO_FALLING}$			220		mV
EN off timer delay	$t_{EN_OFF_DELAY}$	EN_OFF_TIMER = 010b		22		min
V_{BATT} low falling threshold	$V_{BATT_LOW_FALLING}$	GPIO4 = 11b	1.07	1.12	1.17	V
V_{BATT} low rising threshold	$V_{BATT_LOW_RISING}$	GPIO4 = 11b	1.12	1.18	1.24	V
ATTACH output high	$V_{ATTACH_OUT_HIGH}$		4.5			V
ATTACH output low	$V_{ATTACH_OUT_LOW}$	Sink is attached			0.4	V
I_{PWM} duty cycle	I_{PWM_DUTY}	4.7kΩ, pull-up resistor to VCC, 3A PDO				
Plug orientation (POL) output low	V_{POL_LOW}	CC1 = 5.1kΩ			0.4	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
POL output high	$V_{POL_OUT_HIGH}$	CC2 = 5.1kΩ, 10kΩ, pull-up resistor to VCC	4.5			V
GPIO2						
Power share input low	V_{PS_LOW}	10kΩ pull-up resistor to VCC			0.4	V
Power share input high	V_{PS_HIGH}	10kΩ pull-up resistor to VCC	3			V
POL output low	$V_{POL_OUT_LOW}$	CC1 = 5.1kΩ			0.4	V
POL output high	$V_{POL_OUT_HIGH}$	CC2 = 5.1kΩ, 10kΩ, pull-up resistor to VCC	4.5			V
QC_12 pull-down resistance	R_{QC_12}	DP/DM enter QC 12V		8		Ω
I2C_MODE						
Logic high threshold	V_{I2C_HIGH}	Slave mode	1	1.2	1.4	V
Logic high hysteresis	$V_{I2C_HIGH_HYS}$			100		mV
Resistance	R_{I2C_MODE}			1		MΩ
GPIO1						
VSEL1 pull-down resistance	R_{VSEL1}	12V PDO is selected		100		kΩ
VSEL1 output high	$V_{SEL1_OUT_HIGH}$	100kΩ to VCC	4.5			V
INT logic high	V_{INT_HIGH}		4.5			V
INT logic low	V_{INT_LOW}				0.4	V
INT leakage	I_{INT_LKG}				1	µA
PDO_SEL_OUTPUT (SLAVE_DEVICE_SEL = 101b)						
PDO2_SEL_OUT to PDO3_SEL_OUT pull-down resistance	R_{PDO2_LOW}			7		Ω
PDO2_SEL_OUT to PDO4_SEL_OUT leakage	V_{PDO_HIGH}	5V PDO is selected			1	µA
NTC and NTC2						
External thermal-sense rising threshold	V_{NTC_RISING}	R_P = 47kΩ, R_{NTC} = 4.72kΩ (100°C)	7.5	9.1	10.5	%V_{CC}
External thermal-sense falling threshold	$V_{NTC_FALLING}$	R_P = 47kΩ, R_{NTC} = 9.45kΩ (80°C)		16.7		%V_{CC}
Gate Driver (VDRV)						
Gate driver voltage	V_{DRV}	V_{DRV} - V_{BUS}		4.85		V
Gate driver voltage at 15µA	V_{DRV_1}	I_{SOURCE} = 15µA		4.4		V
Pull-down resistor	R_{PULL_DOWN}			5		kΩ
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_SHORT}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = 25°C		25	40	Ω
Apple Divider 3 Mode						
DP output voltage	$V_{DIVIDER_DP}$	V_{OUT} = 5V	2.55	2.75	2.95	V
DM output voltage	$V_{DIVIDER_DM}$	V_{OUT} = 5V	3.35	3.6	3.85	V
DP output resistance	$R_{DIVIDER_DP}$			22		kΩ
DM output resistance	$R_{DIVIDER_DM}$			22		kΩ
1.2V/1.2V Mode						
DP and DM output voltage	$V_{DP/DM_1.2V}$	V_{OUT} = 5V	1.05	1.20	1.35	V
DP and DM output resistance	$R_{DP/DM_1.2V}$			300		kΩ

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Quick Charge 3.0 (QC3.0) Mode						
DP and DM low voltage	V_{QC_LOW}		0.2	0.3	0.4	V
DP and DM high voltage	V_{QC_HIGH}		1.8	2	2.2	V
DP output resistance	R_{DP_QC}			350	1500	kΩ
DM output resistance	R_{DM_QC}			20		kΩ
DM deglitch low time (5)	$t_{DEGLITCH_DM_LOW}$			10		ms
DP deglitch high time	$t_{DEGLITCH_DP_HIGH}$		1000		1500	ms
Output voltage changed deglitch time (5)	$t_{VOUT_DEGLITCH_CHANGE}$		20	40	60	ms
Bus voltage step (5)	$V_{BUS_CONT_STEP}$		150	200	250	mV
V_{BUS} discharge time to 5V when DP < 0.6V (5)	t_{V_UNPLUG}				500	ms
Fast Charge Protocol (FCP) Mode						
DM T_X high voltage	$V_{FCP_TX_HIGH}$	R_{LOAD} = 15kΩ	2.55		5	V
DM T_X low voltage	$V_{FCP_TX_LOW}$	R_{LOAD} = 15kΩ			0.4	V
DM R_X high voltage	$V_{FCP_RX_HIGH}$		1.5		5	V
DM R_X low voltage	$V_{FCP_RX_LOW}$				1	V
DM pull-low resistance (5)	R_{PD_DM}			15		kΩ
PHY unit interval (5)	t_{UI_PHY}	f_{CLK} = 125kHz	144	160	176	µs
Charging Data Port (CDP) Mode (CDP_EN = 1)						
DM CDP output voltage	V_{DM_SRC}	V_{DP} = 0.6V, DM_SINK = 250µA	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC}	V_{DAT_REF}		0.25	0.35	0.45	V
DP rising lower window threshold hysteresis	$V_{DAT_REF_HYS}$			50		mV
DP rising upper window threshold for V_{DM_SRC}	V_{LGC_SRC}		0.8	0.95	1.1	V
DP rising upper window threshold hysteresis	$V_{LGC_SRC_HYS}$			80		mV
USB Type-C (CC1 and CC2 pins)						
CC pull-up current 1	I_{RP1}	V_{BUS} = 5V/3A, T_J = 25°C	304	330	356	µA
CC pull-up current 2	I_{RP2}	V_{BUS} = 5V/1.5A, T_J = 25°C	162	180	198	µA
CC voltage to enable V_{CONN} for 3A Type-C mode	V_{RA1}	T_J = 25°C			0.75	V
CC voltage to enable VBUS_P for 3A Type-C mode	V_{RD1}	T_J = 25°C	0.85		2.45	V
CC detach threshold for 3A Type-C mode	V_{OPEN1}	T_J = 25°C	2.75			V
CC voltage falling debounce timer	$t_{CC_DEBOUNCE}$	V_{BUS} deglitch enabled	100	150	200	ms
CC voltage rising debounce timer	$t_{PD_DEBOUNCE}$	V_{BUS} deglitch disabled	5	10	15	ms
V_{CONN} output power	P_{V_CONN}	VCC supplies V_{CONN}	0.1			W
USB PD						
Unit interval	t_{UI}	T_J = 25°C	3	3.35	3.7	µs
Transmitter						
Biphase mark code (BMC) end drive (5)	t_{ED_BMC}				23	µs
Fall time (5)	t_{FALL}		300			ns
Rise time (5)	t_{RISE}		300			ns
BMC hold low (5)	t_{HLBMC}		1			µs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 5V, T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic voltage high	V_{LOGIC_HIGH}		1	1.15	1.3	V
Logic voltage low	V_{LOGIC_LOW}				100	mV
Output resistance	R_{TX}			50		Ω
Receiver (5)						
CC receiver capacitance	$C_{RECEIVER}$				600	pF
Signal detection transitions	$N_{TRANSITION}$		3			edges
R_X bandwidth limiting filter	t_{RX_FILTER}		100			ns
Time window for detecting non-idle mode	$t_{TRANSITION_WINDOW}$		12		20	µs
Receiver input resistance	R_{BMC_RX}		1			MΩ
I^2C Interface Specifications (5)						
Input logic high	$V_{N_LOGIC_HIGH}$		1.4			V
Input logic low	$V_{IN_LOGIC_LOW}$				0.6	V
Output logic low	$V_{OUT_LOGIC_LOW}$				0.4	V
SCL clock frequency	f_{SCL}			400		kHz
SCL time high	t_{HIGH}		60			ns
SCL time low	t_{LOW}		160			ns
Data set-up time	t_{SU_DAT}		10			ns
Data hold time	t_{HD_DAT}			70		ns
Repeated start set-up time	t_{SU_START}		160			ns
Repeated start hold time	t_{HOLD_START}		160			ns
Bus free time between a start and a stop condition	t_{BUS_FREE}		160			ns
Stop condition set-up time	$t_{SU.STO}$		160			ns
SCL and SDA rise time	t_{RISE}		10		300	ns
SCL and SDA fall time	t_{FALL}		10		300	ns
Suppressed spike pulse width	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Note:

5) Guaranteed by characterization.

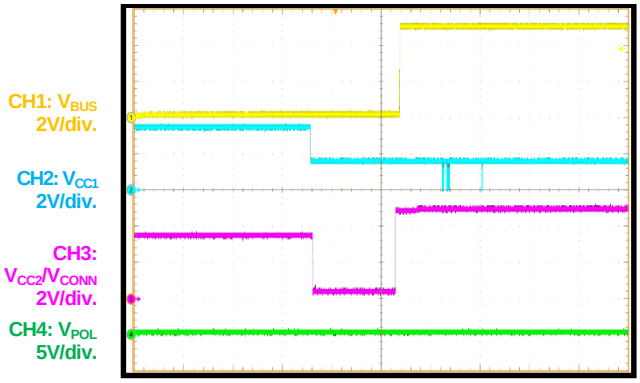
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MP5031's VBUS_P pin to the MP4245's output.

CC1 Attached R_D to Enable VBUS_P

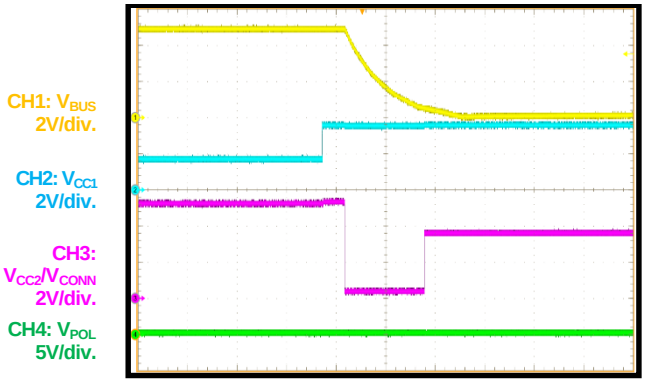
I_{OUT} = 0A



100ms/div.

CC1 Detached R_D to Disable VBUS_P

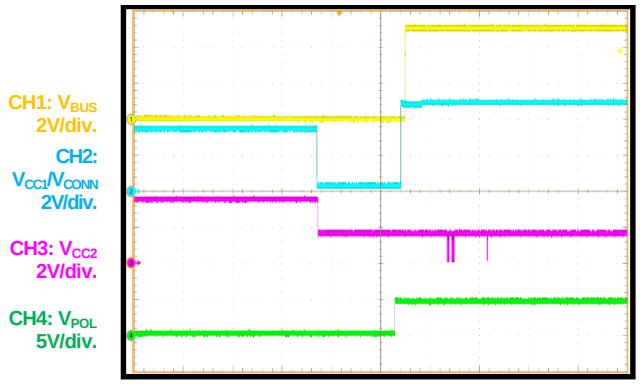
I_{OUT} = 0A



20ms/div.

CC2 Attached R_D to Enable VBUS_P

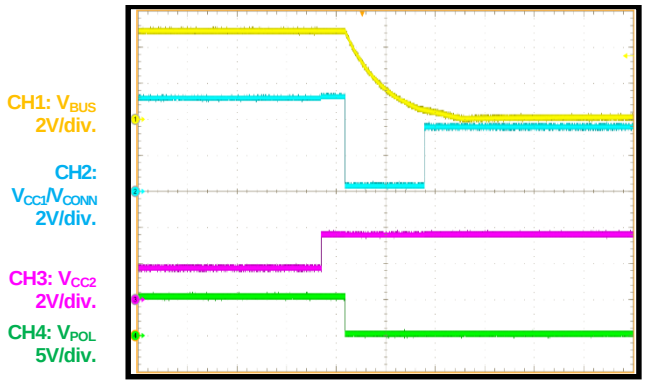
I_{OUT} = 0A



100ms/div.

CC2 Detached R_D to Disable VBUS_P

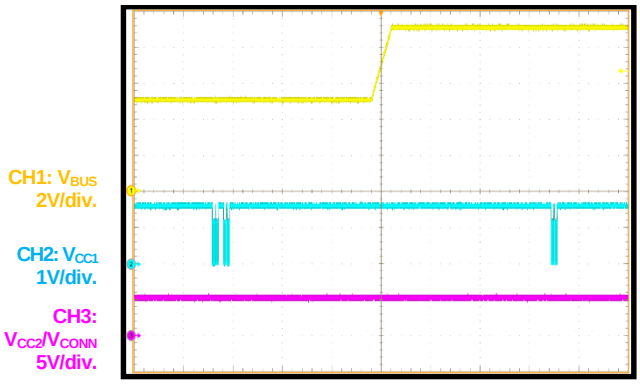
I_{OUT} = 0A



20ms/div.

PDO Transition

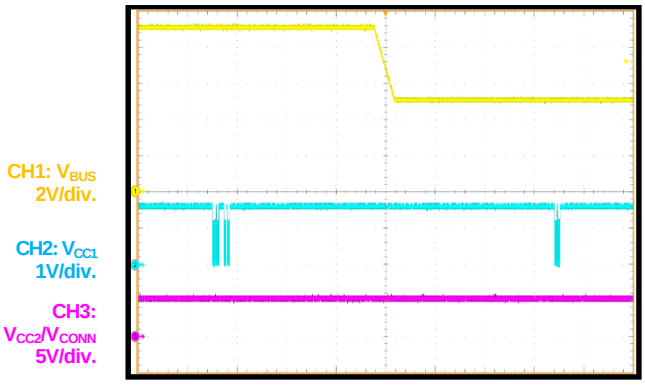
5V PDO to 9V PDO



10ms/div.

PDO Transition

9V PDO to 5V PDO



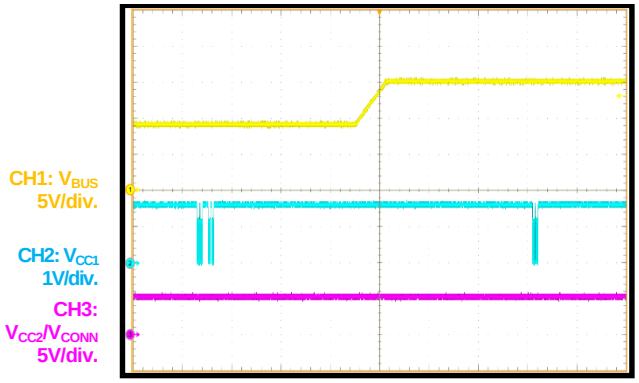
10ms/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

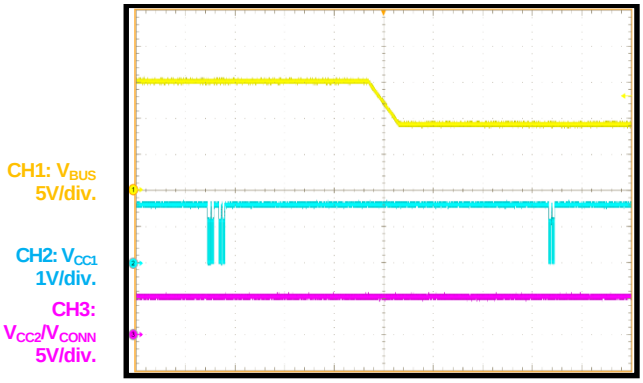
V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MP5031's VBUS_P pin to the MP4245's output.

PDO Transition
9V PDO to 15V PDO



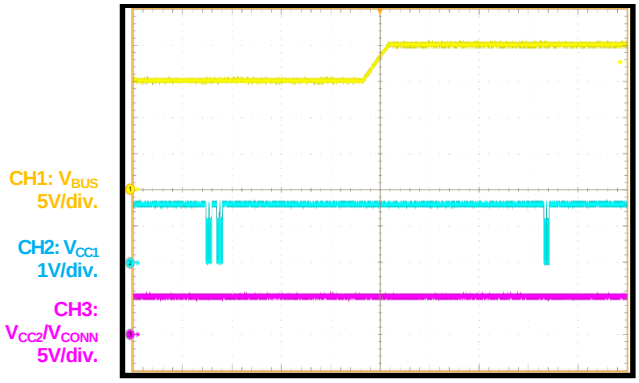
10ms/div.

PDO Transition
15V PDO to 9V PDO



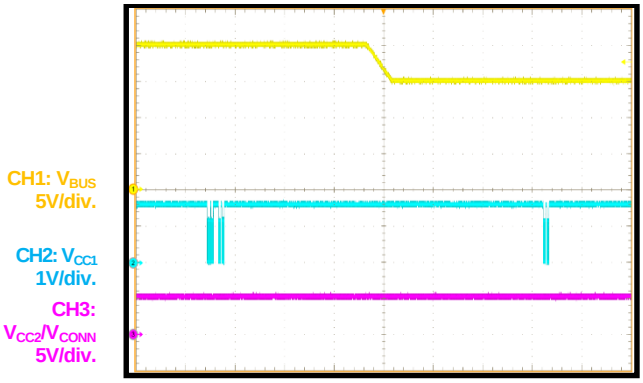
10ms/div.

PDO Transition
15V PDO to 20V PDO



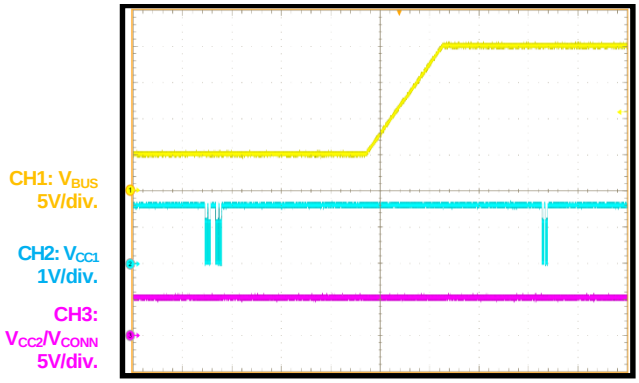
10ms/div.

PDO Transition
20V PDO to 15V PDO



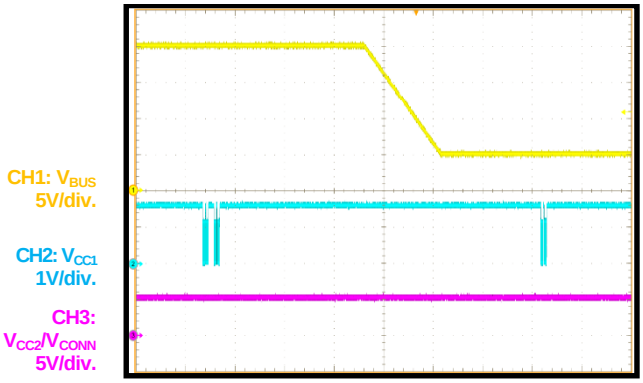
10ms/div.

PDO Transition
5V PDO to 20V PDO



10ms/div.

PDO Transition
20V PDO to 5V PDO



10ms/div.

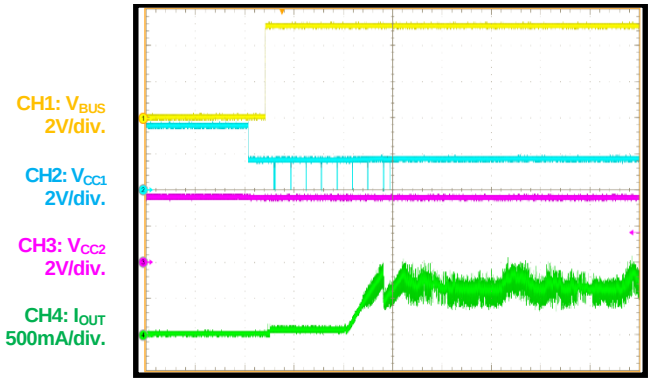
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{CC} = 5V, V_{BUS} = 5V to 20V, T_A = 25°C, unless otherwise noted. Connect the MP5031's VBUS_P pin to the MP4245's output.

Mobile Phone Charging Test

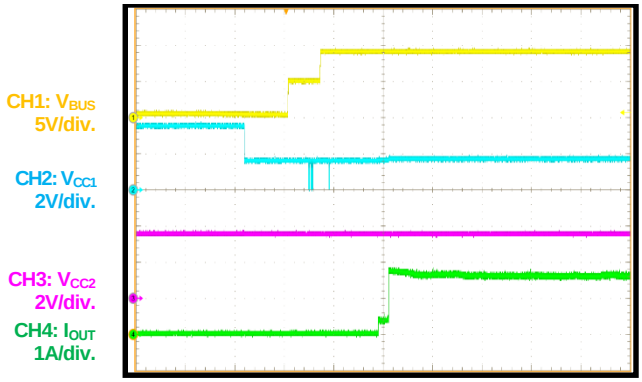
Phone requests 5V PDO



500ms/div.

Mobile Phone Charging Test

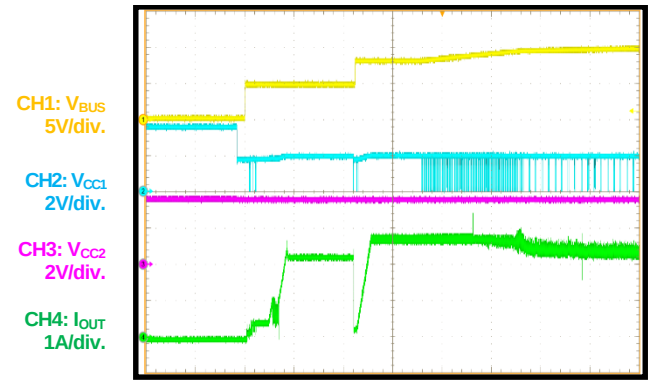
Phone requests 9V PDO



200ms/div.

Mobile Phone Charging Test

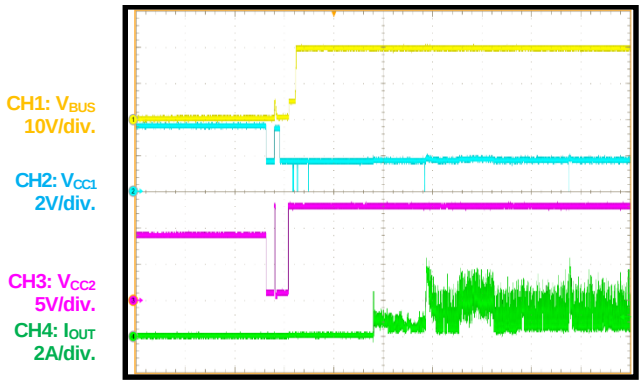
Phone requests 3.3V to 21V APDO



1s/div.

Laptop Charging Test

Laptop requests 20V PDO



1s/div.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

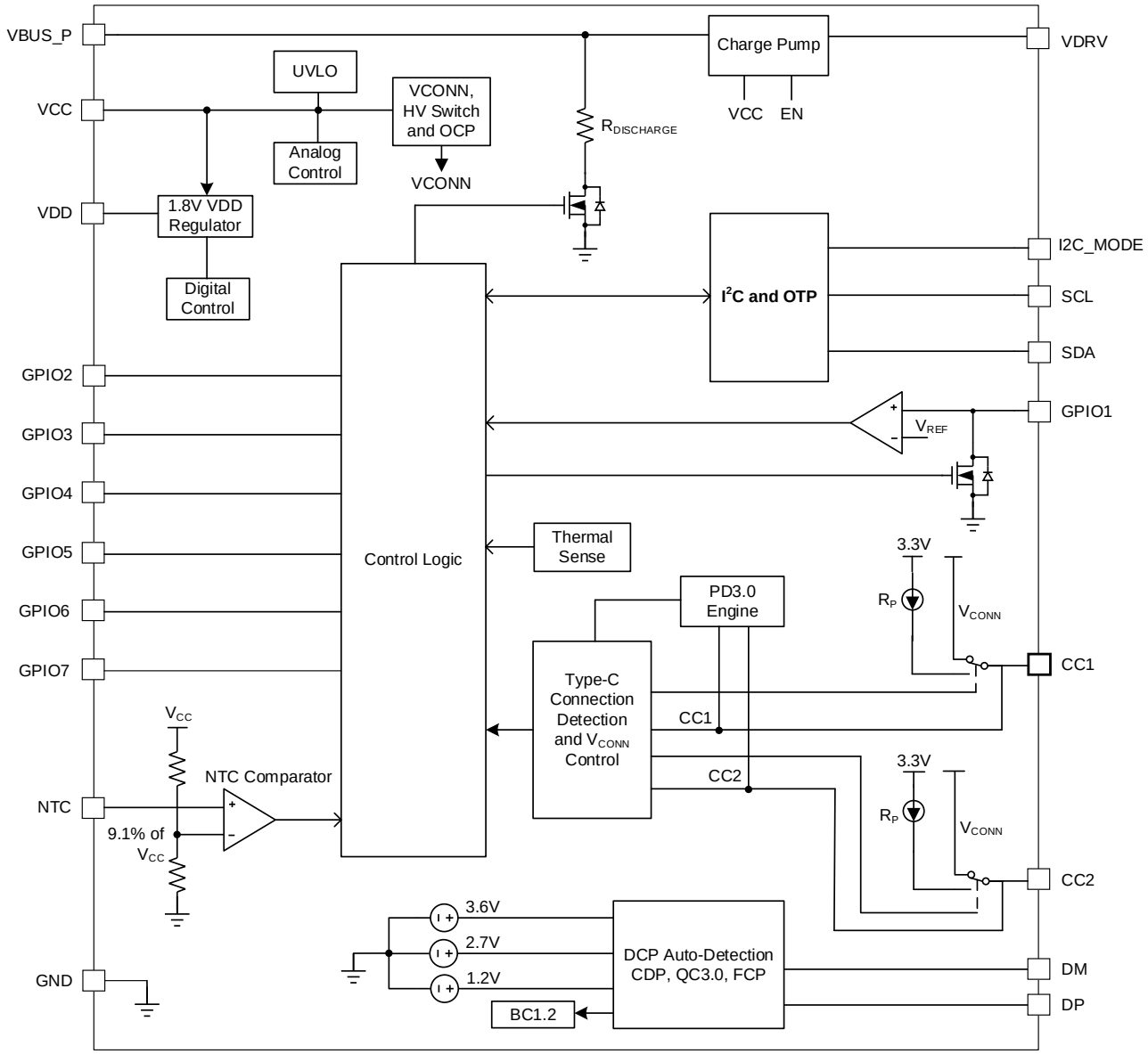


Figure 2: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

OPERATION

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the MP5031 from operating at an insufficient supply voltage. The UVLO comparator monitors the VCC input voltage (V_{CC}).

VCC and VDD Regulator

The VCC pin is biased via an external 5V supply (e.g. the DC/DC converter's VCC pin). A 1µF to 10µF decoupling capacitor is required for VCC.

The 1.8V internal VDD regulator uses VCC as the input. The VDD pin powers most of the digital circuitries, and requires a 0.47µF decoupling capacitor.

Charge Mode Auto-Detection

Legacy USB 2.0 Mode

The MP5031 has a USB-dedicated charging port auto-detection function. This function recognizes most mainstream portable devices, and supports the following charging schemes:

- USB Battery Charging Specification BC1.2, Chinese Telecommunications Industry Standard YD/T 1591-2009
- Apple divider 3 mode
- 1.2V/1.2V mode
- Quick Charge 3.0 (QC3.0), Class A (3.3V to 12V)
- Huawei Fast Charge Protocol (FCP), Class A

The auto-detection function is a state machine that supports the dedicated charging port schemes listed above. The state machine starts in divider 3 mode. If a device compliant with divider 3 mode is attached, then the MP5031 remains in divider 3 mode. Then 3.6V is applied to the DM pin, and 2.7V is applied to the DP pin.

If a BC1.2 device is attached, then the MP5031 operates in 1.2V/1.2V mode or BC1.2 DCP mode. DM and DP are shorted with a resistance below 40Ω. The MP5031 remains in 1.2V/1.2V mode or BC1.2 DCP until the device releases the data line, at which point the device returns to divider 3 mode.

If a QC3.0 or FCP device without power delivery (PD) is attached, then the MP5031 operates in high-voltage quick-charge (QC) mode.

The MP5031 supports BC1.2 charging data port (CDP) handshaking, which can be enabled via the I^2C. If CDP handshaking is enabled, then dedicated charging port mode should be disabled (LEGACY_CHARGING_MODE_SEL = 11b).

If a USB PD contract is established once the sink is attached, then QC3.0 functionality is disabled and BC1.2 short mode remains enabled.

USB Type-C Port

The USB Type-C receptacle, plug, and cable solution (USB Type-C port) uses a configuration process to detect a downward-facing port (DFP) to upward-facing port (UFP) connection. This connection is for V_{BUS} management and determining the host-to-device relationship.

The DFP-to-UFP attachment is detected via the host (DFP) once either the CC1 or CC2 pin senses a specified resistance to ground (GND) at the USB Type-C receptacle. The UFP-to-DFP detachment is detected once CC1 or CC2 is terminated at the USB Type-C receptacle and is no longer connected to GND.

Power is not applied to the USB Type-C host (V_{BUS}) or hub receptacle (V_{CONN}) until the DFP detects the presence of an attached device port (UFP). If a DFP-to-UFP attachment is detected, then the DFP powers the receptacle and begins normal USB operation with the attached device. If a DFP-to-UFP detachment is detected, then the port sourcing V_{BUS} stops powering the receptacle.

The MP5031 is a DFP (host only) with a default 5V/3A power supply capability. The DFP provides V_{CONN} to power the cables and electronics in the plug. If a Type-C host is connected, then one of the CCx pins is confirmed as the cable configuration channel (CC) wire, and the other unconnected CCx pin (VCONN) powers the plug. V_{CONN} has a 100mW maximum power output.

V_{CONN} is disabled until the pull-down resistor connected from CC1 or CC2 to GND (R_A) is detected. R_A's resistance should be below 1.2kΩ.

USB Power Delivery (PD)

In USB PD mode, pairs of directly attached ports use the CC wire as a communication channel to determine the voltage, current, and direction of

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

power flow across the USB cable. These ports operate independently of other USB methods that are used to determine power.

Type-C connectors can support the CC wire as the communication channel. The USB PD engine is disabled until a valid Type-C connection is established. Figure 3 shows a USB PD communication stack.

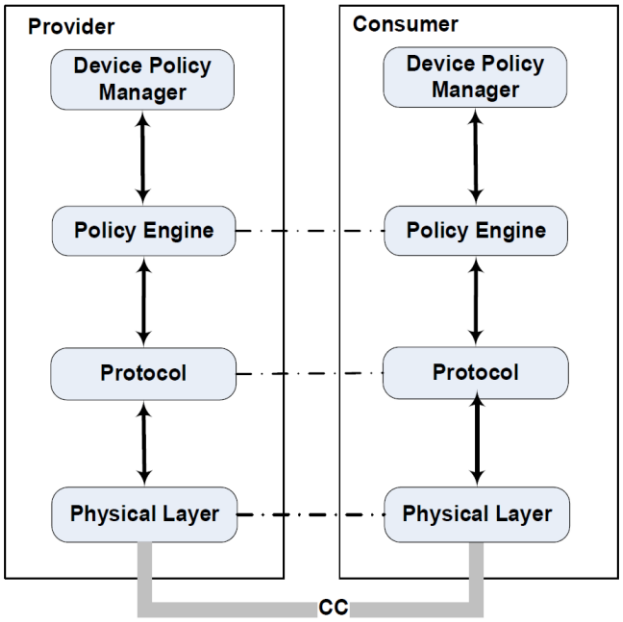


Figure 3: USB PD Communication Stack

The following tables list the MP5031's supported commands. Table 1 lists the control messages.

Table 1: Control Message

Transmitted Message	Received Message
ACCEPT	GET_PPS_STATUS
GET_SINK_CAP	GET_SOURCE_CAP
GET_SINK_CAP_ EXTENDED	GET_SOURCE_CAP_ EXTENDED
GET_STATUS	GET_STATUS
GOODCRC	GOODCRC
GOTOMIN	NOT_SUPPORTED
NOT_SUPPORTED	REJECT
PS_RDY	SOFT_RESET
REJECT	VCONN_SWAP
SOFT_RESET	N/A

Table 2 lists the data messages.

Table 2: Data Messages

Transmitted Message	Received Message
SOURCE_CAPABILITIES	SINK_CAPABILITIES
BIST	REQUEST
ALERT	BIST
N/A	ALERT

Table 3 lists the extended messages.

Table 3: Extended Messages

Transmitted Message	Received Message
STATUS	N/A
PPS_STATUS	N/A
SOURCE_CAPABILITIES_ EXTENDED	N/A

The MP5031 also supports soft reset, hard reset, and cable discovery for VDM signals. Figure 4 shows the device policy manager.

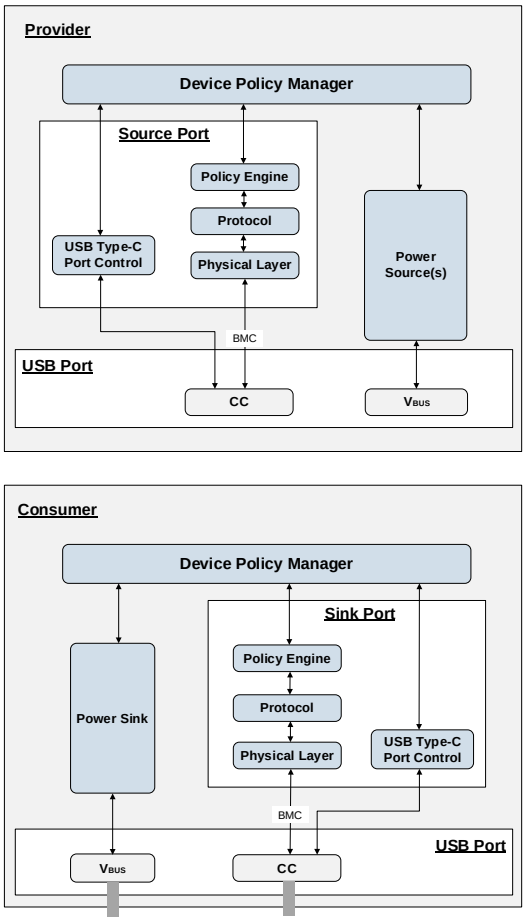


Figure 4: Device Policy Manager

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PD Contract Handshake

Figure 5 shows the MP5031's PD contract handshake sequence.

#	CH	OS	Power	Data	Cable Plug	Type
0	CC2	SOP'			UFP or DFP	Vendor_Defined
1	CC2	SOP'			Cable Plug	GoodCRC
2	CC2	SOP'			Cable Plug	Vendor_Defined
3	CC2	SOP'			UFP or DFP	GoodCRC
4	CC2	SOP	Source	DFP		Source_Capabilities
5	CC2	SOP	Sink	UFP		GoodCRC
6	CC2	SOP	Sink	UFP		Request
7	CC2	SOP	Source	DFP		GoodCRC
8	CC2	SOP	Source	DFP		Accept
9	CC2	SOP	Sink	UFP		GoodCRC
10	CC2	SOP	Source	DFP		PS_RDY
11	CC2	SOP	Sink	UFP		GoodCRC

Figure 5: PD Contract Handshake

V_{BUS} and V_{CONN} Discharge

If the sink is detached or a hard reset occurs, then the MP5031 turns the DC/DC regulator's output voltage (V_{OUT}) off and discharges V_{BUS} via its 200Ω discharge resistor for 200ms. The GPIO7 pin can also control an external MOSFET to discharge V_{OUT} for 200ms. Meanwhile, V_{CONN} is discharged via a 1kΩ discharge resistor for 30ms.

VBUS_P Under-Voltage Lockout (UVLO)

If a DC/DC converter with an I²C interface is selected, then VBUS_P UVLO is enabled by monitoring PG_STATUS. If V_{BUS} is below the UVLO falling threshold (2.97V or 4.5V) during programmable power supply (PPS) operation, then VBUS_UVLO is set to 1 internally, and a hard reset is triggered.

If a DC/DC converter without an I²C interface is selected, then PPS functionality is disabled. During fixed power data object (PDO) operation, the GPIO5 pin can be configured via VBUS_UV_FIXPDO. To detect V_{BUS}, connect GPIO5 to VBUS_P via a 1/5 resistor divider. Table 4 lists how to set the VBUS_P UVLO threshold in a fixed PDO state. If V_{BUS} drops below the UVLO threshold, then VBUS_UV_FIXPDO is set to 1 internally, and a hard reset is triggered.

Table 4: VBUS_P UVLO Threshold (Only Valid for DC/DC Converters without an I²C)

Sink Requested	VBUS_UV_ FIXPDO Threshold	VBUS_P UVLVO Threshold
V_{OUT} = 5V (default)	0.96V	4.8V
V_{OUT} = 9V	1.743V	8.715V
V_{OUT} = 15V	2.938V	14.69V
V_{OUT} = 20V	3.88V	19.4V

Figure 6 shows VBUS_P UVLO detection for DC/DC applications without an I²C.

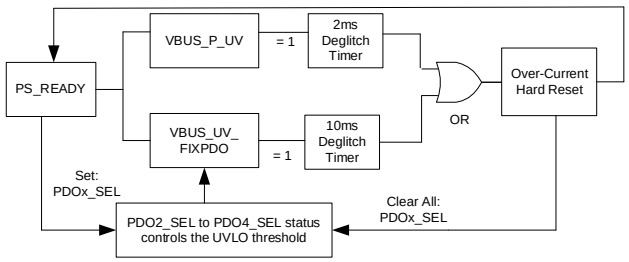


Figure 6: VBUS_P UVLO Detection for DC/DC Applications without an I²C

Start-Up and Shutdown Timing

The GPIO3, GPIO4, and GPIO6 pins can be configured as the EN input function that turns the MP5031 on and off.

If V_{CC} exceeds 4.3V and the GPIOx_EN pin is pulled high, then the PD engine is enabled. The MP5031's start-up time begins after the DC/DC converter start-up time. Its shutdown time begins before the converter's shutdown time (see Figure 7).

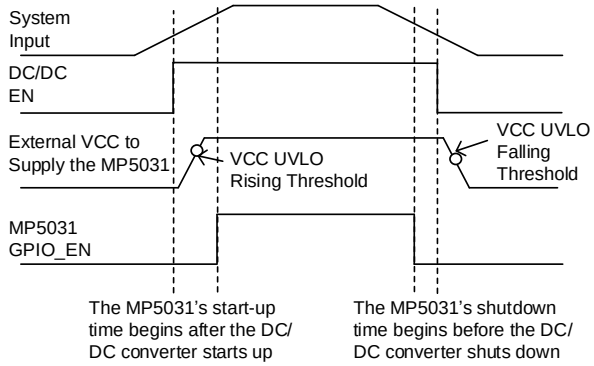


Figure 7: MP5031 Start-Up and Shutdown Timing

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

If the MP298x, MP424x, or MP4255 is used as the DC/DC converter, then the MP5031's V_{CC} is powered by the converter's 5V LDO output powers. If the MP28167-A is the DC/DC converter, then an external 5V LDO regulator is required to power the MP5031. The external 5V LDO regulator's start-up time should begin after the MP28167-A's start-up time.

In an MP298x, MP4255, or MP28167-A PD solution, GPIOx_EN can control the PD engine's start-up and shutdown times.

If GPIOx_EN is connected to the DC/DC converter's VIN pin, then the PD's start-up sequence input voltage (V_{IN_ON}) can be calculated with Equation (1):

$$V_{IN_ON}\ (V) = 1.43V \times (R_{DN2} + R_{UP2}) / R_{DN2} \quad (1)$$

The PD's shutdown sequence V_{IN} (V_{IN_OFF}) can be calculated with Equation (2):

$$V_{IN_OFF}\ (V) = 1.21V \times (R_{DN2} + R_{UP2}) / R_{DN2} \quad (2)$$

Figure 8 shows the MP5031's start-up time schematic.

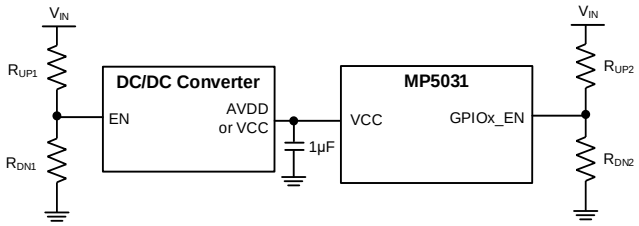


Figure 8: MP5031 Start-Up Time Schematic

Table 5 lists the V_{IN} start-up and shutdown thresholds.

Table 5: V_{IN} Start-Up and Shutdown Thresholds

	DC/DC EN Divider (kΩ)	MP5031 EN Divider (kΩ)	DC/DC Start-Up (V)	DC/DC Shutdown (V)	MP5031 Start-Up (V)	MP5031 Shutdown (V)
MP5031 + MP2984	100/30	100/28.4	5.85	5.07	6.47	5.47
MP5031 + MP4255	100/39	100/28.4	5.7	4.9	6.47	5.47

EN Off Delay Timer

The GPIO3 pin can be configured for EN_OFF_DELAY_OUT functionality. If EN is high, then the MP5031 turns on. If the external EN_OFF signal is received, then EN_OFF_DELAY_OUT remains high for 22min to enable the upstream DC/DC converter (EN_OFF_TIMER = 010b). After the 22min delay time, the USB PD engine turns off and CLK is disabled after a 200ms delay (see Figure 9). Figure 10 and Figure 11 on page 19 show the timing sequence.

If EN_OFF_DELAY functionality is not required, configure the GPIO3 for a function that is not EN_OFF_DELAY_OUT.

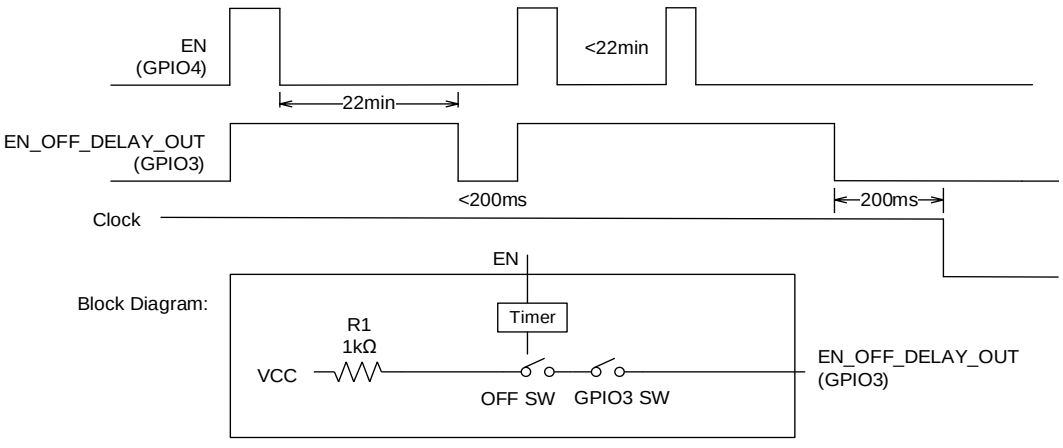


Figure 9: EN Off Timer

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

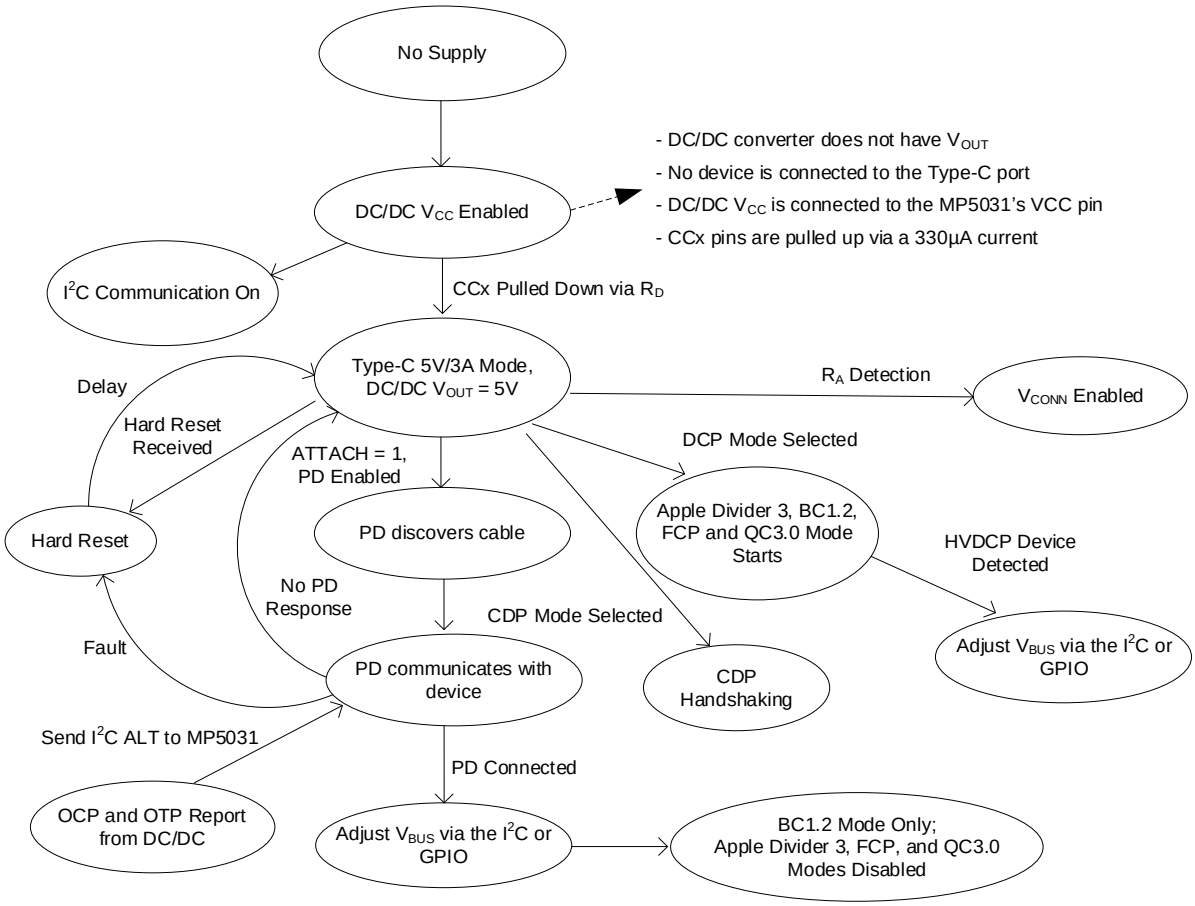


Figure 10: State Machine Diagram

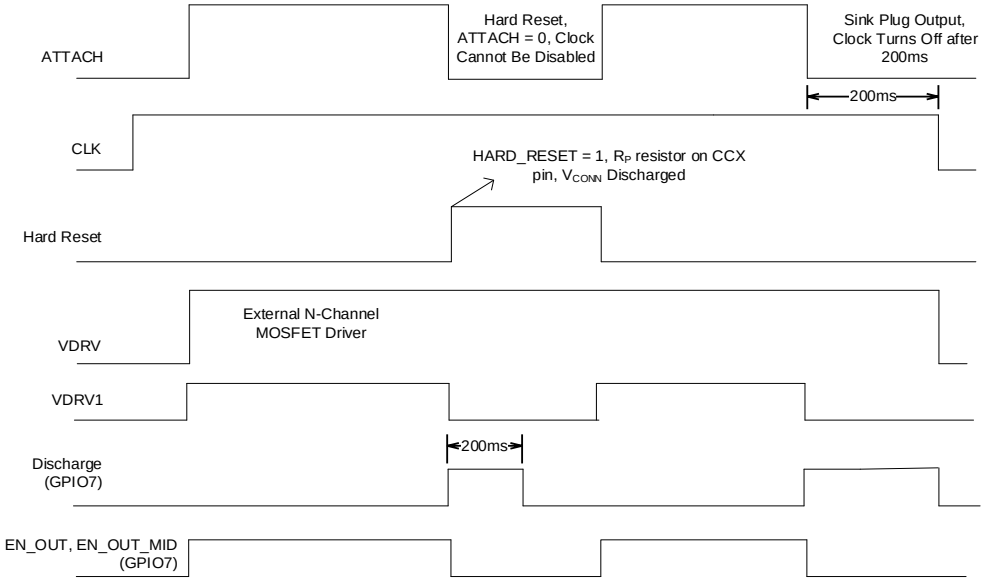


Figure 11: Attached Timing Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

V_{CONN} Over-Current Protection (OCP)

The VCC to V_{CONN} switch has a 20Ω resistance and a 50mA over-current protection (OCP) threshold. If V_{CONN} OCP is triggered, then V_{CONN}'s V_{OUT} latches off. The following actions can re-enable V_{CONN}:

- Cycling power on VIN and EN
- Hard reset
- Detaching and reattaching the USB Type-C device

Bidirectional I²C Interface

The MP5031's SDA and SCL pins support I²C master and slave functions. If operating with an external buck-boost converter (e.g. the MP4245), then the MP5031 operates in I²C master mode. Select I²C slave mode to configure the I²C register.

Float the I2C_MODE pin or pull it to GND to set the MP5031 to I²C master mode. Pull I2C_MODE to VCC to set the MP5031 to I²C slave mode. The digital clock is always on in I²C slave mode (I2C_MODE = VCC). The I²C is active once V_{CC} exceeds the VCC UVLO rising threshold. The Type-C sink does not have to be attached.

The GPIO5 and GPIO6 pins can be configured as a second I²C slave entrance. However, the internal clock must be turned on for full I²C functionality. The SDA, SCL, GPIO5, and GPIO6 pins cannot operate simultaneously in slave mode (see Table 6).

Table 6: SDA, SCL, GPIO5, and GPIO6 I²C Functions

I2C_MODE Input	SDA and SCL Function	GPIO5, GPIO6 Function	Internal Clock
VCC	I²C slave mode	I²C functionality disabled	Always on
GND	I²C master mode	I²C slave mode; the internal clock must be on for full I²C functionality	Use the USB Type-C attachment or write "0x55AA" to register 0x14 to enable the internal clock

Battery Low-Voltage Detection

The GPIO4 and GPIO2 pins can be configured as an input battery voltage-sense pin. If the battery voltage (V_{BATT}) drops below a certain level (this level is configurable), then the USB PD engine updates the source capability based on I²C control bits VBATT_LOW_PULL_PS_EN and VBATT_LOW_PULL_NTC_EN (see Table 7). Once V_{BATT} recovers, the USB PD engine changes the source capabilities to normal. If VBATT_LOW_PULL_NTC_EN = 1, then the source capability returns to normal after a 16s delay.

This function can also be disabled via I²C control bits VBATT_LOW_PULL_PS_EN and VBATT_LOW_PULL_NTC_EN.

It is recommended to have a 1/10 resistor divider ratio for VBATT_SENSE. The internal comparator's falling threshold is 1.12V, and its rising threshold is 1.18V with a 20µs deglitch time.

Table 7: Battery Low Update Source Capability

VBATT_LOW_PULL_PS_EN	0	0	1
VBATT_LOW_PULL_NTC_EN	0	1	0
Low Battery Voltage	The PDO list is based on the PDO_TYPE register setting	Update PDO1 to 5V/2A, the other PDOs are disabled	Disable the PDO with a power rating greater than or equal to PWR_SHARE_TO_PDP

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

The low battery voltage (V_{BATT_LOW}) can be calculated with Equation (3):

$$V_{BATT_LOW}\ (V) = 1.12V \times (R_{DN} + R_{UP}) / R_{DN} \quad (3)$$

Figure 12 shows the VBATT_SENSE resistor divider.

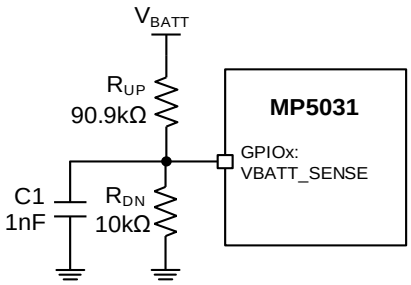


Figure 12: VBATT_SENSE Resistor Divider

Load-Shedding Entry and Recovery

If the NTC or NTC2 (NTC2_PS_EN = 0) falling threshold is triggered (NTC_MODE = 0), then the Type-C resistor pull-up current (R_P) changes from 330µA to 180µA. This occurs regardless of whether there is a PD contract or not.

If the MP424x device is selected (SLAVE_DEVICE_SEL = 001b), an OT_WARNING signal is sent and a PD contract exists, then R_P changes from 330µA to 180µA and the Type-C detection threshold changes accordingly. If a PD contract exists, then the USB PD PDO is updated to 5V/2A, and all other PDOs are disabled.

If the NTC or NTC2 voltage recovers to a normal value and the external DC/DC converter OT_WARNING = 0 after a 16s delay, then R_P returns to 330µA. If there was originally a PD contract, then the MP5031 USB PD engine sends the default PDOs again. If NTC2_PS_EN = 1 and the NTC2 falling threshold is triggered, then the MP5031 updates the PDO list based on PWR_SHARE_TO_PDP.

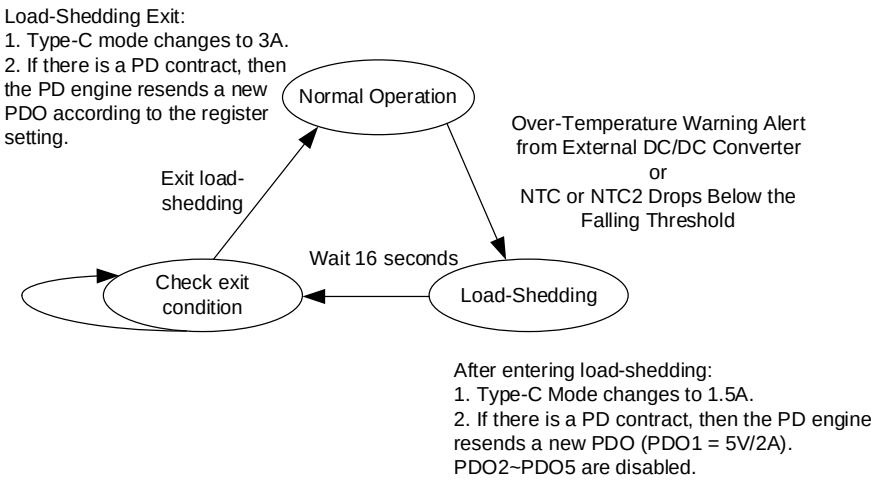


Figure 13: Load-Shedding State Machine (6)

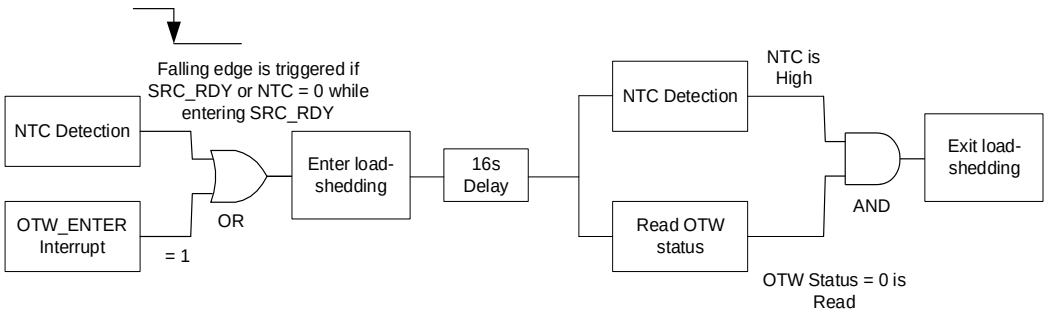


Figure 14: Load-Shedding Logic (6)

Note:

6) NTC2_PS_EN = 0.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the die temperature exceeds 150°C or the NTC/NTC2 falling threshold is triggered (NTC_MODE = 1), then the MP5031 resets the USB PD engine and turns off the DC/DC converter via the I²C or by pulling the converter's enable (EN) pin low. Once the temperature falls below its lower threshold (about 130°C), then the chip turns on again for CCx detection. If the sink is attached, then the MP5031 starts up the USB PD engine. The I²C slave remains operational during thermal shutdown.

Power Sharing

The GPIO2 pin can be configured for power-sharing input functions. If GPIO2 (POWER_SHARE) is pulled low, then the USB PD engine disables the PDO (if the power rating meets or exceeds PWR_SHARE_TO_PDP). All PPS augmented PDOs (APDOs) are disabled.

The GPIO3, GPIO5, or GPIO7 pins can be configured for ATTACH indication. If using multiple devices, and the first MP5031 (MP5031 #1) detects that a sink is attached, then GPIO3 is pulled low. At the same time, the second MP5031 (MP5031 #2) pulls its GPIO2 pin low. MP5031 #2 disables the PDO with a power rating that meets or exceeds PWR_SHARE_TO_PDP, and all PPS APDOs are disabled.

The GPIO2 pin can also be used for power-sharing output functions. If the MP5031's sink-requested PDO power rating meets or exceeds PWR_SHARE_OUTPUT_THLD, then GPIO2 is pulled low (see Figure 15).

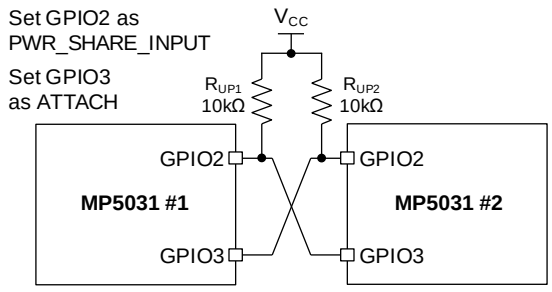


Figure 15: Power-Share Connection between Two MP5031s (7)

Note:

7) Cut total power to 50% per MP5031 device.

I²C Arbitration

The GPIO3 pin can be configured for I²C arbitration (I2C_ARB) functions. If MP5031 #1 sends an I²C command, then GPIO3 is pulled down. GPIO3 is pulled high again after MP5031 #1's I²C command is complete. MP5031 #2 checks the GPIO3 status and sends an I²C command until GPIO3 is pulled high (see Figure 16). The MP5031's I²C arbitration function can be used in the MP4255 reference design.

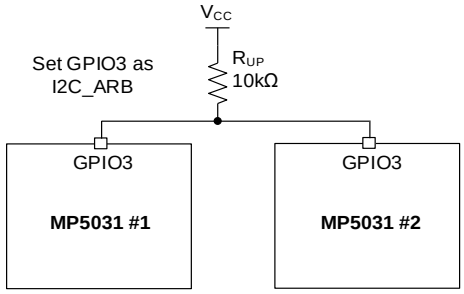


Figure 16: I²C Arbitration Connection

Charging Data Port (CDP) Mode

The MP5031 integrates CDP mode handshaking. Set CDP_EN = 1 to enable CDP mode handshaking. Disable Apple divider 3 mode, FCP, 1.2V/1.2V mode, and any other DCP schemes on the DP and DM pins (LEGACY_CHARGING_MODE_SEL = 11b) (see Figure 17).

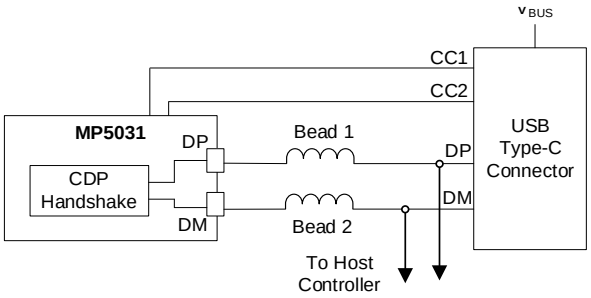


Figure 17: CDP Mode Set-Up

Smart Line Drop Compensation

The MP5031 has smart line drop compensation for when the MP424x or MP298x DC/DC converter is attached. Line drop compensation is active for both fixed PDO or non-PD conditions. If a PPS condition occurs, then line drop compensation is disabled. If the other DC/DC converter is selected, then the line drop compensation is determined by the converter's set-up, and the MP5031 does not disable line drop compensation in a PPS state.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

If an MP424x device is selected (SLAVE_DEVICE_SEL = 001b), then the line drop compensation value is determined by the MP424x's set-up. The MP5031 disables MP424x line drop compensation after entering PPS.

If an MP298x device is selected (SLAVE_DEVICE_SEL = 000B), then the MP5031's GPIO3 pin can be configured for ISENS+ functions, which sense the MP298x's COMP pin voltage (V_{COMP}). GPIO7 can be configured for adjustable functions, which sinks the 2μA current on the MP298x's FB pin once V_{COMP} exceeds 1.2V.

Figure 18 shows the PDO reduced logic and state machine.

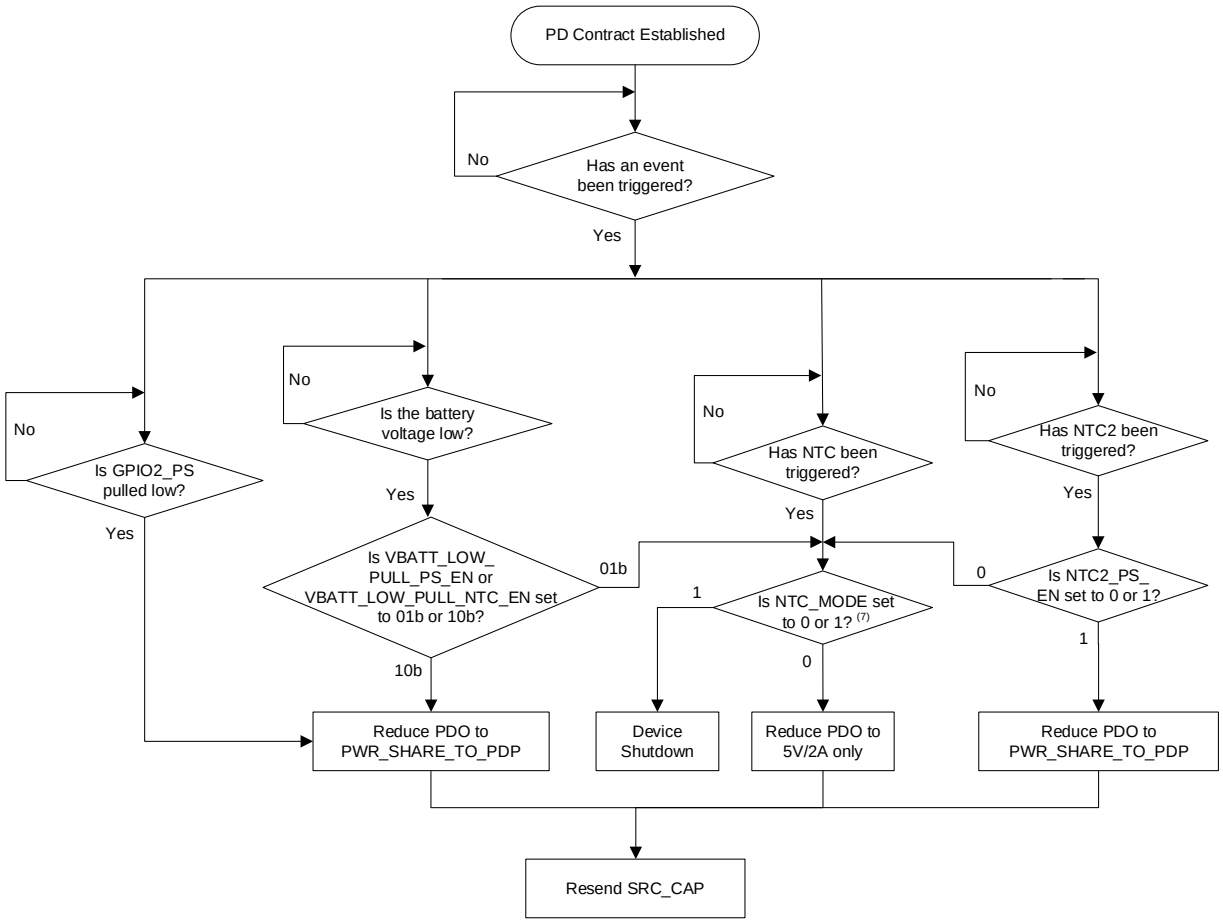


Figure 18: PDO Reduced Logic and State Machine (8)

Note:

8) If NTC and PWR_SHARE_TO_PDP events (GPIO2_PS pulls low, the battery voltage low, or NTC2) are triggered at the same time, then the PDO lists are updated based on the NTC set-up. If NTC_MODE = 1, then the device shuts down. If NTC_MODE = 0, then the PDO list is updated to 5V/2A.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

I²C Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The master generates the ACK-related clock pulse. The transmitter releases the SDA line (high) during the ACK clock pulse. The receiver must pull down the SDA line during the ACK clock pulse to remain stable (low) during the clock pulse's high period.

Figure 19 shows the complete data transfer format. After a start command (S) is sent, a slave address is sent. This address is 7 bits long and is followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated via a stop command (P) that is generated by the master. For a master to continue communicating on a bus, it can generate a repeated start command (Sr) and address another slave without first generating a stop command.

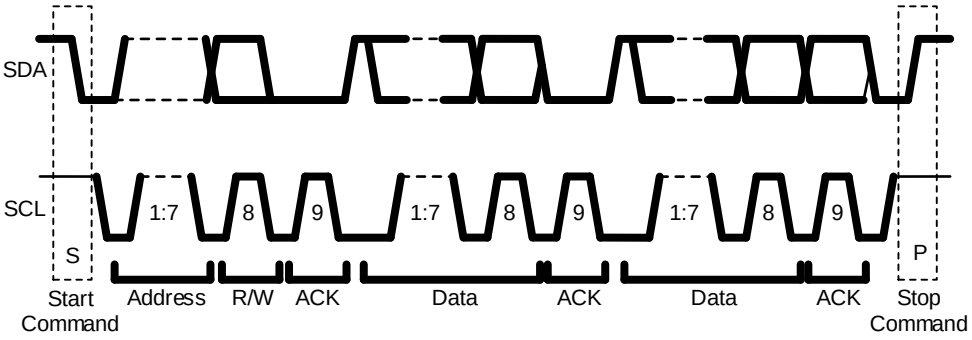


Figure 19: Complete Data Transfer

The MP5031 includes a full I²C slave controller. The I²C slave complies with the I²C specification requirements. It requires a start command, valid I²C address, register address byte, and data byte for a single data update. After receiving each byte, the MP5031 acknowledges the byte by pulling the SDA line low during the high period of a single clock pulse. Then a valid I²C address selects the MP5031, and the MP5031 performs an update on the falling edge of the LSB byte.

Figure 20 shows I²C read and write commands.

I²C Write (Wr)

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	I²C Register Address	A	Data Byte Low	A	Data Byte High	A	P

I²C Read (Rd)

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	I²C Register Address	A	S	Slave Address	Rd	A	Data Byte Low	A	Data Byte High	A	P

Figure 20: I²C Read and Write Commands

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

I²C REGISTER MAP

I²C Slave, I2C_MODE = VCC

Add. (Hex)	Name	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	PDO_TYPE	R/W	OTP_SOFTWARE_REVISION_NO (9)						RESERVED		PDO5_EN (9)	PDO4_EN (9)	PDO3_EN (9)	PDO2_EN (9)	PDO5_TYPE (9)	PDO4_TYPE (9)	PDO3_TYPE (9)	PDO2_TYPE (9)
01	PDO_V1	R	RESERVED						PDO1_VOLTAGE_SETTING (5V)									
02	PDO_I1	R/W	OTP_SUFFIX_CODE (9)						PDO1_CURRENT_SETTING (9) (3A default)									
03	PDO_V2	R/W	PDO2_VOLTAGE_SETTING (9) (9V default)															
04	PDO_I2	R/W	RESERVED						PDO2_CURRENT_SETTING (9) (3A default)									
05	PDO_V3	R/W	PDO3_VOLTAGE_SETTING (9) (15V default)															
06	PDO_I3	R/W	RESERVED						PDO3_CURRENT_SETTING (9) (3A default)									
07	PDO_V4	R/W	PDO4_VOLTAGE_SETTING (9) (20V default)															
08	PDO_I4	R/W	RESERVED						PDO4_CURRENT_SETTING (9) (3A default)									
09	PDO_V5	R/W	PDO5_VOLTAGE_SETTING (9) (3.3V to 21V default)															
0A	PDO_I5	R/W	RESERVED						PDO5_CURRENT_SETTING (9) (3A default)									
0B	CTL1	R/W	VBATT_LOW_PULL_PS_EN (9)	LEGACY_CHARGING_MODE_SEL_1 (9)	NTC2_PS_EN (9)	CDP_EN (9)	LEGACY_CHARGING_MODE_SEL_0 (9)	RESERVED	VBATT_LOW_PULL_NTC_EN (9)	I2C_SLAVE_ADDRESS (9)					TYPE-C_MODE (9)	SLAVE_DEVICE_SEL (9)		
0C	CTL2	R/W	HDRST	SEND_SRC_CAP	USB SUSPEND (9)	USB COMMUNICATE (9)	LPS (9)			TOUCH_CURRENT (9)			TOUCH_TEMP (9)		UNCUKEX TMSG (9)	RESERVED	SRC_CAP (9)	VDRV_EN (9)
0D	CTL3	R/W	PFM_PWM (9)	FREQ_DITHER (9)	EN_OFF_TIMER (9)			GPIO4 (9)		GPIO3 (9)			GPIO2 (9)			GPIO1 (9)		
0E	CTL4	R/W	NTC_MODE (9)	VBUS_UV_THD (9)	RESERVED			VDRV (9)		GPIO7 (9)			GPIO6 (9)			GPO5 (9)		
0F	PWRSHA	R/W	PWR_SHARE_OUTPUT_THLD (8)								POWER_SHARE_TO_PDP_THLD (8)							
10	STATUS 1	R	PPS_OUTPUT_VOLTAGE											BATTERY_SHORT	ANALOG_DETECTED_TYPEC	ANA_OTP	PREVIOUSLY_PD_CONNECTED	LOAD_SHEDDING
11	STATUS 2	R	RESERVED	CABLE_CAP	CAPABILITY_MISMATCH	OBJECT_POSITION			SINK_REQUEST_CURRENT_APDO								RESERVED	
12	ID	R	VENDER ID: 1000				RESERVED											
14	CLK_ON	R/W	Enable (EN) control of the digital clock: 0x55AA to enable the clock, 0x0000 to disable the clock															

Note:

9) These registers are one-time programmable (OTP). If the MP5031's VCC voltage (V_{CC}) exceeds the UVLO rising threshold, then the OTP items are loaded to the I²C register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REGISTER DESCRIPTION

PDO_TYPE

PDO1 is a 5V fixed power data object (PDO). PDO1 is always enabled.

Address: 0x00
Type: Read/write

Bits	Name	Description
D[15:10]	OTP_SOFTWARE_REVISION_NO	Returns the software revision number. Determined by MPS.
D[7]	PDO5_EN	Enables PDO5's power object. 0b: Disabled 1b: Enabled (default)
D[6]	PDO4_EN	Enables PDO4's power object. 0b: Disabled 1b: Enabled (default)
D[5]	PDO3_EN	Enables PDO3's power object. 0b: Disabled 1b: Enabled (default)
D[4]	PDO2_EN	Enables PDO2's power object. 0b: Disabled 1b: Enabled (default)
D[3]	PDO5_TYPE	Sets PDO5's power object. 0b: Fixed PDO 1b: APDO (default)
D[2]	PDO4_TYPE	Sets PDO4's power object. 0b: Fixed PDO (default) 1b: APDO
D[1]	PDO3_TYPE	Sets PDO3's power object. 0b: Fixed PDO (default) 1b: APDO
D[0]	PDO2_TYPE	Sets PDO2's power object. 0b: Fixed PDO (default) 1b: APDO

PDO_V1

Address: 0x01
Type: Read-only

Bits	Name	Description
D[9:0]	PDO1_VOLTAGE_SETTING	Sets PDO1's output voltage (V_{OUT}) in 50mV increments. This bit is fixed to 0001 1001 00b (5V).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PDO_I1

Address: 0x02
Type: Read/write

Bits	Name	Description
D[15:10]	OTP_SUFFIX_CODE	Returns the 4-digit suffix code. This code is assigned by MPS; contact an MPS FAE for details.
D[9:0]	PDO1_CURRENT_SETTING	Sets PDO1's maximum output current (I_{OUT_MAX}) in 10mA increments. The default I_{OUT_MAX} is 3A. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO_V2

Address: 0x03
Type: Read/write
Default PDO Type: Fixed PDO

PDO2_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO2_VOLTAGE_SETTING	Sets PDO2's V_{OUT} in 50mV increments. The default is 9V.

PDO2_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO2_MAXIMUM_VOLTAGE	Sets PDO2's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO2_MINIMUM_VOLTAGE	Sets PDO2's minimum voltage in 100mV increments.

PDO_I2

Address: 0x04
Type: Read/write
Default PDO Type: Fixed PDO

PDO2_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO2_CURRENT_SETTING	Sets PDO2's I_{OUT_MAX} in 10mA increments. The default I_{OUT_MAX} is 3A. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO2_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO2_CURRENT_SETTING	Sets PDO2's maximum current in 50mA increments. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PDO_V3

Address: 0x05
Type: Read/write
Default PDO Type: Fixed PDO

PDO3_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO3_VOLTAGE_SETTING	Sets PDO3's V_{OUT} in 50mV increments. The default is 15V.

PDO3_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO3_MAXIMUM_VOLTAGE	Sets PDO3's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO3_MINIMUM_VOLTAGE	Sets PDO3's minimum voltage in 100mV increments.

PDO_I3

Address: 0x06
Type: Read/write
Default PDO Type: Fixed PDO

PDO3_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO3_CURRENT_SETTING	Sets PDO3's I_{OUT_MAX} in 10mA increments. The default I_{OUT_MAX} is 3A. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO3_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO3_CURRENT_SETTING	Sets PDO3's maximum current in 50mA increments. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO_V4

Address: 0x07
Type: Read/write
Default PDO Type: Fixed PDO

PDO4_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO4_VOLTAGE_SETTING	Sets PDO4's V_{OUT} in 50mV increments. The default is 20V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PDO4_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO4_MAXIMUM_VOLTAGE	Sets PDO4's maximum voltage in 100mV increments. The absolute maximum value is 21V.
D[7:0]	PDO4_MINIMUM_VOLTAGE	Sets PDO4's minimum voltage in 100mV increments.

PDO_I4

Address: 0x08
Type: Read/write
Default PDO Type: Fixed PDO

PDO4_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO4_CURRENT_SETTING	Sets PDO4's I_{OUT_MAX} in 10mA increments. The default I_{OUT_MAX} is 3A. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO4_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO4_CURRENT_SETTING	Sets PDO4's maximum current in 50mA increments. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO_V5

Address: 0x09
Type: Read/write
Default PDO Type: APDO

PDO5_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO5_VOLTAGE_SETTING	Sets PDO5's V_{OUT} in 50mV increments.

PDO5_TYPE is set to 1b (APDO):

Bits	Name	Description
D[15:8]	PDO5_MAXIMUM_VOLTAGE	Sets PDO5's maximum voltage in 100mV increments. The default maximum voltage is 21V.
D[7:0]	PDO5_MINIMUM_VOLTAGE	Sets PDO5's minimum voltage in 100mV increments. The default minimum voltage is 3.3V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PDO_I5

Address: 0x0A
Type: Read/write
Default PDO Type: APDO

PDO5_TYPE is set to 0b (fixed PDO):

Bits	Name	Description
D[15:10]	RESERVED	Reserved. Set to 0b.
D[9:0]	PDO5_CURRENT_SETTING	Sets PDO5's I_{OUT_MAX} in 10mA increments. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

PDO5_TYPE is set to 1b (APDO) (default):

Bits	Name	Description
D[15:7]	RESERVED	Reserved. Set to 0b.
D[6:0]	PDO5_CURRENT_SETTING	Sets PDO5's I_{OUT_MAX} in 50mA increments. The default I_{OUT_MAX} is 3A. If these bits are set above 3A, then the MP5031 checks the cable current rating first. If the current rating is set to 5A, then it writes a setting above 3A. If the cable capability is 3A, then it writes a 3A maximum current capability.

CTL1

Address: 0x0B
Type: Read/write

<table>
<tr><th>Bits</th><th>Name</th><th>Description</th></tr>
<tr><td>D[15], D[8]</td><td>VBATT_LOW_PULL_PS_EN, VBATT_LOW_PULL_NTC_EN</td><td>If the GPIO2 or GPIO4 pin is set to VBATT_SENSE, then these bits control the MP5031's battery low-voltage detection. These bits are set to 01b by default. These bits cannot be set to 11b. The table below lists the configuration options:
<table>
<tr><td>D[15]: VBATT_LOW_PULL_PS_EN</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>D[8]: VBATT_LOW_PULL_NTC_EN</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>PDO List during a Battery Low-Voltage Condition</td><td>The PDO list is based on PDO_TYPE</td><td>Set PDO1 to 5V/2A. Other PDOs are disabled</td><td>Disable the PDO with a power rating greater than or equal to PWR_SHARE_TO_PDP</td></tr>
</table></td></tr>
<tr><td>D[14], D[11]</td><td>LEGACY_CHARGING_MODE_SEL1, LEGACY_CHARGING_MODE_SEL0</td><td>The MP5031 supports different legacy charging modes (e.g. QC3.0, Huawei FCP, BC1.2 DCP, and Apple divider 3 mode). These bits are set to 01b by default. The table below lists the different charging mode selections:
<table>
<tr><td>D[14]: LEGACY_CHARGING_MODE_SEL_1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>D[11]: LEGACY_CHARGING_MODE_SEL_0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>DP/DM Charge Mode</td><td>All modes are active</td><td>DCP mode is active. Divider 3 mode or QC3.0 mode are disabled. Short the DP and DM pins</td><td>Divider 3 mode and DCP mode are active</td><td>DCP mode is active. Divider 3 mode or QC3.0 mode are disabled. Short the DP and DM pins</td></tr>
</table></td></tr>
</table>

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

D[13]	NTC2_PS_EN	Enables the NTC2 power-sharing function. 0b: Disabled (default) 1b: Enabled
D[12]	CDP_EN	Enables charging data port (CDP) mode. This bit is set to 0b by default. 0b: CDP mode is disabled. Charge-only protocol on the DP and DM pins (default) 1b: CDP mode is enabled. CDP protocol on the DP and DM pins. QC3.0 mode, Apple divider 3 mode, and DCP mode are disabled (LEGACY_CHARGING_MODE_SEL = 11b)
D[10:9]	RESERVED	Reserved. Set to 00b.
D[7:4]	I2C_SLAVE_ ADDRESS	Sets the I^2C slave address. This bit is set to 1000b by default.
D[3]	TYPE-C_MODE	Selects 3A or 1.5A Type-C mode. In 5V/3A Type-C mode, the pull-up current (R_P) is 330µA and the detection range (R_D) is between 0.8V and 2.6V. 0b: 3A Type-C mode (default) 1b: 1.5A Type-C mode
D[2:0]	SLAVE_DEVICE_ SEL	Selects the power device that is incorporated set up to operate with the MP5031. These bits are set to 001b by default. 000b: MP298x 001b: MP424x (default) 010b: MP28167-A 011b: MP4255 Page 0 100b: MP4255 Page 1 101b: For non-I^2C DC/DC converters. If PDO2_SEL is selected, then PDO2_SEL is pulled low. If PDO3 is selected, then PDO2_SEL and PDO3_SEL are both pulled low. If PDO4 is selected, then PDO2_SEL, PDO3_SEL, and PDO4_SEL are pulled low. During a hard reset and detach event, both EN_OUT and EN_OUT_MID are low. For more information, see Figure 10 and Figure 11 on page 19 Others values are reserved.

CTL2

The message bits and bytes referenced in bits D[13:3] are defined in the USB Power Delivery Specification Revision 3.0, Version 2.0, which can be downloaded from the official USB website (usb.org).

Address: 0x0C
Type: Read/write

Bits	Name	Description
D[15]	HDRST	Sends the hard-reset command. 0b: Normal state (default) 1b: Sends a hard-reset command to the sink. After the hard reset message is sent, this bit auto-resets to 0b
D[14]	SEND_SRC_CAP	Sends the source capability command. The power delivery (PD) engine only sends a SOURCE_CAP message once the PS_RDY signal is ready. 0b: Normal state (default) 1b: Sends the source capability command. After SOURCE_CAP is sent, this bit auto-resets to 0b If there is a change in the PDO configuration in I^2C registers 0x01~0x09, then set SEND_SRC_CAP to have the new PDO take effect. After sending a new source capability, the MP5031 clears this bit. Set register 0x00 to have the new PDO take effect immediately.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

D[13]	USB_SUSPEND	Sets whether USB suspend functions are supported. This bit is defined in the Fixed Supply PDO message bit[28]. 0b: USB suspend functions are not supported (default) 1b: USB suspend functions are supported
D[12]	USB_COMMUNICATE	Sets whether USB communication capabilities are supported. This bit is defined in the Fixed Supply PDO message bit[26]. 0b: USB communication capabilities are not supported (default) 1b: USB communication capabilities are supported
D[11:9]	LPS	Sets the LPS compliance. These bits are defined in the SOURCE_CAPABILITIES_EXTENDED message byte 12, bits[2:0]. These bits are set to 101b by default. D[11]: LPS bit D[10]: PS1 bit D[9]: PS2 bit
D[8:6]	TOUCH_CURRENT	Sets the touch current bits[2:0]. These bits are defined in the SOURCE_CAPABILITIES_EXTENDED message byte 13, bits[2:0]. These bits are set to 000b by default. D[8] indicates the touch current bit[2].
D[5:4]	TOUCH_TEMP	Sets the default touch temperature value to 0, 1, or 2. These bits are defined in SOURCE_CAPABILITIES_EXTENDED message byte 20, bits[1:0]. These bits are set to 00b by default.
D[3]	UNCUKEXTMSG	Sets the unchunked extend message bit. This bit is defined in Fixed Supply PDO message bit[24]. This bit is set to 1b by default.
D[2]	RESERVED	Reserved. Always write 0b to this bit.
D[1]	SRC_CAP	Sends the source capability control bit twice when a PD2.0 device is attached. 0b: Sends source capability twice (default) 1b: Sends source capability once
D[0]	VDRV_EN	Enables the VDRV functions. The VDRV pin has a 5.1kΩ pull-down resistor when it is disabled. 0b: VDRV output disabled (default) 1b: VDRV functions enabled

CTL3

Address: 0x0D
Type: Read/write

Bits	Name	Description
D[15]	PFM_PWM	Sets the MP28167-A and MP298x operation modes. 0b: Pulse-frequency modulation (PFM) mode. If the MP28167-A is selected as the I^2C slave, then its 0x04 register D[4] = 0. If the MP298x is selected as the I^2C slave, then its 0x02 register D[2] = 0 1b: Pulse-width modulation (PWM) mode (default). If the MP28167-A is selected as the I^2C slave, then its 0x04 register D[4] = 1. If the MP298x is selected as the I^2C slave, then its 0x02 register D[2] = 1
D[14]	FREQ_DITHER	Enables the MP298x's frequency dithering. 0b: Frequency dithering is disabled, and the MP298x operates in fixed-frequency mode (default). If the MP298x is selected as the I^2C slave, then its 0x02 register D[4] = 0 1b: Frequency dithering is enabled. If the MP298x is selected as the I^2C slave, then its 0x02 register D[4] = 1 For other devices, such as the MP4245, ignore this bit.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

D[13:11]	EN_OFF_TIMER	Sets the EN off timer delay. These bits are only valid when GPIO4 is set for EN functionality. 000b: No delay 001b: 10min 010b: 22min (default) 011b: 40min 100b: 80min 101b: 120min
D[10:9]	GPIO4	Configures the GPIO4 pin's functionality. 00b: Reserved (default). GPIO4 can be floated or tied to GND 01b: EN function. If the external input exceeds 1.4V, then the MP5031 is enabled. If the external input drops below 1.2V, then the MP5031 is disabled and in a low I_Q state. The EN off timer delay can be configured via EN_OFF_TIMER 10b: NTC2 function. For more information, see the Load-Shedding Entry and Recovery section on page 21. 11b: GPIO4 functions as the VBATT_SENSE pin, and monitors V_{BATT}. If V_{BATT} is low (the resistor divider ratio is 1/10), then the PD updates the source capability. The internal comparator's falling threshold is 1.1V, and its rising threshold is 1.15V with a 20μs deglitch time. The internal comparator begins operating once V_{CC} exceeds the under-voltage lockout (UVLO) threshold after a 5s delay time
D[8:6]	GPIO3	Configures the GPIO3 pin's functionality. GPIO3 low-voltage pin supports 5.5V operation and has an internal ESD Zener diode. 000b: I2C_ARB function (default). Tri-state input/output (input high, input low, and output low) to avoid having two I^2C masters. This function is similar to the structure of GPIO2 when it is set to PWE_SHARE. For more information, see the I^2C Arbitration section on page 22 001b: EN function. If the external input exceeds 1.4V, then the MP5031 is enabled. If the external input drops below 1.2V, then the MP5031 is disabled and is in a low I_Q state 010b: ATTACH function. GPIO3 is an open drain that is pulled low once a Type-C port is attached 011b: EN_OFF_DELAY_OUT function. If EN goes low, then GPIO3 still outputs high. GPIO3 is floated after 22 minutes. This signal can be used to control the upstream DC/DC converter's enable (EN) pin 100b: Plug orientation (POL) output low 101b: PDO3_SEL_OUT. GPIO3 is an open-drain output. If PDO3 is selected, then this pin is pulled low. The pull-down speed is slow (typically 1ms to drop from 100kΩ to 2Ω) 110b: ISENS+ function. If the MP298x is selected, then GPIO3+ is used for line drop compensation. To sense current information, connect ISENS+ to the MP298x's COMP pin 111b: I_{PWM} function. The PWM output sets the external buck-boost converter's programmable power supply (PPS) configuration channel (CC) current limit. GPIO3 must be pulled up externally. The PWM signal frequency is 10kHz
D[5:3]	GPIO2	Configures the GPIO2 pin's functionality. GPIO2 is a low-voltage pin. 000b: QC_12 function. For QC2.0 mode, GPIO2 goes low and enables a 12V V_{OUT} 001b: POL output. GPIO2 is an open-drain output that indicates the plug orientation. If CC1 is selected as the CC line, then POL is pulled low. If CC2 is selected as the CC line, then POL is an open drain 010b: GPIO2 is pulled low 110b: PWR_SHARE function (default). For more information, see the Power Sharing section on page 22 111b: VBATT_SENSE pin

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

D[2:0]	GPIO1	Configures the GPIO1 pin's functionality. GPIO1 is a low-voltage pin that supports 5.5V operation. 000b: PDO2_SEL_OUT. GPIO1 is an open-drain output. If PDO2 is selected, then GPIO1 is pulled low. The pull-down speed is slow (typically 1ms to drop from 100kΩ to 2Ω). For QC2.0 mode, GPIO1 goes low and enables a 9V V_{OUT} (GPIO1 can be configured for either QC2.0 or PD protocol when set to 000b) 001b: Interrupt (INT) input pin (default). GPIO1 is a high-impedance pin that monitors the input signal. In application, INT should be connected to the external DC/DC converter's ALT pin to receive interruption information from the I^2C slave 010b: GPIO1 is pulled low 011b: GPIO1 is an open drain 100b: VSEL1. V_{OUT} selection pin. For more information, see the GPIO Summary section on page 37 100b~111b: Reserved

CTL4

Address: 0x0E
Type: Read/write

Bits	Name	Description
D[15]	NTC_MODE	Sets the NTC behavior. 0b: If NTC is triggered, then the MP5031 initiates load-shedding (default) 1b: If NTC is triggered, then the MP5031 shuts down. This process is similar to internal thermal shutdown. The ENO_MID output is set to a voltage that enables the DC/DC converter without requiring V_{OUT}
D[14]	VBUS_UV_THD	Sets the VBUS_P UVLO falling threshold. If the minimum APDO voltage is 3.3V, then set the UVLO threshold to 2.97V. If the minimum APDO voltage is 5V, then set the UVLO threshold to 4.5V. 0b: The VBUS_P UVLO falling threshold is 2.97V (default) 1b: The VBUS_P UVLO falling threshold is 4.5V
D[10:9]	VDRV	Sets the VDRV pin's functionality. 00b: VDRV function (default). VDRV is the external N-channel MOSFET gate driver signal. If the sink is attached, then VDRV turns the external N-channel MOSFET on, and power flows from the DC/DC output to the sink. If the sink is detached, then VDRV turns the external N-channel MOSFET off to isolate the power path 01b: VDRV1 function. For information on the timing sequence, see Figure 11 on page 19
D[8:6]	GPIO7	Configures the GPIO7 pin's functionality. GPIO7 is a low-voltage pin. 000b: DISCHG pin. GPIO7 operates as the output discharge function. The discharge function turns on for 200ms and then turns off. DISCHG only outputs a control signal. Add an external N-channel MOSFET between VBUS_P and GND 001b: ATTACH function. GPIO7 is an open drain, and is pulled low once a Type-C port is attached 011b: EN_OUT_MID function (default). If a hard reset or a detach event occurs, then GPIO7 clamps the voltage at 1V 100b: EN_OUT. This output controls the upstream DC/DC output. If a hard reset occurs, then the PD engine pulls GPIO7 to GND. GPIO7 is an open-drain output during normal operation 101b: Adjustable function. This function is used for the MP298x's line drop compensation. If the COMP voltage exceeds 1.2V, then GPIO7 sinks a 2μA current

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

D[5:3]	GPIO6	Configures the GPIO6 pin's functionality. 000b: PDO4_SEL_OUT. If PDO4 is selected, then GPIO6 is an open-drain output 001b: VSEL2. GPIO6 is the V_{OUT} selection pin 010b: POL output (default). GPIO6 is an open-drain output that indicates the plug orientation. If CC1 is selected as the CC line, then POL is pulled low. If CC2 is selected as the CC line, then POL is an open drain 011b: EN function. If the external input exceeds 1.4V, then the MP5031 is enabled. If the external input drops below 1.2V, then the MP5031 is disabled and is in a low I_Q state 100b: SYNC_OUT2. GPIO6 is the PWM output that syncs the external buck-boost converter's f_{SW}. It is an open-drain output with a 25% duty cycle, 450kHz frequency, and 180° phase delay based on GPIO5 101b: NTC2 function. For more information, see the Load-Shedding Entry and Recovery section on page 21 110b: I2C_SLV_SDA. GPIO6 is an I^2C slave data pin
D[2:0]	GPIO5	Configures the GPIO5 pin's functionality. 000b: I2C_SLV_SCL (default). GPIO5 is the I^2C slave's clock pin 001b: IPWM. The PWM output sets the external buck-boost converter's PPS CC current limit. GPIO5 must be pulled up internally to 1.8V via a 2kΩ pull-up resistor. The PWM signal frequency is 10kHz 010b: SYNC_OUT1. GPIO5 is the PWM output that syncs the external buck-boost converter's f_{SW}. It is an open-drain output with a 25% duty cycle, 250kHz frequency, and 0° phase delay 011b: GPIO5 is the PWM output that syncs the external buck-boost converter's f_{SW}. It is an open-drain output with a 25% duty cycle, 350kHz frequency, and 0° phase delay 100b: SYNC_OUT1. GPIO5 is the PWM output that syncs the external buck-boost converter's f_{SW}. It is an open-drain output with a 25% duty cycle, 450kHz frequency, and 0° phase delay 101b: ATTACH function. GPIO5 is an open-drain output, and is pulled low once a Type-C port is attached. 111b: VBUS_UV_FIXPDO. GPIO5 is a V_{BUS} detection input. Connect a 1/5 resistor divider to V_{BUS}

PWRSHA

Address: 0x0F
Type: Read/write

Bits	Name	Description
D[15:8]	PWR_SHARE_ OUTPUT_THLD	Sets the sink-requested PDO power rating threshold. If the sink-requested PDO power rating meets or exceeds this threshold while GPIO2 is set to PWR_SHARE, then the GPIO2 pin is pulled low. The default value is 0x3C (60W). 0x01: 1W … 0xFF: 255W
D[7:0]	PWR_SHARE_ INPUT_TO_PDP_ THLD	Sets the port's PD power rating. If the GPIO2 pin is pulled low while set to PWR_SHARE, then the battery voltage is low (VBATT_LOW_PULL_PS_EN = 1b) or NTC2 is triggered (NTC2_PS_EN = 1b). All PDOs with a power rating that meets or exceeds this threshold are disabled. The default value is 0x3C (60W). 0x01: 1W … 0xFF: 255W

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

STATUS1

This register is read clear.

Address: 0x10
Type: Read-only

Bits	Name	Description
D[15:5]	PPS_OUTPUT_ VOLTAGE	Records the sink requested for PPS V_{OUT} in 20mV. This bit is only valid when the selected PDO is APDO.
D[4]	BATTERY_SHORT	This bit is set if CC1, CC2, DP, or DM is shorted to the input battery.
D[3]	ANALOG_ DETECTED_TYPEC	Detects whether a Type-C device is attached.
D[2]	ANA_OTP	Indicates whether the MP5031 has entered over-temperature protection (OTP), excluding thermal shutdowns caused by NTC or NTC2. It also indicates if the external power device enters OTP (the digital side provides the OTP information for the external device).
D[1]	PREVIOUSLY_PD_ CONNECTED	Indicates whether the MP5031 has a PD contract.
D[0]	LOAD_ SHEDDING	Indicates whether the device has entered load-shedding (see Figure 13 on page 21 for more details).

STATUS2

Read clear.

Address: 0x11
Type: Read-only

Bits	Name	Description
D[15]	RESERVED	Reserved.
D[14]	CABLE_CAP	1b: Cable capability is 5A 0b: Cable capability is 3A
D[13]	CAPABILITY_ MISMATCH	A sink request sets the capability mismatch bit.
D[12:10]	OBJECT_POSITION	If a sink is attached, these bits indicate the sink-requested PDO position. 000b: Non-PD device is attached 001b: Sink-requested PDO1 (5V PDO) 010b: Sink-requested PDO2 011b: Sink-requested PDO3 100b: Sink-requested PDO4 101b: Sink-requested PDO5
D[9:2]	SINK_REQUEST_ CURRENT_APDO	Returns the sink-requested APDO current in 50mA increments.
D[1:0]	RESERVED	Reserved.

ID

Address: 0x12
Type: Read-only

Bits	Name	Description
D[15:12]	VENDOR_ID	Vendor ID. The default is 1000b.
D[11:0]	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CLK_ON

Address: 0x14
Type: Read/write

Bits	Name	Description
D[15:0]	CLK_ON	Enables the digital clock (CLK). Set these bits to 0x55AA to enable the digital clock; set them to 0x0000 to disable the clock. If GPIO5 and GPIO6 are configured as I2C_SLV_SCL and I2C_SLV_SDA, respectively, then CLK should be enabled when sending I^2C write commands via GPIO5/GPIO6, and CLK should be disabled after the I^2C command ends. CLK does not need to be enabled when only reading the I^2C register via GPIO5 and GPIO6.

I^2C Bus Slave Address

The slave address is a 7-bit address followed by an 8th data direction bit (read or write). The A4 to A1 bits are OTP-configurable.

Table 8: I^2C Bus Slave Address

Bit	A7	A6	A5	A4	A3	A2	A1
Setting Value	0	1	0	1 (10)	0 (10)	0 (10)	0 (10)

Note:

10) The slave address is 0x28 (A[7:1] = 0101 000) by default.

GPIO Summary

For more information on the GPIO functions, see the CTL3 register description on page 32 and the CTL4 register description on page 34.

Table 9: GPIO Function Options

Name	Function Options							
GPIO1	INT	PDO2_ SEL_OUT	VSEL1	-	-	-	-	-
GPIO2	PWR_ SHARE	QC_12	POL	VBATT_ SENSE	-	-	-	-
GPIO3	I2C_ARB	PDO3_ SEL_OUT	POL	EN_OFF_ DELAY_ OUT	ISENS+	IPWM (11)	ATTACH	EN
GPIO4	EN	NTC2	VBATT_ SENSE	-	-	-	-	-
GPIO5	SYNC_ OUT1	IPWM (11)	VBUS_UV _FIXPDO	I2C_SLV_ SCL	ATTACH	-	-	-
GPIO6	SYNC_ OUT2	PDO4_ SEL_OUT	VSEL2	I2C_SLV_ SDA	NTC2	POL	EN	-
GPIO7	DISCHG	EN_OUT	EN_OUT_ MID	ADJ	ATTACH	-	-	-
VDRV	VDRV	VDRV1	-	-	-	-	-	-

Note:

11) I_{PWM} on the GPIO3 pin must be pulled up externally. I_{PWM} on the GPIO5 pin is pulled up internally.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

Table 10: V_{OUT} Voltage vs. GPIO Output for Non-I²C DC/DC Converter Use Case

V_{OUT}	PDO2_SEL_OUT (or QC_9)	QC_12	PDO3_SEL_OUT	PDO4_SEL_OUT
5V	Open drain	Open drain	Open drain	Open drain
9V	0	Open drain	Open drain	Open drain
12V	0	0	Open drain	Open drain
15V	0	Open drain	0	Open drain
20V	0	Open drain	0	0

Table 11: V_{OUT} vs. VSEL1 and VSEL2 Output Statuses (12)

V_{OUT}	VSEL1	VSEL2
5V	Open drain	Open drain
9V	0	Open drain
15V	Open drain	0
20V	0	0
12V	100kΩ to GND	0

Note:

12) VSEL1 and VSEL2 can control the MP2491C's V_{OUT}.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

APPLICATION INFORMATION

PCB Layout Guidelines [13]

Efficient PCB layout is critical for stable operation and improved ESD performance. A 2-layer or 4-layer layout is recommended. For the best results, refer to Figure 21 and follow the guidelines below:

1. Place the VCC and VDD decoupling capacitors as close to the VCC and VDD pins as possible.
2. Place nine vias on the IC's exposed pad, and connect the exposed pad to GND.
3. Place the ESD diodes as close to the IC as possible.
4. Use short, direct, and wide traces to connect the CC1, CC2, DP, and DM pins to the ESD diodes cathode.
5. Use multiple vias to connect the ESD diode anode to GND.
6. Use short, direct, and wide traces to connect CC1 and CC2 to the USB Type-C receptacle.

Note:

13) The recommended layout is based on Figure 22 in the Typical Application Circuits section on page 40.

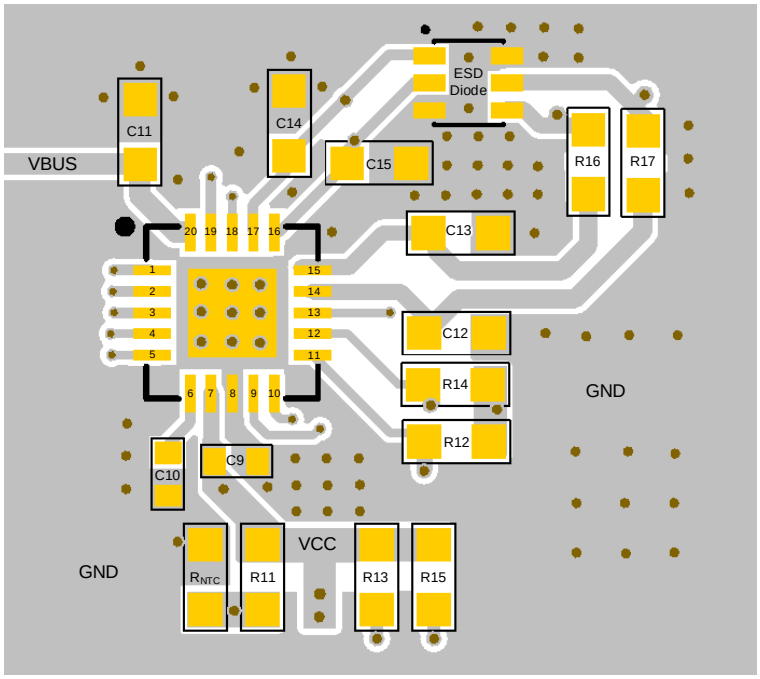


Figure 21: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

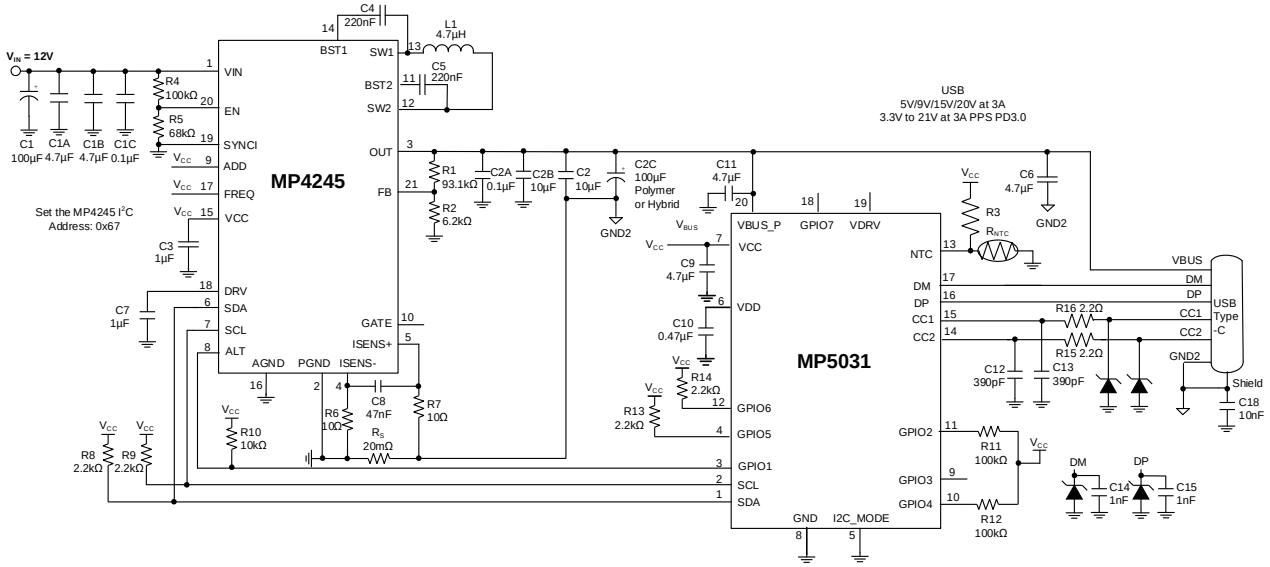


Figure 22: MP4245 and MP5031 60W PD Application (14)

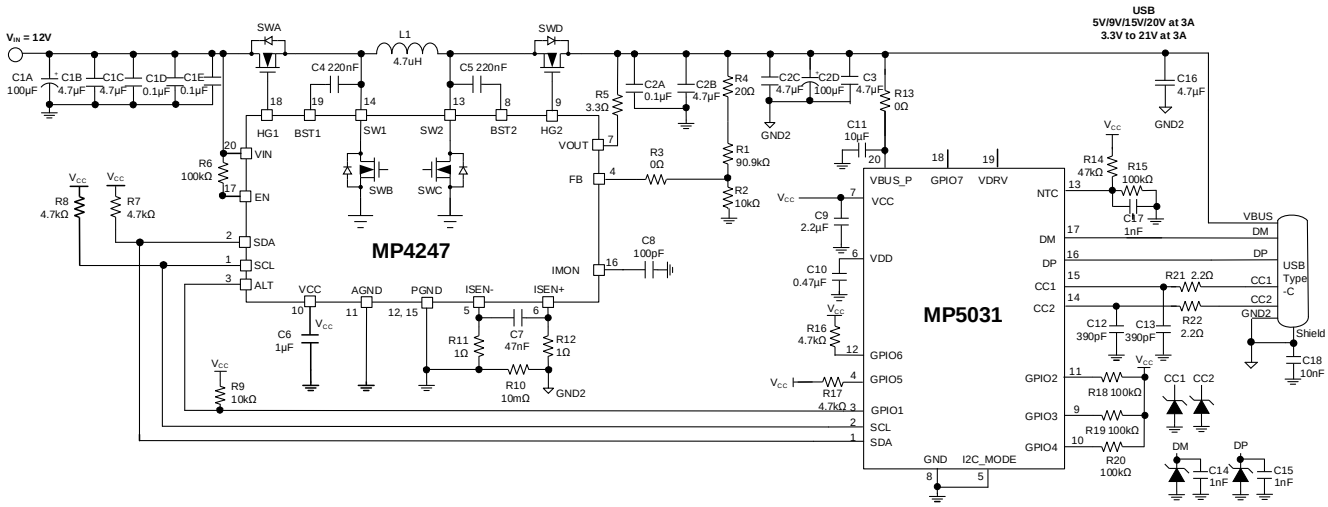


Figure 23: MP4247 and MP5031 60W PD Application (14)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

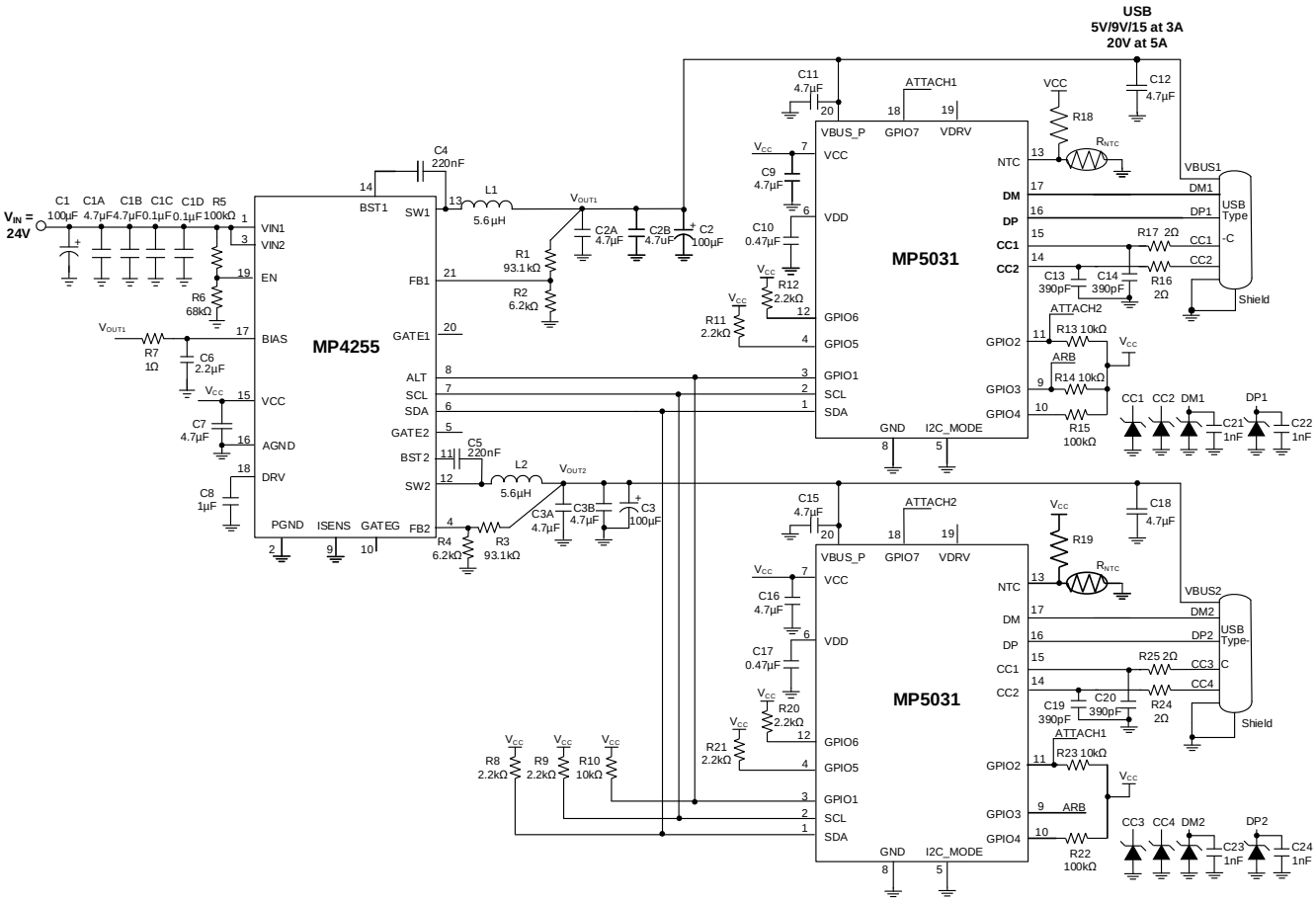


Figure 24: MP4255 and MP5031 Dual-Port 100W Shared PD Application (14)

Note:

14) Add a TVS filter and RC filter to the DP, DM, CC1, and CC2 pins to ensure that they pass ±8kV/±15kV IEC Contact/Air Discharge ESD.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

MP5031GRE-00A3 CONFIGURATION TABLES

Table 12: PDO Configuration Table

OTP Items	Enabled/Disabled	PDO Type	Voltage	Current
PDO1	Enabled	Fixed PDO	5V	3A
PDO2	1b: Enabled (default)	0b: Fixed PDO (default)	9V (default)	3A
PDO3	1b: Enabled (default)	0b: Fixed PDO (default)	15V (default)	3A
PDO4	1b: Enabled (default)	0b: Fixed PDO (default)	20V (default)	3A
PDO5	1b: Enabled (default)	1b: APDO (default)	3.3V to 21V (default)	3A

Table 13: Configuration Table

OTP Items	Description	Value
GPIO1	Configures the GPIO1 pin's functionality.	001b: Interrupt input pin (default)
GPIO2	Configures the GPIO2 pin's functionality.	110b: PWR_SHARE function (default)
GPIO3	Configures the GPIO3 pin's functionality.	000b: I2C_ARB function (default)
GPIO4	Configures the GPIO4 pin's functionality.	00b: RESERVED (default)
GPIO5	Configures the GPIO5 pin's functionality.	000b: I2C_SLV_SCL (default)
GPIO6	Configures the GPIO6 pin's functionality.	110b: I2C_SLV_SDA (default)
GPIO7	Configures the GPIO7 pin's functionality.	011b: EN_OUT_MID function (default)
VBATT_LOW_PULL_PS_EN	If a low battery voltage condition occurs, then the PDO list is reduced based on PWR_SHARE_TO_PDP_THLD.	0b: Disabled (default)
VBATT_LOW_PULL_NTC_EN	Updates the PDO list to 5V/2A. If a low battery voltage condition occurs, then the other PDOs are disabled.	0b: Disabled
NTC2_PS_EN	Connects NTC2 to the power-share control.	0b: Disabled (default)
LEGACY_CHARGING_MODE_SEL	QC3.0/DCP short mode and Apple divider 3 mode selection.	00b: All modes are active
CDP_EN	Enables CDP mode.	0b: CDP mode disabled, charge-only protocol on DP and DM (default)
I2C_SLAVE_ADDRESS	Sets the MP5031's I²C slave address.	28h (default)
TYPE-C_MODE	Selects 3A or 1.5A Type-C mode.	0b: 3A Type-C mode (default)
SLAVE_DEVICE_SEL	Selects the power device set up to operate with MP5031.	001b: MP424x (default)
VDRV	Sets the VDRV pin function.	00b: VDRV function (default)
VDRV_EN	Enables the VDRV function.	0b: Disabled (default)
PFM_PWM	Sets the MP28167A and MP298x operation modes.	1b: PWM mode (default)
FREQ_DITHER	Enables MP298x frequency dithering.	0b: Fixed-frequency mode (default)
EN_OFF_TIMER	Sets the different EN off timers. Only valid while GPIO4 is set for EN functions.	010b: 20min (default)
NTC_MODE	Sets the MP5031 behavior if NTC is triggered.	1b: The MP5031 shuts down
VBUS_UV_THD	Sets the VBUS_P UV threshold.	0b: VBUS_P falling threshold is 2.97V (default)
PWR_SHARE_OUTPUT_THLD	Sets the sink-requested PDO power rating threshold.	0x3C: 60W (default)
PWR_SHARE_TO_PDP_THLD	Sets the PDO power rating threshold.	0x3C: 60W (default)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

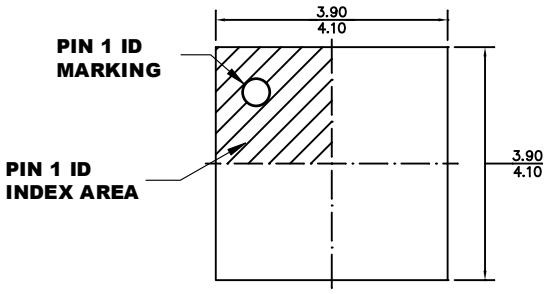
MP5031GRE-00A3 CONFIGURATION TABLES *(continued)*

OTP Items	Description	Value
USB_SUSPEND	Determines whether USB suspension is supported.	0b: Not supported (default)
USB_COMMUNICATE	Determines the USB communication capability.	0b: Not supported (default)
LPS	Determines the LPS compliance.	101b (default)
TOUCH_CURRENT	Sets the touch current bits[2:0].	000b (default)
TOUCH_TEMP	Sets the touch temperature default value to 0, 1, or 2.	00b (default)
UNCUKEXTMSG	Sets the unchunked extend message bit.	1b (default)
OTP_SUFFIX_CODE	OTP suffix code.	0x00A3

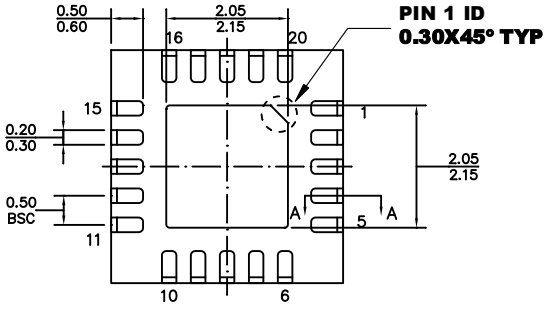
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

PACKAGE INFORMATION

QFN-20 (4mmx4mm)



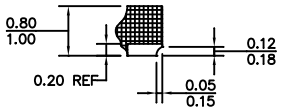
TOP VIEW



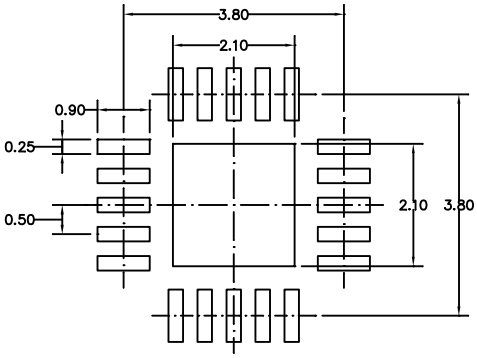
BOTTOM VIEW



SIDE VIEW



SECTION A-A



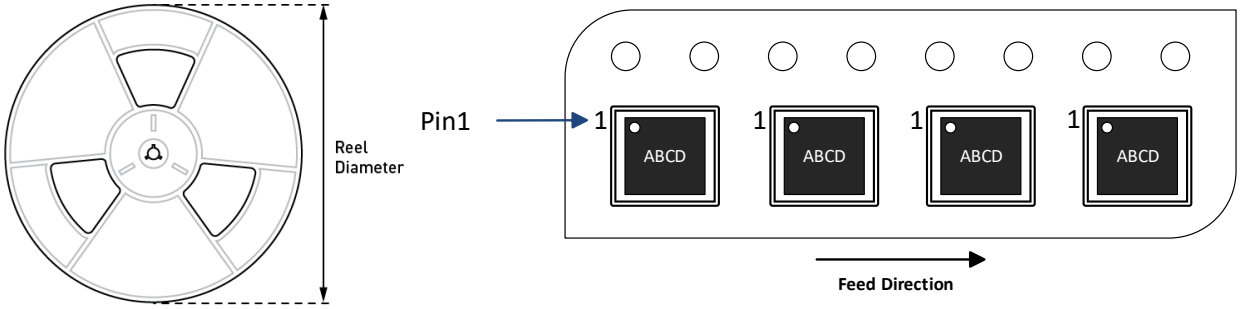
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAXIMUM.
5) JEDEC REFERENCE IS MO-220
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5031GRE-xxxx-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/22/2021	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2021 MPS. All Rights Reserved.