NextGen Components,Inc.

PART CODE: 1210B223K631DC

SPECIFICATION SHEET

SPECIFICATION SHEET NO.	Q0618- 1210B223K631DC
DATE	June 18， 2023
REVISION	A2
DESCRIPITION	Multilayer Ceramic Chip Capacitors, Medium Voltage 1210 (3225 Metric) Series, L3.20mm*W2.50mm,Thickness: 1.35mm Max. Dielectric X7R, Capacitance 0.022µF, Tolerance ±10%, Rated Voltage 630V Operating Temp. Range -55°C ~+125°C Package in Tape/Reel, 3,000pcs/Reel RoHS/RoHS III compliant
CUSTOMER	
CUSTOMER PART NUMBER	
CROSS REF. PART NUMBER	
ORIGINAL PART NUMBER	Aillen 1210B223K631DC
PART CODE	1210B223K631DC

VENDOR APPROVE	
Issued/Checked/Approved	NextGen Components, Inc. Mandy Xu　NextGen Components, Inc. Ruby Zhang　NextGen Components, Inc. Jack Zhang
DATE: June 18， 2023	

CUSTOMER APPROVE
DATE:

NextGen Components, Inc. sales@NextGenComponent.com www.NextGenComponent.com

NextGen Components,Inc.

PART CODE: **1210B223K631DC**

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

MAIN FEATURE

MLCC consists of a conducting material and electrodes. To manufacture a chip-type SMT and achieve miniaturization, high density and high efficiency, ceramic condensers are used. MLCC is made by NP0, X7R, and Y5V dielectric material and which provides medium Voltage product with high electrical precision, stability and reliability.

MAIN FEATURE

• RoHS III Compliant • Wide Operating Temperature Range -55~+125℃ • High capacitance and High Voltage in given case size • A wide selection of sizes is available (0603 to 1812) • Capacitor with lead-free termination (pure Tin)

APPLICATION

• DC to DC converter.• High voltage coupling/DC blocking • Back-lighting inverters • Snubbers in high frequency power convertors

RFQ
Request For Quotation

PART CODE GUIDE

Code	Name	Key Specification Option
1210	Size	0603 (1608): L1.60*W0.80mm; 0805 (2012): L2.00*W1.25mm 1206 (3216:) L3.20*W1.60mm; **1210 (3225): L3.20*W2.50mm** 1812 (4532): L4.50*W3.20mm
B	Dielectric	N: NP0 (C0G); **B: X7R**; Y: Y5V
223	Capacitance	Two significant digits followed by number of Zero, The 3rd digit signifies the multiplying factor, and letter R is decimal point. 0R5: 0.5pF; 1R0:1.0pF; 104: 100nF; **223: 0.022μF**
K	Tolerance	B=±0.1pF; C=±0.25pF; D=±0.5pF; F=±1%; G=±2%; J=±5%; **K=±10%;** M=±20%; Z=-20/+80%
631	Rated Voltage	Two significant digits followed by No. of zeros. “R” is in place of decimal point. 201=200 VDC; 251=250 VDC; 501=500 VDC; **631 =630 VDC**
D	Thickness	A: 0.60±0.10mm; B: 0.85 ±0.15mm; C: 0.95±0.10mm; **D: 1.25±0.10mm** I: 1.25±0.20mm; G: 1.60±0.20mm; K: 2.00±0.20mm; M: 2.50±0.30mm; N: 0.50+0.05mm; S: 0.80+0.10mm; U: 2.80±0.30mm; X: 0.80 ±0.20mm
C	Package	A: 1Kpcs/Reel; B: 2Kpcs/Reel; **C: 3Kpcs/Reel;** D: 4Kpcs/Reel; I: 10Kpcs/Reel; K: 0.5 Kpcs/Reel; F: others
	Internal Control	Internal Code: Letter + Number; Blank: N/A;

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

DIMENSION (Unit: mm)

Image for reference



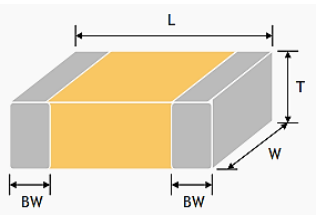


Table 1

Size Code	L	W	T	BW
0603 (1608)	1.60±0.15	0.80±0.15	0.95	0.20
0805 (2012)	2.00±0.20	1.25±0.20	1.45	0.30
1206 (3216)	3.20±0.20	1.60±0.20	1.80	0.30
	3.20+0.3/-0.1	1.60+0.3/-0.1	1.90	
1210 (3225)	3.20±0.40	2.50±0.30	2.80	0.30
1812 (4532)	4.50±0.40	3.20±0.30	2.80	0.26

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

GENERAL ELECTRONICAL CHARACTERISTICS

Table 2

Dielectric	NP0 (C0G)	X7R	Y5V
Size	0603, 0805, 1206, 1210, 1812		0805, 1206, 1210, 1812
Capacitance range*	0.5pF to 39.0nF	100pF to 1.0μF	10nF to 1.0μF
Capacitance Tolerance	Cap≤5pF: B (±0.1pF), C (±0.25pF) 5pF<Cap<10pF: C (±0.25pF), D (±0.5pF) Cap≥10pF: F (±1%), G (±2%), J (±5%), K (±10%)	J (±5%), K (±10%), M (±20%)	Z (-20/+80%)
Rated Voltage	200V, 250V, 500V, 630V		200V, 250V
Tan δ*	Cap<30pF: Q≥400+20C Cap≥30pF: Q≥1000	≤2.5% (Apply 1.0±0.2Vrms, 1.0KHz±10%)	≤5%
Insulation resistance at Ur**	≥100GΩ or R•C≥1000 whichever is smaller	≥10GΩ or R•C≥100Ω-F whichever is smaller	
Operating Temperature	-55 ~+125°C		-25 ~+85°C
Capacitance Characteristic	±30ppm/℃	±15%	+30/-80%
Termination	Cu (or Ag)/Ni/Sn (lead-free termination)		

Note:

1) * Measured at the condition of 30~70% related humidity.
2) NP0: Apply 1.0±0.2Vrms, 1.0MHz±10% for Cap≦1000pF and 1.0±0.2Vrms, 1.0kHz±10% for Cap>1000pF, 25°C at ambient temperature.
3) X7R: Apply 1.0±0.2Vrms, 1.0kHz±10%, at 25°C ambient temperature.
4) Y5V: Apply 1.0±0.2Vrms, 1.0kHz±10%, at 20°C ambient temperature.
5) ** Measured at 500VDC for 60 sec, for UR>500VDC

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0603, 0805, 1206 SIZES

Table 3-A

Size	0603		0805				1206			
VDC (V)	200	250	200	250	500	630	200	250	500	630
0.5pF (0R5)	S	S	A	A	A	A				
1.0pF (1R0)	S	S	A	A	A	A				
1.2pF (1R2)	S	S	A	A	A	A				
1.5pF (1R5)	S	S	A	A	A	A	B	B	B	B
1.8pF (1R8)	S	S	A	A	A	A	B	B	B	B
2.2pF (2R2)	S	S	A	A	A	A	B	B	B	B
2.7pF (2R7)	S	S	A	A	A	A	B	B	B	B
3.3pF (3R3)	S	S	A	A	A	A	B	B	B	B
3.9pF (3R9)	S	S	A	A	A	A	B	B	B	B
4.7pF (4R7)	S	S	A	A	A	A	B	B	B	B
5.6pF (5R6)	S	S	A	A	A	A	B	B	B	B
6.8pF (6R8)	S	S	A	A	A	A	B	B	B	B
8.2pF (8R2)	S	S	A	A	A	A	B	B	B	B
10pF (100)	S	S	A	A	A	A	B	B	B	B
12pF (120)	S	S	A	A	A	A	B	B	B	B
15pF (150)	S	S	A	A	A	A	B	B	B	B
18pF (180)	S	S	A	A	A	A	B	B	B	B
20pF (200)	S	S	A	A	A	A	B	B	B	B
22pF (220)	S	S	A	A	A	A	B	B	B	B
27pF (270)	S	S	A	A	A	A	B	B	B	B
30pF (300)	S	S	A	A	A	A	B	B	B	B
33pF (330)	S	S	A	A	A	A	B	B	B	B
39pF (390)	S	S	A	A	A	A	B	B	B	B
47pF (470)	S	S	A	A	A	A	B	B	B	B
56pF (560)	S	S	A	A	A	A	B	B	B	B
68pF (680)	S	S	A	A	A	A	B	B	B	B
82pF (820)	S	S	A	A	A	A	B	B	B	B
100pF (101)	S	S	A	A	A	A	B	B	B	B
120pF (121)	S	S	A	B	D	D	B	B	B	B
150pF (151)	S	S	B	D	D	D	B	B	B	B

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 0603, 0805, 1206 SIZES

Table 3-B

Size	0603		0805				1206			
VDC (V)	200	250	200	250	500	630	200	250	500	630
180pF (181)	S	S	B	D	D	D	B	B	B	B
220pF (221)	S	S	D	D	D	D	B	B	B	B
270pF (271)	X	X	D	D	D	D	B	C	C	C
330pF (331)	X	X	D	D	D	D	B	C	C	C
390pF (391)	X	X	D	D	D	D	B	C	C	C
470pF (471)	X	X	D	D	I	I	C	C	C	C
560pF (561)	X	X	D	D	I	I	C	C	C	C
680pF (681)			D	D	I	I	C	D	D	D
820pF (821)			D	D	I	I	C	D	D	D
1,000pF (102)			D	D	I	I	C	G	G	G
1,200pF (122)			D	D			C	G	G	G
1,500pF (152)			D	D			D	G	G	G
1,800pF (182)			D	D			D	G	G	G
2,200pF (222)			D	D			D	G	G	G
2,700pF (272)							D	G		
3,300pF (332)							D	G		
3,900pF (392)							D	G		
4,700pF (472)							D	G		

CAPACITANCE RANGE - NP0 DIELECTRIC 1210. 1812SIZES

Table 3-C

Size	1210				1812			
VDC (V)	200	250	500	630	200	250	500	630
10pF (100)	C	C	C	C	D	D	D	D
12pF (120)	C	C	C	C	D	D	D	D
15pF (150)	C	C	C	C	D	D	D	D
18pF (180)	C	C	C	C	D	D	D	D
20pF (200)	C	C	C	C	D	D	D	D
22pF (220)	C	C	C	C	D	D	D	D
27pF (270)	C	C	C	C	D	D	D	D
33pF (330)	C	C	C	C	D	D	D	D

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 1210. 1812SIZES

Table 3-D

Size	1210				1812			
VDC (V)	200	250	500	630	200	250	500	630
39pF (390)	C	C	C	C	D	D	D	D
47pF (470)	C	C	C	C	D	D	D	D
56pF (560)	C	C	C	C	D	D	D	D
68pF (680)	C	C	C	C	D	D	D	D
82pF (820)	C	C	C	C	D	D	D	D
100pF (101)	C	C	C	C	D	D	D	D
120pF (121)	C	C	C	C	D	D	D	D
150pF (151)	C	C	C	C	D	D	D	D
180pF (181)	C	C	C	C	D	D	D	D
220pF (221)	C	C	C	C	D	D	D	D
270pF (271)	C	C	C	C	D	D	D	D
330pF (331)	C	C	C	C	D	D	D	D
390pF (391)	C	C	C	C	D	D	D	D
470pF (471)	C	C	C	C	D	D	D	D
560pF (561)	C	C	C	C	D	D	D	D
680pF (681)	C	C	C	C	D	D	D	D
820pF (821)	C	C	C	C	D	D	D	D
1,000pF (102)	D	D	D	D	D	D	D	D
1,200pF (122)	D	D	D	D	D	D	D	D
1,500pF (152)	D	D	D	D	D	D	D	D
1,800pF (182)	D	D	D	D	D	D	D	D
2,200pF (222)	D	D	D	D	D	D	D	D
2,700pF (272)	D	D	D	D	D	D	D	D
3,300pF (332)	D	D	D	D	D	D	D	D
3,900pF (392)	D	D	D	D	D	D	D	D
4,700pF (472)	G	G			D	D	D	D
5,600pF (562)	G	G			D	D	D	D
6,800pF (682)	G	G			D	D	D	D
8,200pF (822)	G	G					D	D

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE - NP0 DIELECTRIC 1210. 1812SIZES

Table 3-E

Size	1210				1812			
VDC (V)	200	250	500	630	200	250	500	630
0.010µF (103)	G	G					D	D
0.022µF (223)	M	M					K	K
0.033µF (333)	M	M					M	M

CAPACITANCE RANGE – X7R DIELECTRIC 0603, 0805 1206 SIZES

Table 4-A

Size	0603		0805				1206			
VDC (V)	200	250	200	250	500	630	200	250	500	630
100pF (101)	X	X	B	B	B	B	D	D	D	D
120pF (121)	X	X	B	B	B	B	D	D	D	D
150pF (151)	X	X	B	B	B	B	D	D	D	D
180pF (181)	X	X	B	B	B	B	D	D	D	D
220pF (221)	X	X	B	B	B	B	D	D	D	D
270pF (271)	X	X	B	B	B	B	D	D	D	D
330pF (331)	X	X	B	B	B	B	D	D	D	D
390pF (391)	X	X	B	B	B	B	D	D	D	D
470pF (471)	X	X	B	B	B	B	D	D	D	D
560pF (561)	X	X	B	B	B	B	D	D	D	D
680pF (681)	X	X	B	B	B	B	D	D	D	D
820pF (821)	X	X	B	B	B	B	D	D	D	D
1,000pF (102)	X	X	B	B	B	B	D	D	D	D
1,200pF (122)	X	X	B	B	B	B	D	D	D	D
1,500pF (152)	X	X	B	B	B	B	D	D	D	D
1,800pF (182)	X	X	B	B	B	B	D	D	D	D
2,200pF (222)	X	X	B	B	B	B	D	D	D	D
2,700pF (272)	X	X	B	B	B	B	D	D	D	D
3,300pF (332)	X	X	B	B	B	B	D	D	D	D
3,900pF (392)	X	X	B	B	B	B	D	D	D	D
4,700pF (472)	X	X	B	B	D	D	D	D	D	D
5,600pF (562)	X	X	D	D	D	D	D	D	D	D

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 0603, 0805 1206 SIZES

Table 4-B

Size	0603		0805				1206			
VDC (V)	200	250	200	250	500	630	200	250	500	630
6,800pF (682)	X	X	D	D	D	D	D	D	D	D
8,200pF (822)	X	X	D	D	D	D	D	D	D	D
0.010µF (103)	X	X	D	D	D	D	D	B/D	D	D
0.012µF (123)			D	D	D	D	D	D	D	D
0.015µF (153)			D	D	D	D	D	D	D	D
0.018µF (183)			D	D	D	D	D	D	D	D
0.022µF (223)			D	D	D	D	D	D	G	G
0.027µF (273)			D	D			D	D	G	G
0.033µF (333)			D	D			G	G	G	G
0.039µF (393)			D	D			G	G	G	G
0.047µF (473)			D	D			G	G	G	G
0.056µF (563)			D	D			G	G	G	G

CAPACITANCE RANGE – X7R DIELECTRIC 0805 1206 SIZES

Table 4-C

Size	0805		1206					
VDC (V)	200	250	200	250	400	450	500	630
0.068µF (683)	D	D	G	G	G	G		
0.082µF (823)	D		G	G	G	G		
0.10µF (104)	D		G	G	G	G		
0.12µF (124)			G	G				
0.15µF (154)			G	G				
0.18µF (184)			G	G				
0.22µF (224)			G	G				

CAPACITANCE RANGE – X7R DIELECTRIC 1210, 1812 SIZES

Table 4-D

Size	1210				1812			
VDC (V)	200	250	500	630	200	250	500	630
100pF (101)	D	D	D	D				
120pF (121)	D	D	D	D				
150pF (151)	D	D	D	D				

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

CAPACITANCE RANGE – X7R DIELECTRIC 1210, 1812 SIZES

Table 4-E

Size	1210				1812			
VDC (V)	200	250	500	630	200	250	500	630
180pF (181)	D	D	D	D				
220pF (221)	D	D	D	D				
270pF (271)	D	D	D	D				
330pF (331)	D	D	D	D				
390pF (391)	D	D	D	D				
470pF (471)	D	D	D	D				
560pF (561)	D	D	D	D				
680pF (681)	C	C	D	D				
820pF (821)	C	C	D	D				
1,000pF (102)	C	C	D	D	D	D	D	D
1,200pF (122)	C	C	D	D	D	D	D	D
1,500pF (152)	C	C	D	D	D	D	D	D
1,800pF (182)	C	C	D	D	D	D	D	D
2,200pF (222)	C	C	D	D	D	D	D	D
2,700pF (272)	C	C	D	D	D	D	D	D
3,300pF (332)	C	C	D	D	D	D	D	D
3,900pF (392)	C	C	D	D	D	D	D	D
4,700pF (472)	C	C	D	D	D	D	D	D
5,600pF (562)	C	C	D	D	D	D	D	D
6,800pF (682)	C	C	D	D	D	D	D	D
8,200pF (822)	C	C	D	D	D	D	D	D
0.010µF (103)	C	C	D	D	D	D	D	D
0.012µF (123)	C	C	D	D	D	D	D	D
0.015µF (153)	C	C	D	D	D	D	D	D
0.018µF (183)	C	C	D	D	D	D	D	D
0.022µF (223)	C	C	D	D	D	D	D	D
0.027µF (273)	C	C	G	G	D	D	D	D
0.033µF (333)	C	C	G	G	D	D	D	D
0.039µF (393)	C	C	G	G	D	D	D	D

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

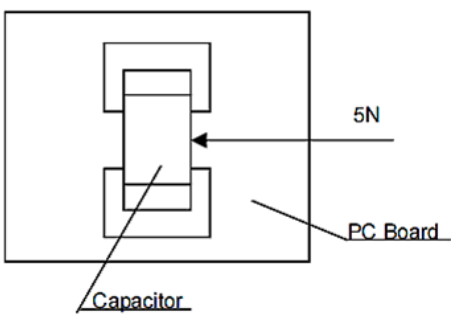
CAPACITANCE RANGE – X7R DIELECTRIC 1210, 1812 SIZES

Table 4-F

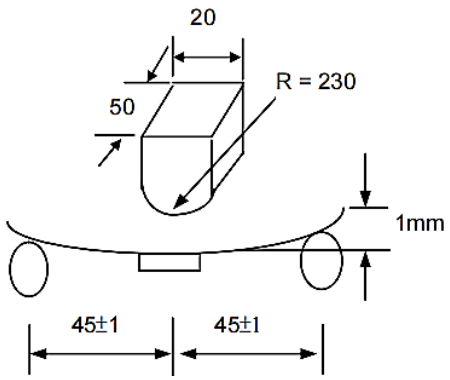
Size	1210						1812			
VDC (V)	200	250	400	450	500	630	200	250	500	630
0.047µF (473)	D	D			G	G	D	D	D	D
0.056µF (563)	D	D			G	G	D	D	K	K
0.068µF (683)	D	D			K	K	D	D	K	K
0.082µF (823)	D	D			K	K	D	D	K	K
0.010µF (103)	C	C			D	D	D	D	D	D
0.012µF (123)	C	C			D	D	D	D	D	D
0.015µF (153)	C	C			D	D	D	D	D	D
0.018µF (183)	C	C			D	D	D	D	D	D
0.022µF (223)	C	C			D	D	D	D	D	D
0.027µF (273)	C	C			G	G	D	D	D	D
0.033µF (333)	C	C			G	G	D	D	D	D
0.039µF (393)	C	C			G	G	D	D	D	D
0.047µF (473)	D	D			K	K	D	D	D	D
0.056µF (563)	D	D			G	G	D	D	K	K
0.068µF (683)	G	G			K	K	D	D	K	K
0.082µF (823)	G	G			K	K	D	D	K	K
0.10µF (104)	G	G			K	K	D	D	K	K
0.12µF (124)	G	G	M	M	M	M	D	D	M	M
0.15µF (154)	M	M	M	M	M	M	K	K	M	M
0.18µF (184)	M	M	M	M			K	K	M	M
0.22µF (224)	M	M	M	M			K	K	M	M
0.27µF (274)	M	M	M	M			K	K	M	
0.33µF (334)	M	M	M	M			K	K	M	
0.39µF (394)	M	M					K	K	M	
0.47µF (474)	M	M					K	K	M	
0.56µF (564)	M	M					M	M		
0.68µF (684)	M	M					M	M		
0.84µF (844)							M	M		
1.0µF (105)							M	M		

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>Visual and Mechanical</td><td>-</td><td>* No remarkable defect.
* Dimensions to conform to individual spec. sheet.</td></tr>
<tr><td>Capacitance</td><td rowspan="2">Class I: C0G (NP0)
≦1000pF, 1.0±0.2Vrms, 1MHz±10%
＞1000pF, 1.0±0.2Vrms,1KHz±10%
Class II: (X7R,Y5V)
1.0±0.2Vrms, 1KHz±10%</td><td>* Shall not exceed the limits given in the detailed spec.</td></tr>
<tr><td>Q/D.F (Dissipation Factor)</td><td>NP0: Cap≧30pF, Q≧1000;
Cap<30pF,Q≧400+20C
X7R: ≦2.5% ; Y5V: ≦5.0%</td></tr>
<tr><td>Dielectric Strength</td><td>* To apply voltage:
100V =2.5 times of UR; 200V/250V =2 times of UR
500V/630V =1.5 times of UR ; * Duration: 1 to 5 sec.</td><td>* No evidence of damage or flash over during test.</td></tr>
<tr><td>Insulation Resistance</td><td>UR=100V: To apply voltage at UR for max. 120 sec.
UR>100V:To apply voltage at UR (500V max.) for 60 sec .</td><td>≥10GΩ or RxC≥100Ω-F whichever is smaller.</td></tr>
<tr><td>Temperature Coefficient</td><td>With no electrical load @Oprtating Temp. Range
<table>
<tr><th>T.C</th><th>Temp. (°C)</th></tr>
<tr><td>NP0(C0G)</td><td>-55~125 at 25</td></tr>
<tr><td>X7R</td><td>-55~125 at 25</td></tr>
<tr><td>Y5V</td><td>-25~ 85 at 25</td></tr>
</table></td><td>
<table>
<tr><th>T.C</th><th>Capacitance Change</th></tr>
<tr><td>NP0 (C0G)</td><td>Within ±30ppm/℃</td></tr>
<tr><td>X7R</td><td>Within ±15%</td></tr>
<tr><td>Y5V</td><td>Within +30%/-80%</td></tr>
</table></td></tr>
<tr><td>Adhesive Strength of Termination</td><td>* Capacitors mounted on a substrate. A force of 5N(≤ 0603) or 10N(> 0603) applied perpendicular to the place of substrate and parallel the line joining the center of terminations for 10±1 second.

</td><td>* No remarkable damage or removal of the terminations.</td></tr>
</table>

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

Item	Test Condition	Requirements
Vibration Resistance	Vibration frequency: 10~55 Hz/min. * Total amplitude: 1.5mm * Test time: 6 hrs. (Two hrs each in three * mutually perpendicular directions.)	* No remarkable damage. * Cap change and Q/D.F.: To meet initial spec.
Resistance to Flexure of Substrate	* The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1mm per second until the deflection becomes 1mm. 	* No remarkable damage. * Cap change: C0G(NPO): within ±5.0% or ±0.5pF whichever is larger. X7R: within ±12.5% Y5V: within ±30% (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test.)
Resistance to Soldering Heat	* Solder temperature: 260±5° C * Dipping time: 10±1 sec * Preheating: 120 to 150° C for 1 minute before immerse the capacitor in a eutectic solder. * Before initial measurement (Class II only): To apply de-aging at 150° C for 1hr then set for 24±2 hrs at room temp. * Measurement to be made after de-aging at 150° C for 1hr then set for 24±2 hrs at room	* No remarkable damage. * Cap change: NP0: within ±2.5% or 0.25pF whichever is larger X7R: within ±7.5%; Y5V: within ±20% * Q/D.F, C0G(NPO) / X7R / Y5V : ≤ 1.0 × initial requirements. * 25% max. leaching on each edge.

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>Resistance to Soldering Heat</td><td>* Solder temperature: 260±5° C
* Dipping time: 10±1 sec
* Preheating: 120 to 150° C for 1 minute before immerse the capacitor in a eutectic solder.
* Before initial measurement (Class II only): To apply de-aging at 150° C for 1hr then set for 24±2 hrs at room temp.
* Measurement to be made after de-aging at 150° C for 1hr then set for 24±2 hrs at room</td><td>* No remarkable damage.
* Cap change:
NP0: within ±2.5% or 0.25pF whichever is larger
X7R: within ±7.5%;
Y5V: within ±20%
* Q/D.F,
C0G(NPO) / X7R / Y5V : ≤ 1.0 × initial requirements.
* 25% max. leaching on each edge.</td></tr>
<tr><td>Temperature Cycle</td><td>*Conduct the five cycles according to the temperatures and time.
<table>
<tr><th>Step</th><th>Temp. (°C)</th><th>Time(min)</th></tr>
<tr><td>1</td><td>Min. operating temp.+0/-3</td><td>30±3</td></tr>
<tr><td>2</td><td>Room temp.</td><td>2~3</td></tr>
<tr><td>3</td><td>Max. operating temp.+3/-0</td><td>30±3</td></tr>
<tr><td>4</td><td>Room temp.</td><td>2~3</td></tr>
</table>
* Before initial measurement (Class II only): Perform 150+0/-10° C for 1 hr and then set for 48±4 hrs at room temp.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
* Cap change：
NP0: within ±2.5% or 0.25pF whichever is larger
X7R: within ±7.5%
Y5V: within ±20%
* Q/D.F.,
C0G(NPO) / X7R / Y5V : ≤ 1.0 × Initial requirement
* I.R. ≥ 0.25 × initial requirements.</td></tr>
<tr><td>Solder ability</td><td>* Solder temperature: 235±5° C
* Dipping time: 2±0.5 sec.</td><td>95% min. coverage of all metalized area</td></tr>
</table>

RELIABILITY TEST CONDITIONS AND REQUIREMENTS

<table>
<tr><th>Item</th><th>Test Condition</th><th>Requirements</th></tr>
<tr><td>High Temperature Load (Endurance)</td><td>Test temp.:
C0G(NPO), X7R: 125±3° C :; Y5V: 85±3° C
* To apply voltage:
(1) UR≤ 250V: 200% of rated voltage.
Exception item
<table>
<tr><th>UR</th><th>Size</th><th>Cap</th><th>Voltage</th></tr>
<tr><td rowspan="2">100V</td><td>0805</td><td>≥ 124</td><td rowspan="3">1.5 times of UR</td></tr>
<tr><td>1206/1210</td><td>≥ 105</td></tr>
<tr><td rowspan="2">200V and 250V</td><td>1210</td><td>> 224</td></tr>
<tr><td>1812</td><td>> 474</td></tr>
</table>
(2) 250 < UR ≤500V: 150% of rated voltage.
(3) UR > 500V: 120% of rated voltage.
(4) 1206,NP0 ≥1.5pF: 100% of rated voltage.
* Test temp.: 40±2° C
* Humidity: 90~95% RH
* Test time: 1000+24/-0 hrs.
* Measurement to be made after keeping at room temp. for 24±2 hrs (Class I) or 48±4 hrs (Class II).</td><td>* No remarkable damage.
* Cap change:
C0G(NPO) : within ±3% or ±0.3pF whichever is larger
X7R : within ±12.5%
Y5V : within ±30%
* Q/D.F Value:
C0G(NPO): Cap≥30pF :Q≥350;
10pF≤Cap<30pF :Q≥275+2.5C;
Cap<10pF :Q≥200+10C
X7R: ≤3.0%
Y5V: ≤7.5%
• I.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.</td></tr>
<tr><td>Resistance to Soldering Heat</td><td>* Solder temperature: 260±5° C
* Dipping time: 10±1 sec
* Preheating: 120 to 150° C for 1 minute before immerse the capacitor in a eutectic solder.
* Before initial measurement (Class II only): To apply de-aging at 150° C for 1hr then set for 24±2 hrs at room temp.
* Measurement to be made after de-aging at 150° C for 1hr then set for 24±2 hrs at room</td><td>* No remarkable damage.
* Cap change:
NP0: within ±2.5% or 0.25pF whichever is larger
X7R: within ±7.5%;
Y5V: within ±20%
* Q/D.F,
C0G(NPO) / X7R / Y5V : ≤ 1.0 × initial requirements.
* 25% max. leaching on each edge.</td></tr>
</table>

RECOMMENDED PROFILE CONDITIONS

PREHEAT:

In order to minimize the risk of thermal shock during soldering, a carefully controlled preheat is required. The rate of preheat should not exceed 4℃ per second and the final preheat temperature should be within 100℃ of the soldering temperature for small chips such as 0603, 0805 and 1206, within 50℃ of the soldering temperature for bigger chips such as 1210 and 1812, etc

SOLDERING

(1) Use middy activated rosin RA and RMA fluxes do not use activated flux. The amount of solder in each solder joint should be controlled to prevent the damage of chip capacitors caused by the stress between solder, chips, and substrate.

(2) Hand soldering with temperature-controlled iron not exceeding 30 watts and diameter of tip less than 1.2 mm is recommended, tip of iron should not contact the ceramic body directly, and the temperature of iron should be set to not more than 260℃.

(3) For bigger chips such as 1210 and 1812, etc. wave soldering and hand soldering are no recommended.

(4) Refer IPC/JEDEC J-STD-020D Method recommended soldering profiles :

Reflow not sooner than 15 minutes and not longer than 4 hrs after removal from the temperature/humidity chamber, subject the sample to 3 cycle of the appropriate reflow conditions as defined as blow Table description.

(5) Lead-free : Soldering temperature = 235 to 260℃, depending on product.

(6) Maximum temperature = Minimum temperature (235℃)+ΔT+ Tolerance for oven process and measurement (5 ~ 7℃)

(7) Time at peak temperature = 10sec, Dwell above 217℃ = 90sec, Ramping rate = 3℃/sec(heating) and 6 ℃/sec (heating).

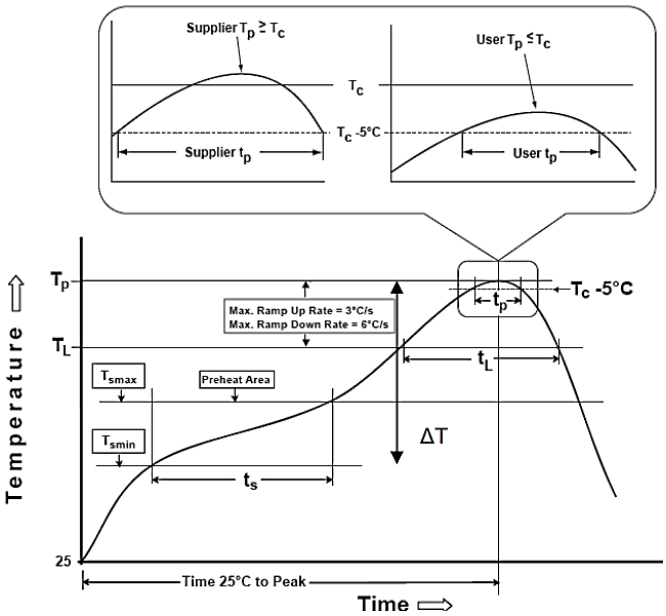
COOLING

After soldering, cool the chips and the substrate gradually to room temperature. Natural cooling in air is recommended to minimize stress in the solder joint. A cooling rate not exceeding 4℃ per second should be used when forced cooling is necessary.

CLEANING

All flux residues must be removed by using suitable electronic-grade vapor-cleaning solvents to eliminate contamination that could cause electrolytic surface corrosion. Good results can be obtained by using ultrasonic cleaning of the solvent. The choice of the proper system is depends upon many factors such as component mix, flux, and solder paste and assembly method. The ability of the cleaning system to remove flux residues and contamination from under the chips is very important.

RECOMMENDED PROFILE CONDITIONS



Chip Size	ΔT
0603, 0805, 1206	100 ℃
1210, 1812	50 ℃

Soldering	Solder Temp.(Tc)	Soldering Time (tp)
Reflow	235 – 260 ℃	< 15 sec.
Wave	230 – 260 ℃	< 5 sec.

Profile Feature		Pb-Free Assembly
Preheat /Soak	Temperature Min.(Tsmin)	150℃
	Temperature Max.(Tsmax)	200℃
	Time(ts) from (Tsmin~Tsmax)	60 to 120 seconds
Ramp-up rate(TL to Tp)		3 ℃/second max.
Liquidous temperature(TL)		217℃
Time(tL) maintained above TL		60 to 150 seconds
Peak package body temperature(Tp)		For user Tp must not exceed the Classification temp 260℃ For suppliers Tp must equal or exceed the Classification temp 260℃
Time(Tp)* within 5 of the specified ℃ classification temperature(Tc)		30* second
Ramp-down rate (Tp to TL)		6 /second max.
Time 25 to peak temperature 260 ℃ ℃		8 minutes max.

Note: For example, Tc is 260℃ and time tp is 15sec. for user: The peak temperature must not exceed 260℃. The time above 255℃ must not exceed 15 seconds.

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

PACKAGING STYLE AND QUANTITY

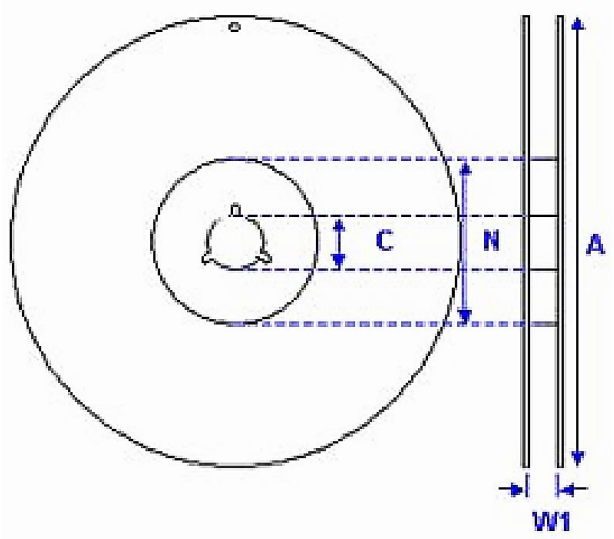
Size	Thickness (Symbol)		Paper Tape		Plastic Tape	
			7" Reel	13" Reel	7" Reel	13" Reel
0603 (1608)	0.50±0.10	N	4,000			
	0.80±0.07	S	4,000	15,000		
	0.80+0.15/-0.10	X	4,000	15,000		
0805 (2012)	0.50±0.10	N	4,000	15,000		
	0.60±0.10	A	4,000	15,000		
	0.85±0.15	B	4,000	15,000		
	0.85±0.10	T	4,000	15,000		
	1.25±0.15	C			3,000	10,000
1206 (3216)	0.85±0.15	B	4,000	15,000		
	0.85±0.10	T	4,000	15,000		
	0.95±0.10	I			3,000	10,000
	1.15±0.15	J			3,000	10,000
	1.25±0.15	C			3,000	10,000
	1.60±0.15	D			2,000	10,000
	1.60+0.30/-0.10	P			2,000	9,000
1210 (3225)	0.85±0.10	T			3,000	10,000
	0.95±0.10	I			3,000	10,000
	1.25±0.15	C			3,000	10,000
	1.60±0.15	D			2,000	
	2.00±0.20	K			1,000	6,000
	2.50±0.30	M			1,000	6,000

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

PACKAGING STYLE AND QUANTITY

Size	Thickness (Symbol) (mm)		Paper Tape		Plastic Tape	
			Pcs/7" Reel	pcs/13" Reel	Pcs/7" Reel	Pcs/13" Reel
1812 (4532)	1.25±0.15	C			1,000	5,000
	1.60±0.15	D			1,000	
	2.00±0.20	K			1,000	
	2.50±0.30	M			500	3,000
	2.80±0.30	U			500	

REEL DIMENSION (Unit: mm)

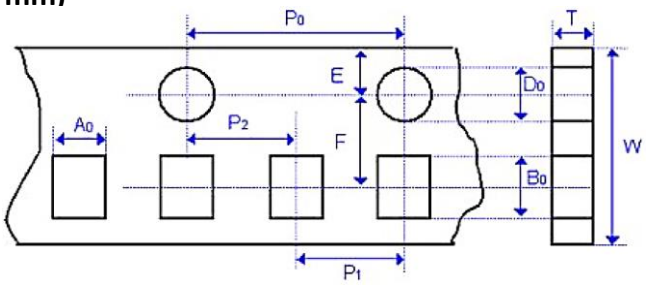


Size Code	0603, 0805, 1206, 1210			1812
Reel Size	7"	10"	13"	7"
C	13.0+0.5/-0.2	13.0+0.5/-0.2	13.0+0.5/-0.2	13.0+0.5/-0.2
W 1	8.4+1.5/0	8.4+1.5/-0	8.4+1.5/-0	12.4+2.0/-0
A	178.0±0.10	250.0±1.0	330.0±1.0	178.0±0.10
N	60.0+1.0/-0	100.0±1.0	100±1.0	60.0+1.0/-0

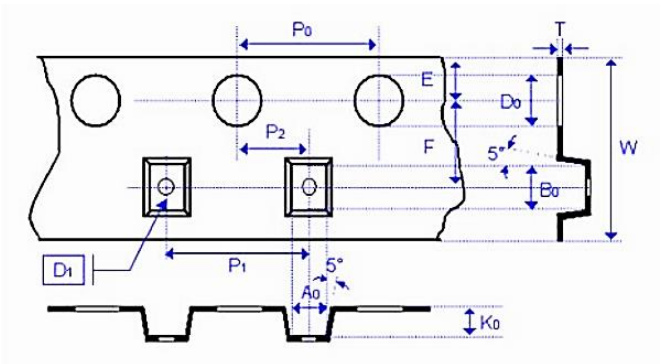
MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

TAPE DIMENSION (Unit: mm)

Paper Tape



Plastic Tape



Size	0603	0805		
Thickness	S, B, X	A, H	B, X	C
A0	1.05 +/-0.30	1.5+/-0.20	1.5 +/-0.20	< 1.80
B0	1.80 +/-0.30	2.30 +/-0.20	2.30 +/-0.20	< 2.70
T	≦1.20	≦1.15	≦1.20	0.23 +/-0.1
K0	-	-	-	< 2.50
W	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30
P0	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10
10xP0	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20
P1	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10
P2	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05
D0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0
D1	-	-	-	1.00 +/-0.10
E	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10
F	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05

MULTILAYER CERAMIC CHIP CAPACITORS 1210 SERIES

TAPE DIMENSION (Unit: mm)

Size	1206			1210		
Thickness	B	I, C,	D,	B	I, C, D, K	M
A0	1.90 +/-0.50	< 2.00	< 2.30	< 3.05	< 3.05	< 3.20
B0	3.50 +/-0.50	< 3.70	< 4.00	< 3.80	< 3.80	< 4.00
T	≦1.20	0.23 +/-0.1	0.23 +/-0.1	0.23 +/-0.1	0.23 +/-0.1	0.23 +/-0.1
K0	-	< 2.50	< 2.50	< 1.50	< 2.50	< 3.20
W	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30	8.00 +/-0.30
P0	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10
10xP0	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20	40.0 +/-0.20
P1	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10	4.00 +/-0.10
P2	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05	2.00 +/-0.05
D0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0	1.50 +0.1/-0
D1	-	1.00 +/-0.10	1.00 +/-0.10	1.00 +/-0.10	1.00 +/-0.10	1.00 +/-0.10
E	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10	1.75 +/-0.10
F	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05	3.50 +/-0.05

Size	1812	
Thickness	C, D, K	M
A0	< 3.90	< 3.90
B0	< 5.30	< 5.30
T	0.25 +/-0.1	0.25 +/-0.1
K0	< 2.50	< 3.50
W	12.00 +/-0.30	12.00 +/-0.30
P0	4.00 +/-0.10	4.00 +/-0.10
10xP0	40.0 +/-0.20	40.0 +/-0.20
P1	8.00 +/-0.10	8.00 +/-0.10
P2	2.00 +/-0.10	2.00 +/-0.10
D0	1.50 +0.1/-0	1.50 +0.1/-0
D1	1.50 +/-0.10	1.50 +/-0.10
E	1.75 +/-0.10	1.75 +/-0.10
F	5.50 +/-0.10	5.50 +/-0.10

STORAGE AND HANDLING CONDITIONS

(1) To store products at 5 to 40℃ ambient temperature and 20 to 70%. related humidity conditions.

(2) No harmful gases containing sulfuric acid, ammonia, hydrogen sulfide or chlorine. Packaging should not be opened until the capacitors are required for use. If opened, the pack should be re-sealed as soon as is practicable. Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesion performance. The capacitors should be used within one year and checked the solderability before use.

(3) Don't open the tape until the parts are to be used, use the chips within 3 months after the tape is opened.

(4) For product of high dielectric constant (Class2 & 3, characteristics B/W & Y), the Electro static capacity changes with the passage of time due to the inherent characteristics of ceramic dielectric materials. The changed capacity reverts to nominal at the temperature it reaches during the soldering process.

(5) HANDLING : Chip capacitors are dense, hard, brittle, and abrasive materials. They are liable to suffer mechanical damage, in the form of cracks or chips. Chip Capacitors should be handled with care to avoid contamination or damage. To use vacuum or plastic tweezers to pick up or plastic tweezers is recommended for manual placement. Tape and reeled packages are suitable for automatic pick and placement machine.

CAUTIONS

(1) The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solder ability. Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)

(2) In corrosive atmosphere, solder ability might be degraded, and silver migration might occur to cause low reliability.

(3) Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sun light, the solder ability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

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