MPQ4228-C

3A, 36V, Step-Down Converter with USB Charging Port Supporting CDP and Type-C 5V @ 3A DFP Mode, AEC-Q100 Qualified

DESCRIPTION

The MPQ4228-C integrates a monolithic, step-down switch-mode converter with a single USB current-limit switch, as well as a Type-C 5V @ 3A mode configuration channel for USB ports. It achieves 3A of output current across a wide input supply range, with excellent load and line regulation.

The USB switch's output is current-limited. The USB port supports charging downstream port (CDP) schemes. The USB port also supports USB Type-C 5V @ 3A DFP mode.

Fault condition protections include hiccup current limiting, output over-voltage protection (OVP), DP/DM/CC1/CC2 short-to-battery protection, and thermal shutdown (TSD).

The MPQ4228-C requires a minimal number of readily available, standard external components, and is available in a QFN-22 (4mmx4mm) package.

FEATURES

- Supports BC1.2 CDP Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- USB_OUT, DP/DM, CC1/CC2 Pins Short-to-Battery Protection
- Wide 4.2V to 36V Continuous Operating Input Range
- Passes Apple MFI R33 Certification Test
- Passes USB-IF Type-C Certification Test
- Selectable Switching Frequency (420kHz and 2.2MHz with Spread Spectrum)
- Integrated High Bandwidth USB2.0 Data Switch with OVP
- Adjustable Line Drop Compensation
- Accurate 3.55A and 2.85A USB Current Limit
- Integrated 20mΩ Low $R_{DS(ON)}$ USB Switch
- 145°C Internal Load-Shedding Entry Temperature
- EN Shutdown Discharge Function
- Fault Indication for OCP, OVP, and OTP
- Frequency Synchronization from 200kHz to 2.2MHz
- Hiccup Current Limit for both Buck and USB
- OVP for USB Switch
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating for CC1 and CC2 Pins
- ±8kV IEC 61000-4-2 Contact Discharge ESD Rating with External Small ESD Diodes on DP and DM Pins
- ±15kV IEC 61000-4-2 Air Discharge ESD Rating for DP, DM, CC1, and CC2 Pins
- Available in a QFN-22 (4mmx4mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

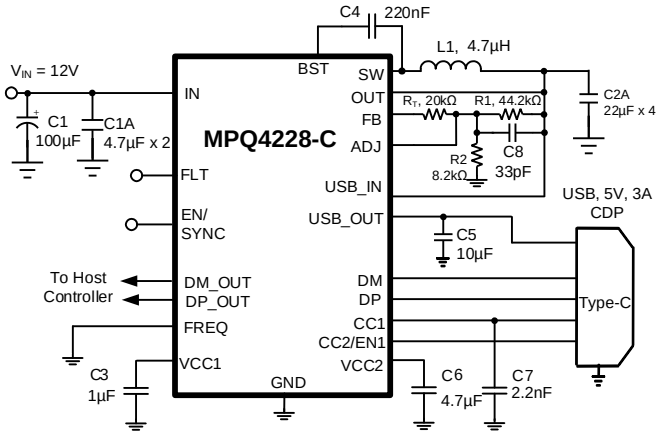
APPLICATIONS

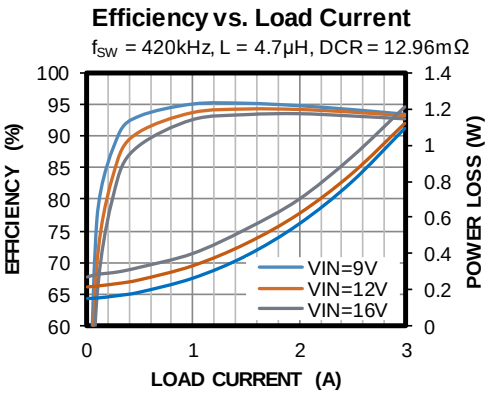
- USB Charging Downstream Ports (CDP)
- USB Type-C DFP Ports
- USB Hubs

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ4228GRE-C-AEC1	QFN-22 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MPQ4228GRE-C-AEC1–Z).

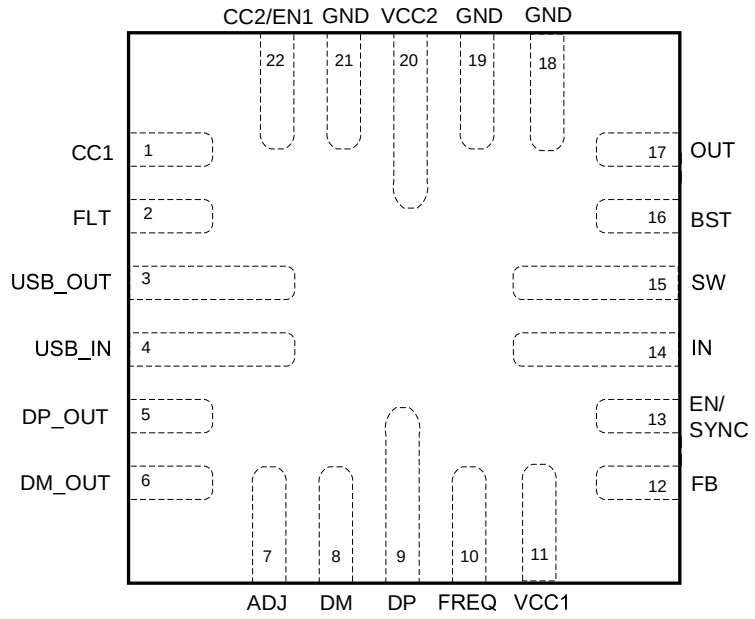
TOP MARKING

MPSYWW
MP4228
LLLLLL
CE

MP4228: Product code of MPQ4228GRE-C-AEC1
MPS: MPS prefix
Y: Year code
WW: Week code
LLLLLL: Lot number
CE: Product suffix and package code

PACKAGE REFERENCE

TOP VIEW



QFN-22 (4mmx4mm) with Wettable Flanks

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PIN FUNCTIONS

Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 detects connections, and configures the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin.
2	FLT	**Fault indicator.** The FLT pin indicates if the following protections occur: USB over-current protection (OCP) and short-circuit protection (SCP), USB_IN over-voltage protection (OVP), DP/DM/CCx short-to-battery, and thermal shutdown. FLT is an open drain under normal conditions. FLT is pulled low if a fault occurs.
3	USB_OUT	**USB bus voltage output.**
4	USB_IN	**USB bus voltage input.**
5	DP_OUT	**D+ data line to USB host controller.**
6	DM_OUT	**D- data line to USB host controller.**
7	ADJ	**Line drop compensation pin.** ADJ sinks a current from the DC/DC converter's FB pin to ground. The regulates the step-down converter's output voltage.
8	DM	**D- data line to USB connector.** DM is the input/output used to handshake with portable devices.
9	DP	**D+ data line to USB connector.** DP is the input/output used to handshake with portable devices.
10	FREQ	**Frequency select pin.** If FREQ is equal to GND, the device operates at 420kHz with spread spectrum (±10% dithering) in FCCM mode. If FREQ is floating, the device operates at 420kHz with spread spectrum (±10% dithering) in PFM mode. If FREQ is equal to VCC1, the device operates at 2.2MHz with spread spectrum (±10% dithering) in FCCM mode.
11	VCC1	**Internal 5V LDO regulator output.** Decouple VCC1 with a 1µF capacitor.
12	FB	**Feedback.** To set the output voltage, connect FB to the tap of an external resistor divider from the output to GND. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 400mV. This prevents current limit runaway if a short circuit occurs.
13	EN/SYNC	**On/off control input.** The EN pin is internally pulled to ground by a 500kΩ resistor. Apply an external CLK on this pin to synchronize the switching frequency.
14	IN	**Supply voltage.** The MPQ4228-C operates from a 4.2V to 36V input rail. IN requires a capacitor (C1) to decouple the input rail. Connect IN to input capacitor using a wide PCB trace.
15	SW	**Switch output.** Use a wide PCB trace to connect the SW pin to the inductor.
16	BST	**Bootstrap.** Connect a 220nF capacitor between the SW and BST pins to form a floating supply across the high-side switch driver.
17	OUT	**Buck output.** Connect OUT to an external power supply ($5V \leq V_{OUT} \leq 20V$) or connect this pin to the buck's VOUT to reduce power dissipation and increase efficiency. Float OUT or connect OUT to ground if it is not used.
18, 19, 21	GND	**Power ground.**
20	VCC2	**Internal 3.45V LDO regulator output.** Decouple VCC2 with a 4.7µF capacitor.
22	CC2/EN1	**Configuration channel.** CC2 detects connections, and configures the interface across the USB Type-C cables and connectors in Type-C mode. Once a connection is established, CC1 or CC2 is reassigned to provide power to the plug's VCONN pin. When CC1 is connected to ground via a 97.6kΩ resistor, the MPQ4228-C works in Type-A mode. In Type-A mode, this pin functions as EN1. Pull EN1 high to enable the USB switch. Float EN1 or pull it low to disable the USB. Apply a midldle-level voltage (1V to 1.85V) to EN1 to force the chip to enter client mode. The buck output is still operational when EN1 is pulled low.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}, V_{OUT}).....-0.4V to +40V
V_{SW}.....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (+43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{USB_IN, USB_OUT} .....-0.3V to +24V
V_{CC1}, V_{CC2}, V_{DM}, V_{DP} .....-0.3V to +18V
V_{FLT}.....-0.3V to +6.5V
V_{FREQ}, $V_{EN/SYNC}$ .....-0.3V to +5.5V (2)
All other pins .....-0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3) (6)
QFN-22 (4mmx4mm)..... 3.47W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings (4)

Human body model (HBM)
DP/DM/CC1/CC2/USB_OUT to GND …....±8kV
All other pins.....±2kV
Charged device model (CDM)
DP/DM/CC1/CC2/USB_OUT.....±2kV
All other pins.....±750V

Recommended Operating Conditions (5)

Operation input voltage range .....4.2V to 36V
Output voltage rage.....5V (typical)
Output current..... 3A
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-22 (4mmx4mm)		
EVQ4228-C-RE-00B (6)	36	5.... °C/W
JESD51-7 (7)	46	38... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For details on the EN pin's absolute maximum rating, see the EN Control section on page 17.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) -T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM with regard to GND.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on 4-layer PCB, 57.4mmx57.4mm.
7) Measured on JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JESD board. They do not represent the performance obtained in an actual application

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{IN}	V_{EN} = 0V, T_J = 25°C			1	μA
		V_{EN} = 0V, T_J = -40°C to +150°C			8	
Buck supply current (quiescent)	$I_{Q_CL_VBUSDIS}$	CC pin is floating, V_{FB} = 1V		0.75	1.1	mA
Overall supply current (quiescent)	I_Q	CC1 connected to ground with a 5.1kΩ resistor, VFB = 1V		1	1.5	mA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN falling threshold	$V_{EN_FALLING}$		1.05	1.25	1.45	V
EN input current	I_{EN1}	V_{EN} = 2V		4.5	6	μA
	I_{EN2}	V_{EN} = 0		0	0.2	
Thermal shutdown (8)	T_{STD}			165		°C
Thermal hysteresis (8)	T_{STD_HYS}			20		°C
VCC1 regulator	V_{CC1}	I_{CC} = 0mA	4.8	5	5.2	V
VCC1 load regulation	V_{CC1_LOG}	I_{CC} = 5mA		1.5	4	%
VCC2 regulator	V_{CC2}	I_{CC} = 0mA	3.15	3.45	3.75	V
Step-Down Converter						
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO}		3.5	3.7	3.9	V
V_{IN} under-voltage lockout falling threshold	V_{UVLO_FALL}		3.05	3.25	3.45	V
HS switch on resistance	$R_{DS(ON)_HS}$			50	90	mΩ
LS switch on resistance	$R_{DS(ON)_LS}$			30	60	mΩ
Output discharge resistance	R_{DIS}			200		Ω
Feedback voltage	V_{FB}		776	792	808	mV
Feedback current	I_{FB}	V_{FB} = 820mV		10	100	nA
Sync frequency range	f_{SYNC}		0.2		2.4	MHz
Oscillator frequency	f_{SW1}	V_{FB} = 750mV, FREQ is floating	340	420	500	kHz
	f_{SW2} (8)	V_{FB} = 750mV, FREQ = VCC		2.2		MHz
Frequency spread spectrum range	f_{SW3}	FREQ = GND, based on 420kHz		±10		%
	f_{SW4} (8)	FREQ = VCC, based on 2.2MHz		±10		%
Maximum duty cycle	D_{MAX}	Based on 420kHz	94.5	96		%
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V, T_J = -40°C to +150°C			10	
High-side peak current limit	I_{LIMIT1}	T_J = -40°C to +150°C	7	10		A
Low-side valley current limit (8)	I_{LIMIT2}			9		A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-side negative current limit (8)	I_{LSNEG}			-3		A
Minimum on time (8)	t_{ON_MIN}			60		ns
Output over-voltage protection	V_{OVP1}			115		%
Output OVP recovery	V_{OVP1_R}			105		%
Soft-start time	t_{SS}	Output from 10% to 90%		1.5		ms
USB Switch						
Under-voltage lockout rising threshold	V_{USB_UVR}		2.8	3.0	3.2	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			400		mV
EN1 logic high input	V_{EN1_H}	Turn on the USB output	2.2			V
EN1 middle input voltage	V_{EN1_M}	Enter client mode	1		1.85	V
EN1 logic low input	V_{EN1_L}	Turn off the USB switch and data switch			0.4	V
Switch on resistance	$R_{DS(ON)_SW}$			20	40	mΩ
Input discharge resistance	R_{DIS_USB}	Turn on during IN OVP		200		Ω
USB input OVP rising treshold	V_{USB_OV}		5.85	6.05	6.3	V
USB input OVP recovery threshold	$V_{OV_RECOVERY}$		5.5	5.75	6	V
Current limit	I_{LIMIT1}	V_{OUT} drops 10%, Type-C mode, room temperature	3.20	3.55	3.90	A
	I_{LIMIT2}	V_{OUT} drops 10%, Type-A Mode, room temperature	2.55	2.85	3.15	A
USB_OUT soft-start time	t_{USB_SS}	V_{OUT} = 5V, from 10% to 90%		0.45		ms
V_{BUS} enter hiccup hold time	t_{HICP_ON}	V_{OUT} = 5V, OC, hiccup on time		2		ms
Hiccup mode off time	t_{HICP_OFF}	V_{OUT} = 5V, V_{BUS} connected to GND		2		s
DM, DP pins OVP rising	$V_{OV_DM_DP}$		3.75	4	4.25	V
DM, DP pins OVP hysteresis	$V_{OV_DM_DP_HYS}$			100		mV
Line drop compensation gain	G_{ADJ_SINK}	ADJ sink current/I_{OUT} current, I_{OUT} = 3A	-20%	2.05	+20%	uA/A
FLT output low voltage	V_{FLT_L}	I_{SINK} = 1mA			0.15	V
FLT leakage current	I_{FLT_LKG}	6.5V pull-up voltage			1	uA
FLT deglitch time	t_{FLT_DEG}	Over-current condition		2		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +150°C, typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CDP Mode						
DM CDP output voltage	V_{DM_SRC1}	VDP = 0.6V, DM_Sink = 250µA	0.5	0.6	0.7	V
	V_{DM_SRC2}	VDP = 0.6V, DM to GND = 22.5Ω			20	mV
	V_{DM_SRC3}	VDP = 0V			250	mV
DP rising lower window threshold for V_{DM_SRC} EN	V_{DAT_REF}		0.30	0.35	0.4	V
DP rising lower window threshold hysteresis	$V_{DAT_REF_HYS}$			20		mV
DP rising upper window threshold for V_{DM_SRC}	V_{LGC_SRC}		0.8	0.9	1.0	V
DP rising upper window threshold hysteresis	$V_{LGC_SRC_HYS}$			50		mV
V_{DM_SRC} on/off deglitch time	$t_{DM_SRC_DEGH}$			5	20	ms
DP to ground resistance	R_{DP_DOWN}	VDP = 0.6V		18.5		kΩ
DP/DM on resistance	$R_{ON_DP/DM}$	VDP_OUT = DM_OUT = 0V and 2.4V		2		Ω
DP/DM on resistance matching	R_{ON_MAT}			50	150	mΩ
DP to DP_OUT capacitance (8)	C_{DP}	Data switch on, same for DM switch		9		pF
3dB bandwidth of analog data SW (8)	f_{BW}			900		MHz
USB Type-C 5V @ 3A Mode – CC1, CC2						
CC resistor to disable Type-C mode	R_A	CC1 pin, for Type-C mode applications add a 2.2nF capacitor on CC1	95.3	97.6	100	kΩ
CC pull-up current to detect Type-A mode	I_{PLL}		8	10	12	uA
CC voltage to enable VCONN	V_R				0.75	V
CC voltage to enable V_{BUS}	V_{RD}	Room temperature	0.85		2.45	V
CC voltage with 5.1kΩ R_D	V_{CC_RD}	CC pin connected to 5.1kΩ pull-down resistor, room temperature	1.31	1.683	2.04	V
CC detach threshold	V_{OPEN}		2.65			V
CC voltage falling debounce timer	$t_{CC_DEBOUNCE}$	V_{BUS} enable deglitch	100	150	200	ms
CC voltage rising debounce timer	$t_{PD_DEBOUNCE}$	V_{BUS} disable deglitch	0	10	20	ms
V_{CONN} output power	P_{VCONN}	VCONN comes from buck output with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, after output discharge turn-off	72.4			kΩ

Notes:

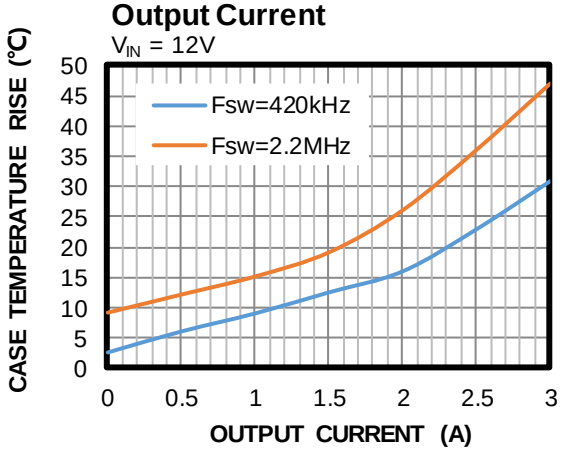
8) Guaranteed by engineering sample characterization.

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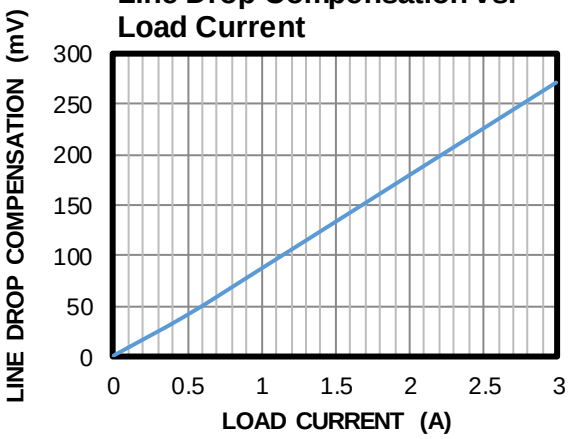
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Case Temperature Rise vs. Output Current

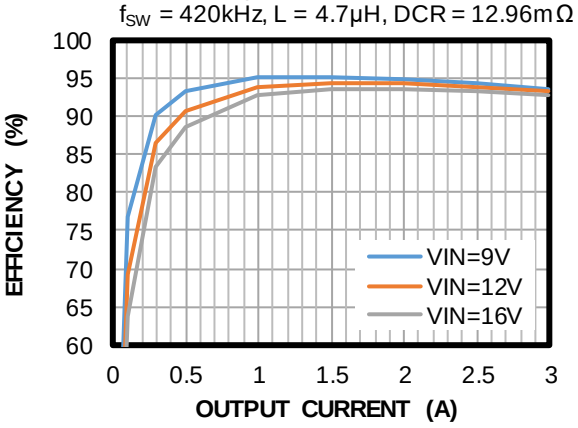


Line Drop Compensation vs. Load Current



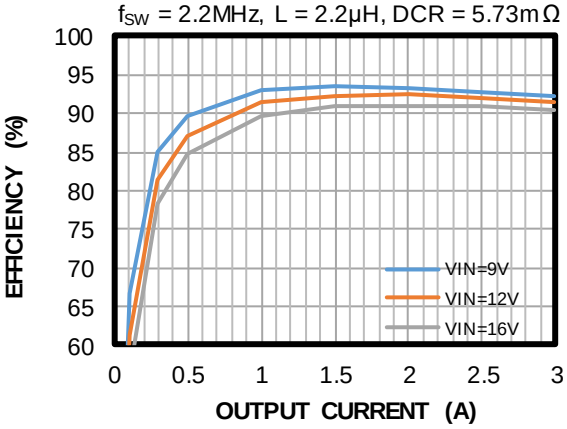
Efficiency vs. Load Current

f_{SW} = 420kHz, L = 4.7µH, DCR = 12.96mΩ



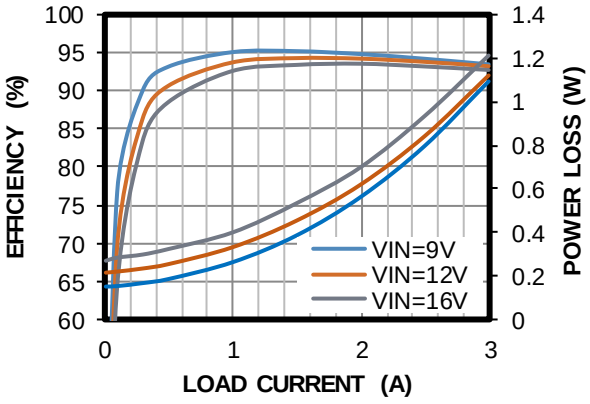
Efficiency vs. Load Current

f_{SW} = 2.2MHz, L = 2.2µH, DCR = 5.73mΩ



Efficiency vs. Load Current

f_{SW} = 420kHz, L = 4.7µH, DCR = 12.96mΩ



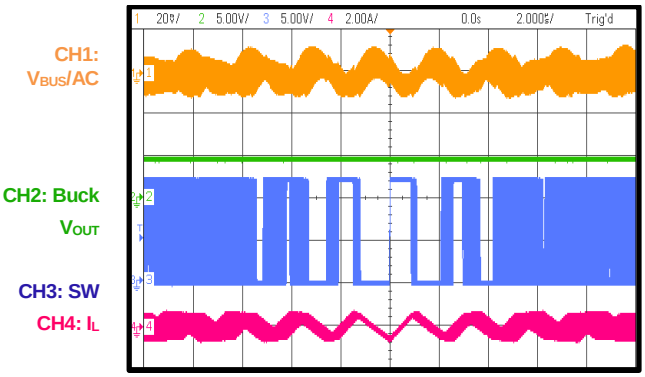
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

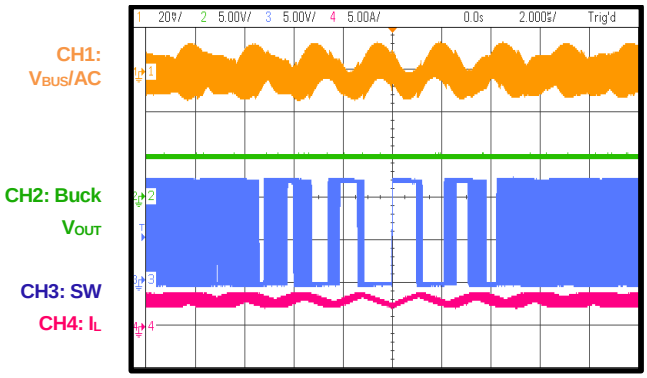
Steady State

Frequency spread spectrum is enabled,
I_{OUT} = 0A



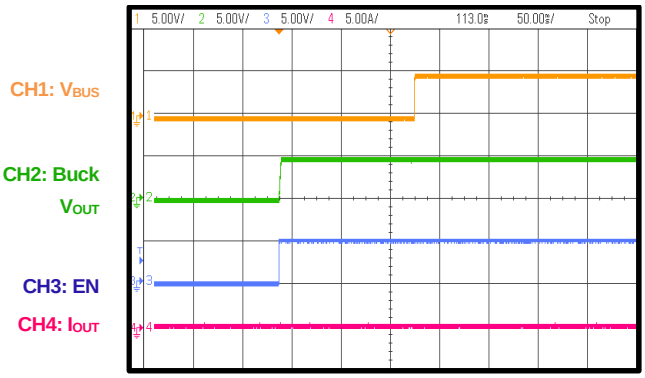
Steady State

Frequency spread spectrum is enabled,
I_{OUT} = 3A



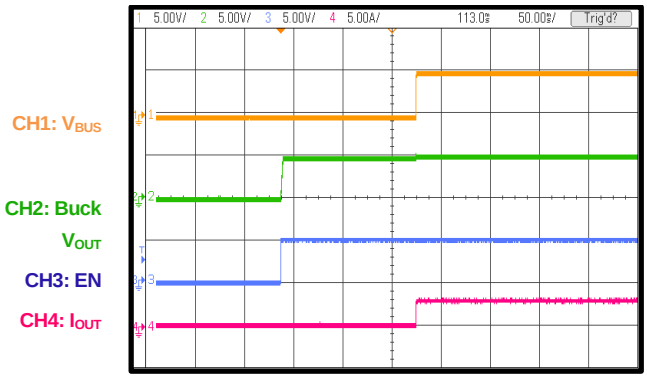
Start-Up through EN

I_{OUT} = 0A



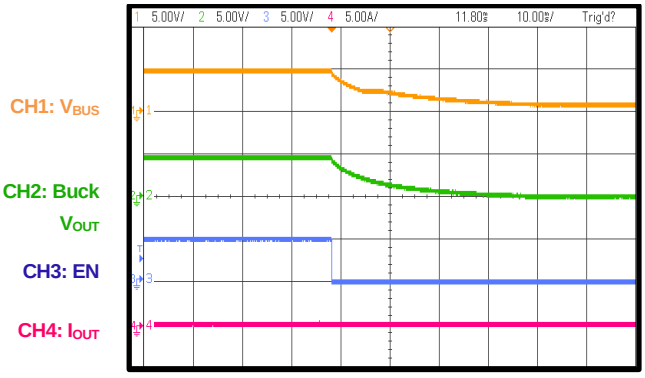
Start-Up through EN

I_{OUT} = 3A



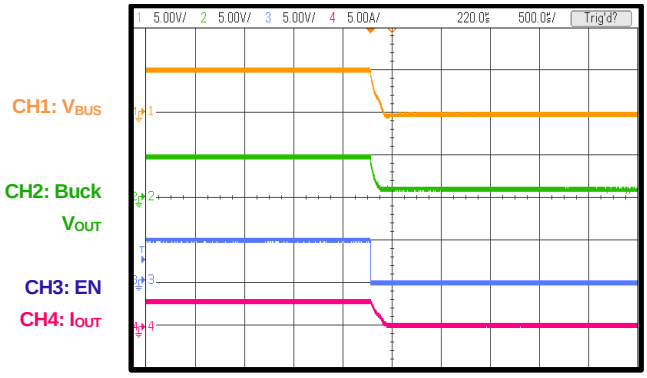
Shutdown through EN

I_{OUT} = 0A



Shutdown through EN

I_{OUT} = 3A

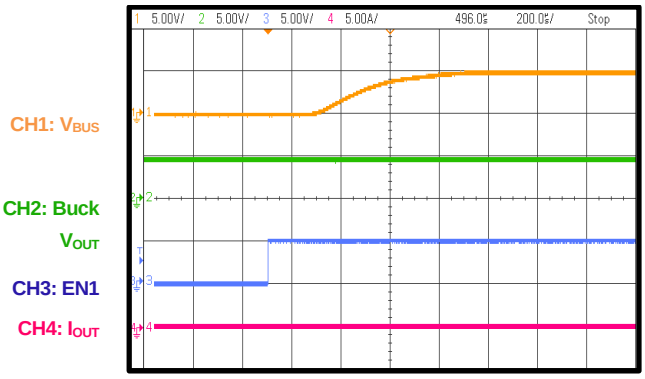


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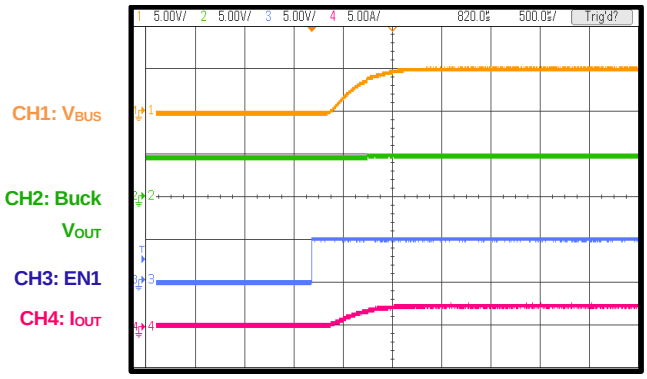
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

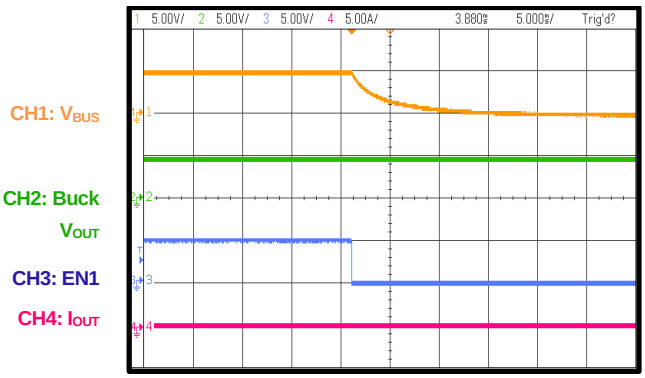
Start-Up through EN1
Type-A mode, I_{OUT} = 0A



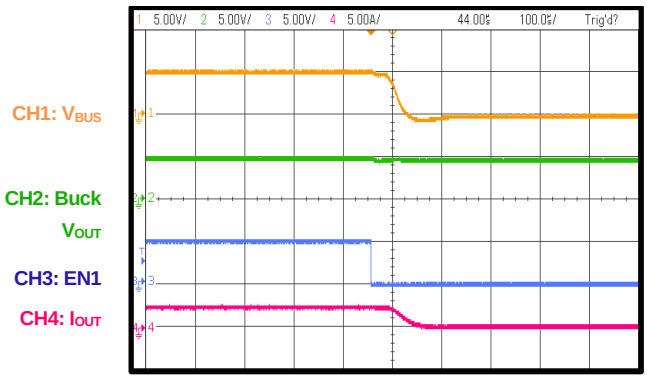
Start-Up through EN1
Type-A mode, I_{OUT} = 2.4A



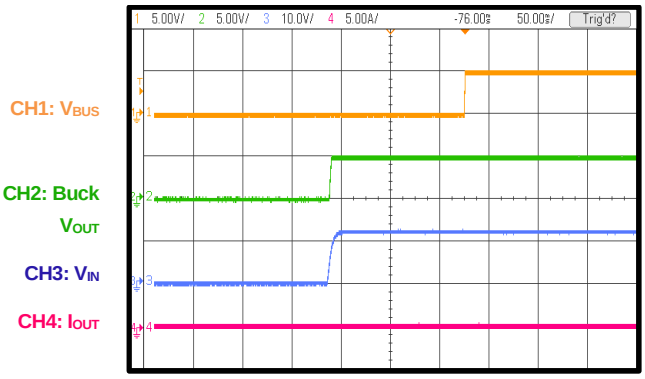
Shutdown through EN1
Type-A mode, I_{OUT} = 0A



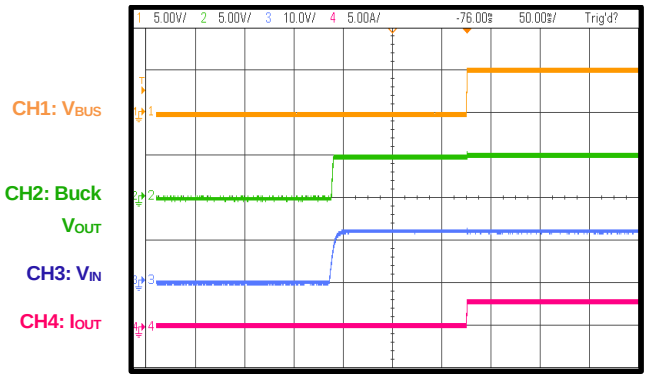
Shutdown through EN1
Type-A mode, I_{OUT} = 2.4A



Start-Up
I_{OUT} = 0A



Start-Up
I_{OUT} = 3A



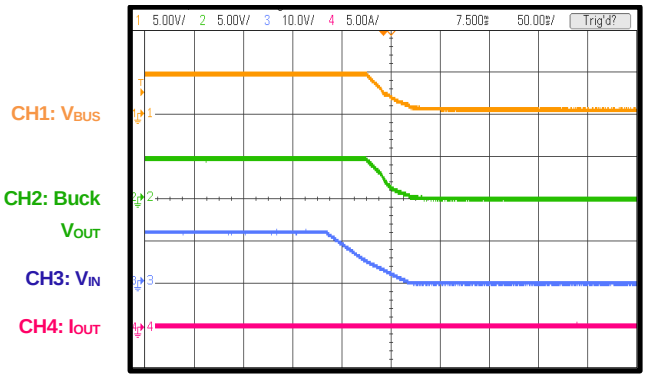
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

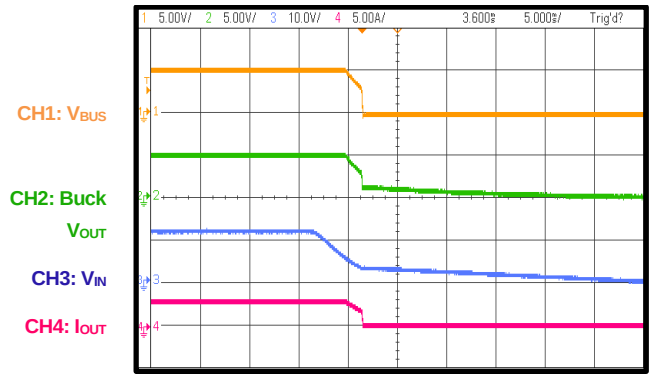
Shutdown

I_{OUT} = 0A



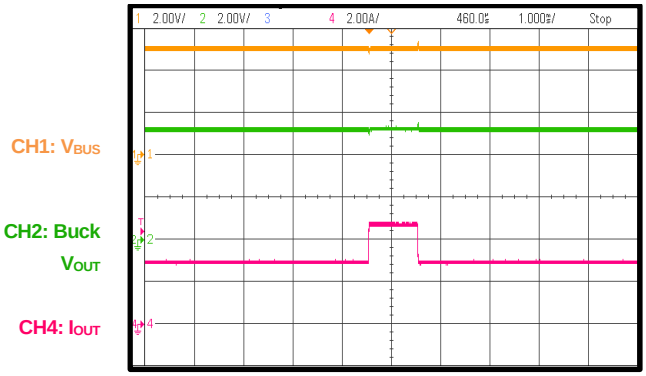
Shutdown

I_{OUT} = 3A



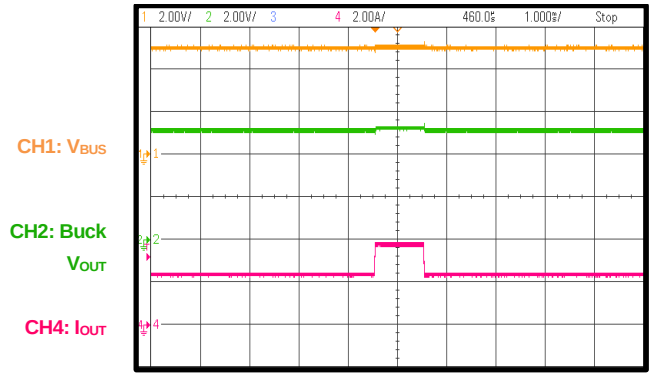
MFI Over-Current Pulse Test

Type-C mode, I_{OUT} = 3A to 4.8A, 1ms hold time



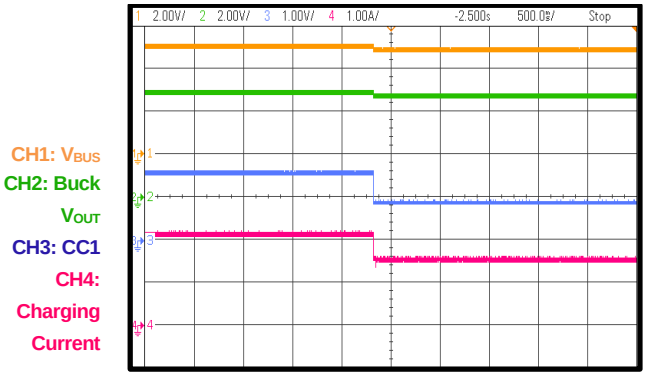
MFI Over-Current Pulse Test

Type-A mode, I_{OUT} = 2.4A to 3.84A, 1ms hold time



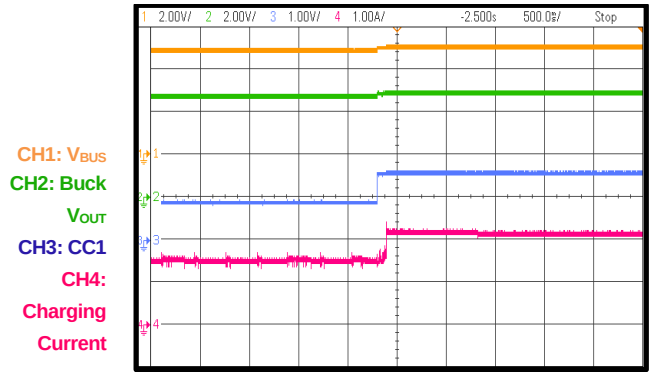
Load Shedding Entry

Connect to mobile phone during testing



Load Shedding Recovery

Connect to mobile phone during testing



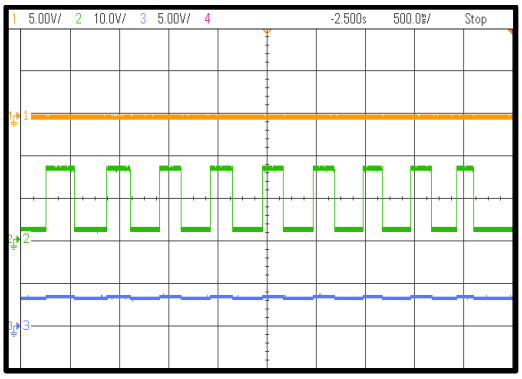
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

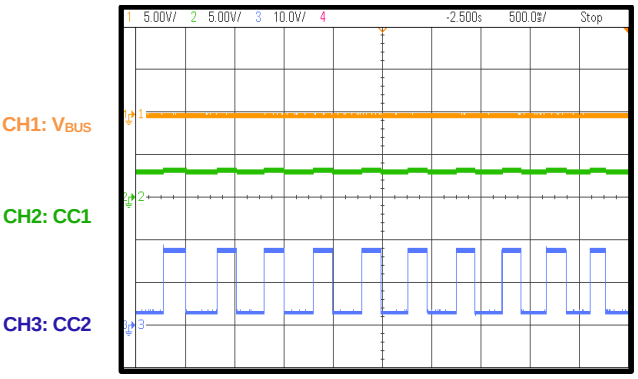
CC1 Short-to-Battery

$V_{BATTERY}$ = 18V, CC1 = CC2 = floating



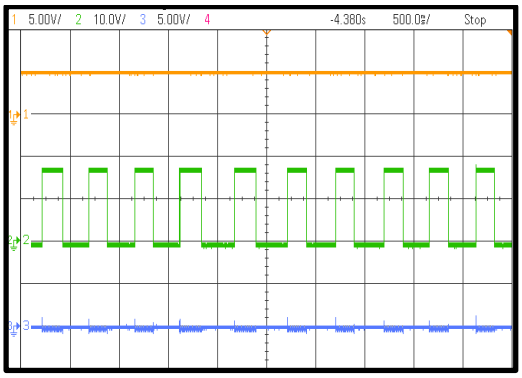
CC2 Short-to-Battery

$V_{BATTERY}$ = 18V, CC1 = CC2 = floating



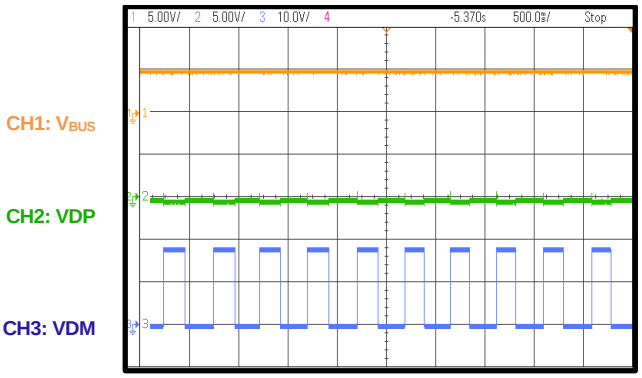
DP Short-to-Battery

$V_{BATTERY}$ = 18V, CC1 connected to ground with a 5.1kΩ resistor



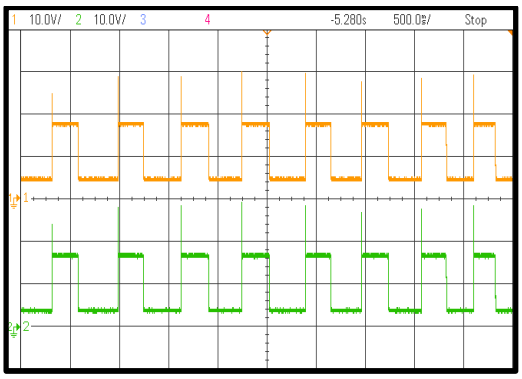
DM Short-to-Battery

$V_{BATTERY}$ = 18V, CC1 connected to ground with a 5.1kΩ resistor



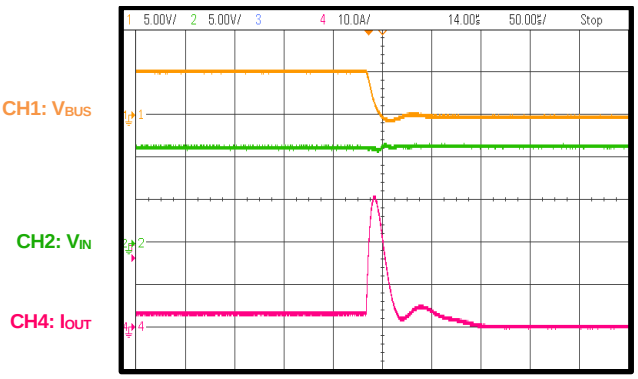
USB-OUT Short-to-Battery

$V_{BATTERY}$ = 18V, CC1 connected to ground with a 5.1kΩ resistor



USB_OUT Short-to-GND Entry

I_{OUT} = 3A

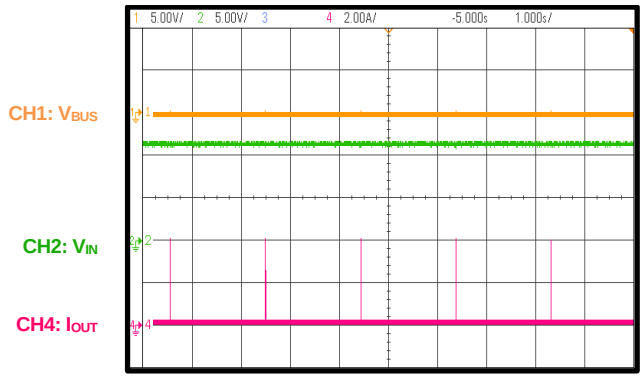


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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

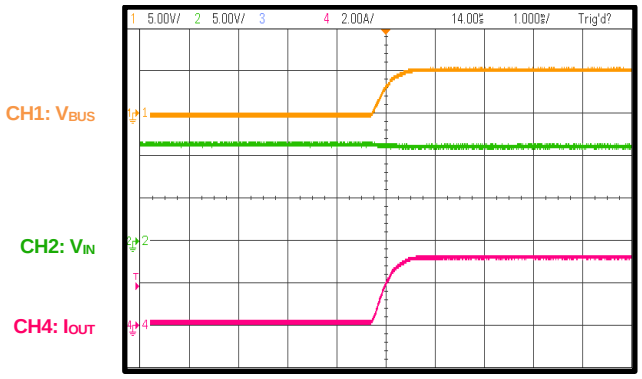
V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

USB_OUT Short-to-GND Steady State



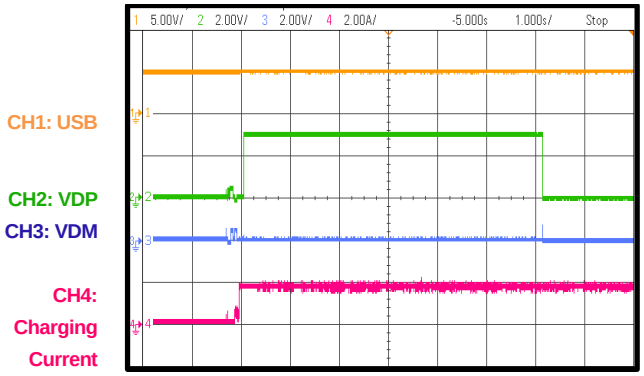
USB_OUT Short-to-GND Recovery

I_{OUT} = 3A



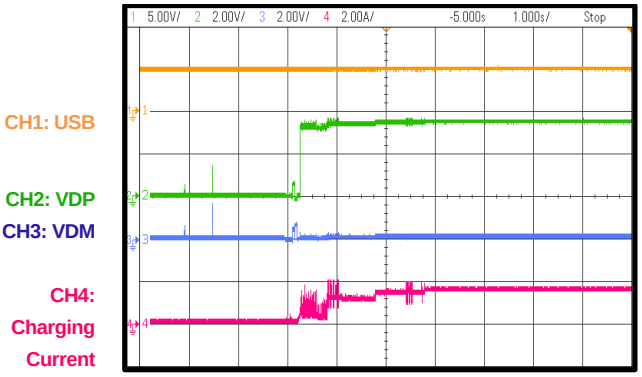
Android Device Charging Test

Mobile phone plugged in



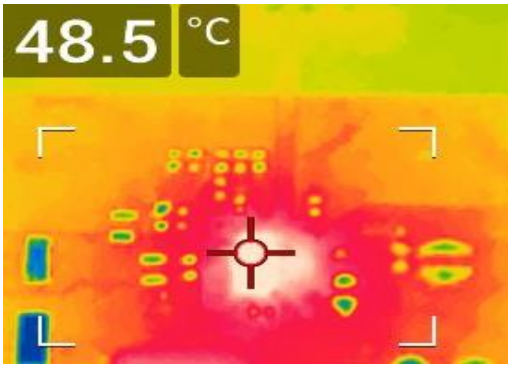
Apple Device Charging Test

Mobile phone plugged in



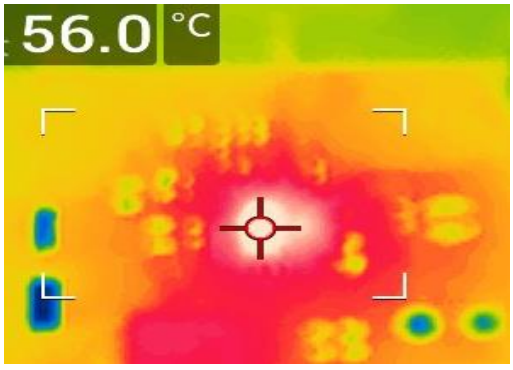
Case Temperature Test

V_{IN} = 12V, USB = 5V, I_{OUT} = 2.4A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, middle layers 1/2: 1oz



Case Temperature Test

V_{IN} = 12V, USB = 5V, I_{OUT} = 3A, measured on 4-layer PCB, 57.4mmx57.4mm, top/bottom layer: 2oz, middle layers 1/2: 1oz



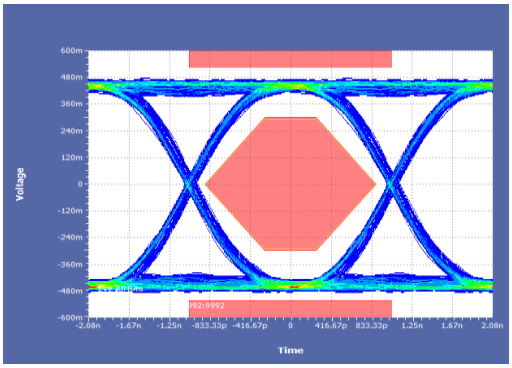
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 420kHz with spread spectrum, CC1 connected to ground with a 5.1kΩ resistor, T_A = 25°C, unless otherwise noted.

Eye Diagram

Measured on EVB with 50cm cable with MPQ4228-C data switch (see Figure 16 on page 27 for more details)



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FUNCTIONAL BLOCK DIAGRAM

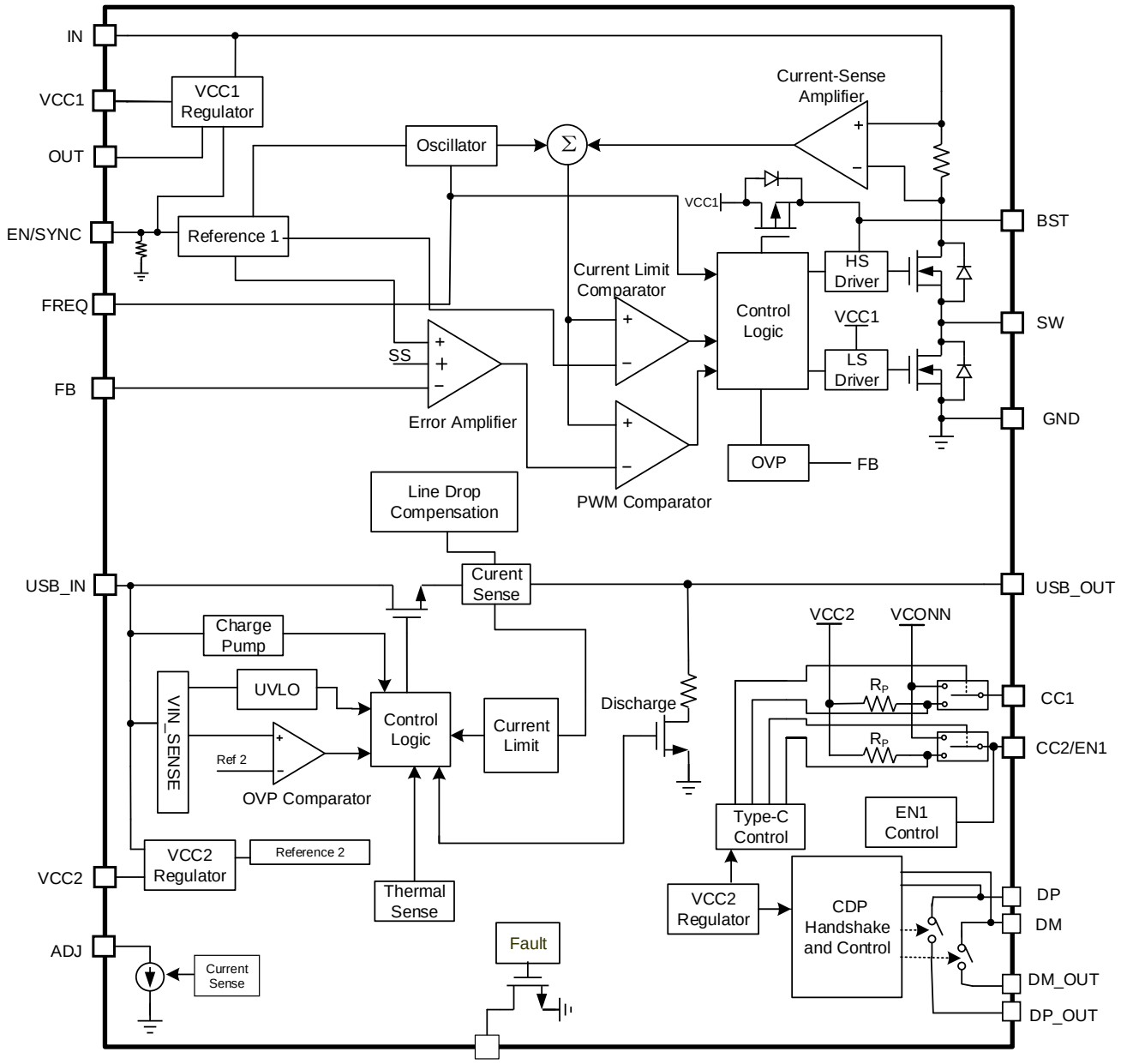


Figure 1: Functional Block Diagram

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OPERATION

BUCK CONVERTER

The MPQ4228-C integrates a monolithic, synchronous, rectified, step-down switch-mode converter with internal power MOSFETs and a USB current-limit switch with charging port auto-detection. It offers a compact solution to achieve 3A of continuous output current across a wide input supply range, with excellent load and line regulation.

The MPQ4228-C operates in fixed-frequency, peak current mode control to regulate the output voltage. The internal clock initiates the PWM cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle begins. If the current value does not reach 96% of the value set by COMP within one PWM period, the power MOSET is forced to turn off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage to the internal 0.792V reference (REF) and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC1 Regulator

The 5V internal regulator powers most of the internal circuitries. This regulator takes either the Buck VOUT or VIN as supply. When VIN exceeds 5V, the output of the regulator is in full regulation. If the VIN is less than 5V, the output decreases with the VIN. When output voltage is established and higher than 4.75V, VCC1 regulator uses VOUT power via OUT pin to save LDO power loss. The VCC1 requires an external 0.22µF-1uF ceramic decouple capacitor.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn the regulator on; drive EN low to turn it off. An internal 500kΩ resistor connected from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip. The EN pin is clamped internally using a 6.5V-series Zener diode (see Figure 2). It is recommended to connect EN to VIN and GND through resistor dividers. When selecting a pull-up resistor, ensure that its resistance can limit the current flowing into EN to below 100µA.

For example, if the EN pull-up resistor is 100kΩ, and the pull-down resistor is 36kΩ, the IC starts up when V_{IN} exceeds 6V.

If the EN pin is directly connected to a voltage source without a pull-up resistor, the voltage amplitude must be limited ≤5.5V to prevent damage to the Zener diode.

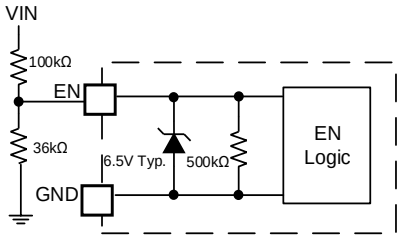


Figure 2: 6.5V-Type Zener Diode

Connect an external clock that ranges between 200kHz and 2.2MHz to EN pin. This synchronizes the internal clock. The MPQ4228-C operates with a fixed frequency without spread spectrum functionality while the external clock is synching. It is recommend to float FREQ when synchronizing the switching frequency to an external clock.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 3.7V, and its falling threshold is 3.25V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates an SS voltage that ramps up from 0V to 5V. When the SS voltage (V_{SS}) is below the reference voltage (V_{REF}), the error amplifier uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the error amplifier uses V_{REF} as the reference.

If the device's output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side

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switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Buck Over-Current Protection (OCP)

The MPQ4228-C has a cycle-by-cycle over-current (OC) limit. If the inductor peak current exceeds the current-limit threshold, and the FB voltage drops below the under-voltage (UV) threshold (typically 50% below the reference), the MPQ4228-C enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short-circuit current, alleviates thermal issues, and protects the regulator. The MPQ4228-C exits hiccup mode once the OC condition is removed.

Over-Voltage Protection (OVP)

The MPQ4228-C detects the output voltage through the FB pin. If the OUT voltage exceeds 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The device stops switching and turns on the discharge resistor connected from OUT to ground until the OUT voltage drops below 105% of the target voltage.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} and VCC through D1, M1, C4, L1, and C2 (see Figure 3). The BST capacitor's C4 voltage is quickly charged by VCC through M1. The 1μA VIN-to-BST current source can also charge the BST capacitor when the low-side switch is not on.

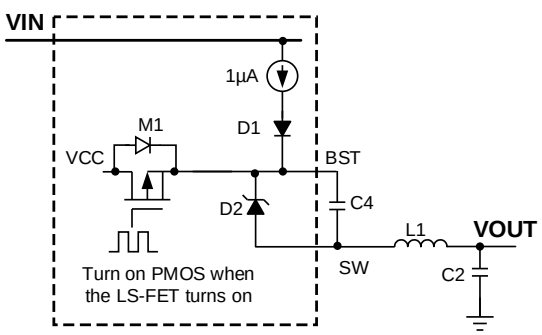


Figure 3: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN going low, VIN going low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Discharge

The MPQ4228-C has an output discharge function that provides a resistive discharge path for the external output capacitor. This function is active when the part is disabled (e.g. the input voltage is under the UVLO threshold or EN goes low). If an over-voltage condition occurs, the discharge path turns off when the OUT pin voltage drops below 0.5V. Then the device waits 200ms for the maximum timer, for UVLO, and for EN to pull low. The discharge path turns on until the OUT voltage drops below 105% of the target voltage.

Switching Frequency

The MPQ4228-C's switching frequency can be adjusted by the FREQ pin. If FREQ is equal to GND, the device operates at 420kHz with spread spectrum (±10% dithering) in FCCM mode. If FREQ is floating, the device operates at 420kHz with spread spectrum (±10% dithering) in PFM mode. If FREQ is equal to VCC1, the device operates at 2.2MHz with spread spectrum (±10% dithering) in FCCM mode (see Table 1).

Table 1: Switching Frequency Selection

FREQ Pin	Operation Mode	Switching Frequency
GND	FCCM with spread spectrum	420kHz
Float	PFM with spread spectrum	420kHz
VCC1	FCCM with spread spectrum	2.2MHz

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Auto-PFM/PWM Operation (FREQ is Floating)

The MPQ4228-C works in continuous conduction mode (CCM) under heavy loads. When the load decreases, the MPQ4228-C enters discontinuous conduction mode (DCM) with a fixed frequency while the inductor current approaches 0A. If the load is further decreased (or there is no load), the inductor peak current drops below the AAM peak current threshold. Then the MPQ4228-C enters pulse-skip mode to further improve light-load efficiency.

Under very light loads or not load, the FB voltage decreases slowly, and COMP ramps up until it reaches V_{AAM}. When the clock goes high, the high-side power MOSFET turns on and remains on until $V_{ILSENSE}$ reaches the value set by the COMP voltage. When $V_{COMP} < V_{AAM}$, the internal clock is blocked, and the device skips some pulses for pulse-frequency modulation (PFM). This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.

As the output current increases from the light-load condition, COMP increases, as well as the switching frequency. If the output current exceeds the critical level set by COMP, the MPQ4228-C resumes fixed-frequency PWM control (see Figure 4).

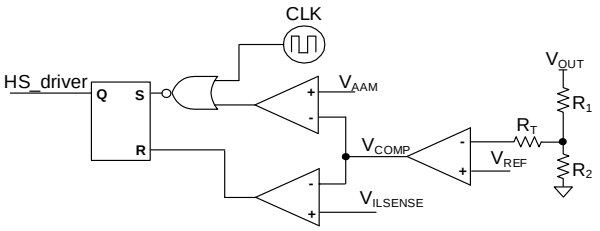


Figure 4: Auto-PFM/PWM Operation Control Logic

Forced CCM Operation (FREQ = GND or VCC1)

The MPQ4228-C works in forced continuous conduction mode (FCCM) continuously. The device operates with a fixed switching frequency, regardless of whether it is operating in light load or full load. The advantage of FCCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charging time. However, FCCM has low efficiency under light loads. A proper inductance should be selected to avoid triggering the low-side switch's negative current limit (typically -3A, from SW to GND). If the negative current limit is triggered, the low-side switch turns off, and the high-side switch turns on when the internal clock begins.

Frequency Spread Spectrum

The purpose of frequency spread spectrum is to minimize the peak emissions at a specific frequency.

The MPQ4228-C uses a 4kHz triangle wave (125µs rising, 125µs falling) to modulate the internal oscillator. The frequency span of the spread spectrum operation is ±10% (see Figure 5).

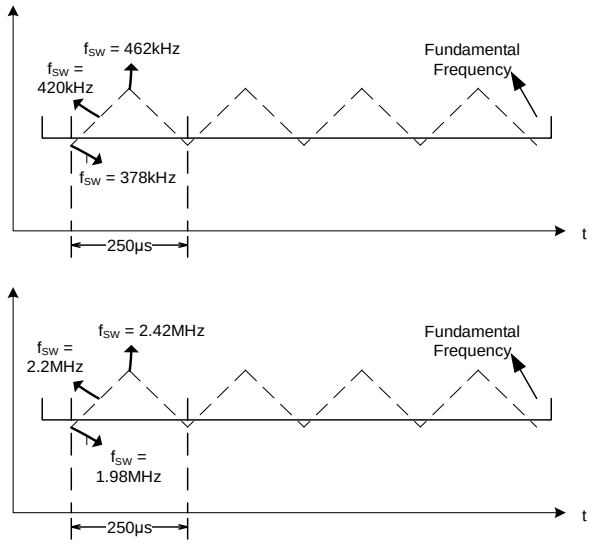


Figure 5: Frequency Spread Spectrum

Float FREQ or connect it to GND for a frequency of 420kHz with frequency spread spectrum. Connect FREQ to VCC for a frequency of 2.2MHz with frequency spread spectrum.

USB CURRENT-LIMIT SWITCH

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. When the input voltage exceeds the USB SW UVLO threshold, the power MOSFET starts to turn on with a controlled slew rate after a fixed delay.

Internal Soft Start

Internal soft start prevents excessive inrush current, and prevents the output voltage from overshooting during start-up.

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Line Drop Compensation

The MPQ4228-C is capable of compensating for an output voltage drop (e.g. high impedance caused by a long trace) to keep a fairly constant 5V load-side voltage. The line drop compensation is accomplished through the ADJ and FB pins (see Figure 6).

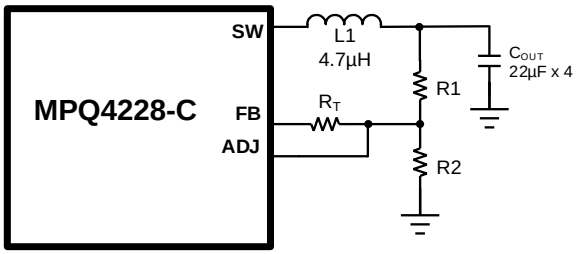


Figure 6: Line Drop Compensation

The MPQ4228-C uses the sensed load current through the internal current-sense MOSFET to sink a current (I_{ADJ}) at ADJ. I_{ADJ} can be calculated with Equation (1):

$$I_{ADJ} = G_{ADJ_SINK} \times I_{USB_LOAD} \quad (1)$$

V_{BUCK_OUT} can be estimated with Equation (2):

$$V_{BUCK_OUT} = \left(\frac{R1}{R2} + 1\right) \times V_{REF} + R1 \times I_{ADJ} \quad (2)$$

This means that the line drop compensation amplitude at certain output current conditions is equal to R1 x G_{ADJ_SINK} x I_{USB_LOAD}. Where G_{ADJ_SINK} is line drop compensate gain (2.05µA/A). The R1 value can also be used to adjust the line drop compensation amplitude.

For example, with a 3A output current, choose R1 to be about 44.2kΩ. This makes the line drop compensation about 272mV. For Type-C mode, the maximum resistance of R1 is 113kΩ (a 22kΩ resistor and 91kΩ resistor in series). When R1 is 113kΩ, the line drop compensation is about 695mV with a 3A output current.

For Type-A mode, the maximum resistance of R1 is 142kΩ (a 51kΩ resistor and 91kΩ resistor in series). When R1 is 142kΩ, the line drop compensation is about 699mV with a 2.4A output current.

USB Input Over-Voltage (OV) and Discharge

An accurate and fast comparator monitors the input for an over-voltage (OV) condition. If the input voltage rises above the threshold, the input-to-ground discharge path is active, and the USB current-limit switch is still enabled. When the input voltage falls below 5.75V, the IC exits OVP.

Output Discharge

When a Type-C device is detached, both the USB_IN and USB_OUT discharge resistors are active for 30ms before turning off. After these resistors turn off, their ground resistance exceeds 72.4kΩ.

Over-Current Protection (OCP)

If the load current reaches the current-limit threshold during normal operation, the device starts a 1.7ms counter. The MPQ4228-C does not limit the output current within this 1.7ms period (see Figure 7).

If the over-current (OC) time exceeds the 1.7ms timer, the USB channel enters hiccup mode with a 2ms on time and a 2s off time. The MPQ4228-C resets the counter if the OC signal disappears during the 1.7ms counter.

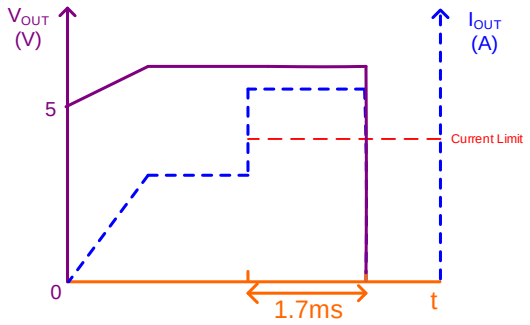


Figure 7: Over-Current Limit

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may exceed the current limit threshold before the control loop can respond. If the current reaches an internal secondary current-limit level (about 10.5A), a fast turn-off circuit activates to turn off the power FET. This limits the peak current through the switch to limit the input voltage drop.

The fast turn-off response time is about 300ns. If the fast turn off works, the power FET stays off for 80µs. After that time period, the power FET turns on again. If the part is still under a short-circuit condition, the MPQ4228-C responds by entering hiccup mode or initiating thermal shutdown. After the short-circuit condition is

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removed, the MPQ4228-C recovers automatically.

Short-to-Battery Protection

The MPQ4228-C provides CC1, CC2, DP, DM, and USB_OUT short-to-battery protections when the IC is enabled and V_{BUS} is on. USB_OUT short-to-battery protection requires parallel a Schottky diode when V_{BUS} is off (see Figure 8).

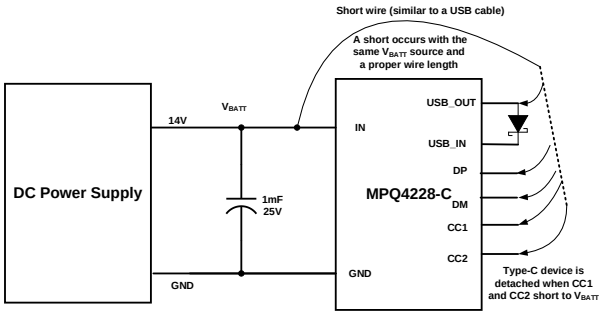


Figure 8: Short-to-Battery Set-Up

If a USB output is shorted to the battery, the USB input rises to trigger over-voltage protection (OVP). Then the USB input discharge path turns on.

During a CC1/CC2 or DP/DM short-to-battery condition, the MPQ4228-C can withstand high voltages on the internal components. Additionally, the ESD breakdown voltage exceeds the battery voltage.

A CC1 or CC2 short-to-battery can occur if the Type-C port is connected with a cable but has no sink (device is detached).

During DP or DM short-to-battery conditions, the MPQ4228-C detects the DP and DM voltages. If these voltages exceed 4V, the device turns off the data switch to disable the DP and DM outputs.

Fault Indication

FLT is the fault indication pin. FLT is in an open-drain state during shutdown, start-up, and normal operation. It asserts (logic low) during the following conditions: USB over-current/short-circuit, USB_IN over-voltage, DP/DM/CC1/CC2 pin over-voltage (short-to-battery), and over-temperature conditions.

FLT asserts low until the fault condition is removed, and the USB output voltage goes back to high. There is a 2ms deglitch time during an over-current condition to prevent a FLT false trigger. The FLT signal is not deglitched during over-voltage (short-to-battery) and over-temperature conditions.

Charging Downstream Port (CDP) Mode

The MPQ4228-C supports a charging downstream port (CDP) mode that complies with the USB2.0 definition of a host or a hub.

DM outputs a 0.6V voltage when DP is forced to be 0.6V. DP does not output a voltage when DM is forced to 0.6V.

USB Type-C Mode and VCONN

For the USB Type-C solution, two pins on the connector (CC1 and CC2) establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up resistor (R_P) and pull-down resistor (R_D, about 5.1kΩ) termination model is utilized (see Figure 9).

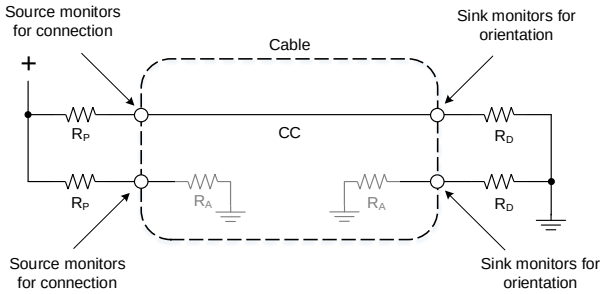


Figure 9: Current Source/Pull-Down CC Model

Initially, a source exposes independent R_P terminations on its CC1 and CC2 pins, and a sink exposes independent R_D terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this connection, the source monitors CC1 and CC2 for a voltage lower than the unterminated voltage. Choose R_P based on the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached.

Two special termination combinations on the CCx pins (as seen by a source) are defined for directly attached accessory modes: R_A/R_A for

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audio adapter accessory mode, and R_D/R_D for debug accessory mode. V_{BUS} is disabled in both of these scenarios (see Figure 10).

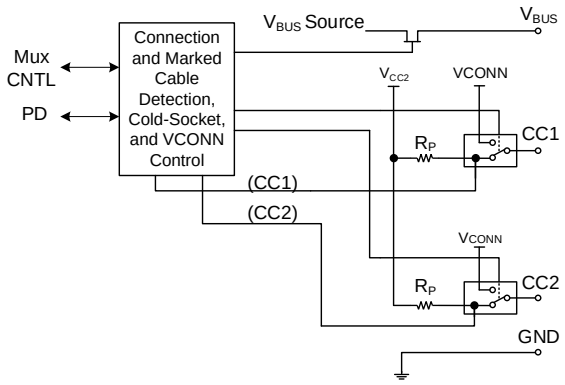


Figure 10: CC1 and CC2 Functional Block

The CC1 and CC2 functional block is described in greater detail below:

1. The source uses a FET to enable/disable power delivery across V_{BUS}. The source is disabled initially.
2. The source supplies pull-up resistors (R_P) on CC1 and CC2, then monitors both to detect a sink. The presence of a pull-down resistor (R_D) on either pin indicates that a sink is being attached. The value of R_P indicates the initial USB Type-C current level supported by the host. The MPQ4228-C's default R_P is 4.7kΩ, which represents a 3A current level.
3. The source uses the CCx's pull-down characteristic to detect and determine which CC pin is intended to supply power to VCONN (when R_A is detected).
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source can dynamically adjust the value of R_P to indicate a change in the available USB Type-C current to the sink (e.g at higher temperatures, the MPQ4228-C changes R_P to 12.7kΩ to indicate a 1.5A current ability).
6. The source monitors the continued presence of R_D to detect if the sink detaches. When a detach event is detected, the source is removed. V_{BUS} and V_{CONN} return to step 2.

Disable Type-C Mode (Type-A Mode)

During initial start-up, the device sources a 10μA current on the CC1 pin for 50μs. To enter Type-A mode, a 97.6kΩ resistor should be connected to CC1 to create an internal 0.976V voltage. The USB is latched at Type-A mode until power is recycled. While the device operates in Type-A mode, Type-C mode is disabled. This means that the CC attached and detached logic is disabled, and V_{BUS} is always enabled. In Type-A mode, the current limit changes to the Type-A specifications.

To trigger Type-A mode, the external pull-down resistor should be 97.6kΩ. Do not connect an extra capacitor to the CC1 pin.

EN1 Function

The EN1 function is active in Type-A mode. Connect a 97.6kΩ resistor to CC1 to enter Type-A mode. Then the CC2 pin acts as the EN1 pin. Apply three level voltage on EN1 for three states: off, client mode, and on

Pull EN1 high to enable the USB switch. Float EN1 or pull it low to disable the USB. Apply a middle-level voltage (1V to 1.85V) to EN1 to force the chip to enter client mode. In client mode, the USB switch is off, but the DP/DM high-speed data switch is on.

Note that the buck output is still active when EN1 is low.

Client Mode

The MPQ4228-C can work in client mode when the MPQ4228-C works in Type-A mode (see Figure 11). It is recommended to use this mode when upgrading software through the USB port.

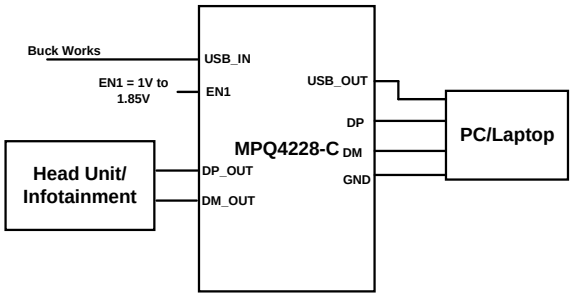


Figure 11: Client Mode

In client mode, the USB_OUT is powered by the external host (e.g. laptop). The DP and DM data switches are on, and the external host (e.g. laptop) can read and update the head unit software.

Type-C Load-Shedding versus Temperature

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When the sensed temperature exceeds 145°C, the USB port's CCx pin pull-up resistor (R_P) changes to 12.7kΩ to indicate that its source capability has changed to 1.5A.

The internal R_D detection threshold also changes to be between 0.4V and 1.6V, while the R_A detection threshold changes to be <0.4V. The current limit is unchanged. If the sensed temperature drops below 105°C, and lasts for 16 seconds, the USB Type-C current capability changes back to 3A (R_P = 4.7kΩ). Line drop compensation is disabled when the IC enters load-shedding protection.

SYSTEM

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. If the USB switch silicon die temperature exceeds 165°C, the device shuts down the USB current-limit switch. The CCx functional block and DP/DM functional blocks are active. When the temperature falls below its lower threshold, (typically 145°C), the USB current-limit switch is enabled.

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APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimal efficiency. The inductor value can be calculated with Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be estimated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Buck Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low-ESR capacitors for optimal performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For automotive applications, a 100µF electrolytic capacitor and two 4.7µF ceramic capacitors are recommended.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional, high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Calculate the output voltage ripple with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor affect the stability of the regulatory system. Four 22uF ceramic capacitors are recommended for a low output ripple and good control loop stability.

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4228-C has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3.7V, while the falling threshold is about 3.25V. If the application requires a higher UVLO threshold, place an external resistor divider between EN/SYNC and IN to raise the UVLO threshold (see Figure 12).

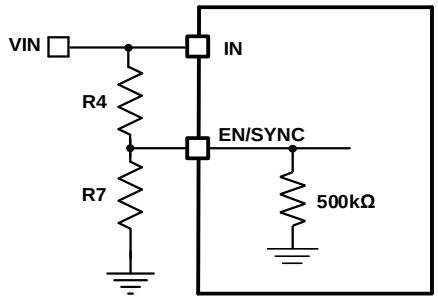


Figure 12: Adjustable UVLO using EN/SYNC Divider

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The UVLO rising and falling thresholds can be calculated with Equation (10) and Equation (11), respectively:

$$INUV_{RISING} = (1+\frac{R4}{500k\Omega//R7})\times V_{EN_RISING} \quad (10)$$

$$INUV_{FALLING} = (1+\frac{R4}{500k\Omega//R7})\times V_{EN_FALLING} \quad (11)$$

Where V_{EN_RISING} is 1.4V, and $V_{EN_FALLING}$ is 1.25V.

When selecting R4, ensure that it is large enough to limit the current flowing into EN/SYNC below 100μA.

ESD Protection for I/O Pins

High ESD levels should be considered for all USB I/O pins.

The CC1 and CC2 pins satisfy ±8kV IEC 61000-4-2 contact discharge ESD ratings, and ±15kV IEC 61000-4-2 air discharge ESD ratings.

The DP and DM pins pass ±8kV IEC 61000-4-2 contact discharge ESD ratings and ±15kV IEC 61000-4-2 air discharge ESD ratings with small external ESD diodes (see Figure 13).

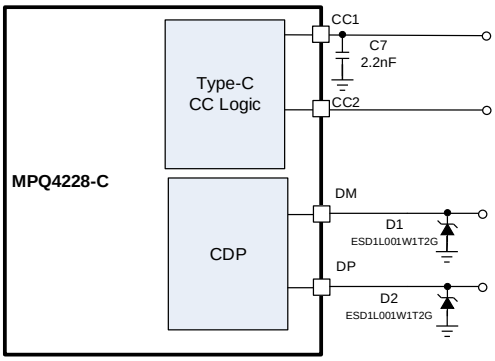


Figure 13: Recommended I/O Pins ESD Enhancing

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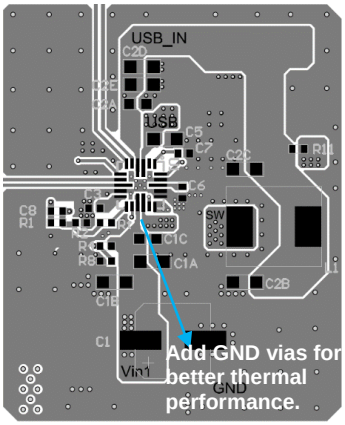
PCB Layout Guidelines [9]

Efficient PCB layout is critical for standard operation and thermal dissipation. Use a 4-layer PCB to improve thermal performance. For the best results, refer to Figure 14 and follow the guidelines below:

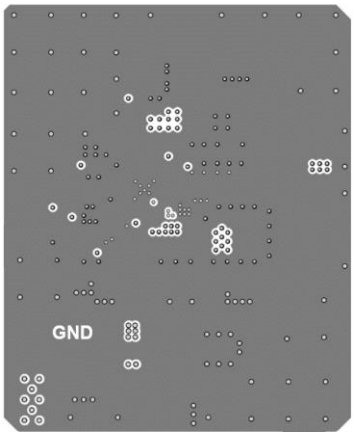
1. Place a ceramic input capacitor as close to IN and GND as possible (especially the small package size (0603) input bypass capacitor).
2. Keep the connection between the input capacitor and IN as short and wide as possible.
3. Place the VCC1/2 capacitors as close to the VCC1/2 pins as possible.
4. Make the trace length between the VCC1/2 pins, VCC1/2 capacitors, and GND as short as possible.
5. Connect a large ground plane directly to GND.
6. Add vias near GND if the bottom layer is a ground plane.
7. Route SW and BST away from sensitive analog areas, such as FB.
8. Place the T-type feedback resistor close to the chip to ensure that the trace connected to FB is as short as possible.
9. Ensure that the SW area is small to reduce the EMC radiated noise.
10. Use as short a length as possible when routing DP, DM, DP_OUT, and DM_OUT. Avoid vias and corners. Use two 45° turns to make a single 90° turn.
11. Route DP, DM, DP_OUT, and DM_OUT with differential pairs, and do not cross the ground of different circuit properties, as well as the complete ground plane. Keep these traces away from high-speed signals.

Notes:

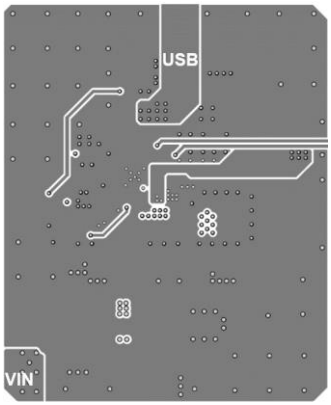
9) The recommended layout is based on the typical application (see Figure 15 on page 27)



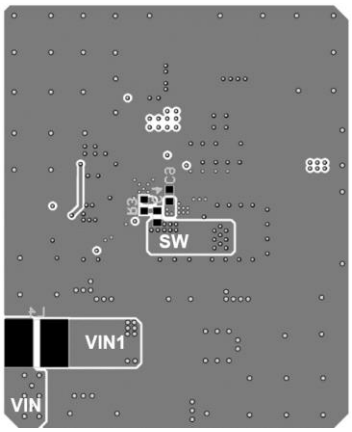
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 14: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS (10)

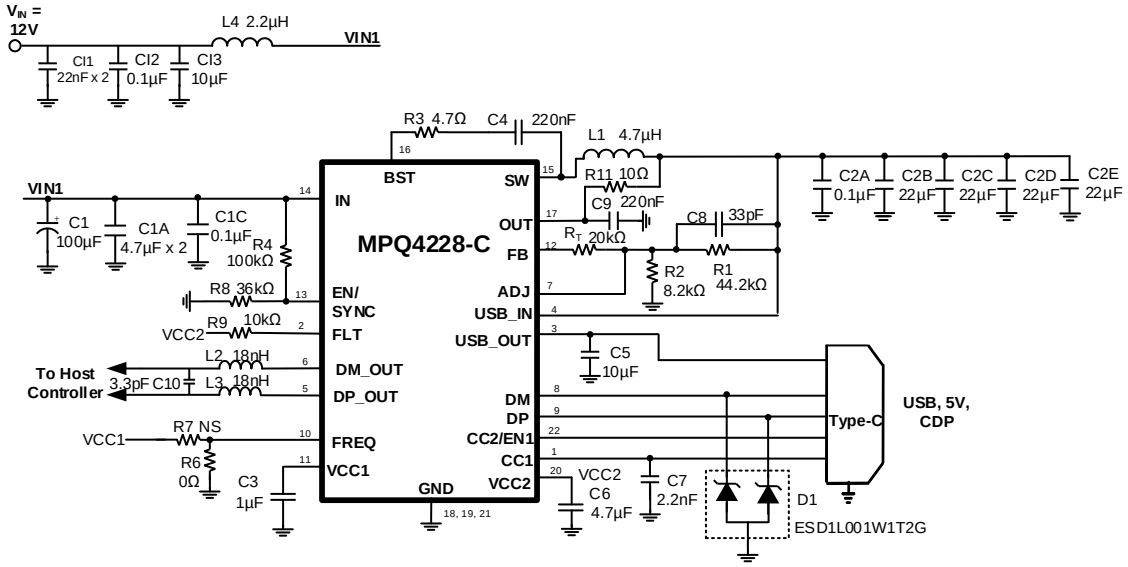


Figure 15: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 420kHz, Type-C DFP with BC1.2 CDP Mode

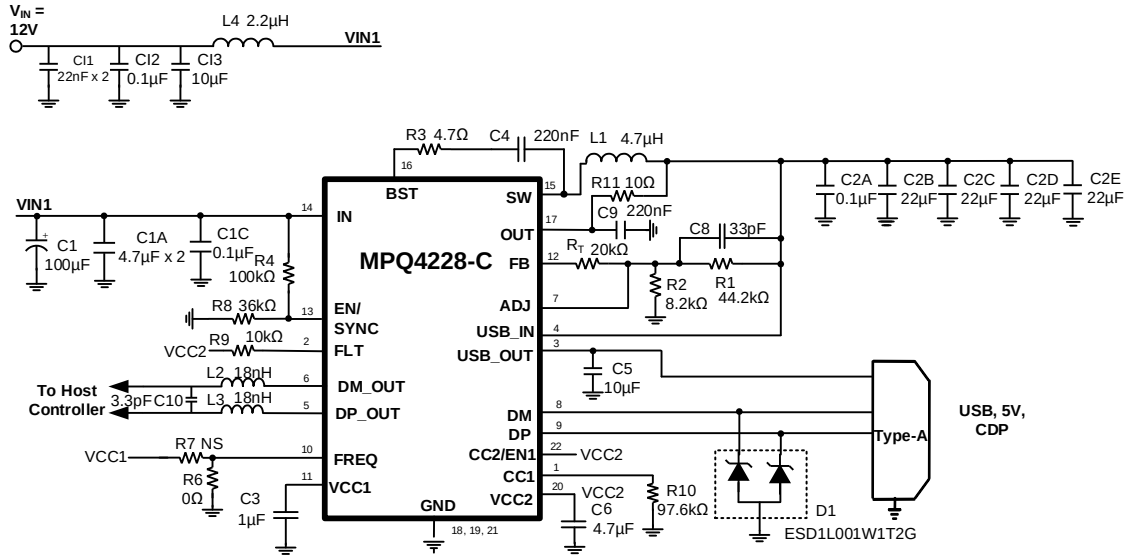


Figure 16: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 2.4A, f_{SW} = 420kHz, Type-A Port with BC1.2 CDP Mode

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TYPICAL APPLICATION CIRCUITS *(continued)* (10)

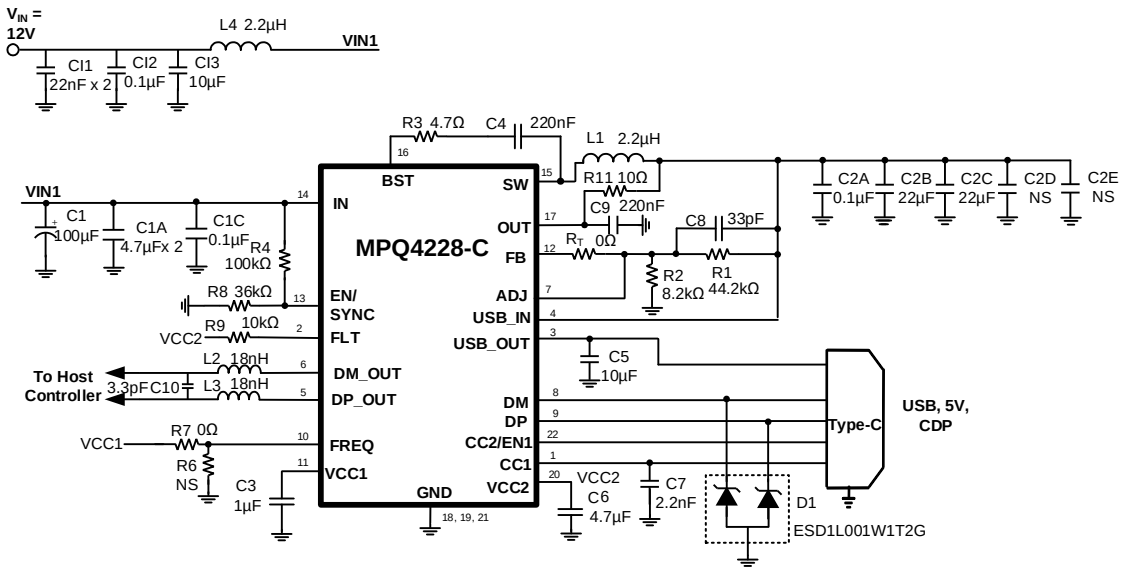


Figure 17: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 2.2MHz, Type-C DFP with BC1.2 CDP Mode

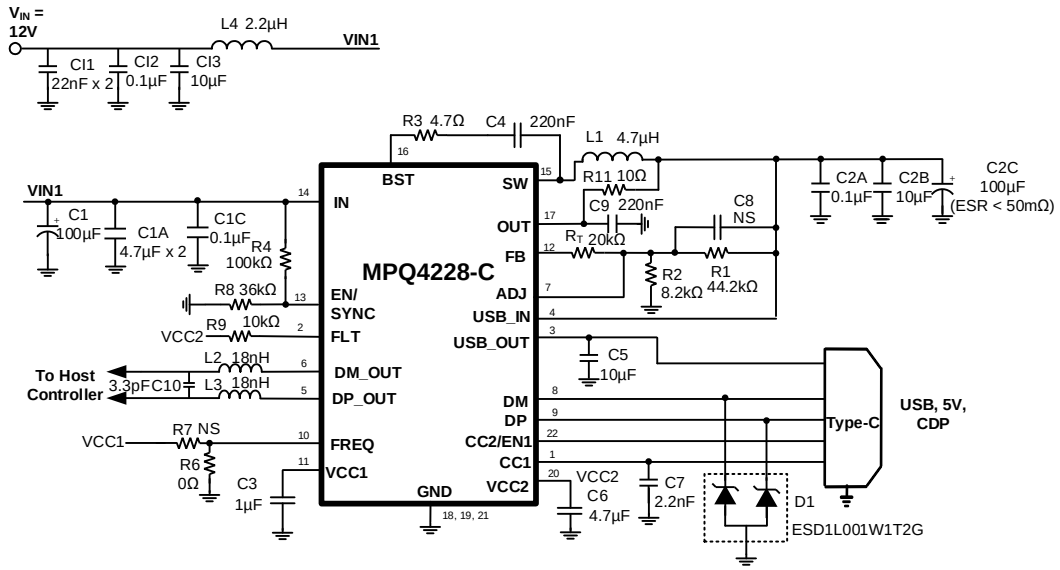


Figure 18: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 3A, f_{SW} = 420kHz, Type-C DFP with BC1.2 CDP Mode (with Aluminum Electronic Buck Output Capacitor)

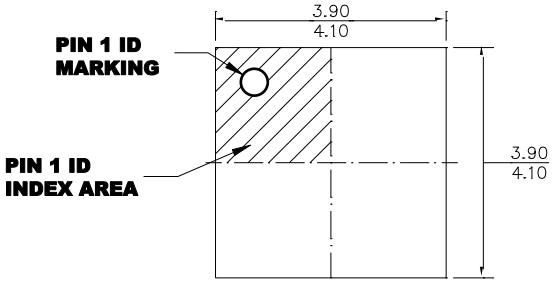
Note:

10) If the typical input voltage exceeds 24V, it is recommended to use a 0Ω BST resistor and add an RC snubber (2.2Ω resistor, 470pF capacitor) between SW and GND.

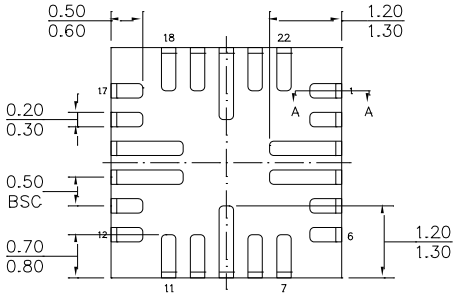
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PACKAGE INFORMATION

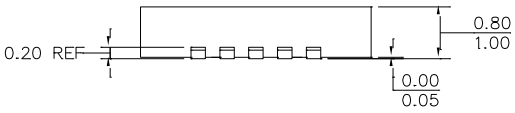
QFN-22 (4mmx4mm)



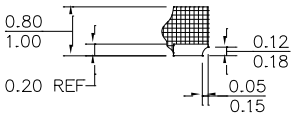
TOP VIEW



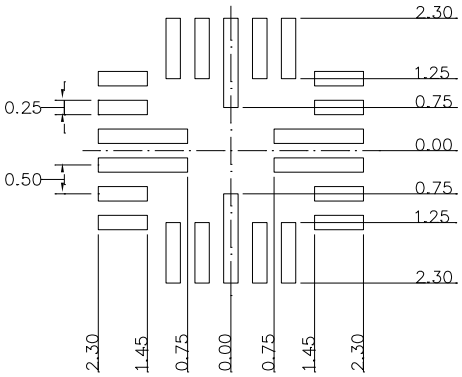
BOTTOM VIEW



SIDE VIEW



SECTION A-A



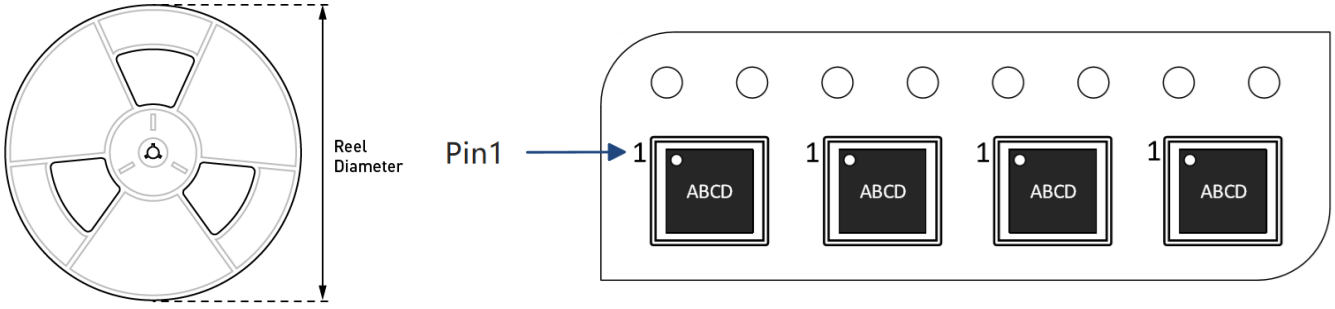
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4228GRE-C-AEC1–Z	QFN-22 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/12/2021	Initial Release	-

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