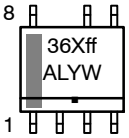
Fixed Frequency Current Mode Controller for Flyback Converters

NCP1236

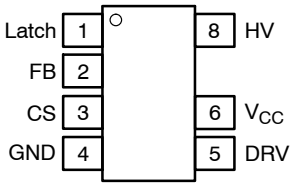
SOIC−7
CASE 751U

MARKING DIAGRAM



36Xff = Specific Device Code
X = A, B, C or D
ff = 65 or 100
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 33 of this data sheet.

The NCP1236 is a new fixed−frequency current−mode controller featuring Dynamic Self−Supply (DSS). This device is pin−to−pin compatible with the previous NCP12xx families.

The DSS function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during transients.

Due to frequency foldback, the controller exhibits excellent efficiency in light load condition while still achieving very low standby power consumption. Internal frequency jittering, ramp compensation, and a versatile latch input make this controller an excellent candidate for converters where components cost is the key constraints.

In addition, the controller includes a new high voltage circuitry that combines a start−up current source and a brown−out detector able to sense the input voltage either from the rectified ac line or the dc filtered bulk voltage. The high voltage sensing circuitry is used for the overpower protection purposes as well. Overpower protection, overload protection, and next protective features increases safety level of the final application.

Finally, due to a careful design, the precision of critical parameters is well controlled over the entire temperature range (−40°C to +125°C).

Features

- Fixed−Frequency Current−Mode Operation with Built−In Ramp Compensation
- 65 kHz or 100 kHz Oscillator Frequency
- Frequency Foldback then Skip Mode for Maximized Performance in Light Load and Standby Conditions
- Timer−Based Overload Protection with Latched (option A) or Auto−Recovery (option B) Operation, Shortened Overload Timer for Increased Safety (options C and D), (see all options on page 2)
- High−voltage Current Source with Brown−Out detection and Dynamic Self−Supply, Simplifying the Design of the V_{CC} Capacitor
- Frequency Modulation for Softened EMI Signature, including during Frequency Foldback mode
- Adjustable Overpower Compensation
- Latch−off Input for Severe Fault Conditions, Allowing Direct Connection of an NTC for Overtemperature Protection (OTP)
- V_{CC} Operation up to 28 V, with Overvoltage Detection
- ±500 mA Peak Source / Sink Current Drive Capability
- 4.0 ms Soft−Start
- Internal Thermal Shutdown
- Pin−to−Pin Compatible with the Existing NCP12xx Series
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- AC−DC Adapters for Notebooks, LCD, and Printers
- Offline Battery Chargers
- Consumer Electronic Power Supplies
- Auxiliary/Housekeeping Power Supplies

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TYPICAL APPLICATION EXAMPLE

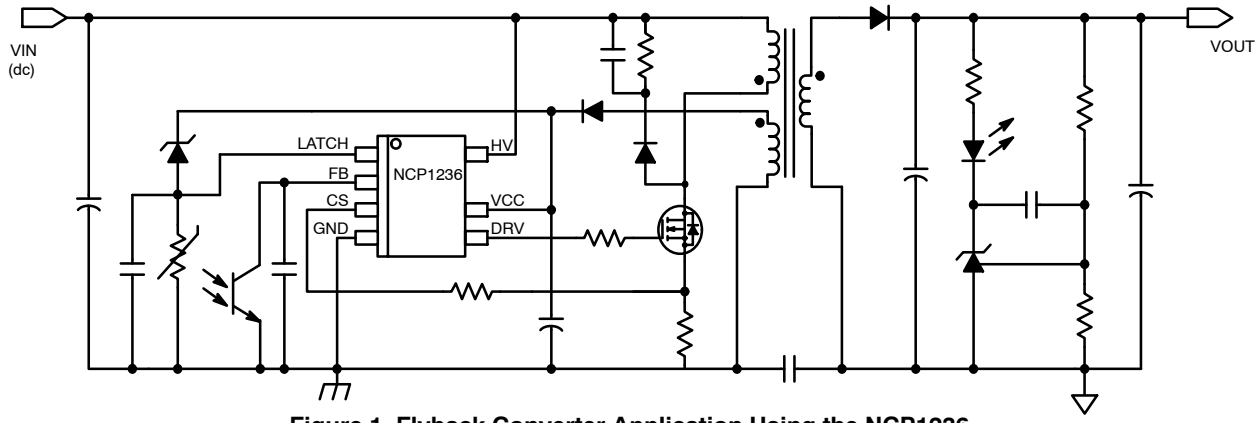

Figure 1. Flyback Converter Application Using the NCP1236

OPTIONS

Part	Option	Frequency	OCP Fault	Fault Timer	Autorecovery Timer
NCP1236	A	65 kHz	Latched	128 ms	1 s
	A	100 kHz	Latched	128 ms	1 s
	B	65 kHz	Autorecovery	128 ms	1 s
	B	100 kHz	Autorecovery	128 ms	1 s
	C	65 kHz	Latched	32 ms	1.5 s
	C	100 kHz	Latched	32 ms	1.5 s
	D	65 kHz	Autorecovery	32 ms	1.5 s
	D	100 kHz	Autorecovery	32 ms	1.5 s

PIN FUNCTION DESCRIPTION

Pin No	Pin Name	Function	Pin Description
1	LATCH	Latch−Off Input	Pull the pin up or down to latch−off the controller. An internal current source allows the direct connection of an NTC for over temperature detection
2	FB	Feedback	An optocoupler collector to ground controls the output regulation.
3	CS	Current Sense	This Input senses the Primary Current for current−mode operation, and Offers an overpower compensation adjustment.
4	GND		IC Ground
5	DRV	Drive output	Drives external MOSFET
6	V_{CC}	V_{CC} input	This supply pin accepts up to 28 Vdc, with overvoltage detection
8	HV	High−voltage pin	Connects to the bulk capacitor or the rectified AC line to perform the functions of Start−up Current Source, Dynamic Self−Supply and brown−out detection

SIMPLIFIED INTERNAL BLOCK SCHEMATIC

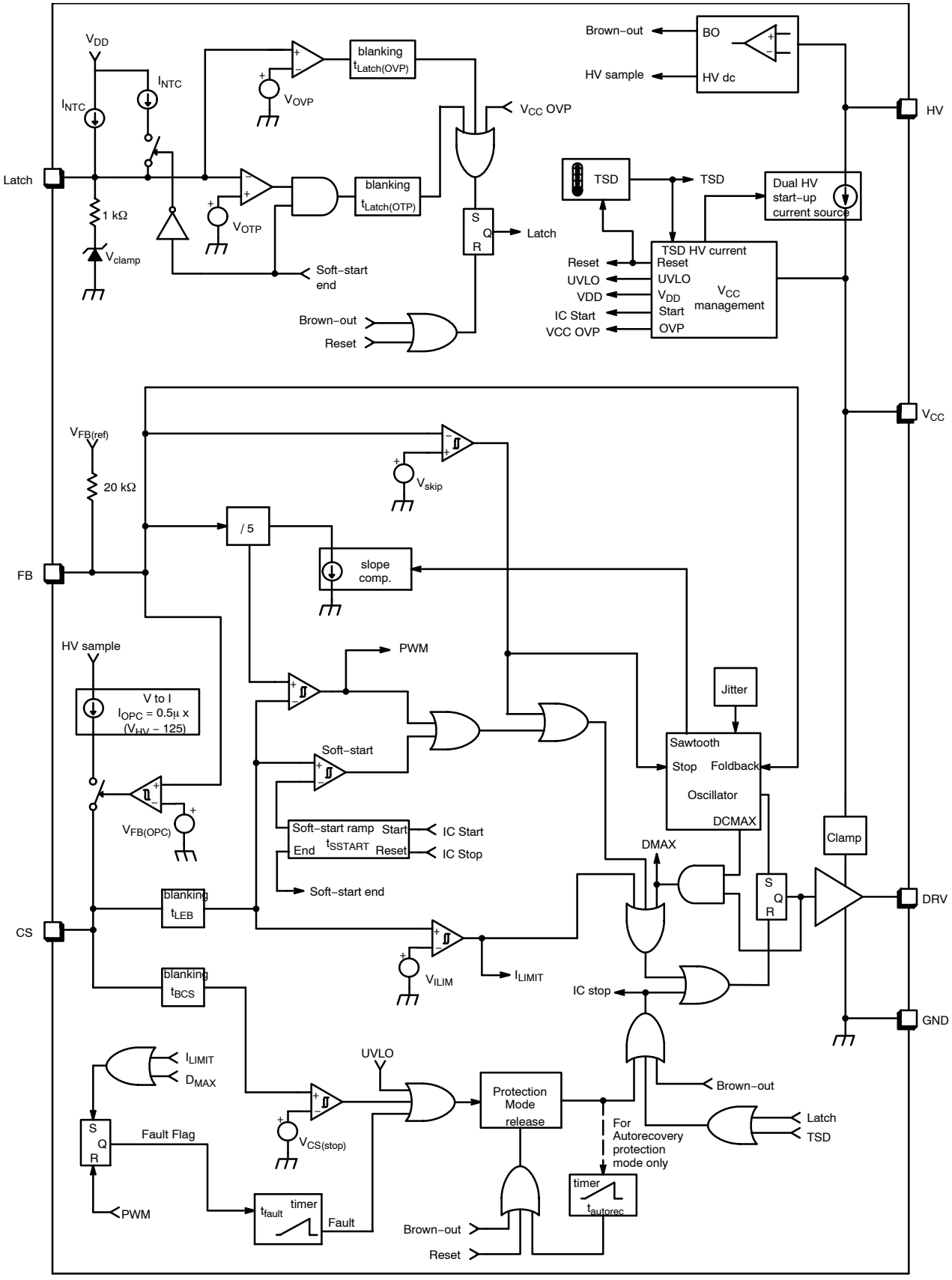

Figure 2. Simplified Internal Block Schematic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Pin (pin 6) (Note 2) Voltage range Current range	 V_{CCMAX} I_{CCMAX}	 −0.3 to 28 ±30	 V mA
High Voltage Pin (pin 8) (Note 2) Voltage range Current range	 V_{HVMAX} I_{HVMAX}	 −0.3 to 500 ±20	 V mA
Driver Pin (pin 5) (Note 2) Voltage range Current range	 V_{DRVMAX} I_{DRVMAX}	 −0.3 to 20 ±1000	 V mA
All other pins (Note 2) Voltage range Current range	 V_{MAX} I_{MAX}	 −0.3 to 10 ±10	 V mA
Thermal Resistance SOIC−7 Junction−to−Air, low conductivity PCB (Note 3) Junction−to−Air, medium conductivity PCB (Note 4) Junction−to−Air, high conductivity PCB (Note 5)	$R_{\theta J-A}$	 162 147 115	°C/W
Temperature Range Operating Junction Temperature Storage Temperature Range	 T_{JMAX} $T_{STRGMAX}$	 −40 to +150 −60 to +150	°C
ESD Capability (Note 1) Human Body Model (All pins except HV) Machine Model		 2000 200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC standard JESD22, Method A114E
   Machine Model Method 200 V per JEDEC standard JESD22, Method A115A
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78
3. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−1 conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 100 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−2 conductivity test PCB. Test conditions were under natural convection or zero air flow.
5. As mounted on a 80 x 100 x 1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51−3 conductivity test PCB. Test conditions were under natural convection or zero air flow.

ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
HIGH VOLTAGE CURRENT SOURCE						
Minimum voltage for current source operation		$V_{HV(min)}$	–	30	40	V
Current flowing out of V_{CC} pin	V_{CC} = 0 V V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start1} I_{start2}	0.2 3	0.5 6	0.8 9	mA
Off−state leakage current	V_{HV} = 500 V	$I_{start(off)}$	–	25	50	μA
SUPPLY						
Turn−on threshold level, V_{CC} going up HV current source stop threshold		$V_{CC(on)}$	11.0	12.0	13.0	V
HV current source restart threshold		$V_{CC(min)}$	9.5	10.5	11.5	V
Turn−off threshold		$V_{CC(off)}$	8.5	9.5	10.5	V
Overvoltage threshold		$V_{CC(ovp)}$	25	26.5	28	V
Blanking duration on $V_{CC(off)}$ and $V_{CC(ovp)}$ detection (Note 7)		$t_{VCC(blank)}$	7	10	13	μs
V_{CC} decreasing level at which the internal logic resets		$V_{CC(reset)}$	3.6	5.0	6.0	V
V_{CC} level for I_{START1} to I_{START2} transition		$V_{CC(inhibit)}$	0.4	1.0	1.6	V
Internal current consumption (Note 6)	DRV open, V_{FB} = 3 V, 65 kHz DRV open, V_{FB} = 3 V, 100 kHz C_{drv} = 1 nF, V_{FB} = 3 V, 65 kHz C_{drv} = 1 nF, V_{FB} = 3 V, 100 kHz Off mode (skip or before start−up) Fault mode (fault or latch)	I_{CC1} I_{CC1} I_{CC2} I_{CC2} I_{CC3} I_{CC4}	1.2 1.2 1.9 2.2 0.67 0.4	1.8 1.9 2.5 2.9 0.9 0.7	2.2 2.3 3.2 3.6 1.13 1.0	mA
BROWN−OUT						
Brown−Out thresholds	V_{HV} going up V_{HV} going down	$V_{HV(start)}$ $V_{HV(stop)}$	92 79	107 92	122 105	V
Timer duration for line cycle drop−out		t_{HV}	47	68	90	ms
OSCILLATOR						
Oscillator frequency		f_{OSC}	60 92	65 100	70 108	kHz
Maximum duty cycle		D_{MAX}	75	80	85	%
Frequency jittering amplitude, in percentage of F_{OSC}		A_{jitter}	±4	±6	±8	%
Frequency jittering modulation frequency		F_{jitter}	85	125	165	Hz
OUTPUT DRIVER						
Rise time, 10% to 90 % of V_{CC}	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{rise}	–	40	70	ns
Fall time, 90% to 10 % of V_{CC}	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF	t_{fall}	–	40	70	ns
Current capability	V_{CC} = $V_{CC(min)}$ + 0.2 V, C_{DRV} = 1 nF DRV high, V_{DRV} = 0 V DRV low, V_{DRV} = V_{CC}	$I_{DRV(source)}$ $I_{DRV(sink)}$	– –	500 500	– –	mA
Clamping voltage (maximum gate voltage)	V_{CC} = V_{CCmax} − 0.2 V, DRV high, R_{DRV} = 33 kΩ, C_{load} = 220 pF	$V_{DRV(clamp)}$	11	13.5	16	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Internal supply current only, current in FB pin not included (current flowing in GND pin only).
7. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
OUTPUT DRIVER						
High−state voltage drop	$V_{CC} = V_{CC(min)}$ + 0.2 V, R_{DRV} = 33 kΩ, DRV high	$V_{DRV(drop)}$	−	−	1	V
CURRENT SENSE						
Input Bias Current	V_{CS} = 0.7 V	I_{bias}	−	0.02	−	μA
Maximum internal current setpoint	V_{FB} > 3.5 V	V_{ILIM}	0.66	0.7	0.74	V
Propagation delay from V_{Ilimit} detection to DRV off	$V_{CS} = V_{ILIM}$	t_{delay}	−	80	110	ns
Leading Edge Blanking Duration for V_{ILIM}		t_{LEB}	190	250	310	ns
Threshold for immediate fault protection activation		$V_{CS(stop)}$	0.95	1.05	1.15	V
Leading Edge Blanking Duration for $V_{CS(stop)}$		t_{BCS}	90	120	150	ns
Slope of the compensation ramp		$S_{comp(65kHz)}$ $S_{comp(100kHz)}$	− −	−32.5 −50	− −	mV / μs
Soft−start duration	From 1st pulse to $V_{CS} = V_{ILIM}$	t_{SSTART}	2.8	4.0	5.2	ms
OVERPOWER COMPENSATION						
V_{HV} to I_{OPC} conversion ratio		K_{OPC}	−	0.54	−	μA / V
Current flowing out of CS pin	V_{HV} = 125 V V_{HV} = 162 V V_{HV} = 325 V V_{HV} = 365 V	$I_{OPC(125)}$ $I_{OPC(162)}$ $I_{OPC(325)}$ $I_{OPC(365)}$	− − − 105	0 20 110 130	− − − 150	μA
FB voltage above which I_{OPC} is applied	V_{HV} = 365 V	$V_{FB(OPCF)}$	2.12	2.35	2.58	V
FB voltage below which is no I_{OPC} applied	V_{HV} = 365 V	$V_{FB(OPCE)}$	−	2.15	−	V
Watchdog timer for dc operation		$t_{WD(OPC)}$	−	32	−	ms
FEEDBACK						
Internal pull−up resistor	T_J = 25°C	$R_{FB(up)}$	15	20	25	kΩ
V_{FB} to internal current setpoint division ratio		K_{FB}	4.7	5	5.3	−
Internal pull−up voltage on the FB pin		$V_{FB(ref)}$	4.3	5	5.7	V
OVERCURRENT PROTECTION						
Fault timer duration	From CS reaching V_{ILIMIT} to DRV stop	t_{fault}	98	128	168	ms
Fault timer duration (for the C version only)	From CS reaching V_{ILIMIT} to DRV stop	t_{fault}	16	32	48	ms
Autorecovery mode latch−off time duration		$t_{autorec}$	0.85	1.00	1.35	s
Autorecovery mode latch−off time duration (for the C version only)		$t_{autorec}$	1.0	1.5	2.0	s

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6. Internal supply current only, current in FB pin not included (current flowing in GND pin only).
7. Guaranteed by design.

ELECTRICAL CHARACTERISTICS (continued)
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, V_{HV} = 125 V, V_{CC} = 11 V unless otherwise noted)

Characteristics	Test Condition	Symbol	Min	Typ	Max	Unit
FREQUENCY FOLDBACK						
Feedback voltage threshold below which frequency foldback starts		$V_{FB(foldS)}$	1.8	2.0	2.2	V
Feedback voltage threshold below which frequency foldback is complete		$V_{FB(foldE)}$	1.22	1.35	1.48	V
Minimum switching frequency	$V_{FB} = V_{skip(in)} + 0.2$	$f_{OSC(min)}$	22	27	32	kHz
SKIP−CYCLE MODE						
Feedback voltage thresholds for skip mode	V_{FB} going down V_{FB} going up	$V_{skip(in)}$ $V_{skip(out)}$	0.63 0.72	0.7 0.80	0.77 0.88	V
LATCH−OFF INPUT						
High threshold	V_{Latch} going up	V_{OVP}	2.35	2.5	2.65	V
Low threshold	V_{Latch} going down	V_{OTP}	0.76	0.8	0.84	V
Current source for direct NTC connection During normal operation During soft−start	V_{Latch} = 0 V	 I_{NTC} $I_{NTC(SSTART)}$	 65 130	 95 190	 105 210	µA
Blanking duration on high latch detection	65 kHz version 100 kHz version	$t_{Latch(OVP)}$	35 25	50 35	70 45	µs
Blanking duration on low latch detection		$t_{Latch(OTP)}$	–	350	–	µs
Clamping voltage	I_{Latch} = 0 mA I_{Latch} = 1 mA	$V_{clamp0(Latch)}$ $V_{clamp1(Latch)}$	1.0 2.0	1.2 2.4	1.4 3.0	V
TEMPERATURE SHUTDOWN						
Temperature shutdown (Note 7)	T_J going up	T_{TSD}	135	150	165	°C
Temperature shutdown hysteresis (Note 7)	T_J going down	$T_{TSD(HYS)}$	20	30	40	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Internal supply current only, current in FB pin not included (current flowing in GND pin only).
7. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

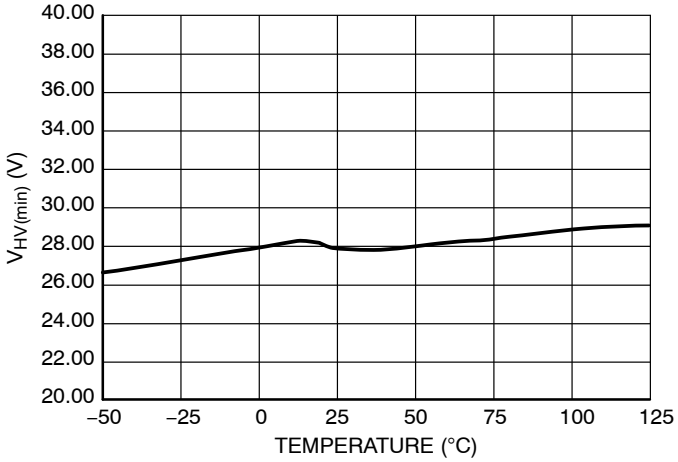


Figure 3. Minimum Current Source Operation $V_{HV(min)}$

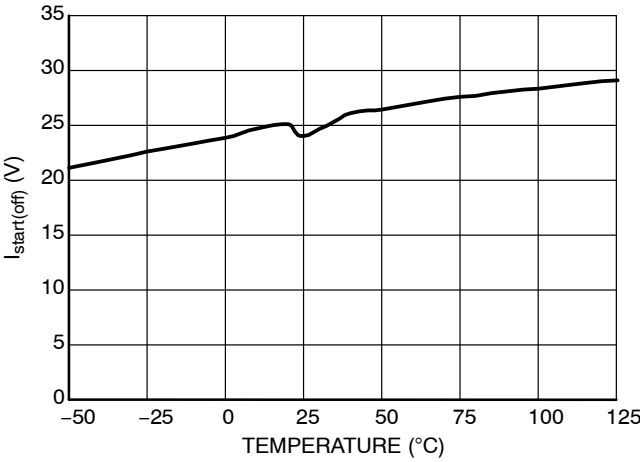


Figure 4. Off−State Leakage Current $I_{start(off)}$

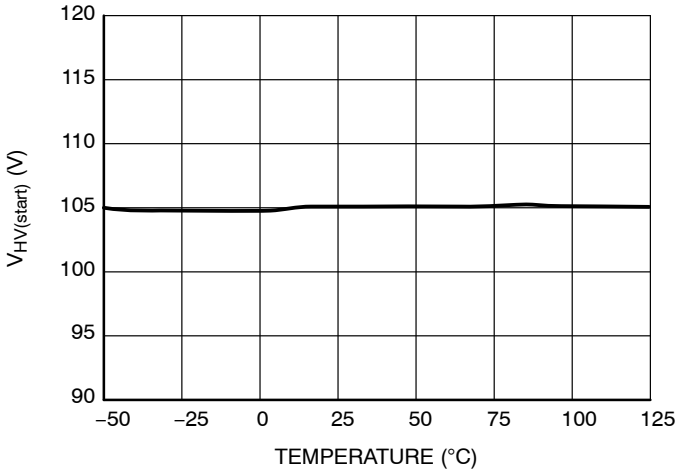


Figure 5. Brown−out Device Start Threshold $V_{HV(start)}$

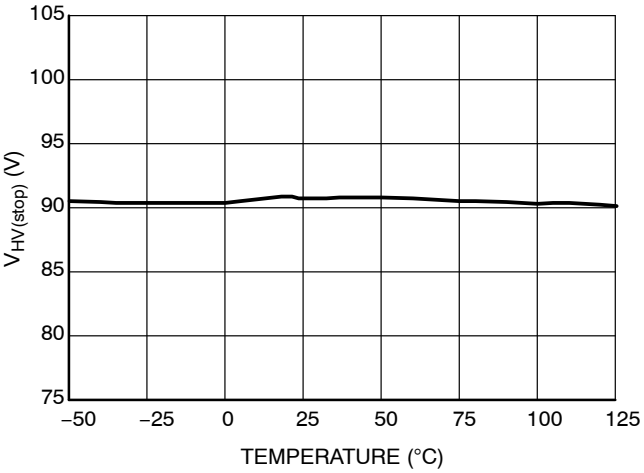


Figure 6. Brown−Out Device Stop Threshold $V_{HV(stop)}$

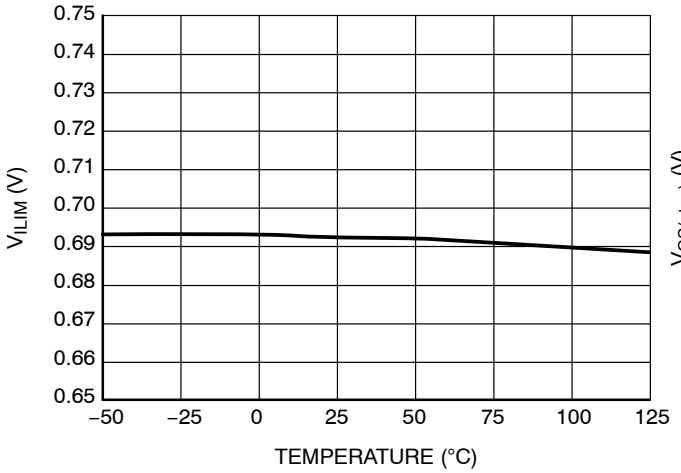


Figure 7. Maximum Internal Current Setpoint V_{ILIM}

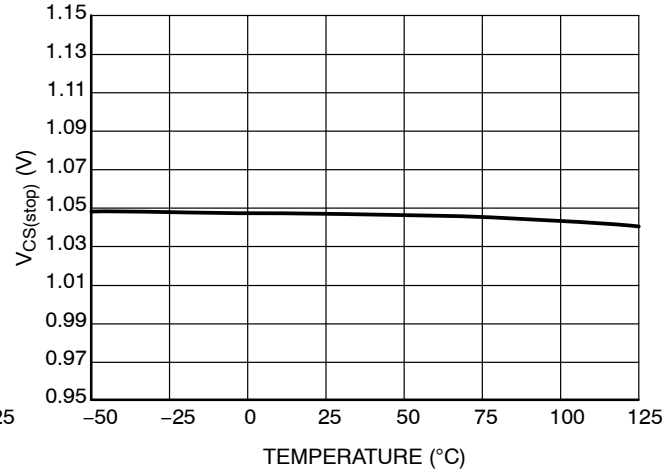


Figure 8. Threshold for Immediate Fault Protection Activation $V_{CS(stop)}$

TYPICAL PERFORMANCE CHARACTERISTICS

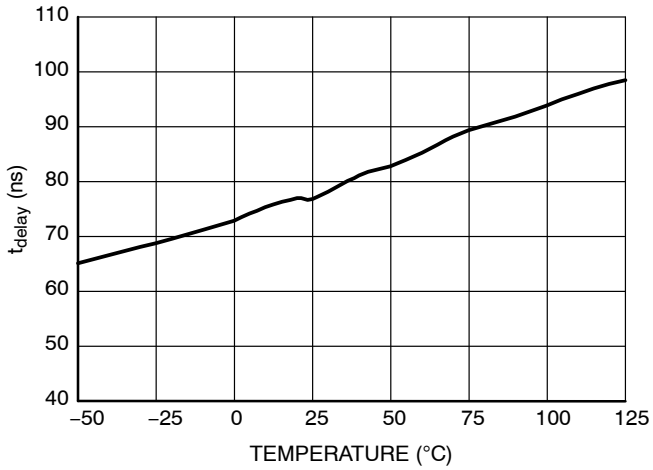


Figure 9. Propagation Delay t_{delay}

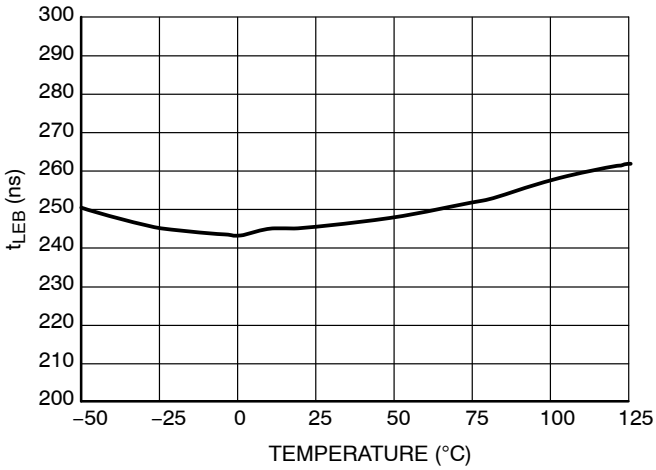


Figure 10. Leading Edge Blanking Duration t_{LEB}

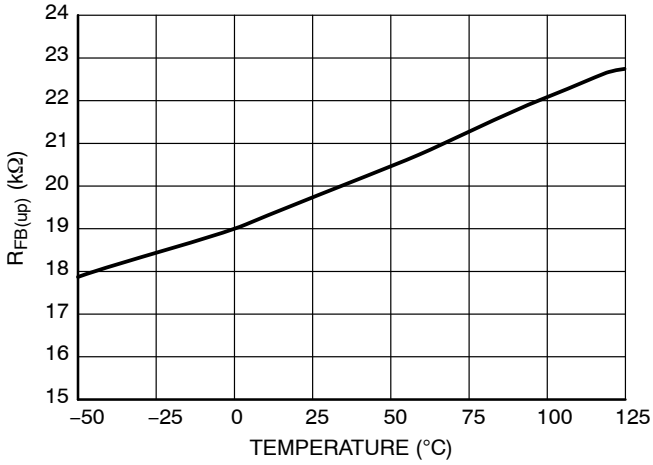


Figure 11. FB Pin Internal Pull−up Resistor $R_{FB(up)}$

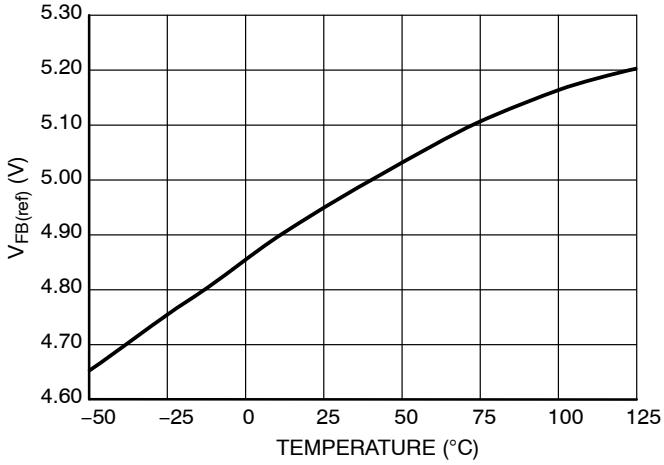


Figure 12. FB Pin Open Voltage $V_{FB(ref)}$

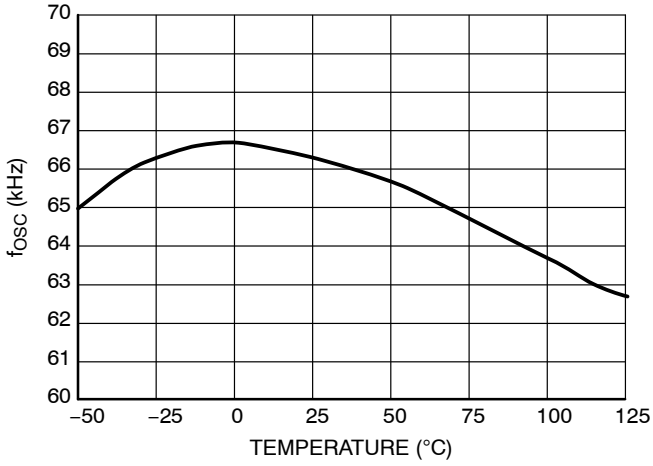


Figure 13. Oscillator Frequency f_{OSC} for the 65 kHz version

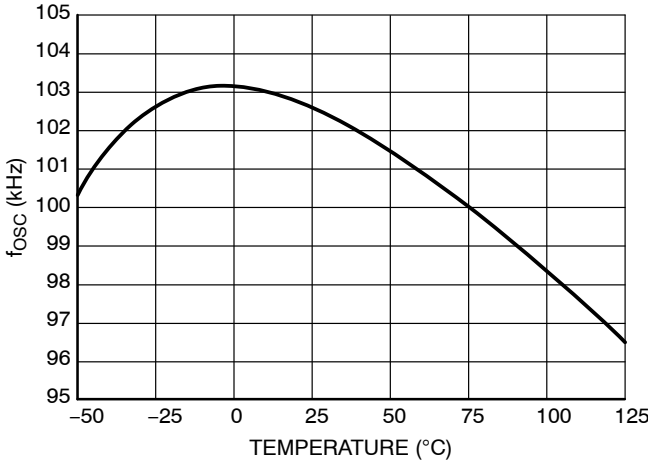


Figure 14. Oscillator Frequency f_{OSC} for the 100 kHz version

TYPICAL PERFORMANCE CHARACTERISTICS

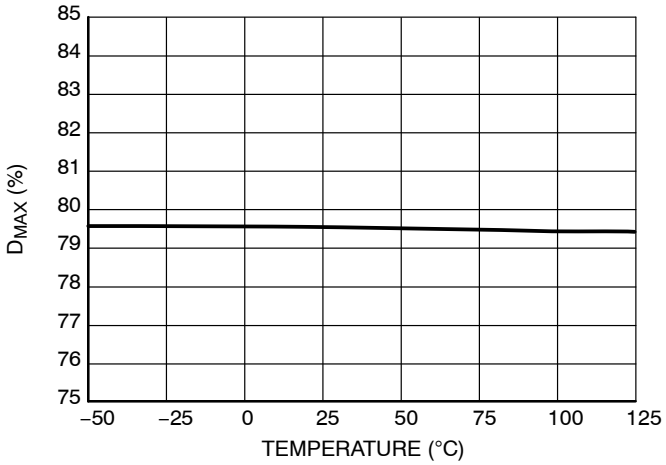


Figure 15. Maximum Duty Cycle D_{MAX}

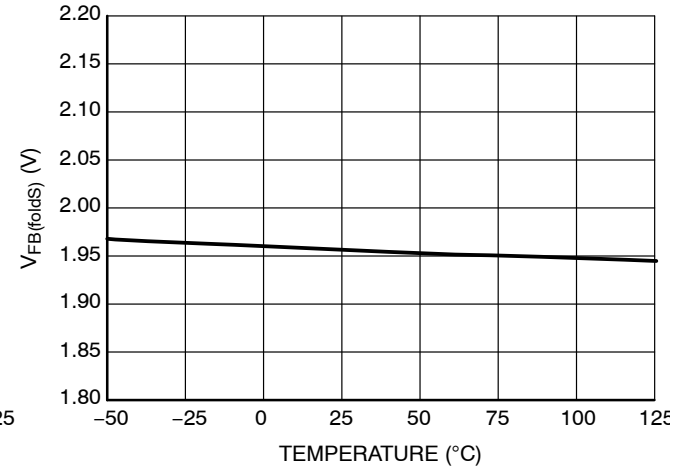


Figure 16. FB Pin Voltage Below Which Frequency Foldback Starts $V_{FB(foldS)}$

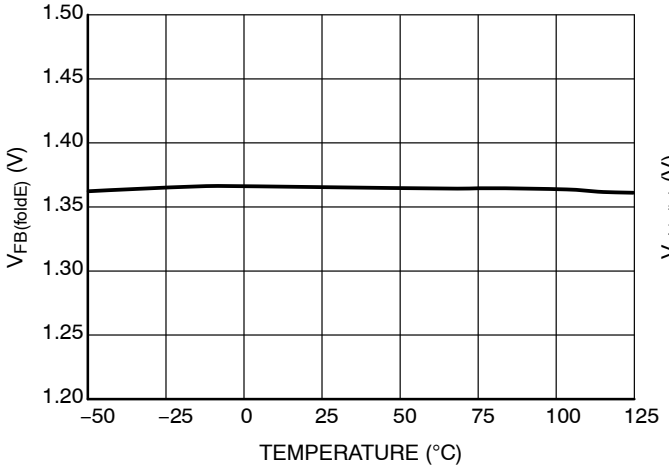


Figure 17. FB Pin Voltage Below Which Frequency Foldback is Complete $V_{FB(foldE)}$

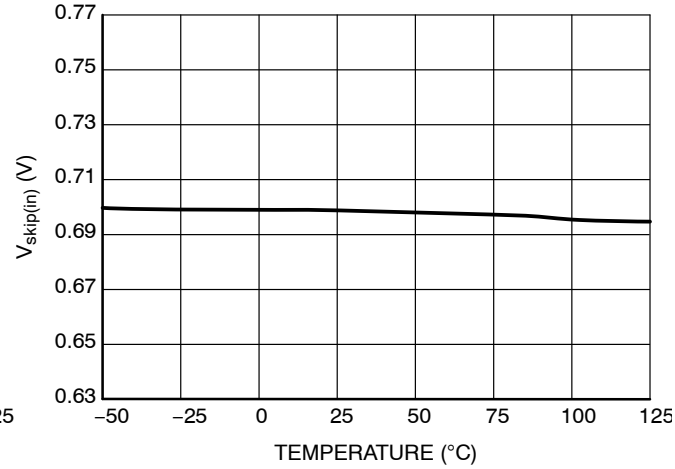


Figure 18. FB Pin Skip−in Level $V_{skip(in)}$

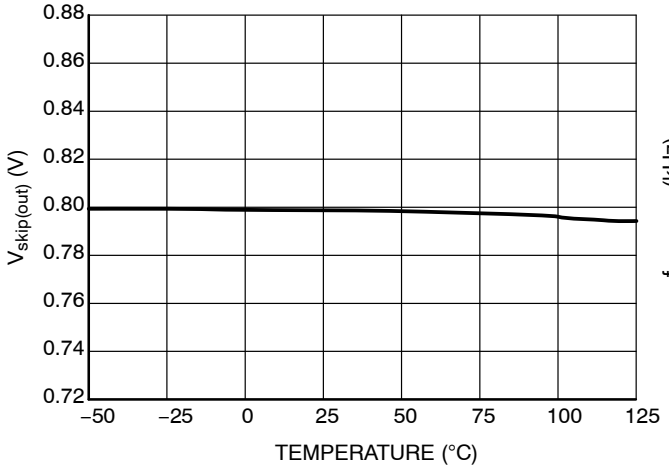


Figure 19. FB Pin Skip−Out Level $V_{skip(out)}$

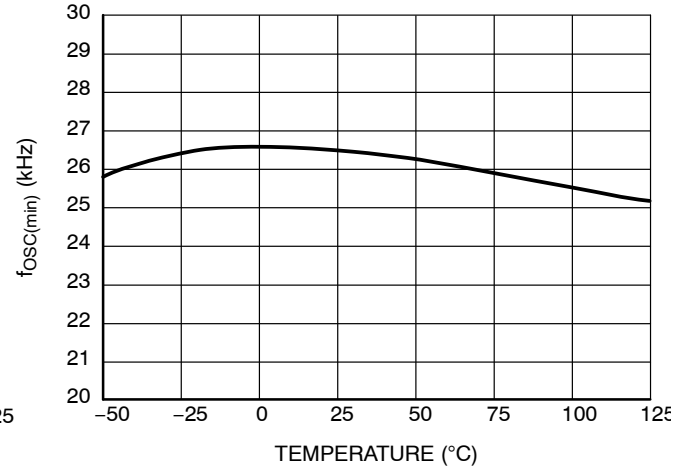


Figure 20. Minimum Switching Frequency $f_{OSC(min)}$

TYPICAL PERFORMANCE CHARACTERISTICS

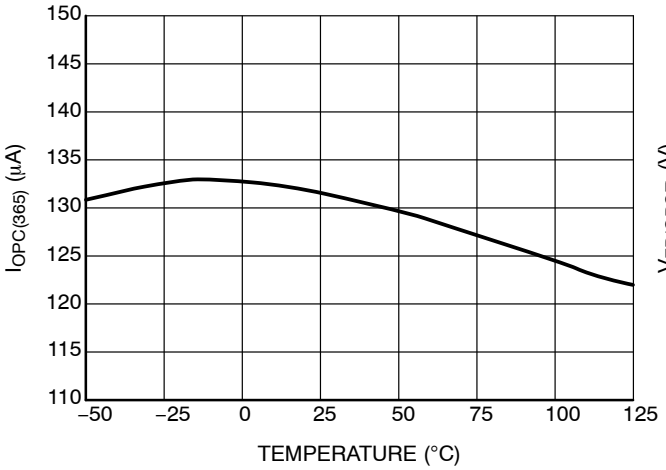


Figure 21. Maximum Overpower Compensating Current $I_{OPC(365)}$ Flowing Out of CS Pin

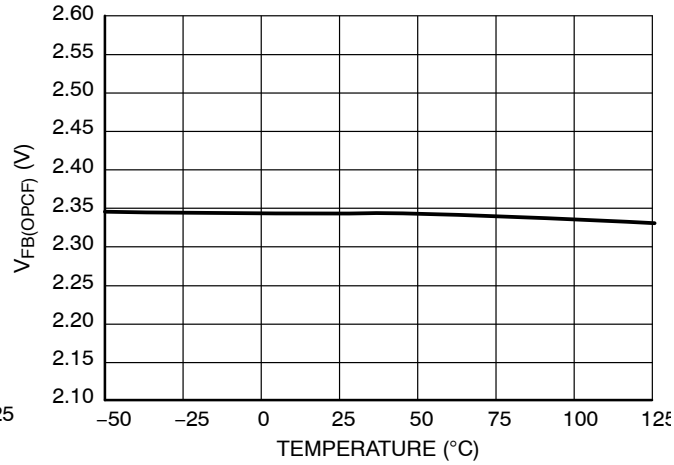


Figure 22. FB Pin Level $V_{FB(OPCF)}$ Above Which is the Overpower Compensation Applied

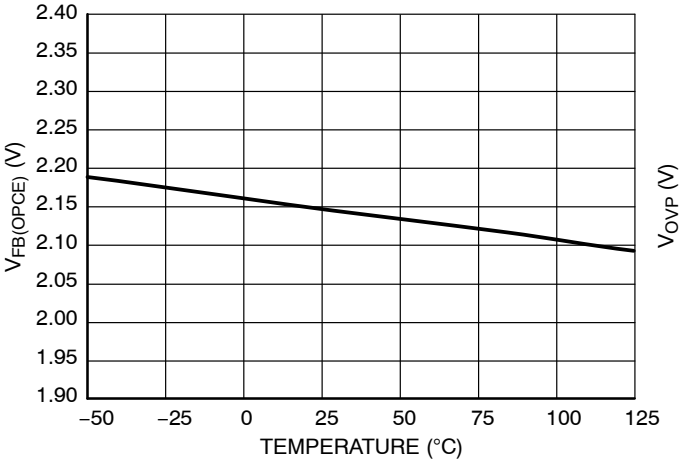


Figure 23. FB Pin Level $V_{FB(OPCE)}$ Below Which is No Overpower Compensation Applied

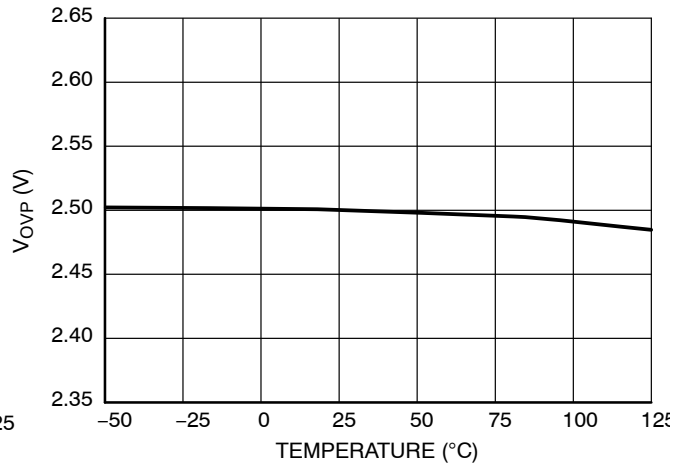


Figure 24. Latch Pin High Threshold V_{OVP}

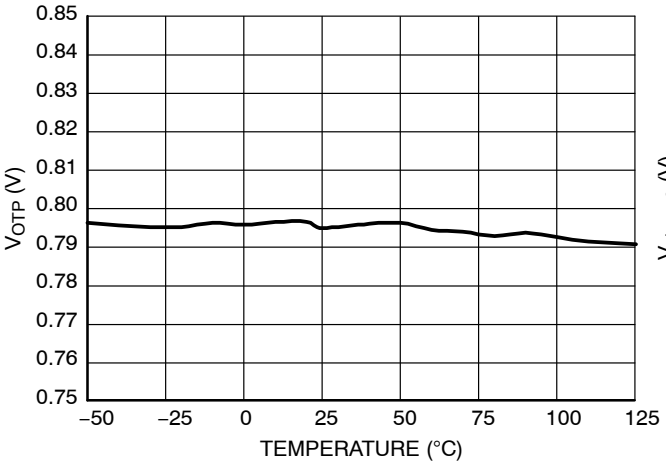


Figure 25. Latch Pin Low Threshold V_{OTP}

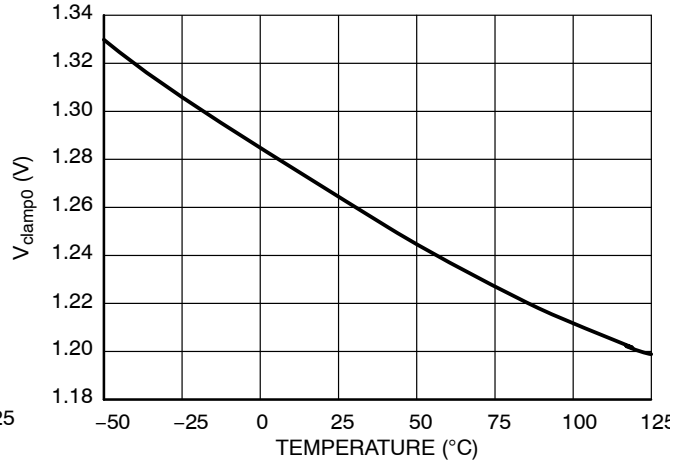


Figure 26. Latch Pin Open Voltage V_{clamp0}

TYPICAL PERFORMANCE CHARACTERISTICS

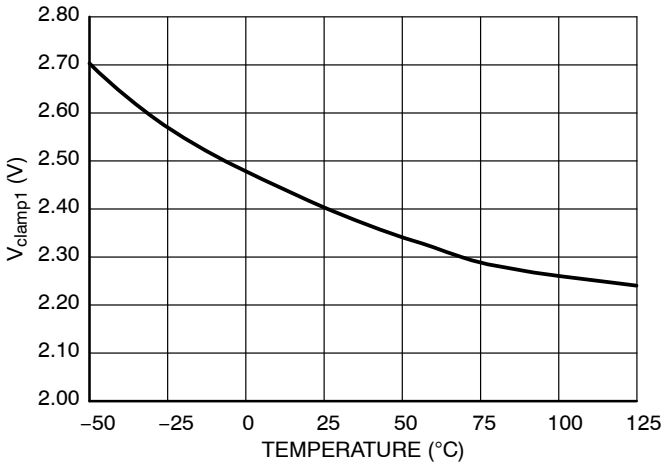


Figure 27. Latch Pin Voltage V_{clamp1} (Latch−off Pin is Sinking 1 mA)

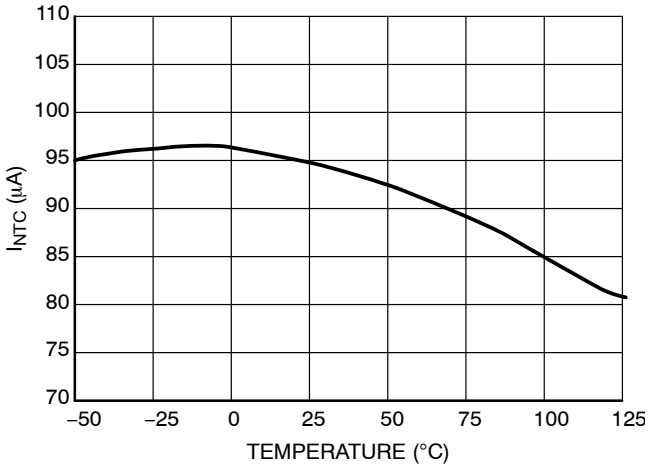


Figure 28. Current I_{NTC} Sourced from the Latch Pin, Allowing Direct NTC Connection

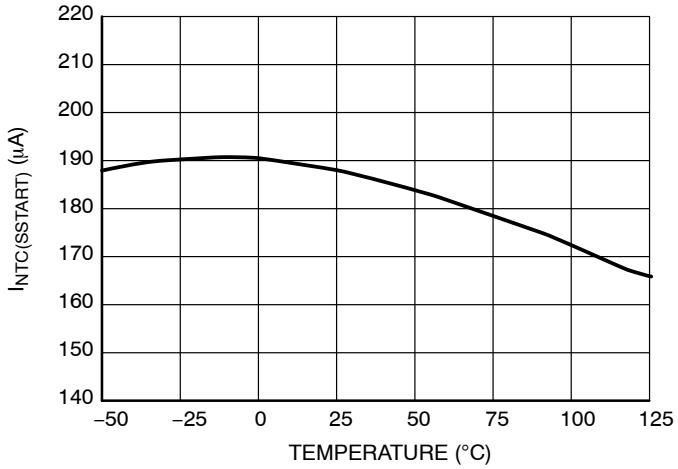


Figure 29. Current $I_{NTC(SSTART)}$ Sourced from the Latch Pin, During Soft−Start

APPLICATION INFORMATION

Introduction

The NCP1236 includes all necessary features to build a safe and efficient power supply based on a fixed−frequency flyback converter. It is particularly well suited for applications where low part count is a key parameter, without sacrificing safety.

- **Current−Mode Operation with slope compensation**: The primary peak current is permanently controlled by the FB voltage, ensuring maximum safety: the DRV turn−off event is dictated by the peak current setpoint. It also ensures that the frequency response of the system stays a first order if in DCM, which eases the design of the FB loop. The controller can be also used in CCM applications with a wide input voltage range thanks to its fixed ramp compensation that prevents the appearance of sub−harmonic oscillations.
- **Fixed−Frequency Oscillator with Jittering**: The NCP1236 is available in different frequency options to fit any application. The internal oscillator features a low−frequency jittering that helps passing the EMI limits by spreading out the energy content of frequency peaks in quasi−peak and average mode of measurement.
- **Latched / Autorecovery Timer−Based Overload Protection**: The overload protection depends only on the FB signal, making it able to work with any transformer, even with very poor coupling or high leakage inductance. When the fault timer elapses the device can be permanently latched in version A or the latch can be reset by an autorecovery restart of the device in version B. The power supply has to be stopped then restarted in order to resume operation, even if the overload condition disapears, in case of usage the A version of the NCP1236. The fault timer duration is internally fixed. The controller also latches off if the voltage on the CS pin reaches 1.5 times the maximum internal setpoint (allowing to detect winding short−circuits), with the same modes of releasing the latch in A or B version.
- **High Voltage Start−Up Current Source with Brown−Out Detection**: Due to **onsemi**'s Very High Voltage technology, the NCP1236 can be directly connected to the high input voltage. The start−up current source ensures a clean start−up and the Dynamic Self−Supply (DSS) restarting the start−up current source to supply the controller if the V_{CC} voltage transiently drops. The high voltage pin also features a high−voltage sensing circuitry, which is able to turn the controller off if the input voltage is too low (brown−out condition). This protection works either with a DC input voltage or a rectified AC input voltage, and is independent of the high voltage ripple.
- **Adjustable Overpower Compensation**: The high input voltage sensed on the HV pin is converted into a current to build on the current sense voltage an offset proportional to the input voltage. By choosing the value of the resistor in series with the CS pin, the amount of compensation can be adjusted to the application.
- **Frequency foldback then skip mode for light load operation**: In order to ensure a high efficiency under all load conditions, the NCP1236 implements a frequency foldback for light load condition and a skip mode for extremely low load condition. The switching frequency is decreased down to 27 kHz to reduce switching losses.
- **Extended VCC range**: The NCP1236 accepts a supply voltage as high as 28 V, with an overvoltage threshold $V_{CC(ovp)}$ (typically 26.5 V) that latches the controller off.
- **Clamped Driver Stage**: Despite the high maximum supply voltage, the voltage on DRV pin is safely clamped below 16 V, allowing the use of any standard MOSFET, and reducing the current consumption of the controller.
- **Dual Latch−off Input**: The NCP1236 can be latched off by 2 ways: The voltage increase applied to its Latch pin (typically an overvoltage) or by a decrease this voltage. Thanks to the internal precise pull−up current source a NTC can be directly connected to the latch pin. This NTC will provide an overtemperature protection by decreasing its resistance and consequently the voltage at Latch pin,
- **Soft−Start**: At every start−up the peak current is gradually increased during 4.0 ms to minimize the stress on power components.
- **Temperature Shutdown**: The NCP1236 is internally protected against self−overheating: if the die temperature is too high, the controller shuts all circuitries down (including the HV start−up current source), allowing the silicon to cool down before attempting to restart. This ensures a safe behavior in case of failure.

Typical Operation

- **Start−up**: The HV start−up current source ensures the charging of the V_{CC} capacitor up to the start−up threshold $V_{CC(on)}$, until the input voltage is high enough (above $V_{HV(start)}$) to allow the switching to start. The controller then delivers pulses, starting with a soft−start period t_{SSTART} during which the peak current linearly increases before the current−mode control takes over. During the soft−start period, the low level latch is ignored, and the latch current is double, to ensure a fast pre−charge of the Latch pin decoupling capacitor.
- **Normal operation**: As long as the feedback voltage is within the regulation range and V_{CC} is maintained above $V_{CC(min)}$, the NCP1236 runs at a fixed frequency (with jittering) in current−mode control. The peak current (sensed on the CS pin) is set by the voltage on the FB pin. Fixed ramp compensation is applied internally to prevent sub−harmonic oscillations from occurring.
- **Light load operation**: When the FB voltage decreases below $V_{FB(foldS)}$, typically corresponding to a load of 33 % of the maximum load (for a DCM design), the switching frequency starts to decrease down to $f_{OSC(min)}$. By lowering the switching losses, this feature helps to improve the efficiency in light load conditions. The frequency jittering is enabled in light load operation as well.
- **No load operation**: When the FB voltage decreases below $V_{skip(in)}$, typically corresponding to a load of 2 % of the maximum load, the controller enters skip mode. By completely stopping the switching while the feedback voltage is below $V_{skip(out)}$, the losses are further reduced. This allows minimizing the power dissipation under extremely low load conditions. As the skip mode is entered at very light loads, for which the peak current is very small, there is no risk of audible noise. V_{CC} can be maintained between $V_{CC(on)}$ and $V_{CC(min)}$ by the DSS, if the auxiliary winding does not provide sufficient level of V_{CC} voltage under this condition.
- **Overload**: The NCP1236 features timer−based overload detection, solely dependent on the feedback information: as soon as the internal peak current setpoint hits the V_{ILIM} clamp, an internal timer starts to count. When the timer elapses, the controller stops and enter the protection mode, autorecovery for the B version (the controller initiates a new start−up after $t_{autorec}$ elapses), or latched for the A version (the latch is released if a brown−out event occurs or V_{CC} is reset).
- **Brown−out**: The NCP1236 features a true AC line monitoring circuitry. It includes a minimum start−up threshold and an autorecovery brown−out protection; both of them independent of the ripple on the input voltage. It can even work with an unfiltered, rectified AC input. The thresholds are fixed, but they are designed to fit most of the standard AC−DC conversion applications.
- **Latch−off**: When the Latch input is pulled up (typically by an over−voltage condition), or pulled down (typically by an over−temperature condition, using the provided current source with an NTC), the controller latches off. A voltage higher than $V_{CC(ovp)}$ on the VCC pin has the same effect. The latch is released when a brown−out condition occurs, or when the V_{CC} is reset.

DETAILED DESCRIPTION

High−Voltage Current Source with Built−in Brown−out Detection

The NCP1236 HV pin can be connected either to the rectified bulk voltage, or to the ac line through a rectifier.

Start−up

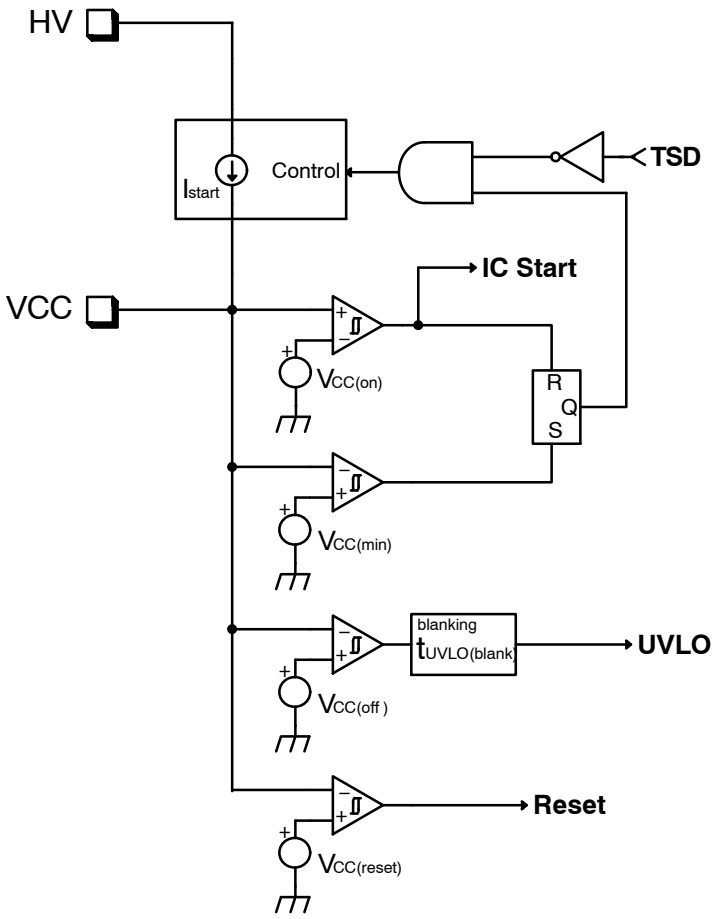


Figure 30. HV Start−up Current Source Functional Schematic

At start−up, the current source turns on when the voltage on the HV pin is higher than $V_{HV(min)}$, and turns off when V_{CC} reaches $V_{CC(on)}$, then turns on again when V_{CC} reaches $V_{CC(min)}$, until the input voltage is high enough to ensure a proper start−up, i.e. when V_{HV} reaches $V_{HV(start)}$. The controller actually starts the next time V_{CC} reaches $V_{CC(on)}$.

Even though the DSS is able to maintain the V_{CC} voltage between $V_{CC(on)}$ and $V_{CC(min)}$ by turning the HV start−up current source on and off, it can only be used in light load condition, otherwise the power dissipation on the die would be too much. As a result, an auxiliary voltage source is needed to supply V_{CC} during normal operation.

The DSS is useful to keep the controller alive when no switching pulses are delivered, e.g. in brown−out condition, or to prevent the controller from stopping during load transients when the V_{CC} might drop.

If the voltage increases above the overvoltage protection threshold $V_{CC(ovp)}$, the controller is latched off.

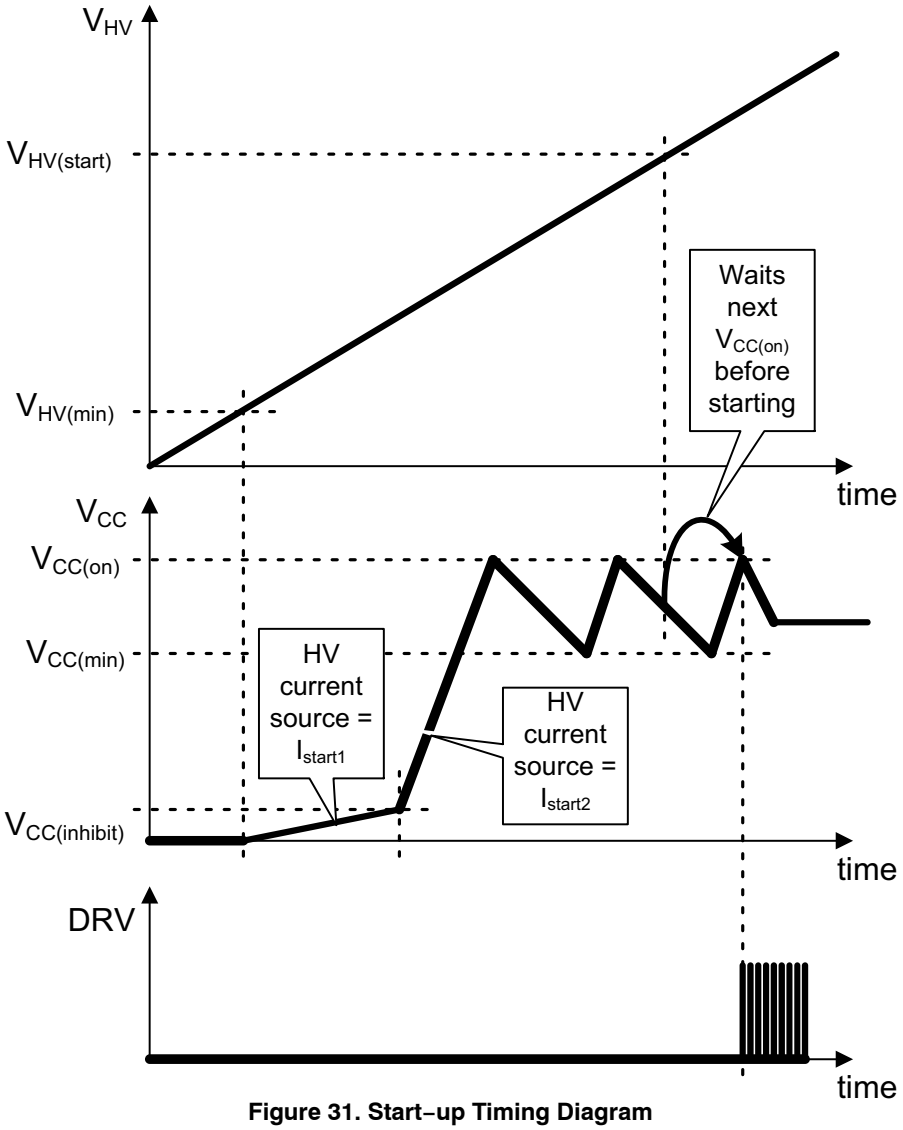


Figure 31. Start−up Timing Diagram

For safety reasons, the start−up current is lowered when V_{CC} is below $V_{CC(inhibit)}$, to reduce the power dissipation in case the V_{CC} pin is shorted to GND (in case of V_{CC} capacitor failure, or external pull−down on V_{CC} to disable the controller).

There are only two conditions for which the current source doesn't turn on when V_{CC} reaches $V_{CC(min)}$: the voltage on HV pin is too low (below $V_{HV(min)}$), or a thermal shutdown condition (TSD) has been detected. In all other conditions, the HV current source will always turn on and off to maintain V_{CC} between $V_{CC(min)}$ and $V_{CC(on)}$.

Brown−out protection

When the input voltage goes below $V_{HV(stop)}$, a brown−out condition is detected, and the controller stops. The HV current source alternatively turns on and off to maintain V_{CC} between $V_{CC(on)}$ and $V_{CC(min)}$ until the input voltage is back above $V_{HV(start)}$.

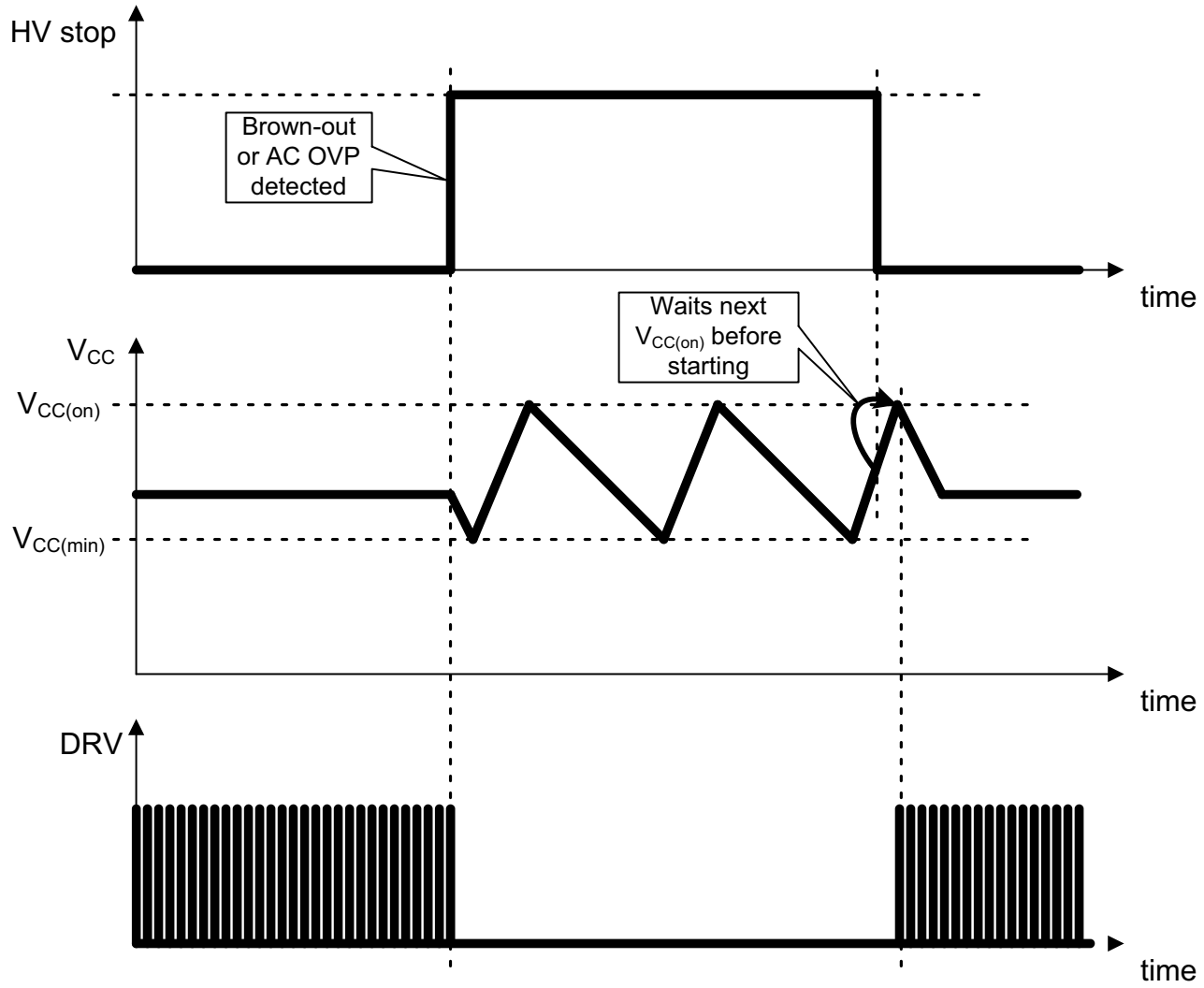


Figure 32. Brown−out Timing Diagram

When V_{HV} crosses the $V_{HV(start)}$ threshold, the controller can start immediately. When it crosses $V_{HV(stop)}$, it triggers a timer of duration t_{HV}: this ensures that the controller doesn't stop in case of line cycle drop−out.

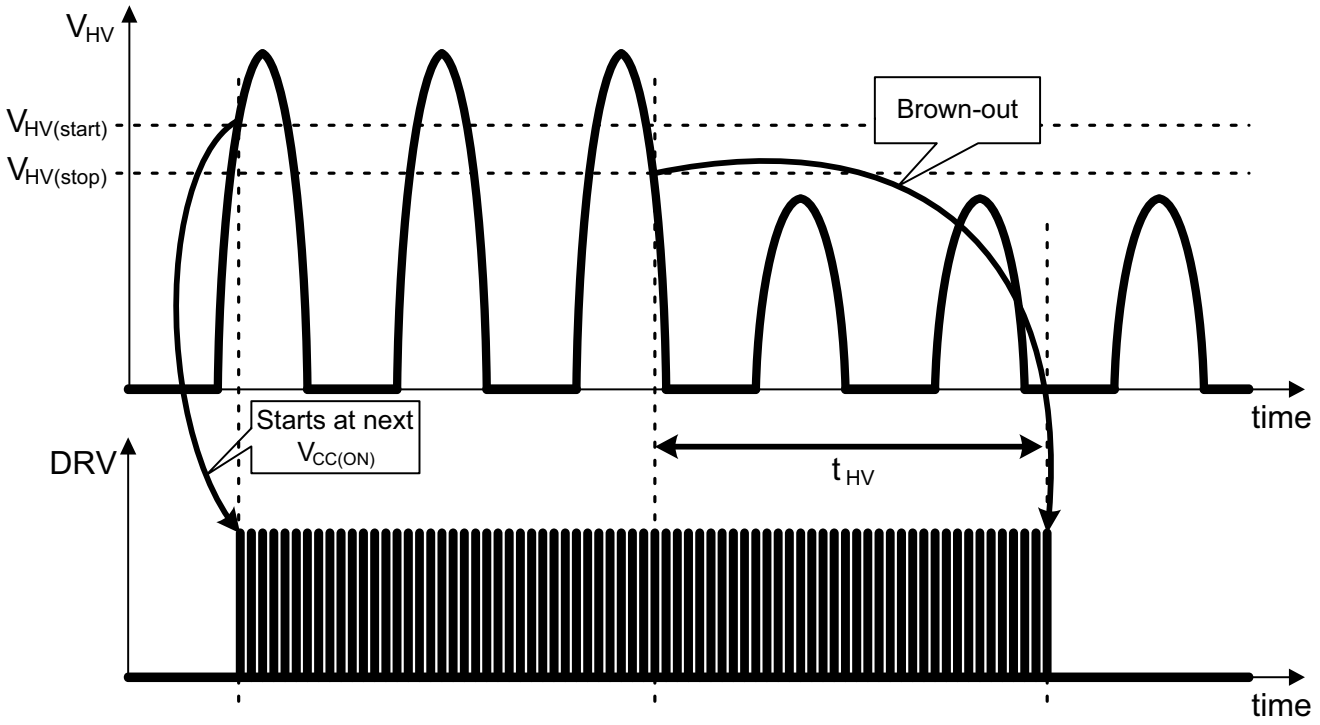


Figure 33. AC Input Brown−out Timing Diagram

Oscillator with Maximum Duty Cycle and Frequency Jittering

The NCP1236 includes an oscillator that sets the switching frequency with an accuracy of ±7%. Two frequency options can be ordered: 65 kHz and 100 kHz. The maximum duty cycle of the DRV pin is 80%, with an accuracy of ±7%.

In order to improve the EMI signature, the switching frequency jitters ±6% around its nominal value, with a triangle−wave shape and at a frequency of 125 Hz. This frequency jittering is active even when the frequency is decreased to improve the EMI in light load condition.

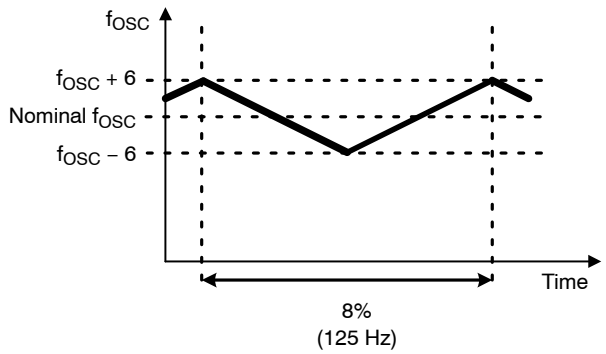


Figure 34. Frequency Jittering

Clamped Driver

The supply voltage for the NCP1236 can be as high as 28 V, but most of the MOSFETs that will be connected to the DRV pin cannot accept more than 20 V on their gate. The driver pin is therefore clamped safely below 16 V. This driver has a typical current capability of ±500 mA.

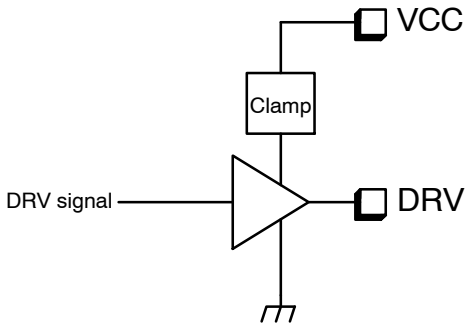


Figure 35. Clamped Driver

CURRENT−MODE CONTROL WITH OVERPOWER COMPENSATION AND SOFT−START

Current sensing

NCP1236 is a current−mode controller, which means that the FB voltage sets the peak current flowing in the inductance and the MOSFET. This is done through a PWM comparator: the current is sensed across a resistor and the resulting voltage is applied to the CS pin. It is applied to one input of the PWM comparator through a 250 ns LEB block. On the other input the FB voltage divided by 5 sets the threshold: when the voltage ramp reaches this threshold, the output driver is turned off.

The maximum value for the current sense is 0.7 V, and it is set by a dedicated comparator.

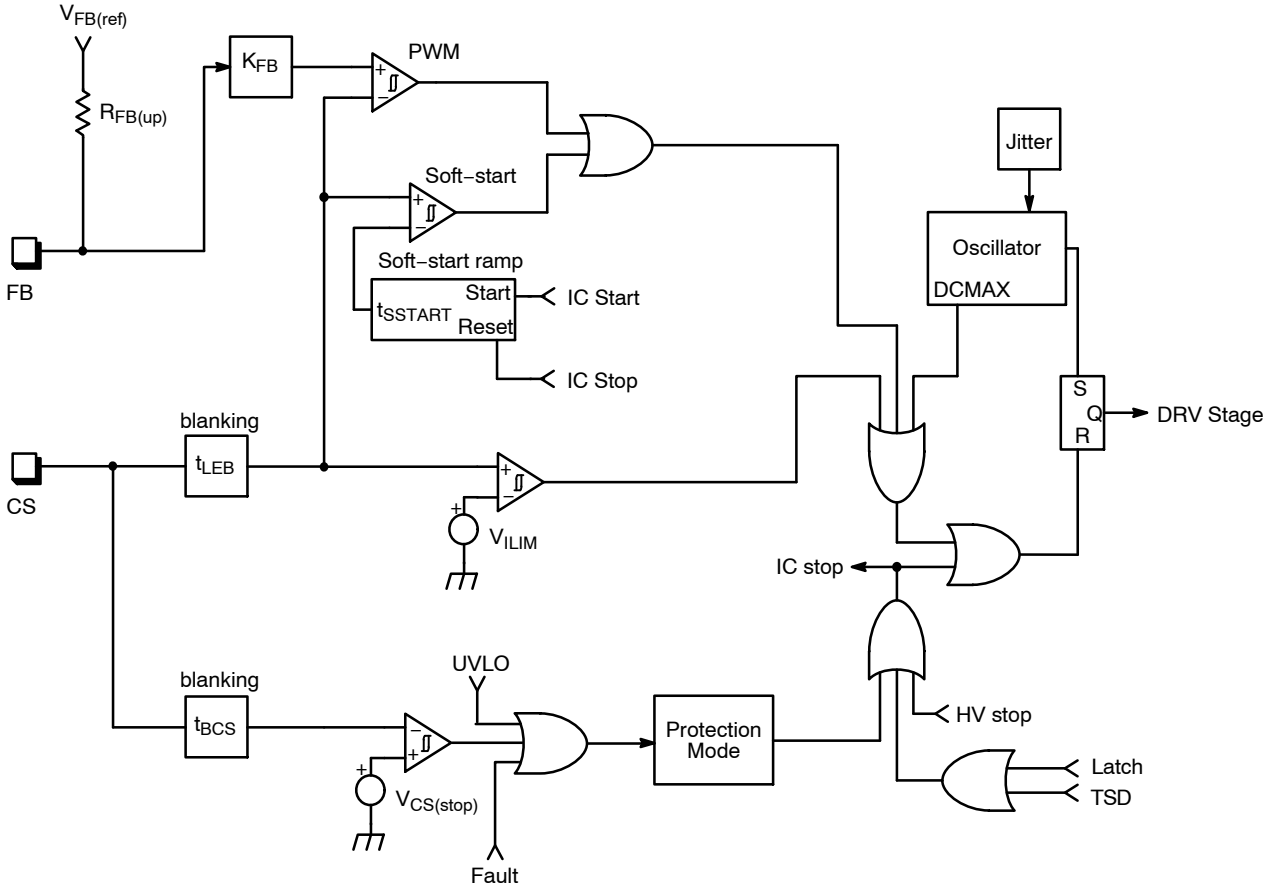


Figure 36. Current Sense Block Schematic

Each time the controller is starting, i.e. the controller was off and starts – or restarts – when V_{CC} reaches $V_{CC(on)}$, a soft−start is applied: the current sense setpoint is linearly increased from 0 (the minimum level can be higher than 0 because of the LEB and propagation delay) until it reaches V_{ILIM} (after a duration of t_{SSTART}), or until the FB loop imposes a setpoint lower than the one imposed by the soft−start (the 2 comparators outputs are OR'ed). The soft−start ramp signal is generated by the D/A converter in the NCP1236, that's why there are observable 15 discrete steps instead the truly linearly increasing current setpoint ramp.

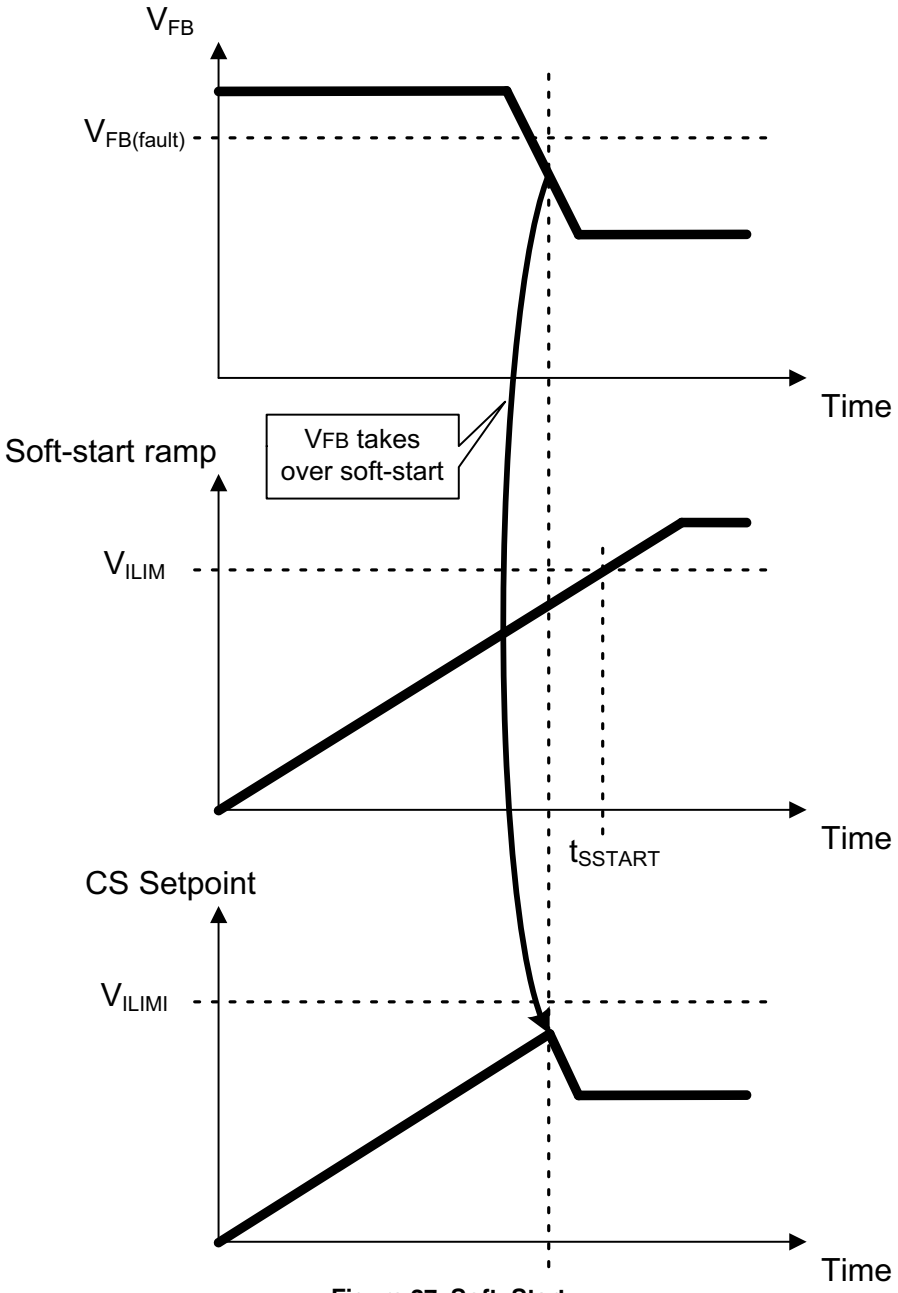


Figure 37. Soft−Start

Under some conditions, like a winding short−circuit for instance, not all the energy stored during the *on* time is transferred to the output during the *off* time, even if the on time duration is at its minimum (imposed by the propagation delay of the detector added to the LEB duration). As a result, the current sense voltage keeps on increasing above V_{ILIM}, because the controller is blind during the LEB blanking time. Dangerously high current can grow in the system if nothing is done to stop the controller. That's what the additional comparator, that senses when the current sense voltage on CS pin reaches $V_{CS(stop)}$ (= 1.5 x V_{ILIM}), does: as soon as this comparator toggles, the controller immediately enters the protection mode (latched or autorecovery according to the chosen option).

Overpower compensation

The power delivered by a flyback power supply is proportional to the square of the peak current in the discontinuous conduction mode:

$$P_{OUT} = \frac{1}{2} \cdot \eta \cdot L_p \cdot F_{SW} \cdot I_p{}^2 \qquad \text{(eq. 1)}$$

Unfortunately, due to the inherent propagation delay of the logic, the actual peak current is higher at high input voltage than at low input voltage, leading to a significant difference in the maximum output power delivered by the power supply.

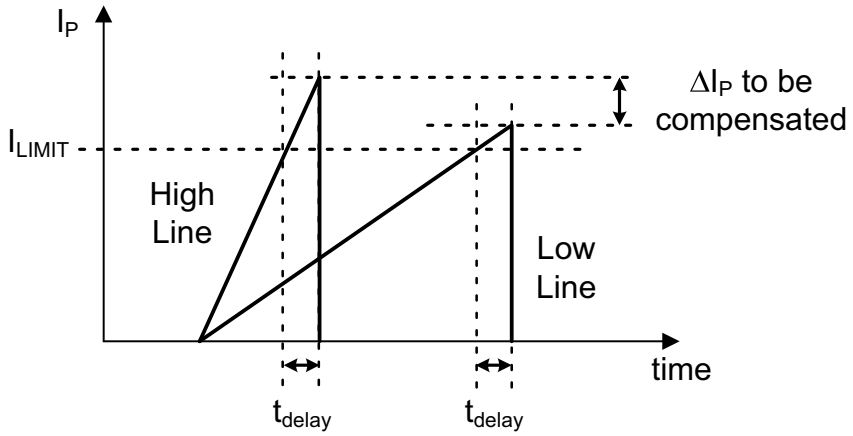


Figure 38. Line Compensation for True Overpower Protection

To compensate this and have an accurate overpower protection, an offset proportional to the input voltage is added on the CS signal by turning on an internal current source: by adding an external resistor in series between the sense resistor and the CS pin, a voltage offset is created across it by the current. The compensation can be adjusted by changing the value of the resistor.

But this offset is unwanted to appear when the current sense signal is small, i.e. in light load conditions, where it would be in the same order of magnitude. Therefore the compensation current is only added when the FB voltage is higher than $V_{FB(OPCE)}$.

However, because the HV pin can be connected to an ac voltage, there is needed an additional circuitry to read or at least closely estimate the actual voltage on the bulk capacitor.

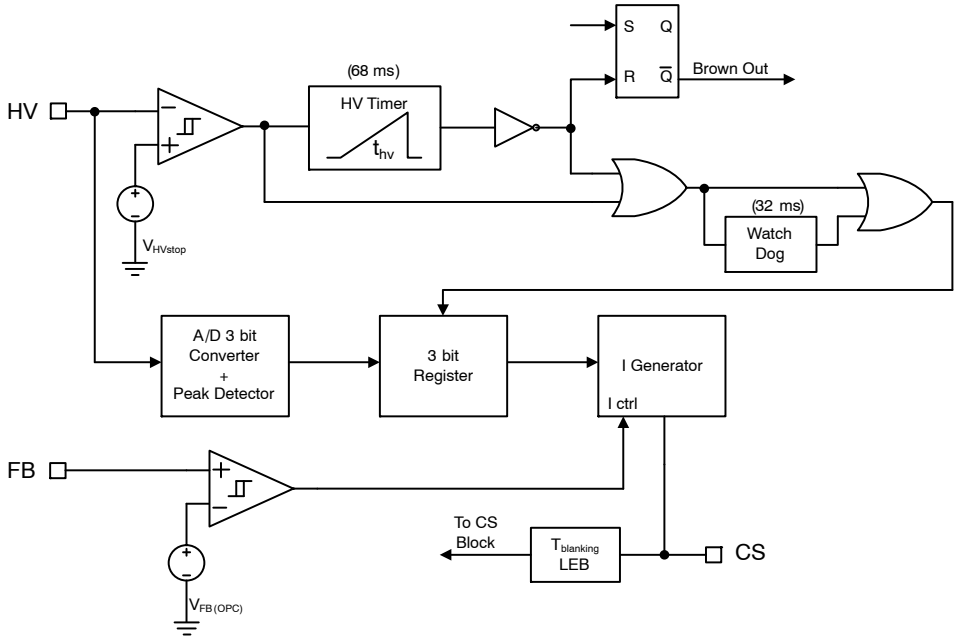


Figure 39. Schematic Overpower Compensation Circuit

A 3 bit A/D converter with the peak detector senses the ac input, and its output is periodically sampled and reset, in order to follow closely the input voltage variations. The sample and reset events are given by the $V_{HV(stop)}$ comparator used for sampling detection for the AC line input. If only the DC high voltage input is used, no reset signal is generated by the $V_{HV(stop)}$ condition and the 32 ms watch dog is used to generate the sampling events for sampling the DC input high voltage line.

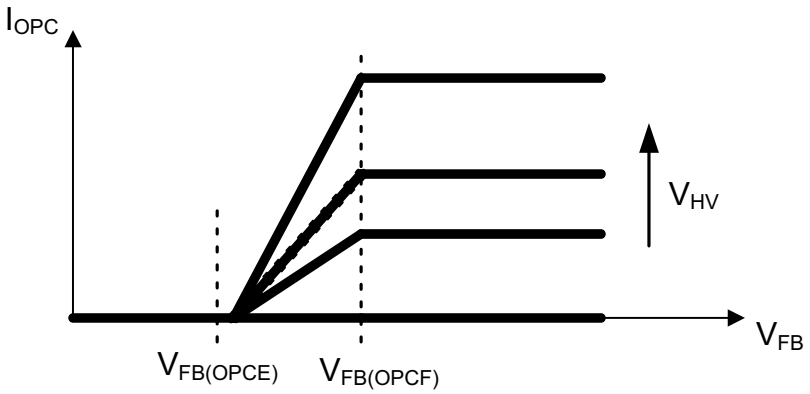


Figure 40. Overpower Compensation Current Relation to Feedback Voltage and Input Voltage

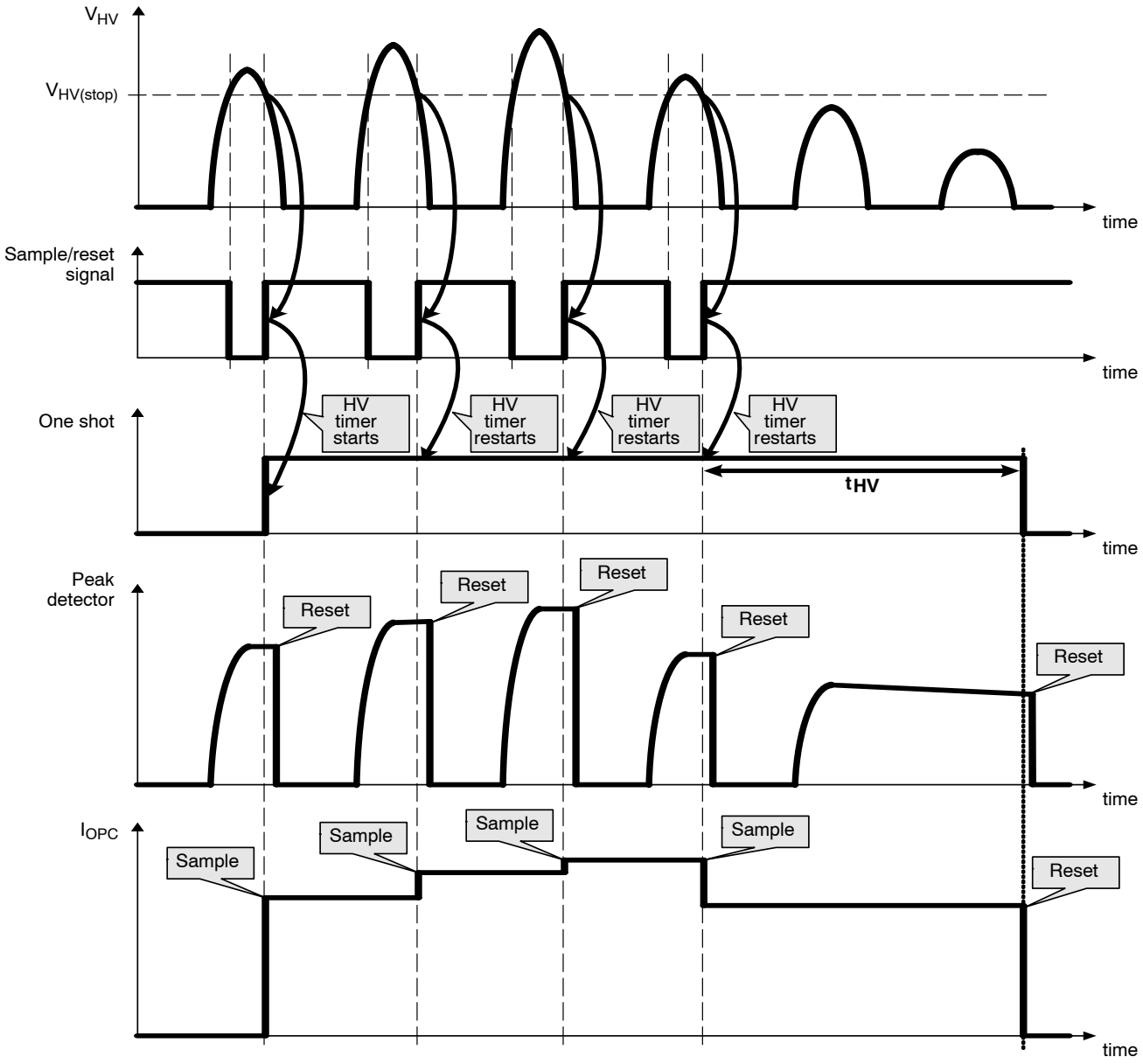


Figure 41. Overpower Compensation

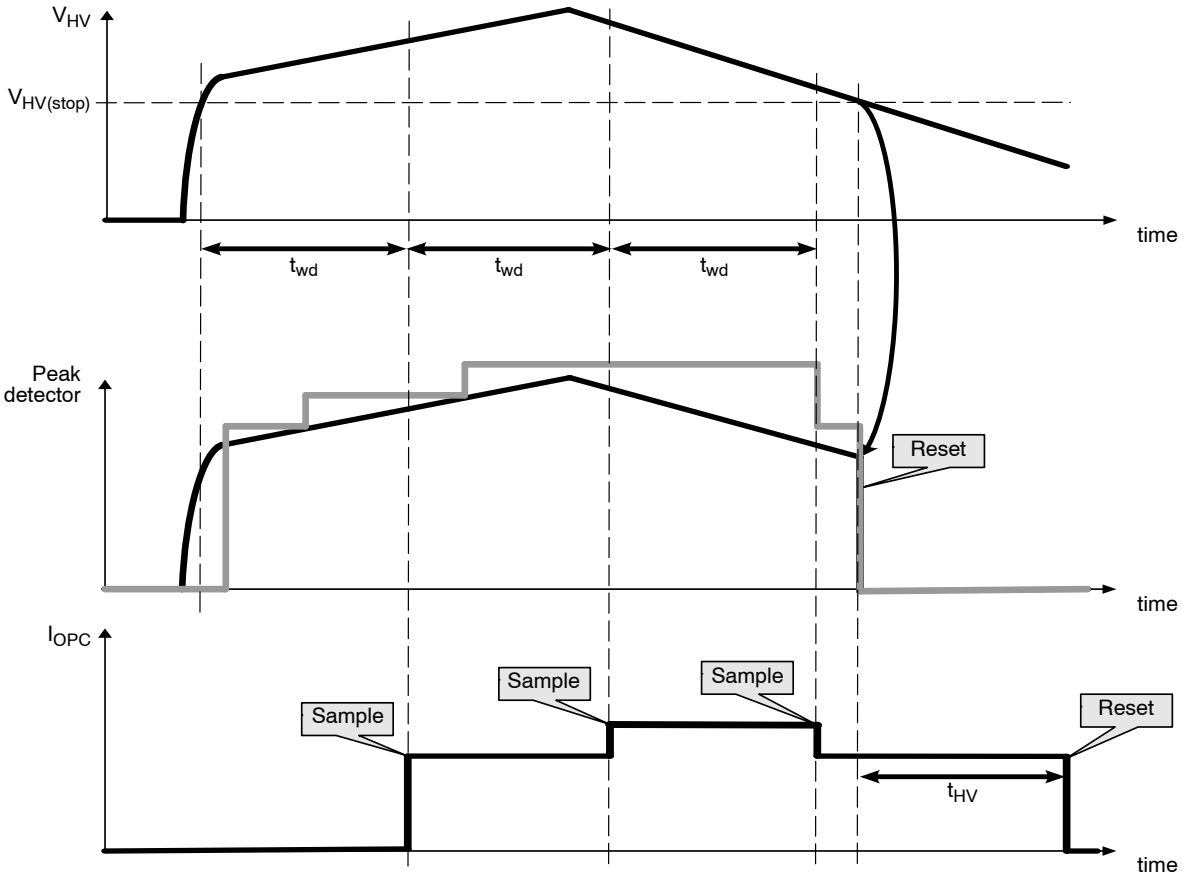


Figure 42. Overpower Compensation

Feedback with Slope Compensation

The ratio from the FB voltage to the current sense setpoint is 5, meaning that the FB voltage corresponding to V_{ILIM} is 3.5 V. There is a pull−up resistor of 20 kΩ from FB pin to an internal reference.

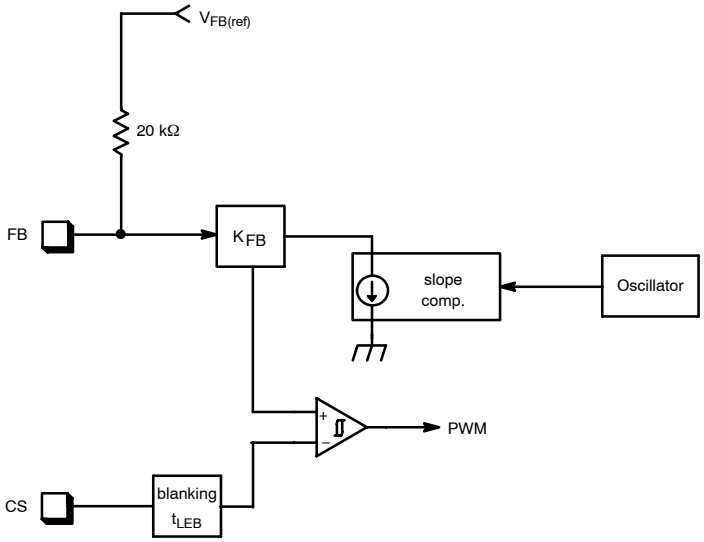


Figure 43. FB Circuitry

In order to allow the NCP1236 to operate in CCM with a duty cycle above 50 %, a fixed slope compensation is internally applied to the current−mode control. The slope appearing on the internal voltage setpoint for the PWM comparator is −32.5 mV/μs typical for the 65 kHz version, and −50 mV/μs for the 100 kHz version.

Overcurrent protection with Fault timer

When an overcurrent occurs on the output of the power supply, the FB loop asks for more power than the controller can deliver, and the CS setpoint reaches V_{ILIMIT}. When this event occurs, an internal t_{fault} timer is started: once the timer elapsed, DRV pulses are stopped and the controller is either latched off (latched protection, version A), or it enters an autorecovery mode (version B). The timer is reset when the CS setpoint goes back below V_{ILIM} before the timer elapses. The fault timer is also started if the driver signal is reset by the max duty cycle.

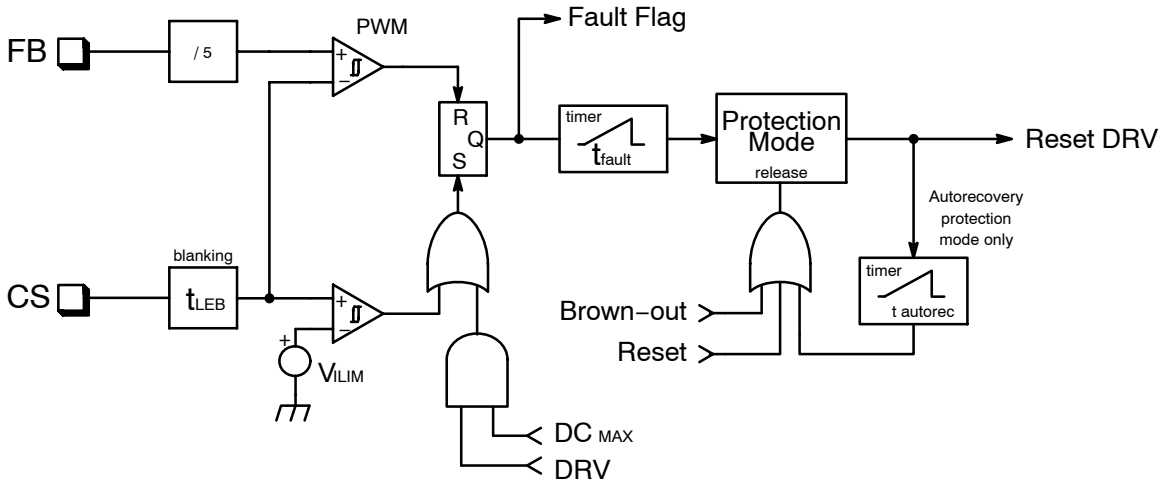


Figure 44. Timer−Based Overcurrent Protection

In autorecovery mode, the controller tries to restart after $t_{autorec}$. If the fault has gone, the supply resumes operation; if not, the system starts a new burst cycle.

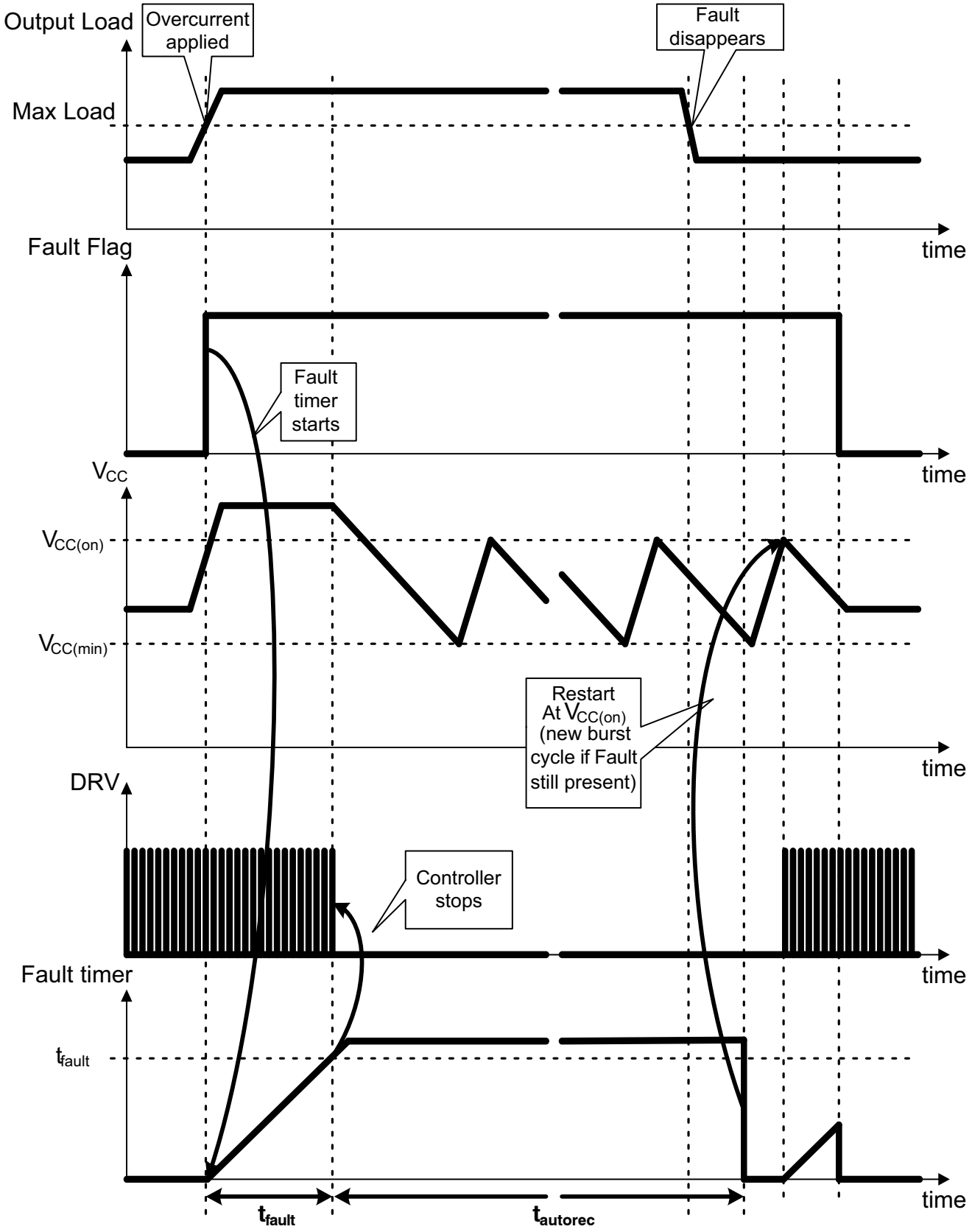


Figure 45. Autorecovery Timer−Based Protection Mode

In the latched version, the controller can restart only if a brown−out or a V_{CC} reset occurs, which in a real application can only happen if the power supply is unplugged from the mains line.

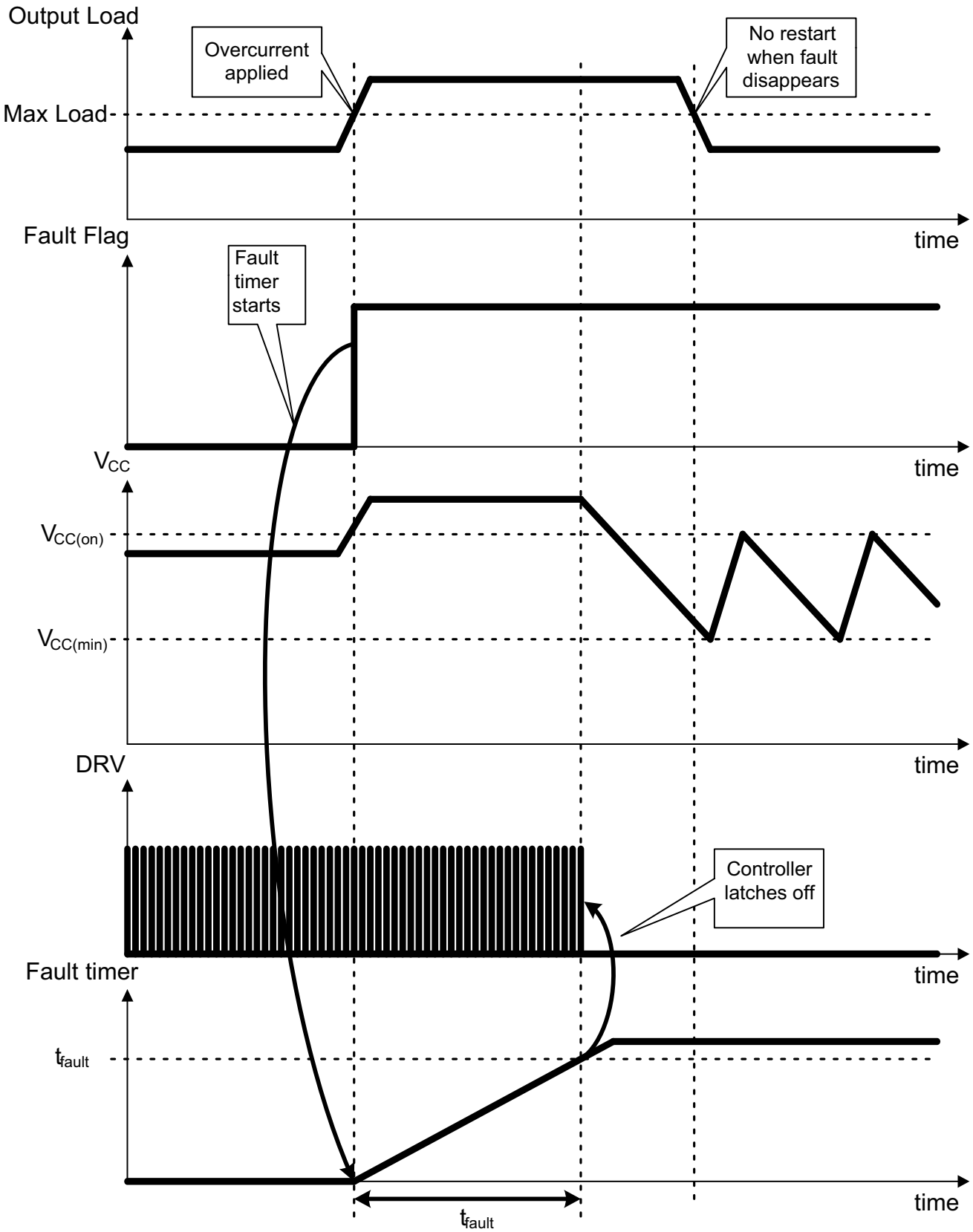


Figure 46. Latched Timer−Based Overcurrent Protection

LOW LOAD OPERATION

Frequency Foldback

In order to improve the efficiency in light load conditions, the frequency of the internal oscillator is linearly reduced from its nominal value down to $f_{OSC(min)}$. This frequency foldback starts when the voltage on FB pin goes below $V_{FB(foldS)}$, and is complete before V_{FB} reaches $V_{skip(in)}$, whatever the nominal switching frequency option is. The current−mode control is still active while the oscillator frequency decreases. Note that the frequency foldback is disabled if the controller runs at its maximum duty cycle.

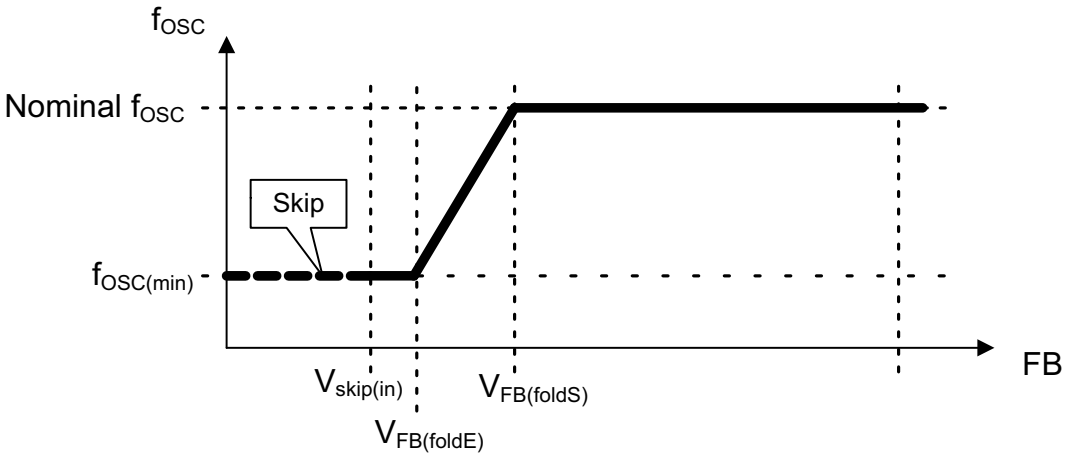


Figure 47. Frequency Foldback when the FB Voltage Decreases

Skip Cycle Mode

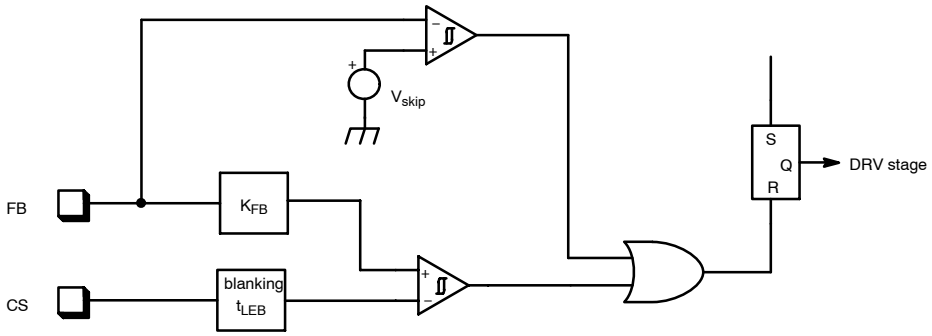


Figure 48. Skip Cycle Schematic

When the FB voltage reaches $V_{skip(in)}$ while decreasing, skip mode is activated: the driver stops, and the internal consumption of the controller is decreased. While V_{FB} is below $V_{skip(out)}$, the controller remains in this state; but as soon as V_{FB} crosses the skip out threshold, the DRV pin starts to pulse again.

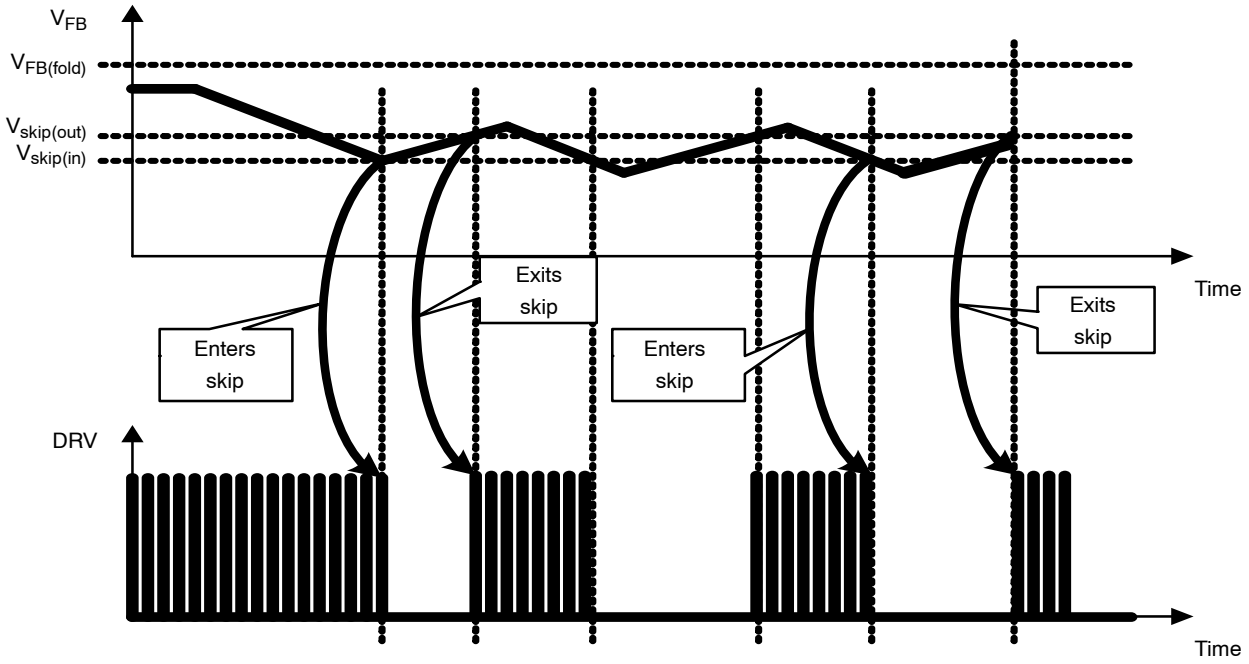


Figure 49. Skip Cycle Timing Diagram

Latch−off Input

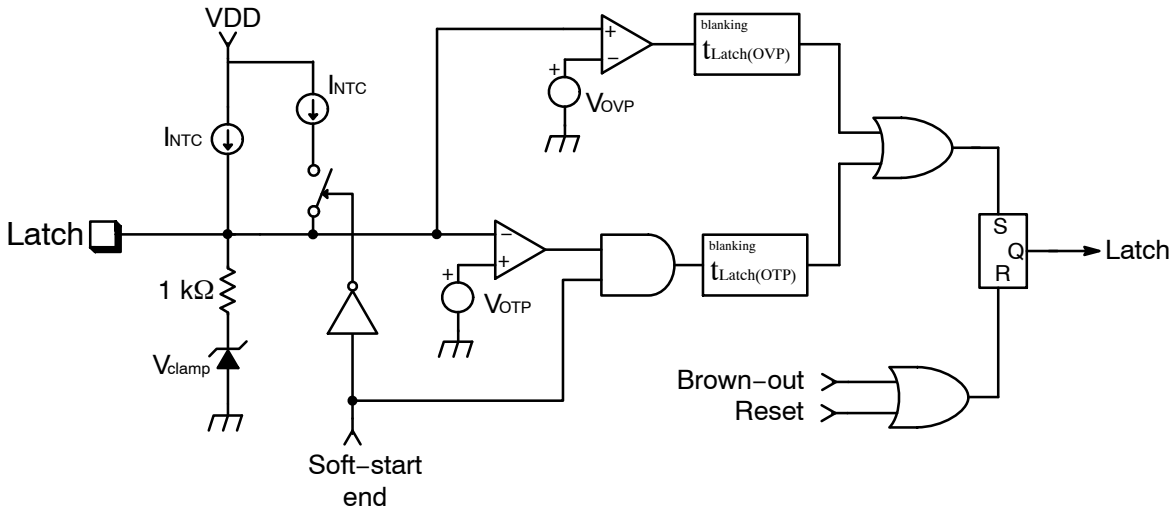


Figure 50. Latch Detection Schematic

The Latch pin is dedicated to the latch−off function: it includes two levels of detection that define a working window, between a high latch and a low latch: within these two thresholds, the controller is allowed to run; but as soon as either the low or the high threshold is crossed, the controller is latched off. The lower threshold is intended to be used with an NTC thermistor, thanks to an internal current source I_{NTC}.

An active clamp prevents the voltage from reaching the high threshold if it is only pulled up by the I_{NTC} current. To reach the high threshold, the pull−up current has to be higher than the pull−down capability of the clamp (typically 1.5 mA at V_{OVP}).

To avoid any false triggering, spikes shorter than 50 μs (for the high latch) or 350 μs (for the low latch) are blanked and only longer signals can actually latch the controller.

Reset occurs when a brown−out condition is detected or the V_{CC} is cycled down to a reset voltage, which in a real application can only happen if the power supply is unplugged from the AC line.

Upon start−up, the internal references take some time before being at their nominal values; so one of the comparators could toggle even if it should not. Therefore the internal logic does not take the latch signal into account before the controller is ready to start: once V_{CC} reaches $V_{CC(on)}$, the latch pin High latch state is taken into account

and the DRV switching starts only if it is allowed; whereas the Low latch (typically sensing an overtemperature) is taken into account only after the soft−start is finished. In addition, the NTC current is doubled to $I_{NTC(SSTART)}$ during the soft−start period, to speed up the charging of the Latch pin capacitor. The maximum value of Latch pin capacitor is given by the following formula (The standard start−up condition is considered and the NTC current is neglected) :

$$C_{LATCHmax} = \frac{t_{SSTARTmin} \cdot I_{NTC(SSTART)min}}{V_{clamp0min}} = \frac{2.8 \cdot 10^{-3} \cdot 130 \cdot 10^{-6}}{1.0} F = 364\ nF \quad \text{(eq. 2)}$$

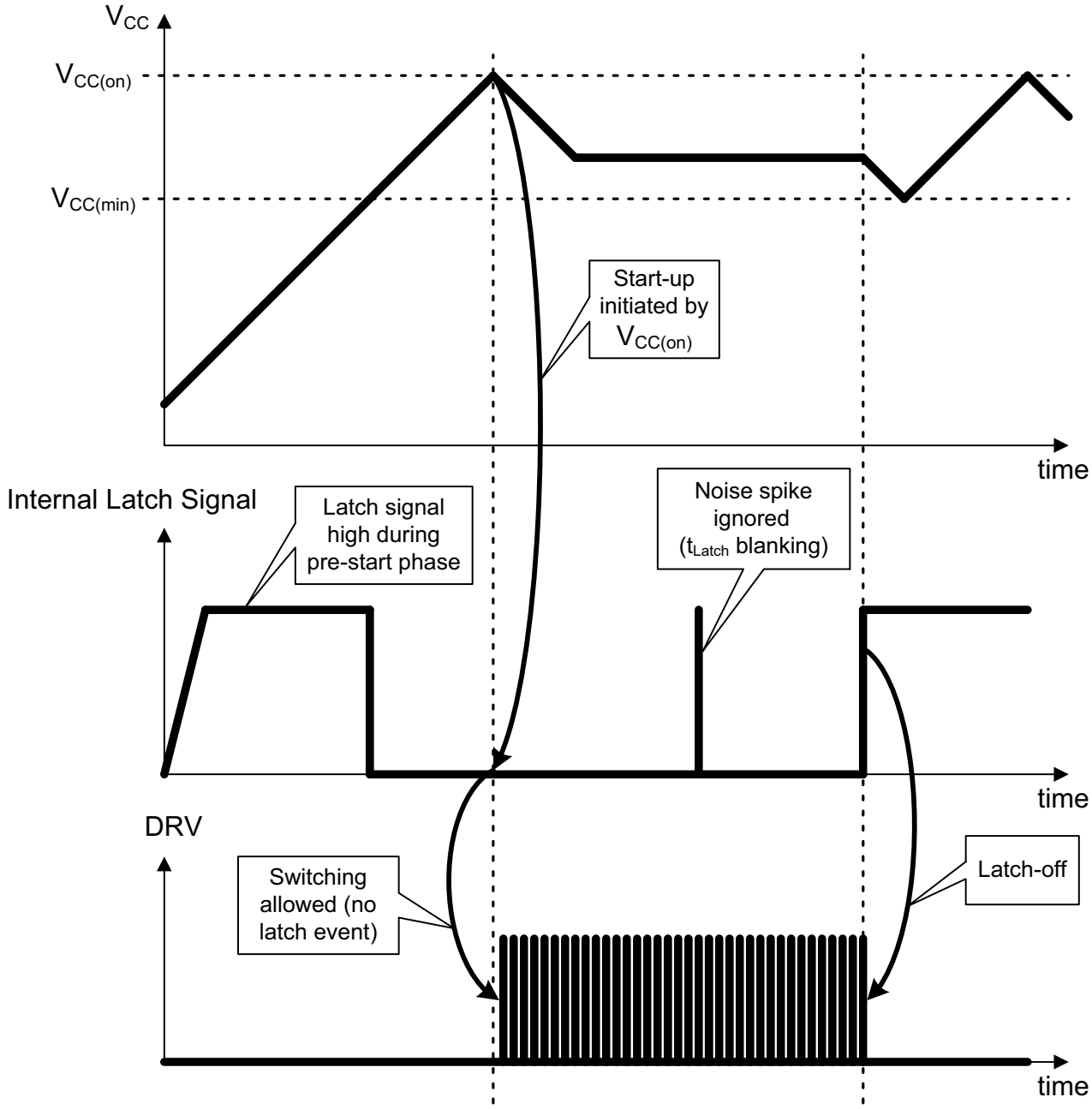


Figure 51. Latch−off Function Timing Diagram

Temperature Shutdown

The die includes a temperature shutdown protection with a trip point guaranteed above 135°C and below 165°C, and a typical hysteresis of 30°C. When the temperature rises above the high threshold, the controller stops switching instantaneously, and the HV current source is turned off. Internal logic state is reset. When the temperature falls below the low threshold, the HV start−up current source is enabled, and a regular start−up sequence takes place.

STATE DIAGRAMS

HV Start−up Current Source

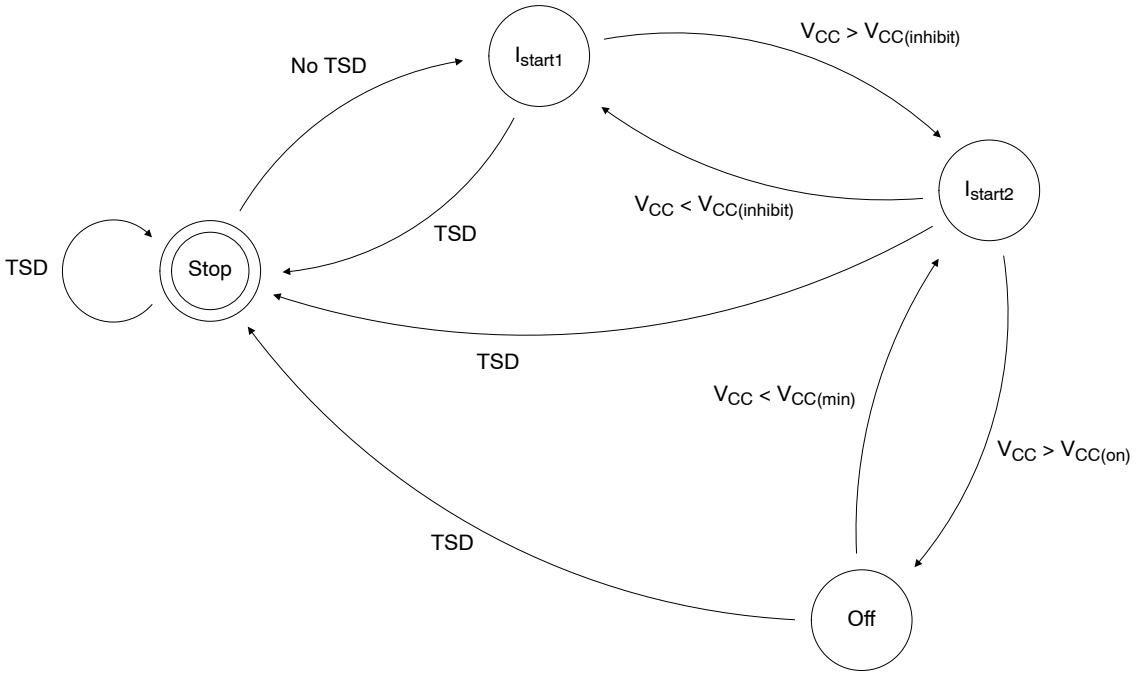


Figure 52. HV Start−up Current Source State Diagram

Controller Operation (Latched Version: A Option)

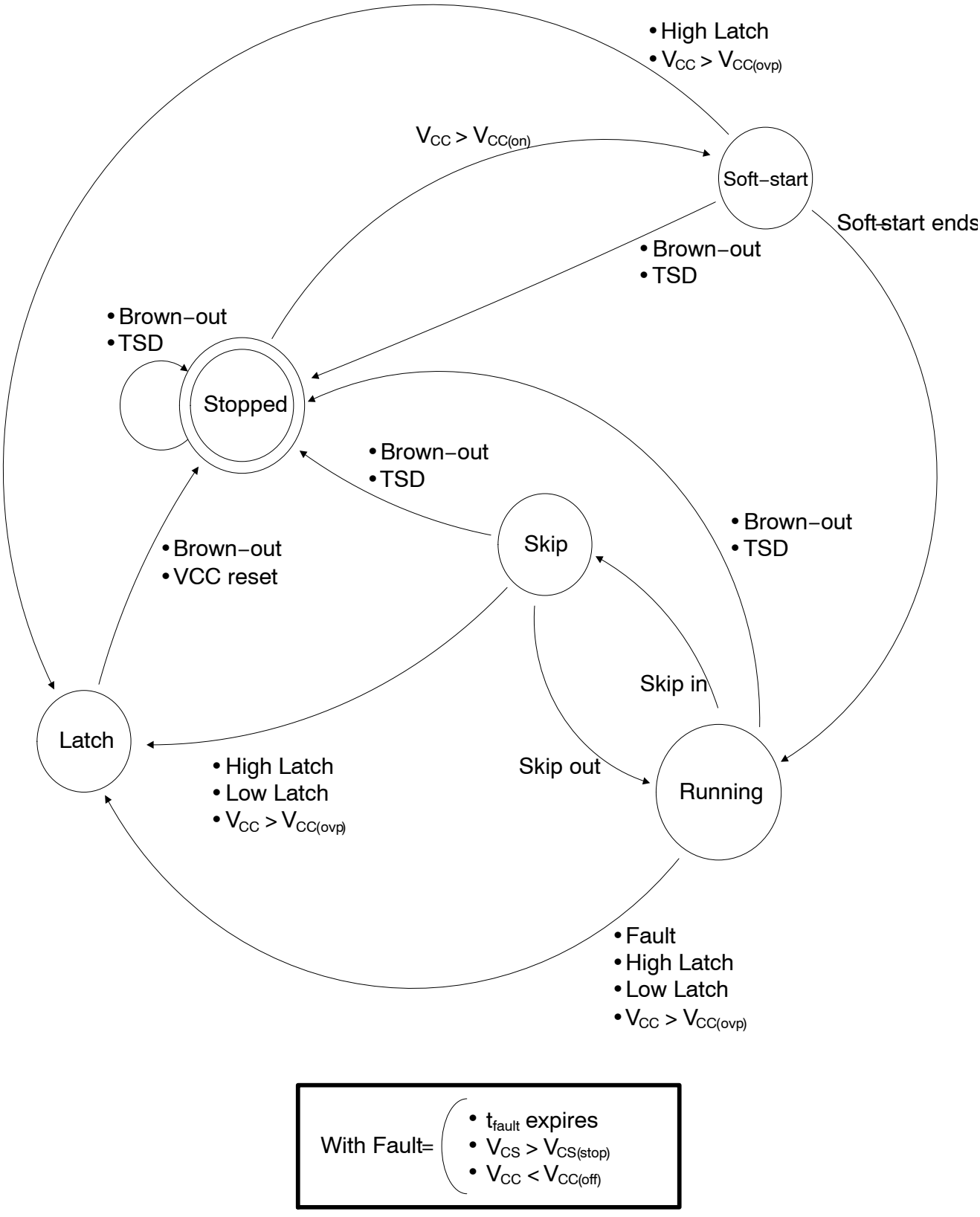


Figure 53. Controller Operation State Diagram (Latched Protection)

Controller Operation (Autorecovery Version: B Option)

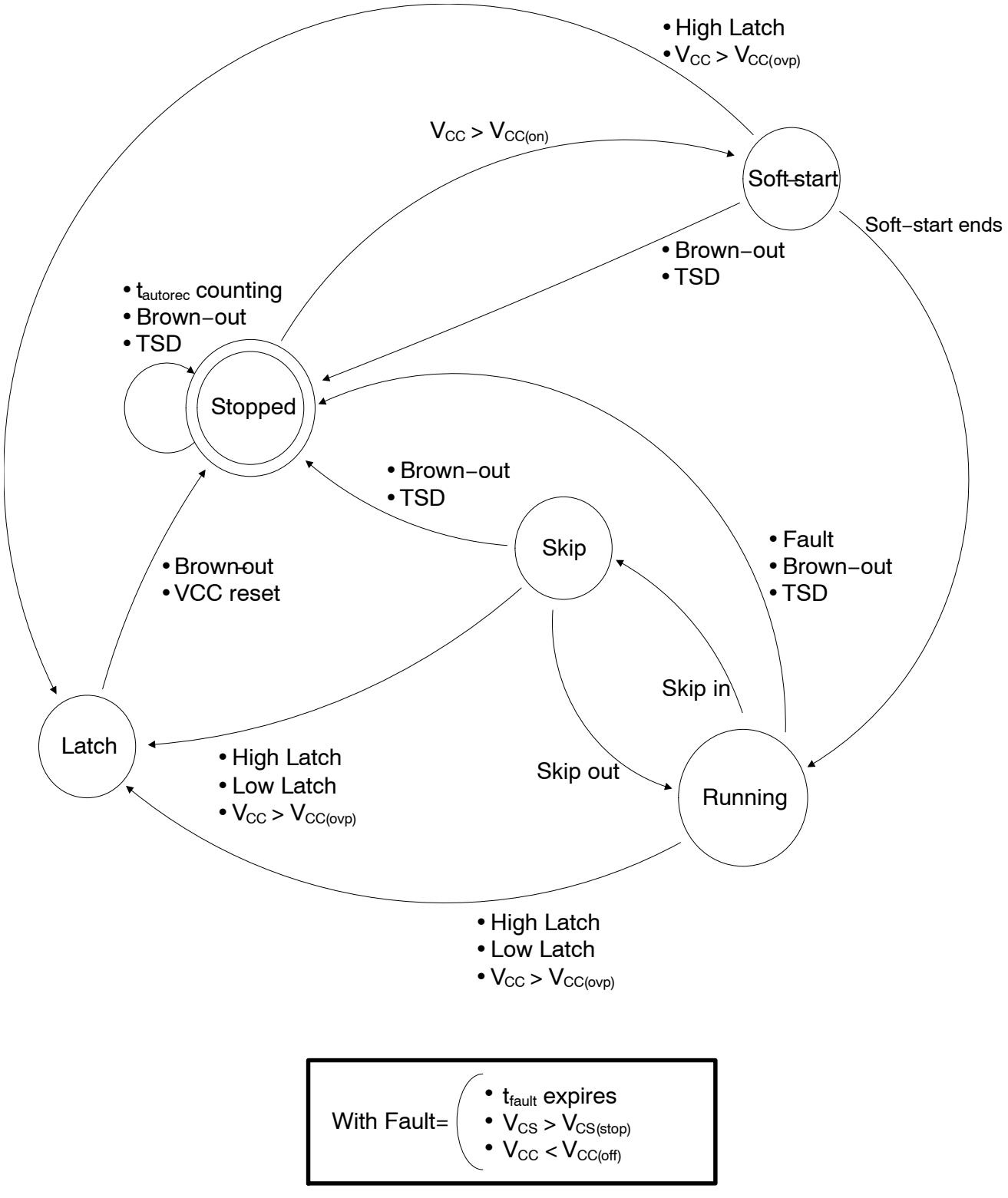


Figure 54. Controller Operation State Diagram (Autorecovery Protection)

Table 1. ORDERING INFORMATION

Part No.	Switching Frequency	Overload Protection	Fault Timer	Package	Shipping†
NCP1236AD65R2G	65 kHz	Latched	128 ms	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP1236AD100R2G	100 kHz	Latched	128 ms		
NCP1236BD65R2G	65 kHz	Autorecovery	128 ms		
NCP1236BD100R2G	100 kHz	Autorecovery	128 ms		
NCP1236CD65R2G (Note 8)	65 kHz	Latched	32 ms		
NCP1236CD100R2G (Note 8)	100 kHz	Latched	32 ms		
NCP1236DD65R2G	65 kHz	Autorecovery	32 ms		
NCP1236DD100R2G (Note 8)	100 kHz	Autorecovery	32 ms		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

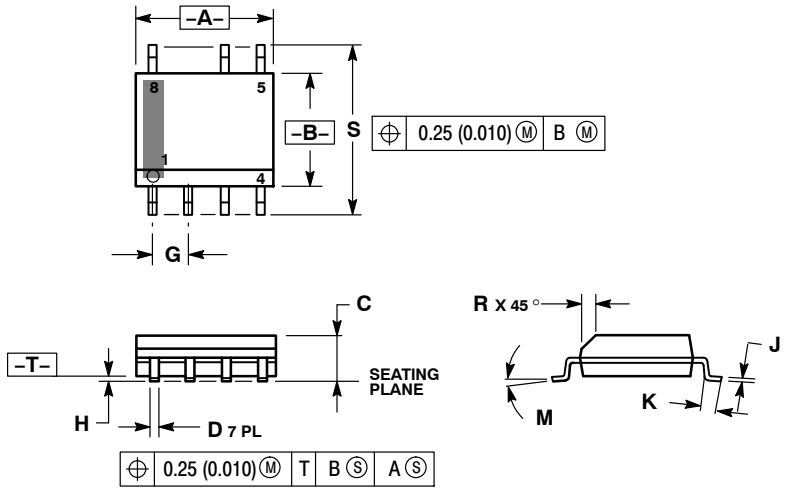
8. Contact your **onsemi** Sales Representative. These parts will be released upon customer request.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−7
CASE 751U
ISSUE E

SCALE 1:1

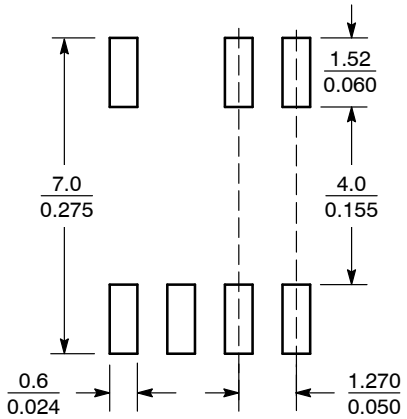
DATE 20 OCT 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

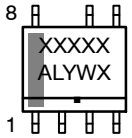
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−7
CASE 751U
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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