Enhanced, High-Efficiency Power Factor Controller NCP1622

The 6−pin PFC controller NCP1622 is designed to drive PFC boost stages. It is based on an innovative **V**alley **S**ynchronized **F**requency **F**old−back (**VSFF**) method. In this mode, the circuit classically operates in **Cr**itical conduction **M**ode (**CrM**) when $V_{control}$ voltage exceeds a programmable value $V_{ctrl,FF}$. When $V_{control}$ is below this preset level $V_{ctrl,FF}$, the NCP1622 (versions [B**] and [D**]) linearly decays the frequency down to about 30 kHz until $V_{control}$ reaches the SKIP mode threshold. **VSFF** maximizes the efficiency at both nominal and light load. In particular, the stand−by losses are reduced to a minimum. Like in **FCCrM** controllers, internal circuitry allows near−unity power factor even when the switching frequency is reduced. Housed in a TSOP6 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

General Features

- Near−Unity Power Factor
- Critical Conduction Mode (CrM)
- Valley Synchronized Frequency Fold−back (VSFF): Low Frequency Operation is Forced at Low Current Levels (9 Pre−programmed Settings)
- Works With or Without a Transformer w/ ZCD Winding (Simple Inductor)
- On−time Modulation to Maintain a Proper Current Shaping in VSFF Mode
- Skip Mode at Very Low Load Current (versions [B**] and [D**])
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer)
- Valley Turn−on
- High Drive Capability: −500 mA / +800 mA
- V_{CC} Range: from 9.5 V to 30 V
- Low Start−up Consumption for:
  - [**C] Version: Low *Vcc* Start−up level (10.5 V)
  - [**A] Version: High *Vcc* Start−up level (17.0 V)
- Line Range Detection for Reduced Crossover Frequency Spread
- This is a Pb−Free Device

Safety Features

- Thermal Shutdown
- Non−latching, Over−Voltage Protection
- Second Over−Voltage Protection
- Brown−Out Detection
- Soft−Start for Smooth Start−up Operation ([**C] Version)
- Over Current Limitation
- Disable Protection if the Feedback Pin is Not Connected
- Low Duty−Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring

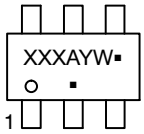
Typical Applications

- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction



TSOP−6
SN SUFFIX
CASE 318G

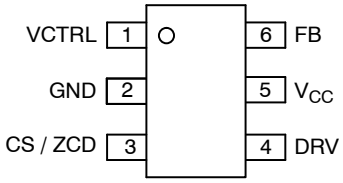
MARKING DIAGRAM



XXX	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2017

DEVICE ORDERING INFORMATION

The coding letters for the product options does not correspond to the marking on the TSOP6 package.
This table shows the correspondence between product option coding and TSOP6 marking.

Operating Part Number (OPN)	L_1, L_2, L_3 Option	Marking	Package Type	Shipping
NCP1622AEASNT1G	AEA	A5A	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP1622BCASNT1G	BCA	3CA		
NCP1622BCCSNT1G	BCC	3CC		
NCP1622BECSNT1G	BEC	3EC		
NCP1622DCCSNT1G	DCC	DC6		

NOTE: Other L_1, L_2, L_3 options are available upon request.

Several product configurations coded with three letters (L_1, L_2, L_3) will be available.

Table 1. NCP1622 1st LETTER CODING OF PRODUCT VERSIONS

L_1	Brown−out Function	Skip Mode Function
A (default)	NO (default)	NO (default)
B	NO (default)	YES (trim)
C	YES (trim)	NO (default)
D	YES (trim)	YES (trim)

Table 2. NCP1622 2nd LETTER CODING OF PRODUCT VERSIONS

L_2	CrM to DCM V_{CTRL} Threshold (V)	$t_{ON,max,LL}$ (μs)	$t_{ON,max,HL}$(μs)
A	0.816	25	8.33
B	1.026	25	8.33
C	1.296	25	8.33
D	1.132	12.5	4.17
E (default)	1.553	12.5	4.17
F	2.079	12.5	4.17
G	1.459	8.3	2.77
H	2.079	8.3	2.77
I	2.840	8.3	2.77
J	0.816	30	10
K	1.026	30	10
L	1.296	30	10

Table 3. NCP1622 3rd LETTER CODING OF PRODUCT VERSIONS

L_3	V_{CC} Startup Level (V)
A (default)	17.0(default)
C	10.5

The non−trimmed (default) version of the product, will be then coded AEA (L_1=A, L_2=E, L_3=A)

L_1 = A meaning NO Brow−out and NO SKIP Mode

L_2 = E meaning E version of Frequency Foldback

L_3 = A meaning 17V V_{CC} Startup voltage

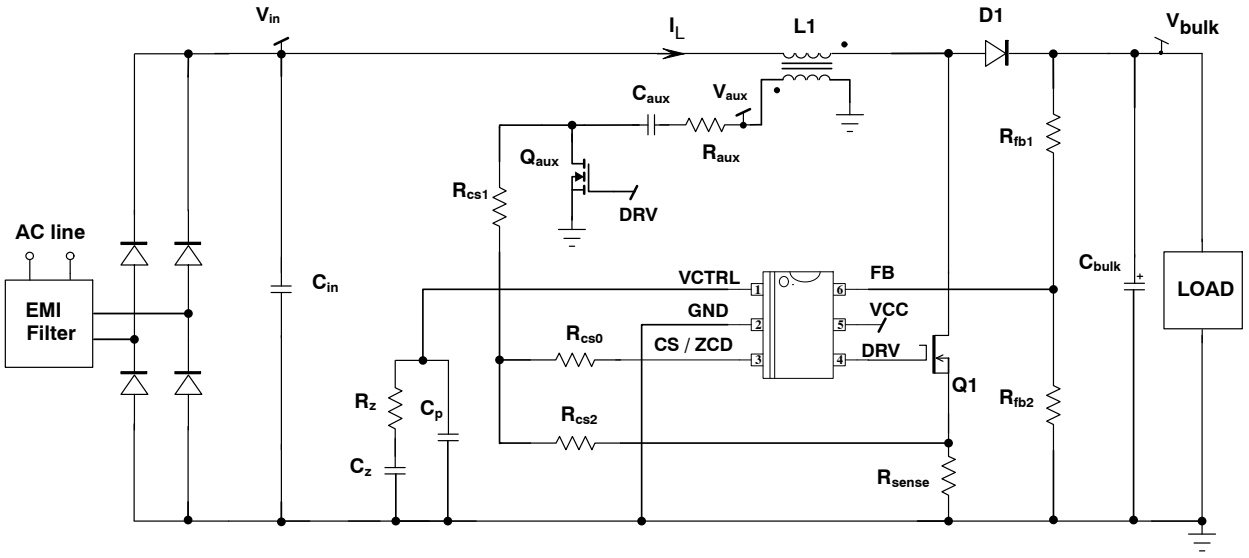


Figure 1. NCP1622 Application Schematic using Auxiliary Winding Voltage

Table 4. DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	VCTRL	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. VCTRL pin is internally pulled down when the circuit is off so that when it starts operation, the power increases slowly to provide a soft−start function. VCTRL pin must not be controlled or pulled down externally.
2	GND	Connect this pin to the PFC stage ground.
3	CS / ZCD	This pin monitors the MOSFET current to limit its maximum current. This pin is the output of a resistor bridge connected between the drain and the source of the power MOSFET. Internal circuitry takes care of extracting V_{in}, V_{out}, I_{ind} and ZCD
4	DRV	The high−current capability of the totem pole gate drive (−0.5 / +0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
5	VCC	This pin is the positive supply of the IC. The circuit starts to operate when VCC exceeds 17.0 V ([**A] Versions) or 10.5 V ([**C] Versions) and turns off when VCC goes below 9.0 V (typical values). After start−up, the operating range is 9.5 V up to 30 V.
6	FB	This pin receives a portion of the PFC output voltage for the regulation and the Dynamic Response Enhancer (DRE) that drastically speeds−up the loop response when the output voltage drops below 95.5% of the desired output level. FB pin voltage V_{FB} is also the input signal for the (non−latching) Over−Voltage (OVP) and Under−Voltage (UVP) comparators. The UVP comparator prevents operation as long as FB pin voltage is lower than V_{UVPH} internal voltage reference. A SOFTOVP comparator gradually reduces the duty−ratio when FB pin voltage exceeds 105% of V_{REF}. If the output voltage still increases, the driver is immediately disabled if the output voltage exceeds 107% of the desired level (fast OVP). A 250 nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently open.

Table 5. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Units
VCTRL	1	$V_{CONTROL}$ pin	−0.3, $V_{ctrl,max}$(*)	V
CS/ZCD	3	CS/ZCD Pin	−0.3, +9	V
DRV	4	Driver Voltage Driver Current	−0.3, V_{DRV} (*) −500, +800	V mA
VCC	5	Power Supply Input	−0.3, + 30	V
VCC	5	Maximum (dV/dt) that can be applied to VCC	TBD upon test engineer measurements	V/s
FB	6	Feedback Pin	−0.3, +9	V
P_D $R_{\theta JA}$		Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 550 145	 mW °C/W
T_J		Operating Junction Temperature Range	−40 to+125	°C
$T_{J,max}$		Maximum Junction Temperature	150	°C
$T_{S,max}$		Storage Temperature Range	−65 to 150	°C
$T_{L,max}$		Lead Temperature (Soldering, 10 s)	300	°C
MSL		Moisture Sensitivity Level	1	−
ESD Capability Human Body Model per JEDEC Standard JESD22−A114F Charge Device Model per JEDEC Standard JESD22−C101F Machine Model per JEDEC Standard JESD22−A115C			 3000 1000 200	V
Latch−Up Protection per JEDEC Standard JESD78			±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*"$V_{ctrl,max}$" is the VCTRL pin clamp voltage. "V_{DRV}" is the DRV clamp voltage ($V_{DRVhigh}$) if V_{CC} is higher than ($V_{DRVhigh}$). "V_{DRV}" is V_{CC} otherwise.

Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: V_{CC} = 18 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 1)

Symbol	Rating	Min	Typ	Max	Unit
Start−up and Supply Circuit					
$V_{CC,on}$	Start−Up Threshold, V_{CC} increasing: [**C] Versions [**A] Versions	 9.75 15.80	 10.50 17.00	 11.25 18.20	V
$V_{CC,off}$	Minimum Operating Voltage, V_{CC} falling	8.50	9.00	9.50	V
$V_{CC,hyst}$	Hysteresis ($V_{CC,on} - V_{CC,off}$) [**C] Versions [**A] Versions	 0.75 6.00	 1.50 8.00	 − −	V
$I_{CC,start}$	Start−Up Current, V_{CC} = 9.4 V, below startup voltage	−	−	70	μA
$I_{CC,op1}$	Operating Consumption, no switching.	−	0.5	1.00	mA
$I_{CC,op2}$	Operating Consumption, 50−kHz switching, no load on DRV pin	−	2.00	3.00	mA
Frequency Fold−back Dead Time for configurations L_2= A,B,C,D,E,F,G,H,I,J,K,L					
$t_{DT,A,1}$	Dead−Time, V_{ctrl} = 0.65V w/ A config	2.00	2.67	3.5	μs
$t_{DT,A,2}$	Dead−Time, V_{ctrl} = 0.75V w/ A config	0.51	0.68	0.85	μs
$t_{DT,B,1}$	Dead−Time, V_{ctrl} = 0.65V w/ B config	5.73	7.64	9.55	μs
$t_{DT,B,2}$	Dead−Time, V_{ctrl} = 0.75V w/ B config	2.91	3.88	4.85	μs
$t_{DT,C,1}$	Dead−Time, V_{ctrl} = 0.65V w/ C config	8.90	11.87	14.84	μs
$t_{DT,C,2}$	Dead−Time, V_{ctrl} = 0.75V w/ C config	5.69	7.58	9.48	μs

1. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: V_{CC} = 18 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{DT,D,1}$	Dead−Time, V_{ctrl} = 0.65V w/ D config	4.98	6.64	8.30	μs
$t_{DT,D,2}$	Dead−Time, V_{ctrl} = 0.75V w/ D config	2.66	3.55	4.44	μs
$t_{DT,E,1}$	Dead−Time, V_{ctrl} = 0.65V w/ E config	9.96	13.28	16.60	μs
$t_{DT,E,2}$	Dead−Time, V_{ctrl} = 0.75V w/ E config	6.70	8.93	10.80	μs
$t_{DT,F,1}$	Dead−Time, V_{ctrl} = 0.65V w/ F config	13.00	17.33	21.66	μs
$t_{DT,F,2}$	Dead−Time, V_{ctrl} = 0.75V w/ F config	9.97	13.29	16.61	μs
$t_{DT,G,1}$	Dead−Time, V_{ctrl} = 0.65V w/ G config	7.98	10.64	13.30	μs
$t_{DT,G,2}$	Dead−Time, V_{ctrl} = 0.75V w/ G config	4.79	6.38	7.98	μs
$t_{DT,H,1}$	Dead−Time, V_{ctrl} = 0.65V w/ H config	14.51	19.35	24.19	μs
$t_{DT,H,2}$	Dead−Time, V_{ctrl} = 0.75V w/ H config	10.41	13.88	17.35	μs
$t_{DT,I,1}$	Dead−Time, V_{ctrl} = 0.65V w/ I config	18.11	24.15	30.19	μs
$t_{DT,I,2}$	Dead−Time, V_{ctrl} = 0.75V w/ I config	14.48	19.31	24.14	μs
$t_{DT,J,1}$	Dead−Time, V_{ctrl} = 0.65V w/ J config	2.00	2.67	3.5	μs
$t_{DT,J,2}$	Dead−Time, V_{ctrl} = 0.75V w/ J config	0.51	0.68	0.85	μs
$t_{DT,K,1}$	Dead−Time, V_{ctrl} = 0.65V w/ K config	5.73	7.64	9.55	μs
$t_{DT,K,2}$	Dead−Time, V_{ctrl} = 0.75V w/ K config	2.91	3.88	4.85	μs
$t_{DT,L,1}$	Dead−Time, V_{ctrl} = 0.65V w/ L config	8.90	11.87	14.84	μs
$t_{DT,L,2}$	Dead−Time, V_{ctrl} = 0.75V w/ L config	5.69	7.58	9.48	μs
CrM to DCM threshold and Hysteresis					
$V_{ctrl,th,A}$	V_{ctrl} threshold CrM to DCM mode w/ A config	−10%	0.816	+10%	V
$V_{ctrl,th,B}$	V_{ctrl} threshold CrM to DCM mode w/ B config	0.923	1.026	1.129	V
$V_{ctrl,th,C}$	V_{ctrl} threshold CrM to DCM mode w/ C config	1.16	1.29	1.43	V
$V_{ctrl,th,D}$	V_{ctrl} threshold CrM to DCM mode w/ D config	−10%	1.132	+10%	V
$V_{ctrl,th,E}$	V_{ctrl} threshold CrM to DCM mode w/ E config	1.398	1.553	1.708	V
$V_{ctrl,th,F}$	V_{ctrl} threshold CrM to DCM mode w/ F config	−10%	2.079	+10%	V
$V_{ctrl,th,G}$	V_{ctrl} threshold CrM to DCM mode w/ G config	−10%	1.459	+10%	V
$V_{ctrl,th,H}$	V_{ctrl} threshold CrM to DCM mode w/ H config	−10%	2.079	+10%	V
$V_{ctrl,th,I}$	V_{ctrl} threshold CrM to DCM mode w/ I config	−10%	2.840	+10%	V
$V_{ctrl,th,J}$	V_{ctrl} threshold CrM to DCM mode w/ J config	−10%	0.816	+10%	V
$V_{ctrl,th,K}$	V_{ctrl} threshold CrM to DCM mode w/ K config	−10%	1.026	+10%	V
$V_{ctrl,th,L}$	V_{ctrl} threshold CrM to DCM mode w/ L config	−10%	1.296	+10%	V
$V_{ctrl,th,hyst}$	Vctrl threshold DCM to CrM minus Vctrl threshold CrM to DCM , all config	–	100	–	mV
SKIP Control ([B] & [D**] Versions)**					
V_{SKIP-H}	V_{ctrl} pin SKIP Level, $V_{control}$ rising	555	617	678	mV
V_{SKIP-L}	V_{ctrl} pin SKIP Level, $V_{control}$ falling	516	593	665	mV
$V_{SKIP-Hyst}$	V_{ctrl} pin SKIP Hysteresis	–	30	–	mV
Gate Drive					
t_R	Output voltage rise−time @ C_L = 1nF, 10−90% of output signal	–	30	–	ns
t_F	Output voltage fall−time @ C_L = 1nF, 10−90% of output signal	–	20	–	ns
R_{OH}	Source resistance @ 200mV under High VCC	–	10	–	Ω
R_{OL}	Sink resistance @200mV above Low VCC	–	7	–	Ω
$V_{DRV,low}$	DRV pin level for V_{CC} = $V_{CC,off}$ +200mV (10−kΩ resistor between DRV and GND)	8.0	–	–	V

1. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: V_{CC} = 18 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 1)

Symbol	Rating	Min	Typ	Max	Unit
$V_{DRV,high}$	DRV pin level at V_{CC} = 30 V (R_L = 33 kΩ & C_L = 1 nF)	10	12	14	V
Regulation Block					
V_{REF}	Feedback Voltage Reference	2.44	2.50	2.56	V
I_{EA}	Error Amplifier Current Capability,sinking and sourcing	15	20	26	μA
G_{EA}	Error Amplifier Gain	110	200	290	μS
V_{ctrl} $V_{ctrl,min}$ $V_{ctrl,max}$	*VCTRL* pin Voltage (V_{ctrl}): – @ V_{FB} = 2 V (OTA is sourcing 20 μA) – @ V_{FB} = 3 V (OTA is sinking 20 μA)	 – –	 4.5 0.5	 – –	V
$V_{out,}L$ / V_{REF}	Ratio (V_{out} Low Detect Threshold / V_{REF}) (guaranteed by design)	–	95.5	–	%
$H_{out,}L$ / V_{REF}	Ratio (V_{out}Low Detect Hysteresis / V_{REF}) (guaranteed by design)	–	0.35	–	%
I_{BOOST}	VCTRL pin Source Current when (V_{OUT} Low Detect) is activated	147	220	277	μA
Current Sense and Zero Current Detection Blocks					
$V_{CS(th)}$	Current Sense Voltage Reference	450	500	550	mV
$V_{CS,OVS(th)}$	Current Sense Overstress Voltage Reference	675	750	825	mV
$t_{LEB,OVS}$	"Overstress" Leading edge Blanking Time (guaranteed by design)	–	250	–	ns
$t_{LEB,OCP}$	"Over−Current Protection" Leading edge Blanking Time (guaranteed by design)	–	400	–	ns
t_{OCP}	Over−Current Protection Delay from $V_{CS/ZCD}$>$V_{CS(th)}$ to DRV low ($dV_{CS/ZCD}$ / dt = 10 V/μs)	–	40	200	ns
$V_{ZCD(th)H}$	Zero Current Detection, $V_{CS/ZCD}$ rising	8.0	40	62	mV
$V_{ZCD(th)L}$	Zero Current Detection, $V_{CS/ZCD}$ falling	−68	−50	−25	mV
$V_{ZCD(hyst)}$	Hysteresis of the Zero Current Detection Comparator	46	84	–	mV
$V_{CL(pos)}$	CS/ZCD Positive Clamp @ $I_{CS/ZCD}$ = 5 mA (guaranteed by design)	–	9.5	–	V
t_{ZCD}	($V_{CS/ZCD}$ < $V_{ZCD(th)L}$) to (DRV high)	–	60	200	ns
t_{SYNC}	Minimum ZCD Pulse Width	–	110	200	ns
t_{WDG}	Watch Dog Timer	80	200	320	μs
$t_{WDG(OS)}$	Watch Dog Timer in "OverStress" Situation	400	800	1200	μs
$I_{ZCD(gnd)}$	Source Current for CS/ZCD pin impedance Testing	–	50	–	μA
$I_{ZCD(Vcc)}$	Pull−up current source referenced to V_{cc} for open pin detection	–	200	–	nA
Static OVP					
D_{MIN}	Duty Cycle, V_{FB} = 3 V (When low clamp of V_{ctrl} is reached)	–	–	0	%
On−Time Control (3 options for maximum t_{ON} value)					
$t_{on,LL,ABC}$	Maximum On Time, $avg(V_{cs})$ = 0.9 V and V_{ctrl} maximum (CrM)	22	25	28	μs
$t_{on,LL,JKL}$	Maximum On Time, $avg(V_{cs})$ = 0.9 V and V_{ctrl} maximum (CrM)	25	30	35	μs
$t_{on,LL,DEF}$	Maximum On Time, $avg(V_{cs})$ = 0.9 V and V_{ctrl} maximum (CrM)	11.4	12.5	13.6	μs
$t_{on,LL,GHI}$	Maximum On Time, $avg(V_{cs})$ = 0.9 V and V_{ctrl} maximum (CrM)	7.3	8.3	9.3	μs
$t_{on,HL,ABC}$	Maximum On Time, $avg(V_{cs})$ = 2.8 V and V_{ctrl} maximum (CrM)	7.49	8.33	9.16	μs
$t_{on,HL,JKL}$	Maximum On Time, $avg(V_{cs})$ = 2.8 V and V_{ctrl} maximum (CrM)	8.0	10	12	μs
$t_{on,HL,DEF}$	Maximum On Time, $avg(V_{cs})$ = 2.8 V and V_{ctrl} maximum (CrM)	3.75	4.17	4.59	μs
$t_{on,HL,GHI}$	Maximum On Time, $avg(V_{cs})$ = 2.8 V and V_{ctrl} maximum (CrM)	2.49	2.77	3.05	μs
$K_{ton,LL-HL}$	t_{ON} @LL over t_{ON} @HL ratio (all t_{ON} versions)	–	3	–	w/o
$t_{on,LL,min}$	Minimum On Time, $avg(V_{cs})$ = 0.9 V (not tested, guaranteed by design)	–	300	–	ns
$t_{on,HL,min}$	Minimum On Time, $avg(V_{cs})$ = 2.8 V (not tested, guaranteed by design)	–	200	–	ns

1. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: V_{CC} = 18 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 1)

Symbol	Rating	Min	Typ	Max	Unit
Feed−back Over and Under−Voltage Protections (OVP and UVP)					
$R_{softOVP}$	Ratio (Soft OVP Threshold, V_{FB} rising) over V_{REF} (or V_{REF2}) (guaranteed by design)	−	105	−	%
$R_{softOVP(HYST)}$	Ratio (Soft OVP Hysteresis) over V_{REF} (or V_{REF2}) (guaranteed by design)	−	1.87	−	%
$R_{fastOVP}$	Ratio (Fast OVP Threshold, V_{FB} rising) over V_{REF} (or V_{REF2}) (guaranteed by design)	−	107	−	%
$R_{fastOVP(HYST)}$	Ratio (Fast OVP Hysteresis) over V_{REF} (or V_{REF2}) (guaranteed by design)	−	4.0	−	%
V_{UVPH}	UVP Threshold, V_{FB} increasing	477	530	583	mV
V_{UVPL}	UVP Threshold, V_{FB} decreasing	252	303	357	mV
$V_{UVP(HYST)}$	UVP Hysteresis	200	225	250	mV
$I_{B,FB}$	FB pin Bias Current @ $V_{FB} = V_{OVP}$ and $V_{FB} = V_{UVP}$	50	200	450	nA
Brown−Out Protection and Feed−Forward (Vsns is an internal pin that replaces Vsense)					
V_{BOH}	Brown−Out Threshold V_{mains} increasing, V_{FB} based ([C**] and [D**] versions)	754	819	894	mV
V_{BOL}	Brown−Out Threshold, V_{mains} decreasing, avg(V_{CS}) based ([C**] and [D**] versions)	659	737	801	mV
$V_{BO(HYST)}$	Brown−Out Comparator Hysteresis ([C**] and [D**] versions)	75	100	−	mV
$t_{BO(blank)}$	Brown−Out Blanking Time ([C**] and [D**] versions)	36	50	67	ms
$I_{VCTRL(BO)}$	VCTRL pin sink current during BO condition	20	30	42	μA
V_{HL}	Comparator Threshold for Line Range Detection, avg(V_{CS}) rising	1.605	1.690	1.774	V
V_{LL}	Comparator Threshold for Line Range Detection, avg(V_{CS}) falling	1.406	1.480	1.554	V
$V_{HL(hyst)}$	Comparator Hysteresis for Line Range Detection	75	100	−	mV
$t_{HL(blank)}$	Blanking Time for Line Range Detection	13	25	43	ms
Thermal Shutdown					
T_{LIMIT}	Thermal Shutdown Threshold	150	−	−	°C
H_{TEMP}	Thermal Shutdown Hysteresis	−	50	−	°C
Second Overvoltage Protection (OVP2)					
$V_{OVP2H,HL}$	OVP2 Threshold, V_{CS} rising, K_{CS} = 138 , @V_{REF2} = 2.5 V	3.048	3.175	3.302	V
$V_{OVP2L,HL}$	OVP2 Threshold, V_{CS} falling, K_{CS} = 138, @V_{REF2} = 2.5 V	2.969	3.093	3.217	V
$V_{OVP2(HYST),HL}$	OVP2 Comparator Hysteresis, K_{CS} = 138, @V_{REF2} = 2.5 V	50	100	−	mV
$t_{LEB,OVP2}$	OVP2 Leading Edge Blanking Time, V_{CS} rising (guaranteed by design)	−	1000	−	ns
$t_{RST(OVP2)}$	Reset Timer for OVP2 latch	400	800	1200	μs

1. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

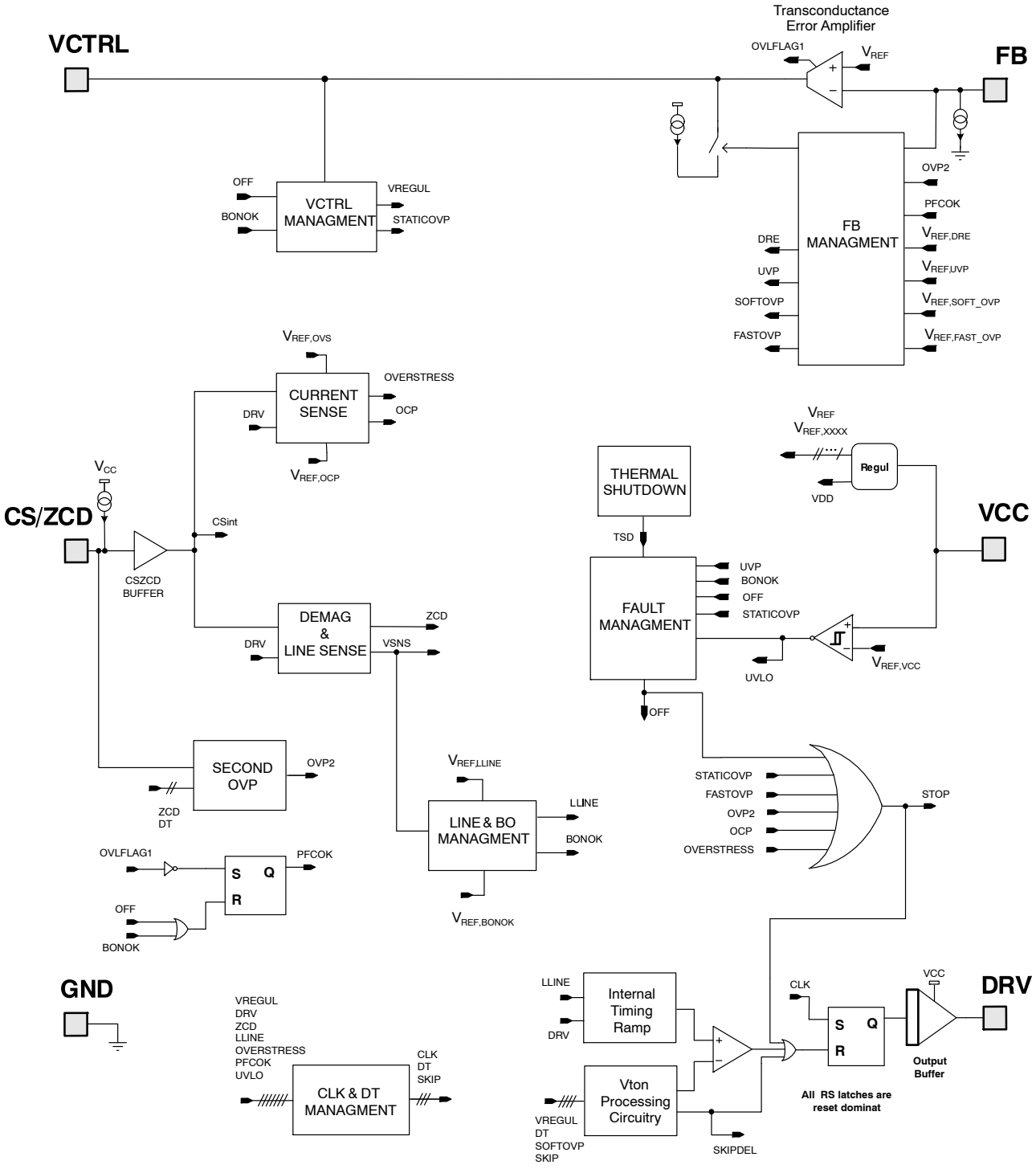


Figure 2. NCP1622 Block Diagram

DETAILED OPERATING DESCRIPTION

Introduction

NCP1622 is designed to optimize the efficiency of your PFC stage throughout the load range. In addition, it incorporates protection features for rugged operation. More generally, NCP1622 is ideal in systems where cost−effectiveness, reliability, low stand−by power and high efficiency are key requirements:

- **Valley Synchronized Frequency Fold−back:** NCP1622 is designed to drive PFC boost stages in so−called *V*alley *S*ynchronized *F*requency *F*old−back (*VSFF*). In this mode, the circuit classically operates in *Cr*itical conduction *M*ode (*CrM*) when V_{ctrl} exceeds a programmable value. When the V_{ctrl} is below this preset level, NCP1622 linearly reduces the frequency down to about 33 kHz before reaching the SKIP threshold voltage (SKIP Mode versions [B**] and [D**]). *VSFF* maximizes the efficiency at both nominal and light load. In particular, stand−by losses are reduced to a minimum. Similarly to *FCCrM* controllers, an internal circuitry allows near−unity power factor even when the switching frequency is reduced.
- **SKIP Mode (Versions [B**] and [D**]):** to further optimize the efficiency, the circuit skips cycles at low load current when V_{ctrl} reaches the SKIP threshold voltage. This is to avoid circuit operation when the power transfer is particularly inefficient at the cost of current distortion. This SKIP function is not present on versions [A**] and [C**]).
- **Low Start−up Current** and large V_{CC} range ([**A] & [**C] versions): The start−up consumption of the circuit is minimized to allow the use of high−impedance start−up resistors to pre−charge the V_{CC} capacitor. Also, the minimum value of the UVLO hysteresis is 6 V to avoid the need for large V_{CC} capacitors and help shorten the start−up time without the need for too dissipative start−up elements. The [**C] version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start−up level (11.25 V) is set low enough so that the circuit can be powered from a 12−V rail. After start−up, the high V_{CC} maximum rating allows a large operating range from 9.5 V up to 30 V.
- **Fast Line / Load Transient Compensation (Dynamic Response Enhancer):** Since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start−up) may cause excessive over or under−shoot. This circuit limits possible deviations from the regulation level as follows:
  - NCP1622 linearly decays the power delivery to zero when the output voltage exceeds 105% of its desired level (soft OVP). If this soft OVP is too smooth and the output continues to rise, the circuit immediately interrupts the power delivery when the output voltage is 107% above its desired level.
  - NCP1622, dramatically speeds−up the regulation loop when the output voltage goes below 95.5% of its regulation level. This function is enabled only after the PFC stage has started−up to allow normal soft−start operation to occur.
- **Safety Protections:** Permanently monitoring the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over−stress making the PFC stage extremely robust and reliable. In addition to the OVP protection, the following methods of protection are provided:
  - **Maximum Current Limit:** The circuit senses the MOSFET current and turns off the power switch if the set current limit is exceeded. In addition, the circuit enters a low duty−cycle operation mode when the current reaches 150% of the current limit as a result of the inductor saturation or a short of the bypass diode.
  - **Under−Voltage Protection:** This circuit turns off when it detects that the output voltage is below 12% of the voltage reference (typically). This feature protects the PFC stage if the ac line is too low or if there is a failure in the feedback network (e.g., bad connection).
  - **Brown−Out Detection:** The circuit detects low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.
  - **Thermal Shutdown:** An internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).
- **Output Stage Totem Pole:** NCP1622 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

NCP1622 Operation Modes

As mentioned, NCP1622 PFC controller implements a Valley Synchronized Frequency Fold−back (***VSFF***) where:

- The circuit operates in classical ***Cr***itical conduction ***M***ode (***CrM***) when V_{ctrl} exceeds a programmable value $V_{ctrl,th,*}$.
- When V_{ctrl} is below this $V_{ctrl,th,*}$, the NCP1622 linearly reduces the operating frequency down to about 33 kHz
- When Vctrl reaches V_{crtl} minimum value or the V_{ctrl} SKIP mode threshold, the system works in low frequency burst mode.

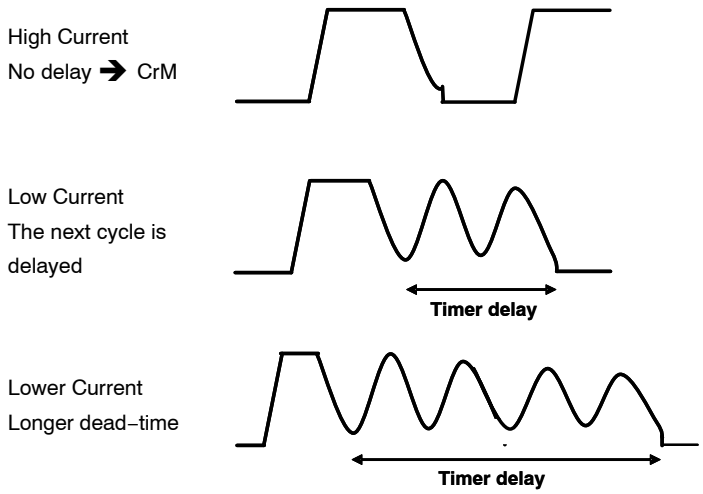


Figure 3. Valley Switching Operation in CrM and DCM Modes

As illustrated in Figure 3, under high load conditions, the boost stage is operating in CrM but as the load is reduced, the controller enters controlled frequency discontinuous operation.

To further reduce the losses, the MOSFET turns on is stretched until its drain−source voltage is at its valley. The end of the dead time is synchronized with the drain−source ringing.

VALLEY SYNCHRONIZED FREQUENCY FOLDBACK (VSFF)

a/ Valley Synchronized (VS)

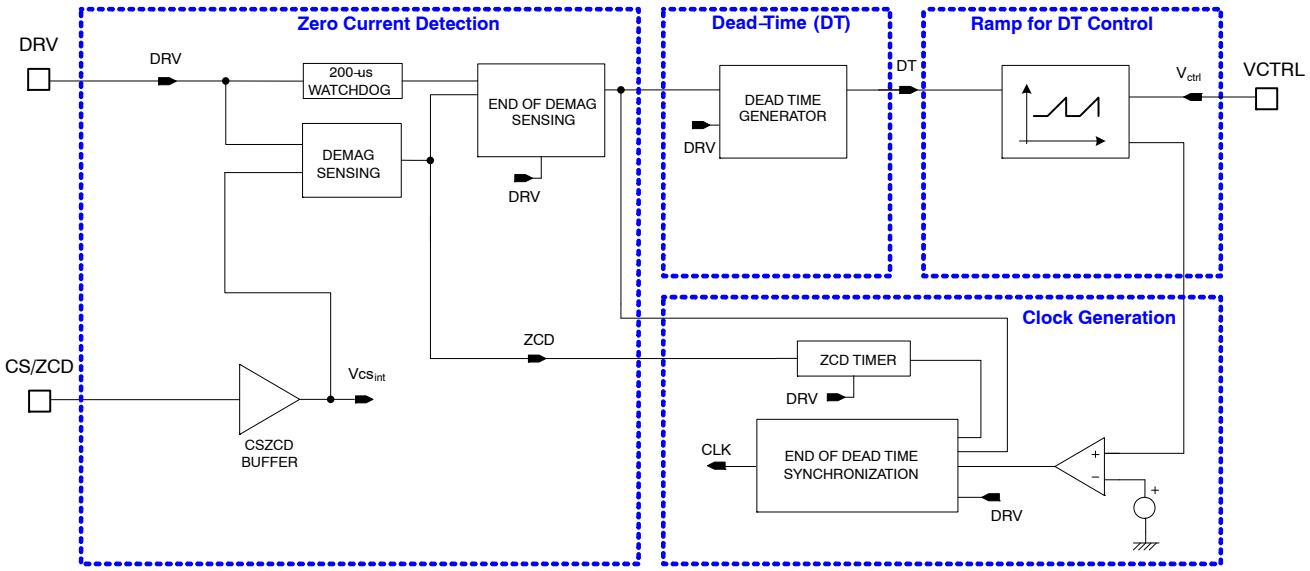


Figure 4. Valley Synchronized Turn−on Block Diagram

Valley Synchronized is the first half of the VSFF system.

Synchronizing the Turn−on with the drain voltage valley maximizes the efficiency at both nominal and light load conditions. In particular, the stand−by losses are reduced to a minimum. The synchronization of Power MOSFET Turn−on (rising edge of CLK signal) with drain voltage valley is depicted on Figure 4. This method avoids system stalls between valleys. Instead, the circuit acts so that the PFC controller transitions from the n valley to (n+1) valley or vice versa from the n valley to (n−1) cleanly as illustrated by the simulation results of Figure 5. When the Line voltage and inductor current are very low, or when the amplitude of the drain voltage gets too low (in the case of long dead times), the turn−on of the power MOSFET is no longer synchronized with the drain valley but will start exactly at the end of a programmed dead time looks to the ZCD TIMER block.

If no demagnetization is sensed the power MOSFET will be turned−on after a watchdog timing of 200−μs.

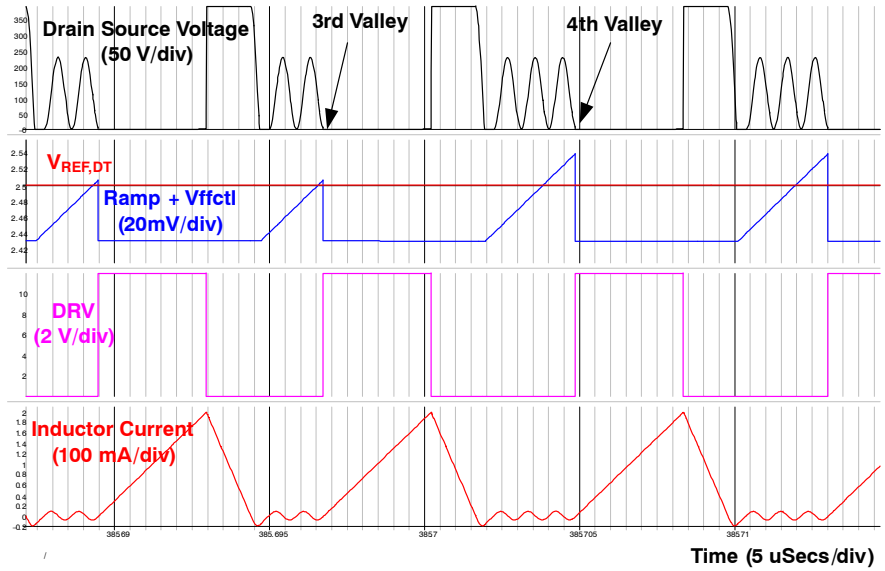


Figure 5. Clean Transition Without Hesitation Between Valleys

b/ Frequency Foldback (FF)

Frequency Foldback is the second half of the VSFF system.

When V_{ctrl} falls below an option−programmable $V_{ctrl,th,*}$ threshold, the NCP1622 enters DCM and linearly reduces the operating frequency down to about 33 kHz by adding a dead−time after the end of inductor demagnetization. The end of the dead−time is synchronized with the valley in the drain voltage, hence the name **V**alley **S**ynchronized (**VS**). The lower the V_{ctrl} value, the longer the dead−time.

The **F**requency **F**oldback (**FF**) system adjusts the on−time versus t_{DT} (see Figure 6) and the output power in order to ensure that the instantaneous mains current is in phase with the mains instantaneous voltage (creating a PF=1).

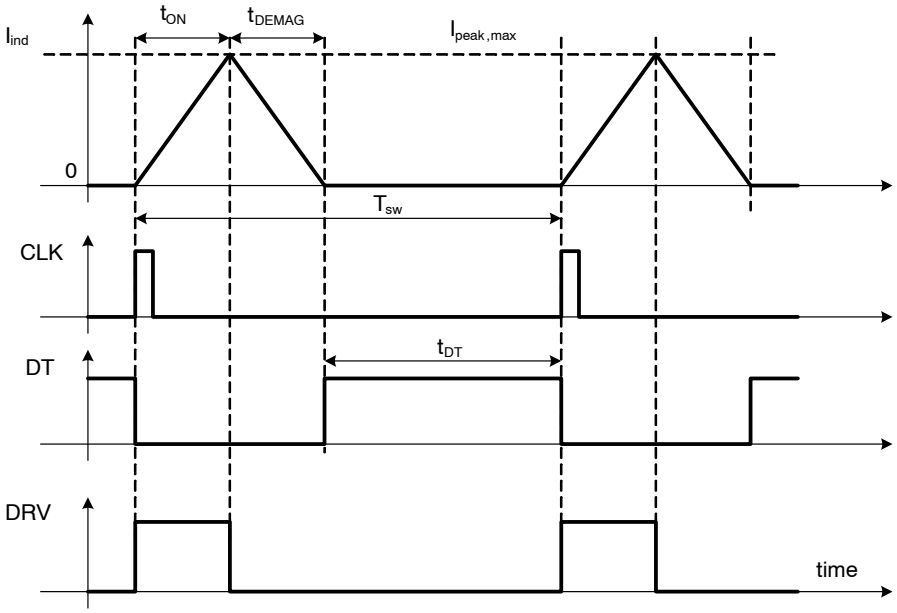


Figure 6. NCP1622 Clock, Dead Time and t_{ON} Waveforms

When the load is at its maximum (the maximum V_{ctrl} value and inductor peak current limitation is not triggering), the controller runs in CrM mode and the frequency ($@V_{in}=V_{in,max}$) has its minimum value. As we start decreasing the output power, the V_{ctrl} voltage decreases, the switching frequency ($@V_{in}=V_{in,max}$) increases and the controller stays in CrM mode until V_{ctrl} reaches a threshold voltage named $V_{ctrl,th,*}$. From this point, continuing to reduce the output power makes the controller to continue increase the dead time (T_{DT}) after the end of demagnetization resulting in a DCM conduction mode and a switching frequency decrease (**F**requency **F**oldback).

When the output power is reduced and we enter DCM mode, the switching frequency decreases down to a value given by the following equation, which is valid down to before entering SKIP mode. This minimum DCM frequency value is dominated by the dead time value, t_{ON} plus t_{DEMAG} being negligible versus t_{DT} that has reached is maximum value $t_{DT,max}$.

$$F_{SW,\,DCM,\,min} = \frac{1}{t_{DT,max} + t_{ON} + t_{DEMAG}} \approx \frac{1}{t_{DT,max}} \quad \text{(eq. 1)}$$

In order to have, depending on customer application, a different limitation of the maximum switching frequency ($@V_{in}=V_{in,max}$), as well as different V_{ctrl} thresholds for CrM to DCM boundary, different product versions are made available (see Table 2).

Coding the second letter (L_2) of the version code with letters A,B,C,D,E,F,G,H,I can be configured at the factory.

The Figure 7 and Figure 8 represent curves generated by an analytical model processed by a MathCad spreadsheet. The differences between the different possible configurations (E for the second letter of product version code is the default configuration) are evident. Notice that Figure 9 shows output power versus V_{ctrl} that depends only on $t_{ON,max}$ and on inductor value (the higher the inductor value, the higher the P_{out} value).

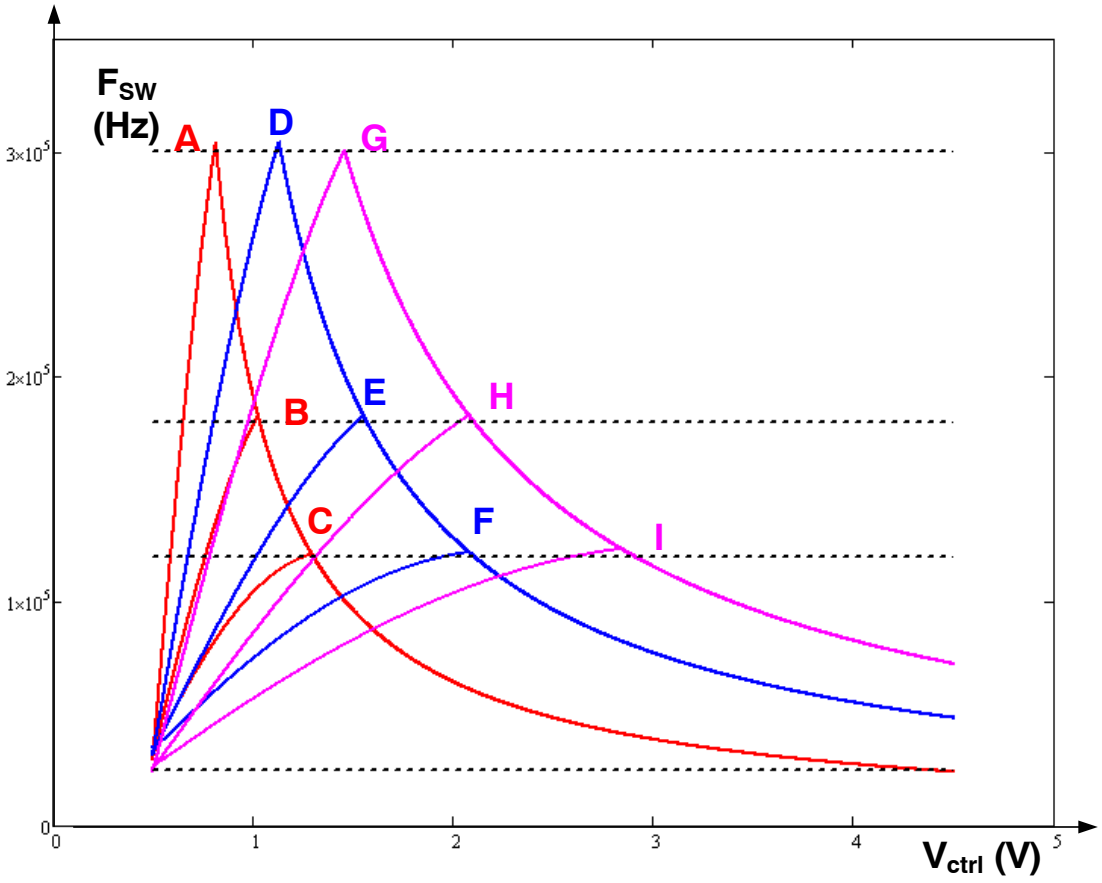


Figure 7. Switching Frequency (@ V_{in} = $V_{in,max}$) versus V_{ctrl} (No L Dependent) : Default = [*E*]

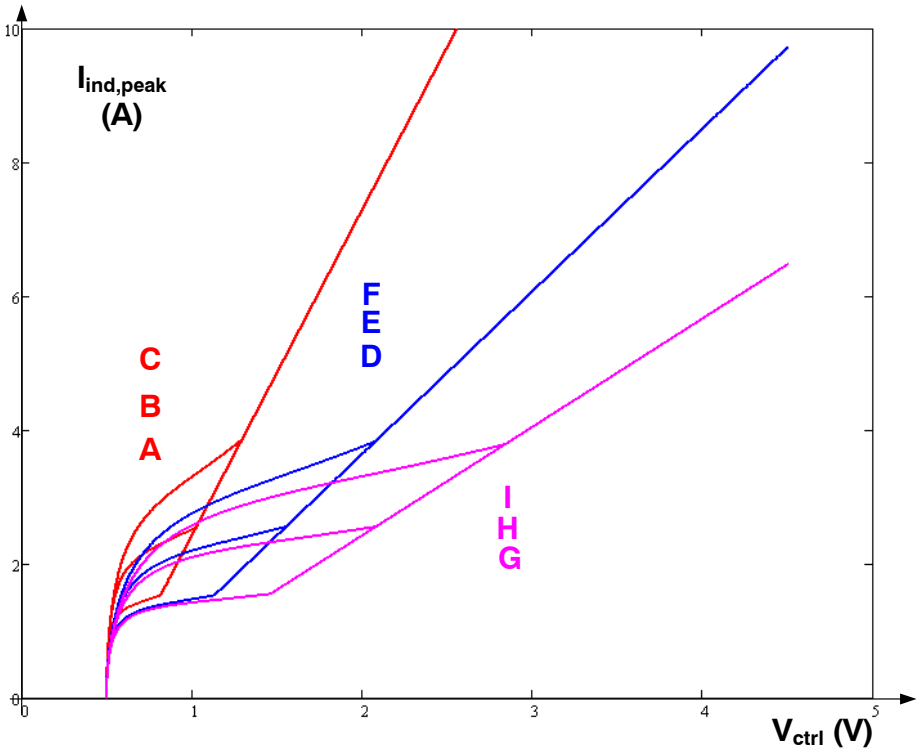


Figure 8. Maximum Inductor Peak Current (@ V_{in} = $V_{in,max}$) versus V_{ctrl} (L Dependent) : Default = [*E*]

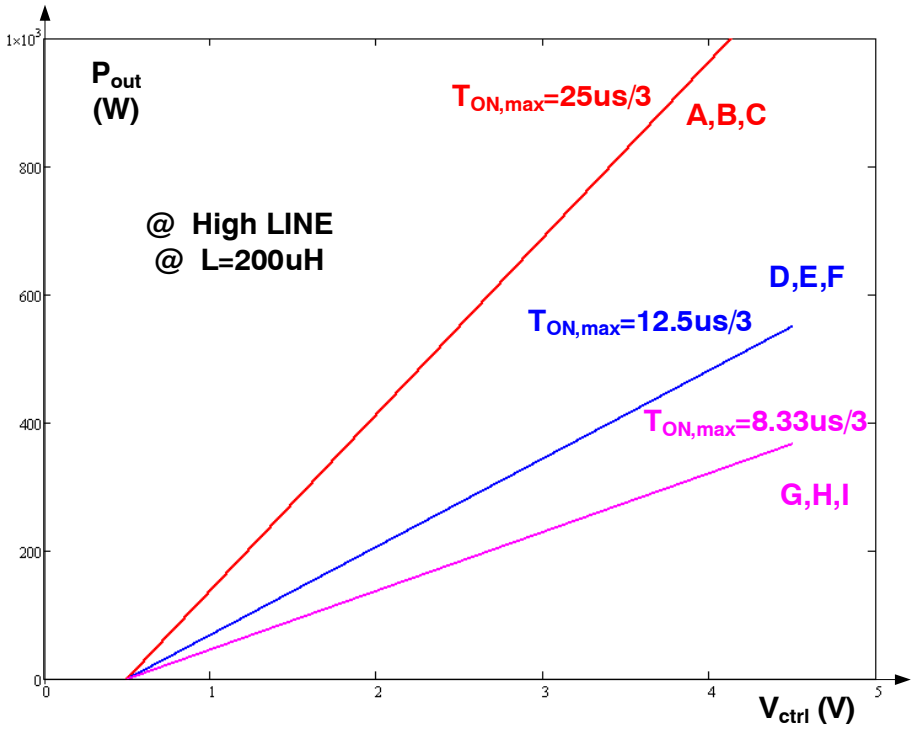


Figure 9. Output Power P_{out} versus V_{ctrl} and $T_{ON,max}$ (L Dependent) : Default = [*E*]

CrM−DCM and DCM−CrM Transition Hysteresis

Hesitation of the system to transition between the modes *CrM* and *DCM* may have a consequences on inductor current shape and distort the mains current, resulting in a bad PF value when the operating point is at the *CrM−DCM* boundary.

To avoid such undesired behavior, a 40 mV hysteresis is added on V_{ctrl} threshold. The V_{ctrl} threshold for transitioning from CrM to DCM mode is named $V_{ctrl,th,}$* (see Table 6) and the V_{ctrl} threshold for transitioning from DCM to CrM mode is $V_{ctrl,th}$,* + 40 mV.

NCP1622 Skip Mode (Active on Versions [B**] and [D**], Disabled on Versions [A**] and [C**])

The circuit also skips cycles when V_{ctrl} decreases towards V_{SKIP-L} threshold. A comparator monitors the V_{ctrl} voltage and inhibits the drive when V_{ctrl} is lower than the SKIP Mode threshold V_{SKIP-L}. Switching resumes when V_{ctrl} exceeds V_{SKIP-H} threshold. The skip mode capability is disabled whenever the PFC stage is not in nominal operation (as dictated by the PFCOK signal − see PFCOK Operation section).

NCP1622 On−time Modulation and V_{TON} Processing Circuit

Let's analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is *on*. The slope is (V_{in}/L) where L is the coil inductance. At the end of the on−time (t_1), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is (t_2). In some cases, the system enters then the dead−time (t_3) that lasts until the next clock is generated.

One can show that the ac line current is given by:

$$I_{in} = V_{in}\frac{t_1(t_1 + t_2)}{2T\,L} \qquad \text{(eq. 2)}$$

Where

$$T = t_1 + t_2 + t_3 \qquad \text{(eq. 3)}$$

is the switching period and V_{in} is the ac line rectified voltage.

In light of this equation, we immediately note that I_{in} is proportional to V_{in} if $[t_1.(t_1+t_2)/T]$ is a constant.

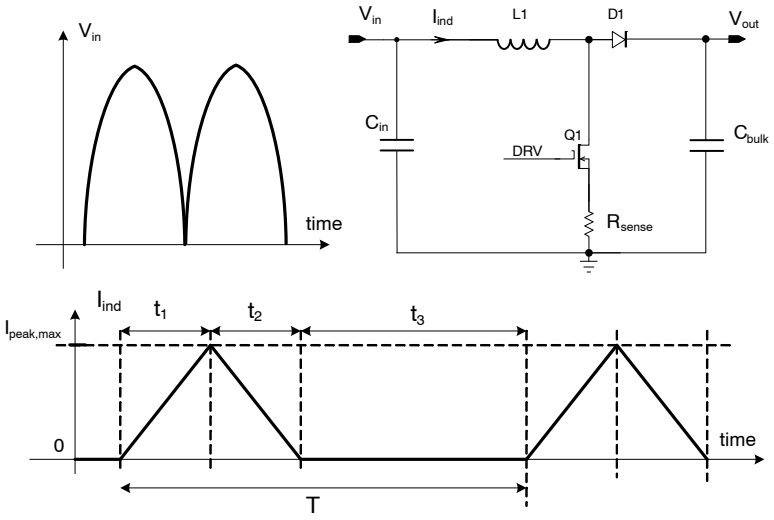


Figure 10. PFC Boost Converter and Inductor Current in DCM

The NCP1622 operates in voltage mode. As portrayed by Figure 10 & Figure 11, the MOSFET on−time t_1 is set by a dedicated circuitry monitoring V_{ctrl} and dead−time t_{DT} ensuring $[t_1.(t_1+t_2)/T]$ is constant and as a result making I_{in} proportional to V_{in} (PF=1)

On−time t_1 is also called t_{on} and its maximum value $t_{on,max}$ is obtained when V_{ctrl} is at maximum level. The internal circuitry makes $t_{on,max}$ at High Line condition (HLINE) to be 3 times the $t_{on,max}$ at Low Line condition (LLINE) (low−pass filtered internal CS−pin voltage is compared to V_{HL} and V_{LL} for deciding whether we are in HLINE or in LLINE). Two other values of $t_{on,max}$ are offered as options (see Figure 9).

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CrM case. This condition is just a particular case of this functioning where (t_3=0), which leads to (t_1+t_2=T) and (V_{ton}=V_{regul}). That is why the NCP1622 automatically adapts to the conditions and transitions from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

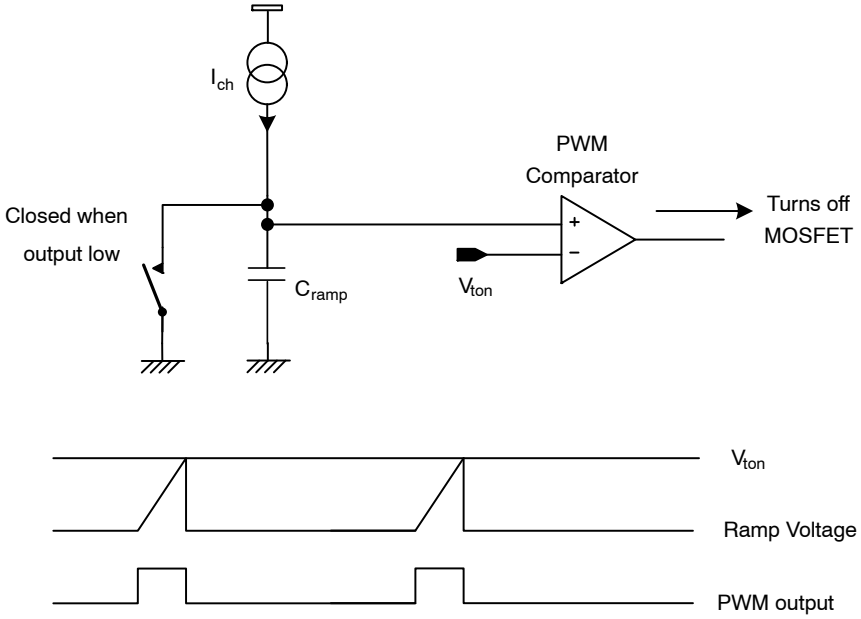


Figure 11. PWM Circuit and Timing Diagram

NCP1622 Regulation Block and Output Voltage Control

A trans−conductance error amplifier (OTA) with access to the inverting input and output is provided. It features a typical trans−conductance gain of 200 μS and a maximum current capability of ±20 μA. The output voltage of the PFC stage is typically scaled down by a resistors divider and monitored by the inverting input (pin FB). Bias current is minimized (less than 500 nA) to allow the use of a high impedance feed−back network. However, it is high enough so that the pin remains in low state if the pin is not connected.

The output of the error amplifier is brought to pin VCTRL for external loop compensation. Typically a type−2 network is applied between pin VCTRL and ground, to set the regulation bandwidth below about 20 Hz and to provide a decent phase boost.

The swing of the error amplifier output is limited within an accurate range:

- It is forced above a voltage drop (V_F) by some circuitry.
- It is clamped not to exceed 4.0 V + the same V_F voltage drop.

The V_F value is 0.5 V typically.

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under−shoot. Over−shoot is limited by the Over−Voltage Protection connected to FB pin (Feedback).

NCP1622 embeds a "**D**ynamic **R**esponse **E**nhancer" circuitry (**DRE**) that contains under−shoots. An internal comparator monitors the FB pin voltage (V_{FB}) and when V_{FB} is lower than 95.5% of its nominal value, it connects a 200 μA current source to speed−up the charge of the compensation network. Effectively this appears as a 10x increase in the loop gain.

The circuit also detects overshoot and immediately reduces the power delivery when the output voltage exceeds 105% of its desired level.

The error amplifier OTA and the OVP, UVP and DRE comparators share the same input information. Based on the typical value of their parameters and if ($V_{out,nom}$) is the output voltage nominal value (e.g., 390 V), we can deduce:

- Output Regulation Level: $V_{out,nom}$
- Output DRE Level: $V_{out,dre}$ = 95.5% x $V_{out,nom}$
- Output Soft OVP Level: $V_{out,sovp}$ = 105% x $V_{out,nom}$
- Output Fast OVP level: $V_{out,fovp}$ = 107% x $V_{out,nom}$

Current Sense and Zero Current Detection (Patent Filed in 2012)

NCP1622 is designed to monitor the current flowing through the power switch during On−time for detecting over current and overstress and to monitor the power MOSFET drain voltage during demagnetization time and dead time in order to generate the ZCD signal.

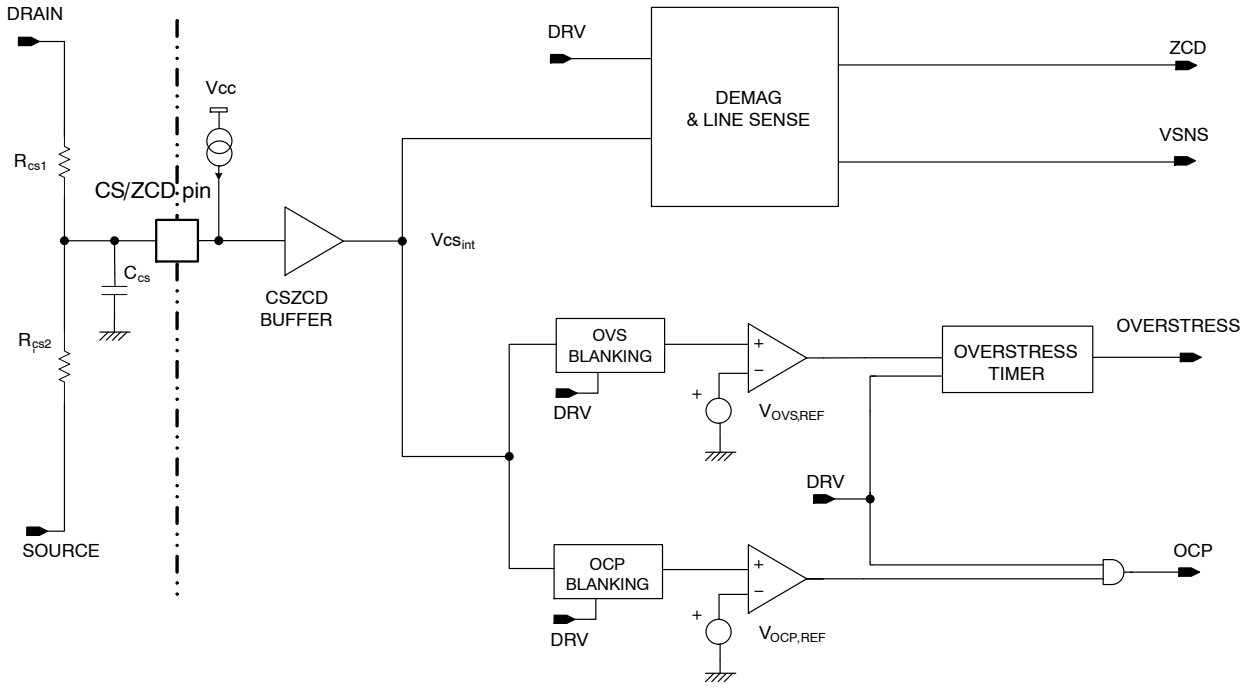


Figure 12. Current Sense, Zero Current Detection Blocks and Vin Sense

Current sense, zero current detection and Vin sense are using the CS/ZCD pin voltage as depicted in the electrical schematic of Figure 12.

Current Sense

The power MOSFET current I is sensed during the T_{ON} phase by the resistor R_{sense} inserted between the MOSFET source and ground (see Figure 13). During T_{ON} phase R_{cs1} and R_{cs2} are almost in parallel and the signal $R_{sense}.I$ is equal to the voltage on pin CS.

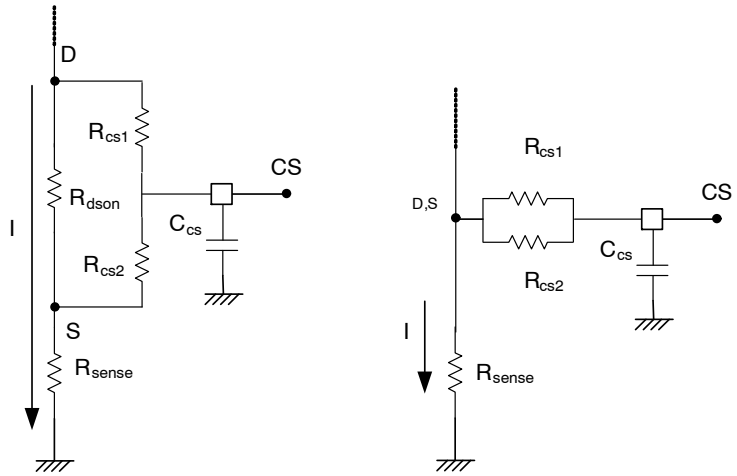


Figure 13. Current Sensing during the T_{ON} Phase

During the On−time and after a 200 ns blanking time, an OCP (Over Current Protection) signal is generated by an OCP comparator, comparing (V_{CS} = V_{CS2}) to a 500 mV internal reference.

When $R_{sense}I_{ds_max} = V_{CS} = V_{CS2}$ = 500 mV we get:

$$I_{ds_max} = \frac{V_{ocp}}{R_{sense}} \quad \text{(eq. 4)}$$

When V_{CS} exceeds the 500 mV internal reference threshold, the OCP signal turns high to reset the PWM latch and forces the driver low. The 200 ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on.

Zero Current Detection

The CS pin is also designed to receive, during t_{DEMAG} and t_{DT}, a scaled down (divided by 138) power MOSFET drain voltage that will be used for Zero Current Detection. It may happen that the MOSFET turns on while a huge current flows through the inductor. As an example such a situation can occur at start−up when large in−rush currents charge the bulk capacitor to the line peak voltage. Traditionally, a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current. If this diode is accidently shorted, the demagnetization will be impossible and cycle after cycle the inductor current will increase so the MOSFET will also see a high current when it turns on. In both cases, the current can be large enough to trigger the OverStress (OVS) comparator. In this case, the "OverStress" signal goes high and disables the driver for an 800 μs delay. This long delay leads to a very low duty−ratio operation in case of "OverStress" fault in order to limit the risk of overheating.

When no signal is received that triggers the ZCD comparator to indicate the end of inductor demagnetization, an internal 200 μs watchdog timer initiates the next drive pulse. At the end of this delay, the circuit senses the CS/ZCD pin impedance to detect a possible grounding of this pin and prevent operation.

Brown−Out Detection (Versions [C**] and [D**])

For an application w/o Vaux (using the Drain) and using Brown−out options ([C**] and [D**]) the Brown−out feature will use the High and Low Brown−out levels.

Brown−out options ([C] and [D**]) must not be used on an application using Vaux** as these options are not designed to work in this case.

By default, the Brown−out flag is set High (BONOK=1), meaning that V_{in},sensed thru CSZCD pin and V_{sns} (V_{sns} is a low−pass filtered scaled down V_{in}) internal signal (see Figure 1), when higher than internal reference voltage V_{BOH} will set the brown−out flag to zero (BONOK=0) and allow the controller to start. After BONOK is set to zero, and switching activity starts, the V_{in} continues to be sensed thru CSZCD pin and when V_{sns} falls under Brown−out internal reference voltage V_{BOL} for 50 ms, BONOK flag will be set to 1. After BONOK flag will be set to 1, drive is not disabled, instead, a 30 μA current source is applied to VCTRL pin to gradually reduce V_{ctrl}. As a result, the circuit only stops pulsing when the STATICOVP function is activated (that is when V_{ctrl} reaches the SKIP detection threshold). At that moment, the circuit stops switching. This method limits any risk of false triggering.

For an application w/Vaux (not using the Drain), Brown−out options ([C] and [D**]) are not be allowed** and the UVP will act like a brown−in. The reason is that before controller starts switching, the V_{out} voltage is equal to $V_{mains,rms}$ and sensed by FB pin and compared to UVP high internal reference voltage V_{UVPH}.

The input of the PFC stage has some impedance that leads to some sag of the input voltage when the input current is large. If the PFC stage suddenly stops while a high current is drawn from the mains, the abrupt decay of the current may make the input voltage rise and the circuit detect a correct line level. Instead, the gradual decrease of $V_{control}$ avoids a line current discontinuity and limits the risk of false triggering.

V_{sns} internal voltage is also used to sense the line for feed−forward. A similar method is used:

- The V_{sns} internal pin voltage is compared to a 1.801 V reference.
- If V_{sns} exceeds 1.801 V, the circuit detects a high−line condition and the loop gain is divided by three (the internal PWM ramp slope is three times steeper)
- Once this occurs, if V_{sns} remains below 1.392 V for 25 ms, the circuit detects a low−line situation (500 mV hysteresis).

At startup, the circuit is in High−line state ("LLINE" Low") and then V_{sns} will be used to determine the High−Line or Low−Line state.

The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications.

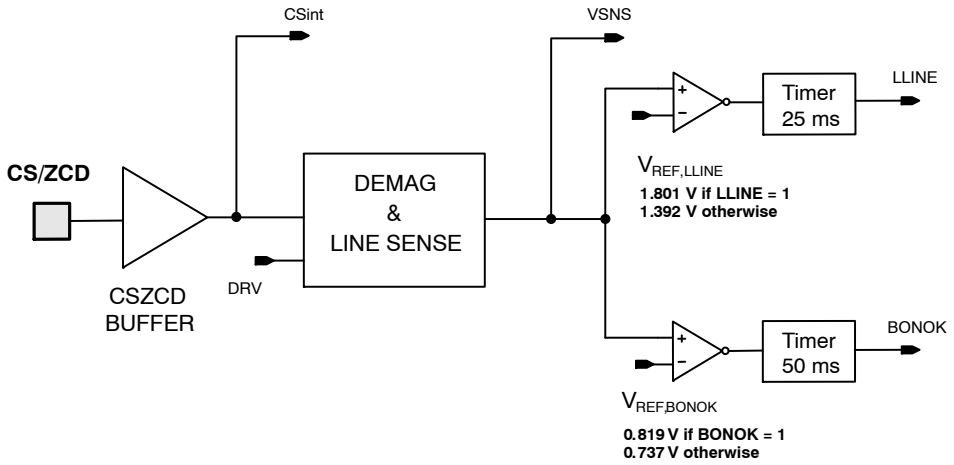


Figure 14. Input Line Sense Monitoring

Thermal Shut−Down (TSD)

An internal thermal circuitry disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150°C. The output stage is then enabled once the temperature drops below about 100°C (50°C hysteresis).

The temperature shutdown remains active as long as the circuit is not reset, that is, as long as V_{CC} is higher than a reset threshold.

Output Drive Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. Its high current capability (−500 mA / +800 mA) allows it to effectively drive high gate charge power MOSFET.

Second Over−Voltage Protection

On top of the existing overvoltage protection, a second and redundant overvoltage protection named OVP2 has been added. This overvoltage protection, senses, during t_{DEMAG} the value of V_{out}, thru the R_{CS1}, R_{CS2} divider bridge connected to the pin CS and compares it to an OVP2 voltage reference $V_{REF,OVP2}$. Because it is not possible to adjust the $V_{REF,OVP2}$ reference to R_{fb1} & Rf_{b2} that programs the V_{out} value, it has been decided to set $V_{REF,OVP2}$ and R_{CS1}, R_{CS2} in order to get OVP2 triggering for Vout voltages much higher than for OVP condition (e.g. OVP2 goes high when Vout goes higher than 438 V)

For V_{out} = 438 V for OVP2 and given a K_{CS} value equal to 1/138 ($K_{CS} = R_{CS2} / (R_{CS1} + R_{CS2})$, this gives $V_{REF,OVP2}$ = 3.175 V for the threshold voltage to which is compared to the CS voltage during t_{off}. When V_{CS} goes above $V_{REF,OVP2}$ threshold of the OVP2 comparator (100 mV hysteresis), and after a 1 μs leading edge blanking time, the OVP2 flag is latched and will stop the switching by resetting the main PWM latch. The OVP2 latch is reset each 800 μs.

OFF Mode

As previously mentioned, the circuit turns off when one of the following faults is detected:

- Incorrect feeding of the circuit (“UVLO” high when $V_{CC} < V_{CC(off)}$, $V_{CC(off)}$ equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown
- Under−Voltage Protection
- Brown−Out Fault and STATICOVP (see Figure 2)

Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized.

More specifically, when the circuit is in OFF state:

- The drive output is kept low
- All the blocks are off except:
  - The UVLO circuitry that keeps monitoring the V_{CC} voltage and controlling the start−up current source accordingly
  - The TSD (thermal shutdown)
  - The Under−Voltage Protection (“UVP”)
  - The brown−out circuitry
- V_{ctrl} is grounded so that when the fault is removed, the device starts−up under the soft start mode (version XB).
- The internal “PFCOK” signal is grounded.
- The output of the “V_{ton} processing block” is grounded

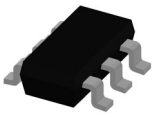
Failure Detection

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted; a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke nor big noise. NCP1622 integrate functions that ease meet this requirement. Among them, we can list:

- ***Floating feedback pin***
  A special internal circuitry detects the floating feedback pin and stops the operation of the IC.
- ***Fault of the GND connection***
  If the GND pin is not connected, internal circuitry detects it and if such a fault is detected for 200 μs, the circuit stops operating.
- ***Detection the CS/ZCD pin improper connection***
  If the CS/ZCD pin is floating or shorted to GND it is detected by internal circuitry and the circuit stops operating.
- ***Boost or bypass diode short***
  The controller addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty−cycle operation until the fault is gone.

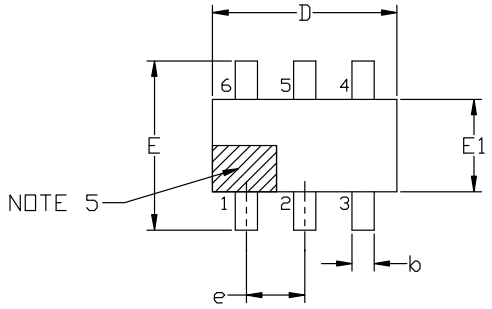
Refer to application note ANDxxxx for more details.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

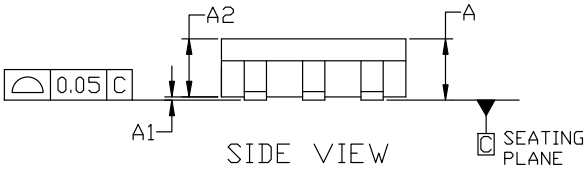


TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

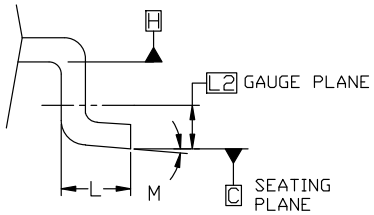
DATE 26 FEB 2024



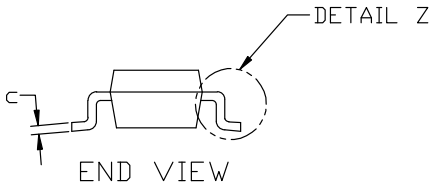
TOP VIEW



SIDE VIEW



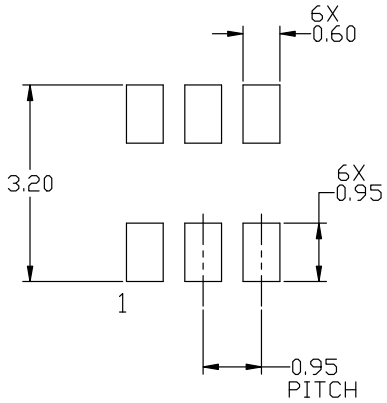
DETAIL Z
SCALE 3:1



END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**TSOP−6 3.00x1.50x0.90, 0.95P**		**PAGE 1 OF 2**

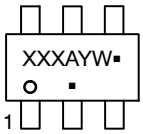
onsemi and ONSEMI. are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

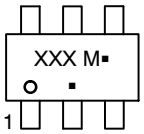
DATE 26 FEB 2024

GENERIC
MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales