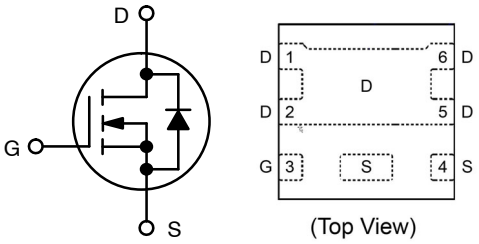
MOSFET - Power, Single N-Channel
60 V, 21 mΩ, 25 A

NVLJWS022N06CL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	21 mΩ @ 10 V	25 A
	29 mΩ @ 4.5 V	

Features
- Small Footprint for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

ELECTRICAL CONNECTION



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

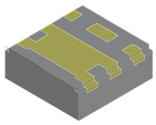
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	25	A
		T_C = 100°C		18	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	28	W
		T_C = 100°C		14	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	7.2	A
		T_A = 100°C		5.1	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	2.4	W
		T_A = 100°C		1.2	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	90	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +175	°C
Source Current (Body Diode)			I_S	24	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 1.1 A)			E_{AS}	42	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State	$R_{\theta JC}$	5.3	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	63	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



WDFNW6 (2.05x2.05)
CASE 515AD

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$/T_J				25		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 16 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}$/T_J				−5.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 8 A		17	21	mΩ
		V_{GS} = 4.5 V	I_D = 8 A		23	29	
Forward Transconductance	g_{FS}	V_{DS} =6 V, I_D = 8 A			22		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			440		pF
Output Capacitance	C_{OSS}				240		
Reverse Transfer Capacitance	C_{RSS}				7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V; I_D = 8 A			3.6		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 8 A			7.6		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 8 A			0.8		nC
Gate−to−Source Charge	Q_{GS}				1.6		
Gate−to−Drain Charge	Q_{GD}				0.9		
Plateau Voltage	V_{GP}				2.9		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 8 A, R_G = 6 Ω			6.0		ns
Rise Time	t_r				1.9		
Turn−Off Delay Time	$t_{d(OFF)}$				15		
Fall Time	t_f				2.1		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 8 A	T_J = 25°C		0.85	1.2	V
			T_J = 125°C		0.73		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 8 A			23		ns
Charge Time	t_a				12		
Discharge Time	t_b				11		
Reverse Recovery Charge	Q_{RR}				12		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

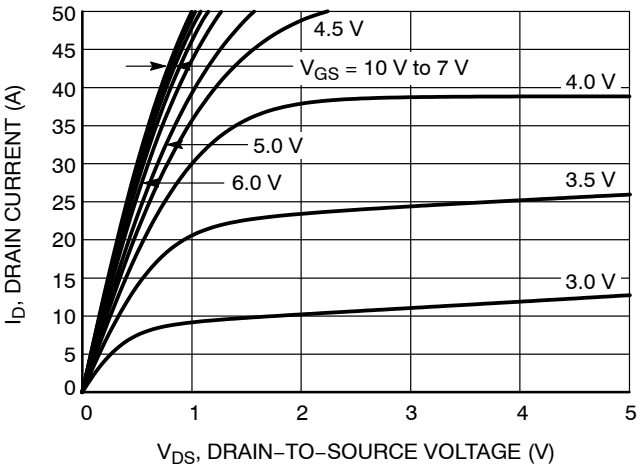


Figure 1. On−Region Characteristics

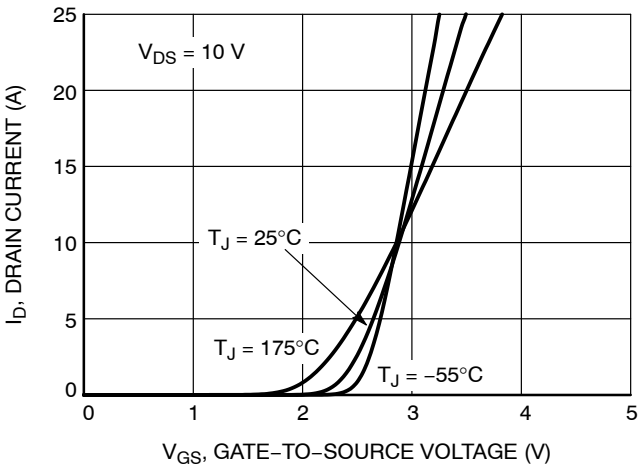


Figure 2. Transfer Characteristics

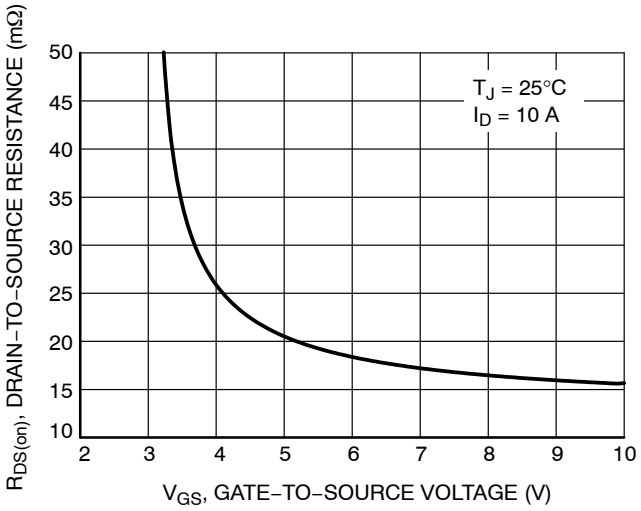


Figure 3. On−Resistance vs. Gate−to−Source Voltage

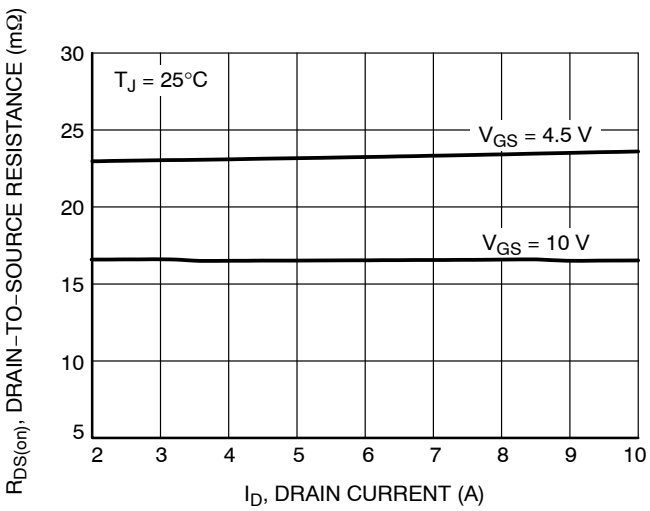


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

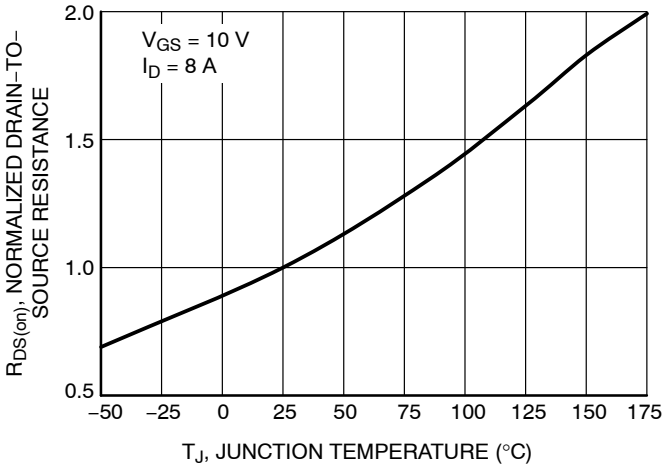


Figure 5. On−Resistance Variation with Temperature

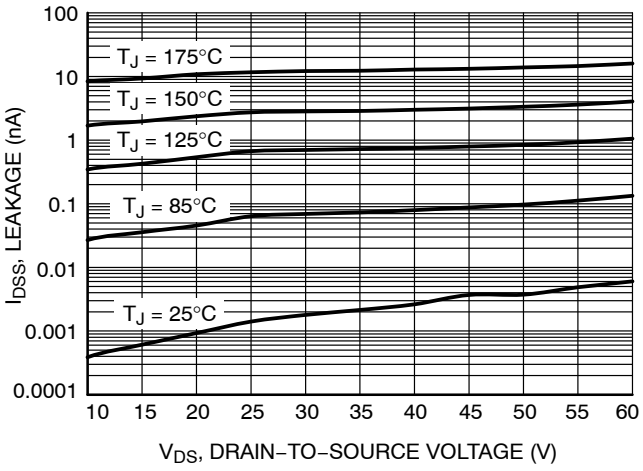


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

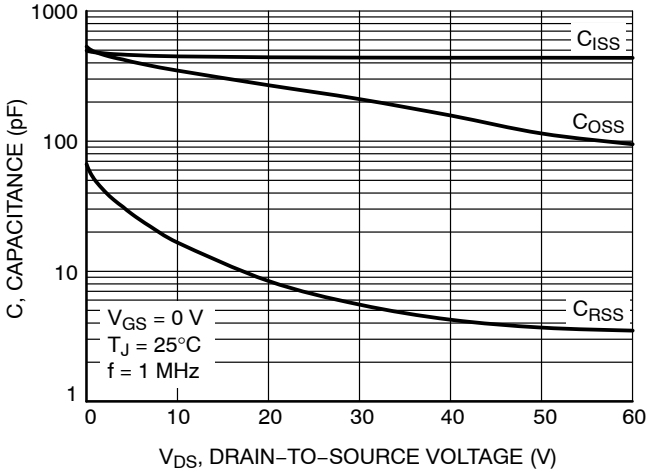


Figure 7. Capacitance Variation

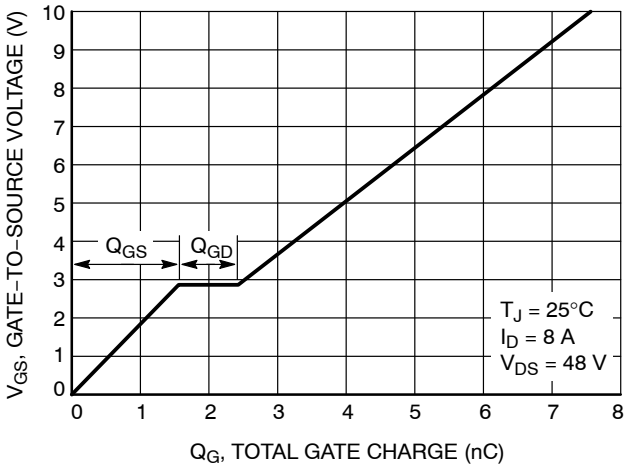


Figure 8. Gate−to−Source Voltage vs. Total Charge

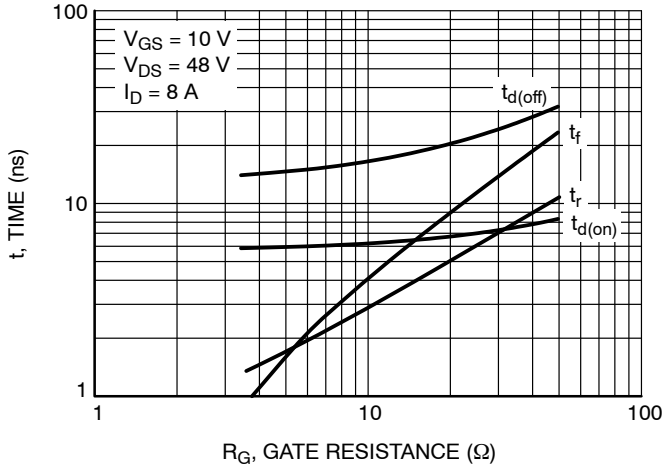


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

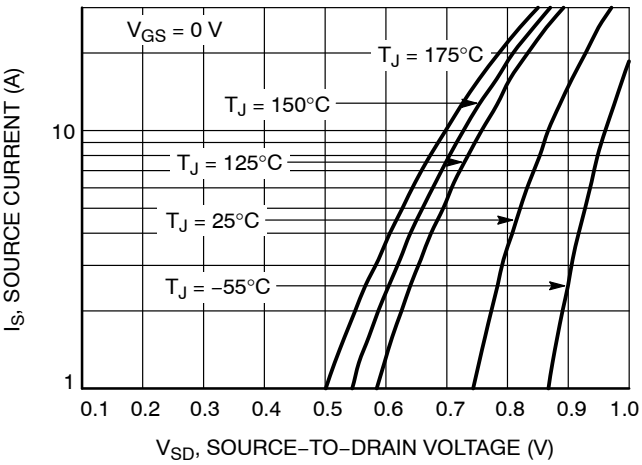


Figure 10. Diode Forward Voltage vs. Current

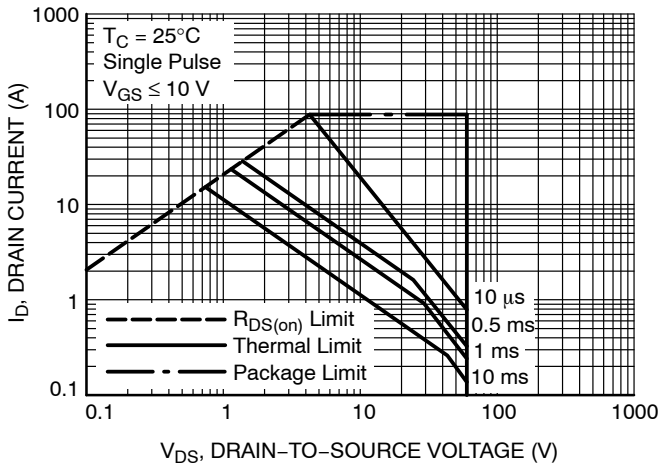


Figure 11. Maximum Rated Forward Biased Safe Operating Area

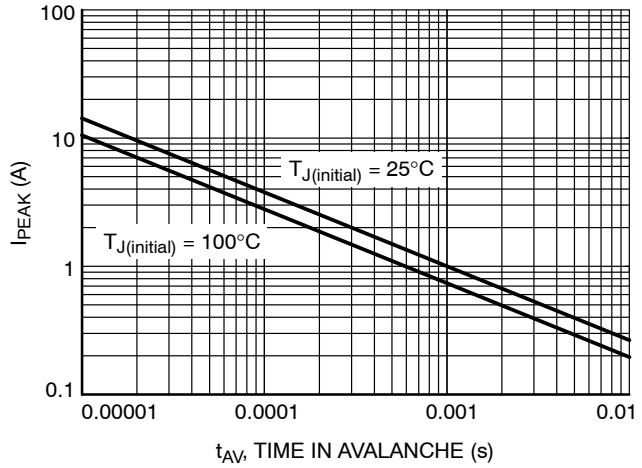


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

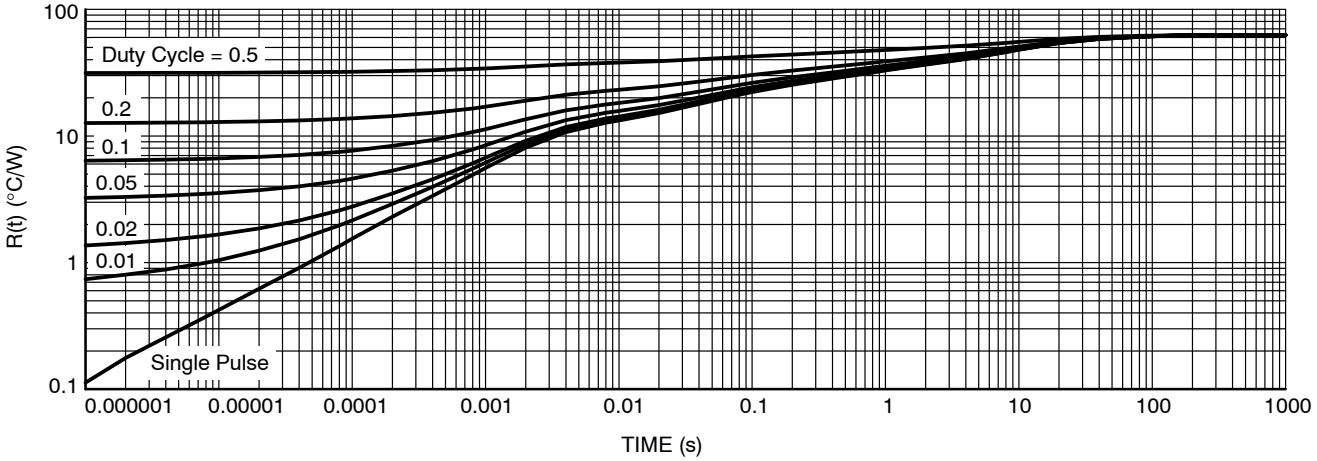


Figure 13. Transient Thermal Impedance

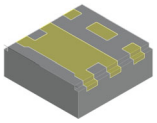
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVLJWS022N06CLTAG	022N	WDFNW6 (Pb−Free, Wettable Flanks)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

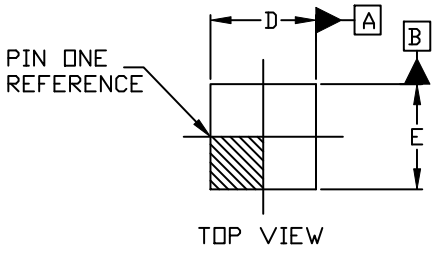
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

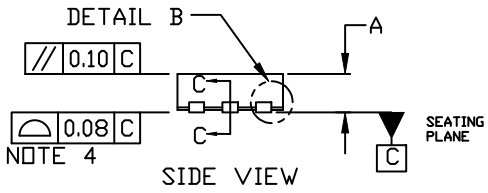


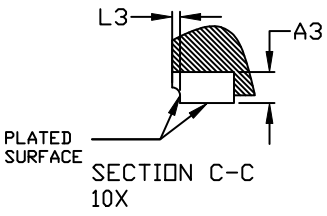
WDFNW6 2.05x2.05, 0.65P
CASE 515AD
ISSUE O

DATE 25 JUN 2021

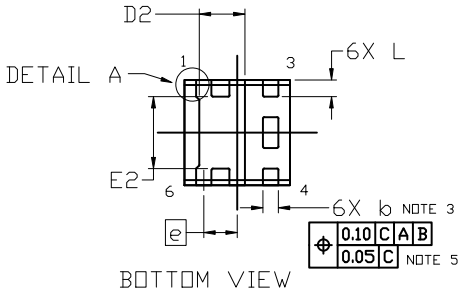


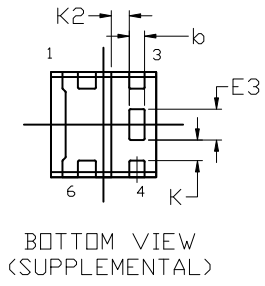
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

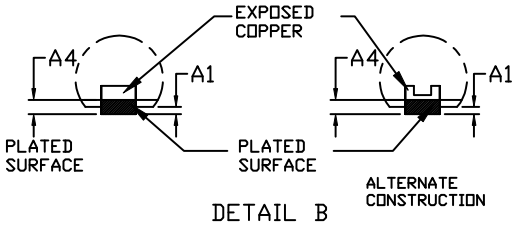


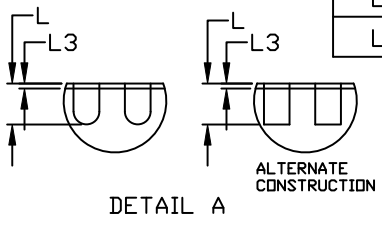


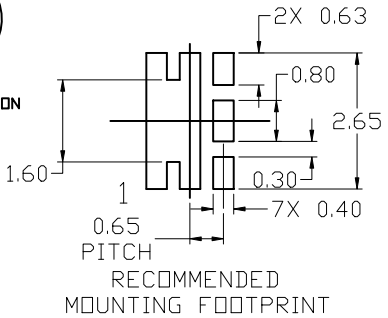
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
E	1.95	2.05	2.15
E2	1.35	1.40	1.45
E3	0.55	0.60	0.65
e		0.65 BSC	
K		0.40 REF	
K2		0.35 REF	
L	0.275	0.325	0.375
L3	---	---	0.09











* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFNW6 2.05x2.05, 0.65P**	**PAGE 1 OF 1**

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