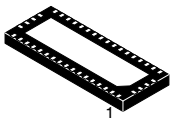
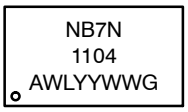
3.3 V USB 3.1 Gen-2 10 Gbps Quad Channel / Dual Port Linear Redriver

NB7NPQ1104M



WQFN42
CASE 510AP

MARKING DIAGRAM



NB7N1104 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

Description

The NB7NPQ1104M is a high performance 2−Port linear redriver designed for USB 3.1 Gen 1 and USB 3.1 Gen 2 applications that supports both 5 Gbps and 10 Gbps data rates. Signal integrity degrades from PCB traces, transmission cables, and inter−symbol interference (ISI). The NB7NPQ1104M compensates for these losses by engaging varying levels of equalization at the input receiver, and flat gain amplification on the output transmitter.

The NB7NPQ1104M offers programmable equalization and flat gain for each independent channel to optimize performance over various physical mediums.

The NB7NPQ1104M contains an automatic receiver detect function which will determine whether the output is active. The receiver detection loop will be active if the corresponding channel's signal detector is idle for a period of time. The channel will then move to Unplug Mode if a load is not detected, or it will return to Low Power Mode (Slumber mode) due to inactivity.

The NB7NPQ1104M comes in a 3.5 x 9 mm WQFN42 package and is specified to operate across the entire industrial temperature range, –40°C to 85°C.

ORDERING INFORMATION

Device	Package	Shipping†
NB7NPQ1104MMTTWG	WQFN42 (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Features

- 3.3 V ± 0.3 V Power Supply
- 5 Gbps & 10 Gbps Serial Link with Linear Amplifier
- Device Supports USB 3.1 Gen 1 and USB 3.1 Gen 2 Data Rates
- Automatic Receiver Detection
- Integrated Input and Output Termination
- Pin Adjustable Receiver Equalization and Flat Gain
- 100−Ω Differential CML I/O's
- Auto Slumber Mode for Adaptive Power Management
- Hot−Plug Capable
- ESD Protection ±4 kV HBM
- Operating Temperature Range Industrial: −40°C to +85°C
- Package: WQFN42, 3.5 x 9 mm
- This is a Pb−Free Device

Typical Applications

- USB3.1 Type−A and Type−C Signal Routing
- Mobile Phone and Tablet
- Computer, Laptop and Notebook
- External Storage Device
- Docking Station and Dongle
- Active Cable, Back Planes
- Gaming Console, Smart T.V.

© Semiconductor Components Industries, LLC, 2019

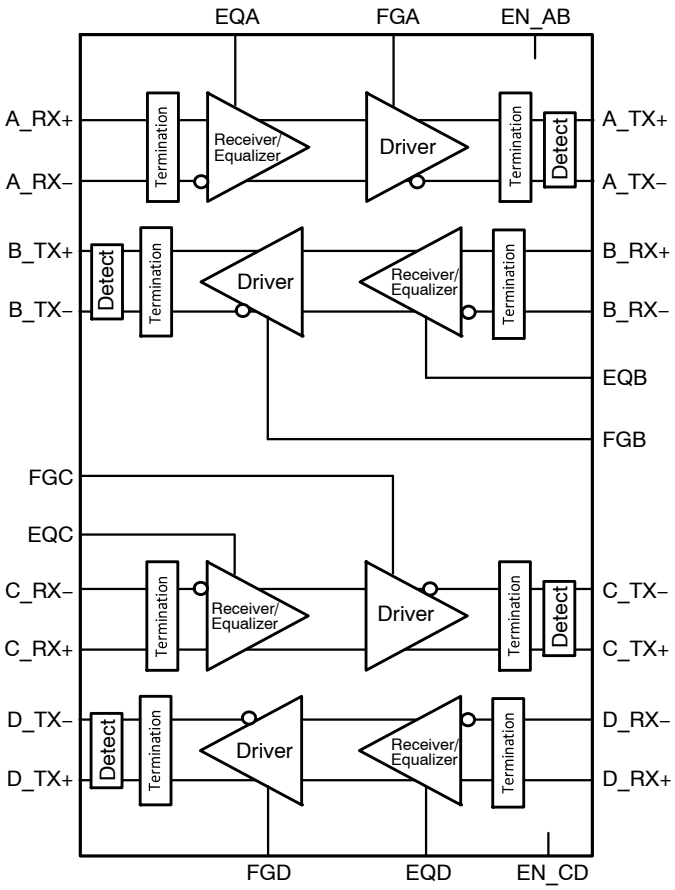


Figure 1. Logic Diagram of NB7NPQ1104M

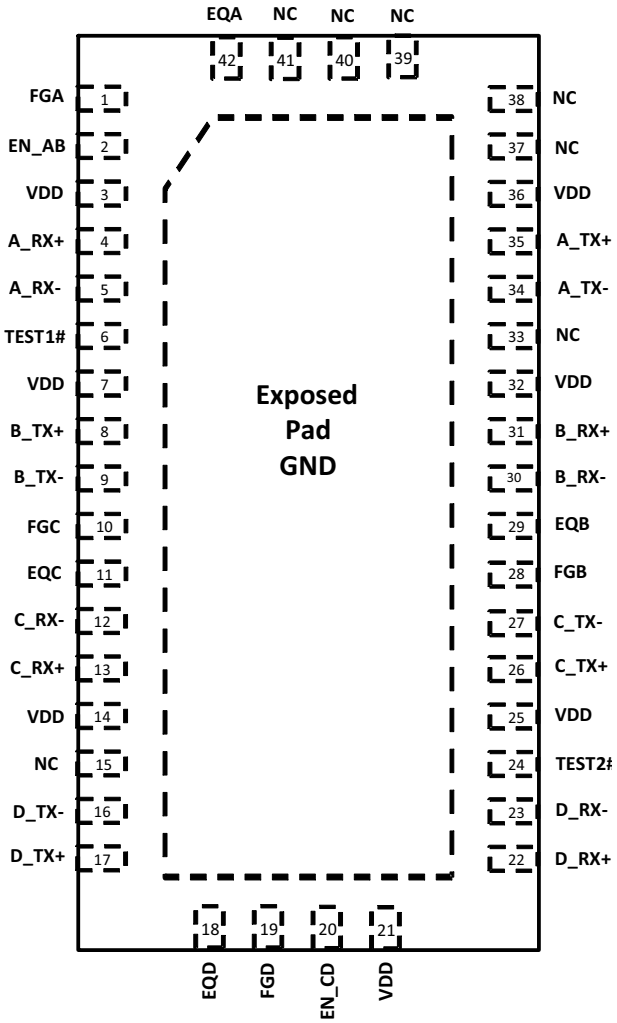


Figure 2. WQFN−42 Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin Number	Pin Name	Type	Description
1	FGA	INPUT	DC flat gain for channel A. 4−level input pin. Internal 100 k−Ω pull−up and 200 k−Ω pull−down.
2	EN_AB	INPUT	Channel AB Enable. Internal 300 k−Ω pull−up. High−Channel is in normal operation. Low−Channel is in power down mode.
3	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
4	A_RX+	INPUT	Channel A Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
5	A_RX−		
6	Test1#	INPUT	Connect to VDD is recommended.
7	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
8	B_TX+	OUTPUT	Channel B Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
9	B_TX−		
10	FGC	INPUT	DC flat gain for channel C. 4−level input pin. Internal 100 k−Ω pull−up and 200 k−Ω pull−down.
11	EQC	INPUT	EQ select for channel C. 4−level input pin. Internal 100 k−Ω pull−up and 200 k−Ω pull−down.
12	C_RX−	INPUT	Channel C Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
13	C_RX+		
14	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
15	NC	NC	No Connect pin: connect to VDD is recommended
16	D_TX−	OUTPUT	Channel D Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
17	D_TX+		
18	EQD	INPUT	EQ select for channel D. 4−level input pin. Internal 100k−Ω pull−up and 200 k−Ω pull−down.
19	FGD	INPUT	DC flat gain for channel D. 4−level input pin. Internal 100k−Ω pull−up and 200 k−Ω pull−down.
20	EN_CD	INPUT	Channel CD Enable. Internal 300k−Ω pull−up. High−Channel is in normal operation. Low−Channel is in power down mode.
21	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
22	D_ RX+	INPUT	Channel D Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
23	D_ RX−		
24	Test2#	INPUT	Connect to VDD is recommended.
25	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
26	C_TX+	OUTPUT	Channel C Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
27	C_TX−		
28	FGB	INPUT	DC flat gain for channel B. 4−level input pin. Internal 100 k−Ω pull−up and 200 k−Ω pull−down.
29	EQB	INPUT	EQ select for channel B. 4−level input pin. Internal 100 k−Ω pull−up and 200 k−Ω pull−down.
30	B_ RX−	INPUT	Channel B Differential CML input pair for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system. UFP/DFP transmitter should provide this capacitor.
31	B_ RX+		
32	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
33	NC	NC	No Connect pin: connect to VDD is recommended
34	A_TX−	OUTPUT	Channel A Differential output for 5 / 10 Gbps USB signals. Must be externally AC−coupled in system.
35	A_TX+		
36	VDD	POWER	3.3 V power supply. VDD pins must be externally connected to power supply.
37, 38, 39, 40, 41	NC	NC	No Connect
42	EQA	INPUT	EQ select for channel A. 4−level input pin. Internal 100k−Ω pull−up and 200k−Ω pull−down.
EP	GND	GND	Exposed pad (EP). EP on the package bottom is thermally connected to the die for improved heat transfer out of the package. The exposed pad is electrically connected to the die and must be soldered to GND on the PC Board.

Power Management

The NB7NPQ1104M has an adaptive power management feature in order to minimize power consumption. When the receiver signal detector is idle, the corresponding channel will change to low power slumber mode. Accordingly, both channels will move to low power slumber mode individually.

While in the low power slumber mode, the receiver signal detector will continue to monitor the input channel. If a channel is in low power slumber mode, the receiver detection loop will be active again. If a load is not detected, then the channel will move to Device Unplug Mode and continuously monitor for the load. When a load is detected, the channel will return to Low Power Slumber Mode and receiver detection will be active again per 6 ms.

Table 2. OPERATING MODES

Mode	R_{IN}	R_{OUT}
PD	67 k−Ω to GND	High−Z
Unplug Mode	High−Z	40 k−Ω to VDD
Low Power Slumber Mode	50−Ω to VDD	40 k−Ω to VDD
Active	50−Ω to VDD	50−Ω to VDD

Table 3. EQUALIZATION SETTING
EQ A/B/C/D are the selection pins for the equalization.

EQA/B/C/D	Equalizer Setting (dB)	
	@2.5 GHz	@5 GHz
L (Tie 0−Ω to GND)	5.0	11.5
R (Tie Rext to GND)	2.7	7.4
F (Leave Open)	4.0	9.9 (Default)
H (Tie 0−Ω to VDD)	6.5	13.1

Table 4. FLAT GAIN SETTING
FGA/B/C/D are the selection pins for the DC gain.

FGA/B/C/D	Flat Gain Settings (dB)
L (Tie 0−Ω to GND)	−1.2
R (Tie Rext to GND)	0
F (Leave Open)	+1.0 (Default)
H (Tie 0−Ω to VDD)	+2.0

Table 5. CHANNEL ENABLE SETTING
EN_AB / EN_CD are the channel enable pins for channels A&B and C&D respectively.

EN	Channel Enable Setting
0	Disabled
1	Enabled (Default)

Table 6. ATTRIBUTES

Parameter		
ESD Protection	Human Body Model Charged Device Model	± 4 kV > 1.5 kV
Moisture Sensitivity, Indefinite Time Out of Dry pack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−O @ 0.125 in
Transistor Count		81034
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test		

1. For additional information, see Application Note AND8003/D.

Table 7. ABSOLUTE MAXIMUM RATINGS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description	Min	Max	Unit
Supply Voltage (Note 2)	V_{DD}	−0.5	4.6	V
Voltage range at any input or output terminal	Differential I/O	−0.5	V_{DD} + 0.5	V
	LVCMOS inputs	−0.5	V_{DD} + 0.5	V
Output Current		−25	+25	mA
Power Dissipation, Continuous			1.2	W
Storage Temperature Range, T_{SG}		−65	150	°C
Maximum Junction Temperature, T_J			125	°C
Junction−to−Ambient Thermal Resistance @ 500 lfm, $Ø_{JA}$ (Note 3)			34	°C/W
Wave Solder, Pb−Free, T_{SOL}			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. All voltage values are with respect to the GND terminals.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 8. RECOMMENDED OPERATING CONDITIONS Over operating free−air temperature range (unless otherwise noted)

Parameter	Description		Min	Typ	Max	Unit
V_{DD}	Main power supply		3.0	3.3	3.6	V
T_A	Operating free−air temperature	Industrial Temperature Range	−40		+85	°C
C_{AC}	AC coupling capacitor		75	100	265	nF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 9. POWER SUPPLY CHARACTERISTICS and LATENCY

Symbol	Parameter	Test Conditions	Min	Typ (Note 4)	Max	Unit
VDD	Supply Voltage		3.0	3.3	3.6	V
IDD_{Active}	Active mode current	EN_AB & EN_CD = 1, 10 Gbps, compliance test pattern		225	334	mA
$IDD_{LPSlumber}$	Low Power Slumber mode current	EN_AB & EN_CD = 1, no input signal longer than TLP-Slumber		0.8	1.2	mA
IDD_{Unplug}	Unplug mode current	EN_AB & EN_CD = 1, no output load is detected		0.5	0.75	mA
IDDpd	Power−down mode current	EN_AB & EN_CD = 0		20	100	μA
tpd	Latency	From Input to Output			2	ns

4. TYP values use VDD = 3.3 V, T_A = 25°C

Table 10. LVCMOS CONTROL PIN CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
2−Level Control Pins LVCMOS Inputs (EN_AB, EN_CD)						
V_{IH}	DC Input Logic High		0.65 x VDD	VDD	VDD	V
V_{IL}	DC Input Logic Low		GND	GND	0.35 x VDD	V
I_{IH}	High−level input current				25	μA
I_{IL}	Low−level input current		−25			μA
4−Level Control Pins LVCMOS Inputs (EQA/B/C/D, FGA/B/C/D)						
V_{IH}	DC Input Logic High; Setting “H”	Input pin connected to VDD	0.92 x VDD	VDD		V
V_{IF}	DC Input Logic 2/3 VDD; Setting “F”	Input pin is left floating (Open) (Note 5)	0.59 x VDD	0.67*VDD	0.75 x VDD	V
V_{IR}	DC Input Logic 1/3 VDD; Setting “R”	R_{ext} 68 kΩ must be between pin and GND	0.25 x VDD	0.33*VDD	0.41 x VDD	V
V_{IL}	DC Input Logic Low; Setting “L”	Input pin connected to GND		GND	0.08 x VDD	V
I_{IH}	High−level input current				50	μA
I_{IL}	Low−level input current		−50			μA
R_{ext}	External Resistor for input setting “R”	Rext connect to GND (±5%)	64.6	68	71.4	kΩ

5. Floating refers to a pin left in an open state, with no external connections.

Table 11. CML RECEIVER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{RX-DIFF-DC}$	Differential Input Impedance (DC)		72	100	120	Ω
$R_{RX-SINGLE-DC}$	Single−ended Input Impedance (DC)	Measured with respect to GND over a voltage of 500 mV max.	18		30	Ω
ZRX−HIZ−DC−PD	Common−mode input impedance for V>0 during reset or power−down (DC)	VCM = 0 to 500 mV	25			kΩ
Cac_coupling	AC coupling capacitance		75		265	nF
VRX−CM−AC−P	Common mode peak voltage	AC up to 5 GHz			150	mVpeak
VRX−CM−DC−Active−Idle−Delta−P	Common mode peak voltage $\|AvgU0(\|V_{RX-D+}+V_{RX-D-}\|)/2 - AvgU1(\|V_{RX-D+}+V_{RX-D-}\|)/2\|$	Between U0 and U1. AC up to 5 GHz			200	mVpeak

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 12. TRANSMITTER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{TX-DIFF-PP}$	Output differential p−p voltage swing at 100 MHz	Differential Swing $\|V_{TX-D+}-V_{TX-D-}\|$			1.2	V_{PPd}
$R_{TX-DIFF-DC}$	Differential TX impedance (DC)		72	100	120	Ω
$V_{TX-RCV-DET}$	Voltage change allowed during receiver detect				600	mV
Cac_coupling	AC coupling capacitance		75		265	nF
TTX−EYE(10Gbps)	Transmitter eye, Include all jitter	At the silicon pad. 10Gbps	0.646			UI
TTX−EYE(5Gbps)	Transmitter eye, Include all jitter	At the silicon pad. 5Gbps	0.625			UI
TTX−DJ−DD(10Gbps)	Transmitter deterministic jitter	At the silicon pad. 10Gbps			0.17	UI
TTX−DJ−DD(5Gbps)	Transmitter deterministic jitter	At the silicon pad. 5Gbps			0.205	UI
Ctxparasitic	Parasitic capacitor for TX				1.1	pF
RTX−DC−CM	Common−mode output impedance (DC)		18		30	Ω
VTX−DC−CM	Instantaneous allowed DC common mode voltage at the connector side of the AC coupling capacitors	$\|V_{TX-D+}+V_{TX-D-}\|/2$	0		2.2	V
VTX−C	Common−mode voltage	$\|V_{TX-D+}+V_{TX-D-}\|/2$	VDD − 1.5		VDD	V
VTX−CM−AC−PP−Active	TX AC common−mode peak−to−peak voltage swing in active mode	$V_{TX-D+}+V_{TX-D-}$ for both time and amplitude			100	mV_{PP}
$V_{TX-CM-DC}$−Active_Idle−Delta	Common mode delta voltage $\|AvgU0(\|V_{TX-D+}+V_{TX-D-}\|)/2 - AvgU1(\|V_{TX-D+}+V_{TX-D-}\|)/2\|$	Between U0 to U1			200	mVpeak
$V_{TX-Idle-DIFF-AC-pp}$	Idle mode AC common mode delta voltage $\|V_{TX-D+}-V_{TX-D-}\|$	Between TX+ and TX− in idle mode. Use the HPF to remove DC components. 1/LPF. No AC and DC signals are applied to RX terminals.			10	mVppd
$V_{TX-Idle-DIFF-DC}$	Idle mode DC common mode delta voltage $\|V_{TX-D+}-V_{TX-D-}\|$	Between TX+ and TX− in idle mode. Use the LPF to remove DC components. 1/HPF. No AC and DC signals are applied to RX terminals.			10	mV

Table 12. TRANSMITTER AC/DC CHARACTERISTICS
VDD = 3.3 V +/− 0.3 V Over operating free−air temperature range (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
CHANNEL PERFORMANCE						
Gp	Peaking gain (Compensation at 5 GHz, relative to 100 MHz, 100 mVp−p sine wave input)	EQx = L EQx = R EQx = F EQx = H		11.5 7.4 9.9 13.1		dB
		Variation around typical	−3		+3	dB
GF	Flat Gain (<100 MHz, EQx=F)	FGx = L FGx = R FGx = F FGx = H		−1.2 0 +1.0 +2.0		dB
		Variation around typical	−3		+3	dB
V_{SW_100M}	−1 dB compression point output swing (100 MHz)			1000		mVppd
V_{SW_5G}	−1 dB compression point output swing (5 GHz)			750		mVppd
DDNEXT	Differential near−end crosstalk (Note 6)	100 MHz to 5GHz, Figure 6		−40		dB
SIGNAL AND FREQUENCY DETECTORS						
Vth_dsm	Low power slumber mode detector threshold	LFPS signal threshold in Low power Slumber mode	100		600	mVppd
Vth_am	Active mode detector threshold	Signal threshold in Active and Slumber mode (Note 7)	45		175	mVppd

6. Measured using a vector network analyzer (VNA) with −15 dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50−Ω.
7. Below the minimum is no signal ≥ 25°C. Above the maximum is active.

PARAMETER MEASUREMENT DIAGRAMS

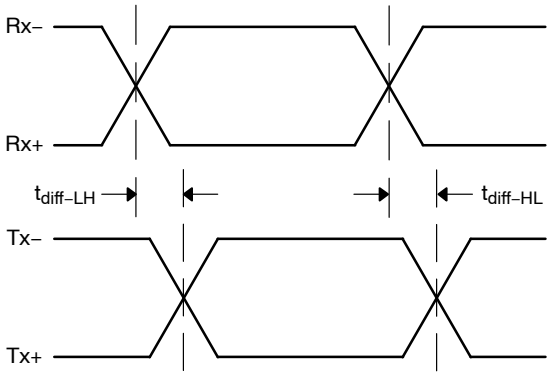


Figure 3. Propagation Delay

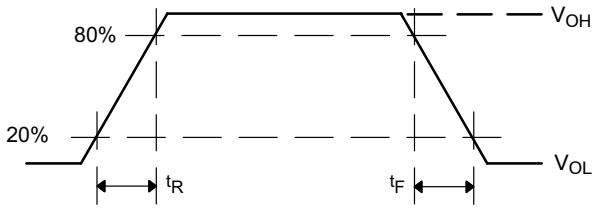


Figure 4. Output Rise and Fall Times

APPLICATION GUIDELINES

LFPS Compliance Testing

As part of USB 3.1 compliance test, the host or peripheral must transmit a LFPS signal that adheres to the spec parameters. The NB7NPQ1104M is tested as a part of a USB compliant system to ensure that it maintains compliance while increasing system performance.

LFPS Functionality

USB 3.1, Gen1 and Gen2 use Low Frequency Periodic Signaling.

(LFPS) to implement functions like exiting low−power modes, performing warm resets and providing link training between host and peripheral devices. LFPS signaling consists of bursts of frequencies ranging between 10 to 50 MHz and can have specific burst lengths or repeat rates.

Ping.LFPS for TX Compliance

During the transmitter compliance, the system under test must transmit certain compliance patterns as defined by the USB−IF. In order to toggle through these patterns for various tests, the receiver must receive a ping.LFPS signal from either the test suite or a separate pattern generator. The standard signal comprises of a single burst period of 100 ns at 20 MHz.

Control Pin Settings

Control pins A1, A0, B1, and B0 control the Flat Gain and the Equalization of channels A and B and control pins C1, C0, D1, and D0 control the Flat Gain and the Equalization of channels C and D of the NB7NPQ1104M Device.

The Float (Default) Setting “F” can be set by leaving the control pins in a floating state. The Redriver will internally bias the control pins to the correct voltage to achieve this if the pin is not connected to a voltage source. The low Setting “L” is set by pulling the control pin to ground. Likewise the high setting “H” is set by pulling the pin high to VCC. The $R_{external}$ setting can be set by adding a 68−K resistor from the control pin to ground. This will bias the Redriver internal voltage to 33% of VCC.

Linear Equalization

The linear equalization that the NB7NPQ1104M provides compensates for losses that occur naturally along board traces and cable lines. Linear Equalization boosts high frequencies and lower frequencies linearly so when transmitting at varying frequencies, the voltage amplitude will remain consistent. This compensation electrically counters losses and allows for longer traces to be possible when routing.

DC Flat Gain

DC flat gain equally boosts high and low frequency signals, and is essential for countering low frequency losses.

DC flat gain can also be used to simulate a higher input signal from a USB Controller. If a USB controller can only provide 800 mV differential to a receiver, it can be boosted to 1128 mV using 2 dB of flat gain.

Total Gain

When using Flat Gain with Equalization in a USB application it is important to make sure that the total voltage does not exceed 1200 mV. Total gain can be calculated by adding the EQ gain to the FG.

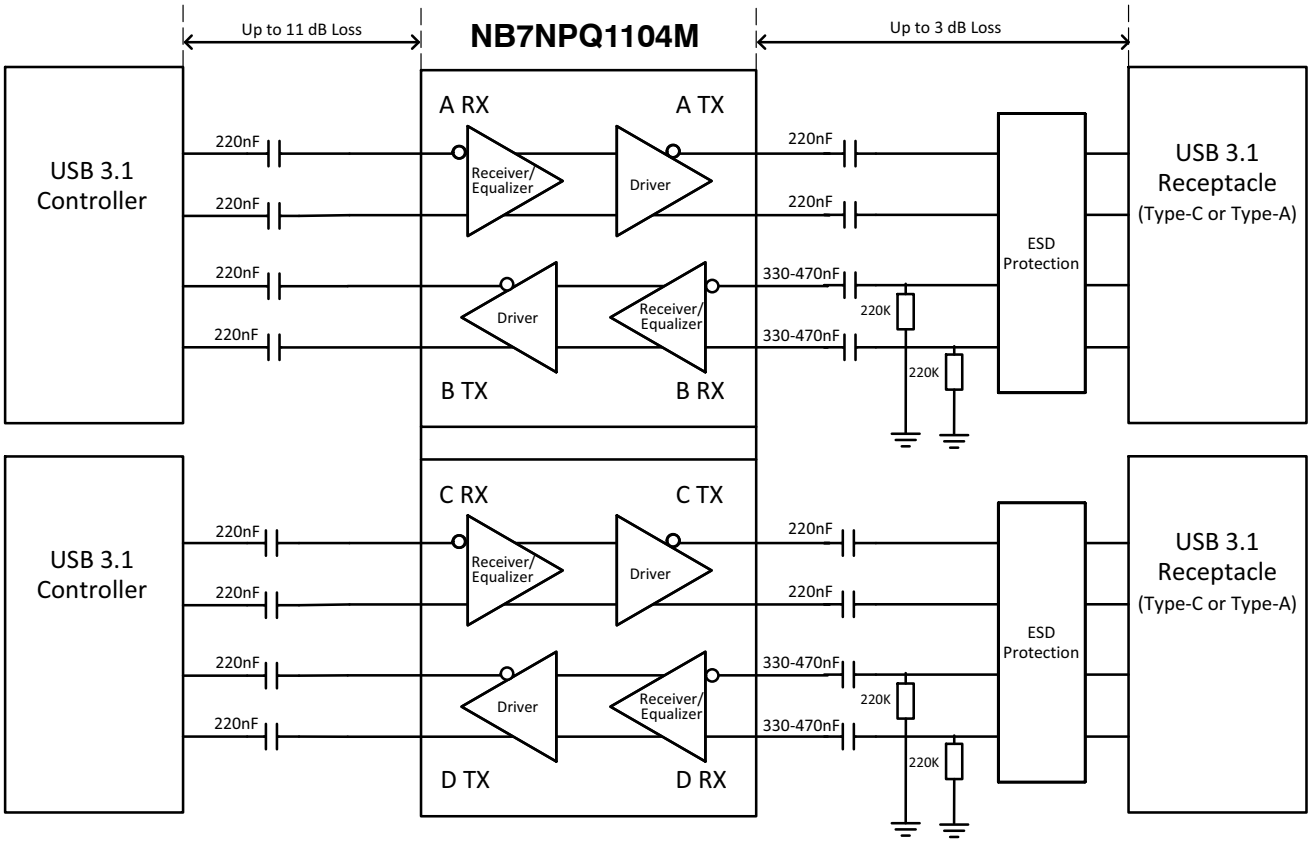


Figure 5. Typical Application

Table 13. DESIGN REQUIREMENTS

Design Parameter	Value
Supply Voltage	3.3 V nominal, (3.135 V to 3.465 V)
Operation Mode (Control Pin Selection)	Floating by Default, adjust for application losses
TX AC Coupling Capacitors	220 nF nominal, 75 nF to 265 nF, see Figure 5
RX AC Coupling Capacitors	330 – 470 nF nominal, see Figure 5
$R_{external}$	68 kΩ, ±5%
RX Pull Down Resistors at Receptacle	200 KΩ to 220 KΩ
Power Supply Capacitors	100 nF to GND close to each Vcc pin, and 10 μF to GND on the Vcc plane
Trace loss of FR4 before NB7NPQ1104M	Up to 11 dB Losses
Trace loss of FR4 after NB7NPQ1104M	Up To 3 dB Losses. Keep as short as possible for best performance.
Linear Range at 5 GHz	900 mV differential
DC Flat Gain Options	−1.2 dB, 0 dB, +1.0 dB, +2.0 dB
Equalization Options	7.4 to 13.1 dB
Differential Trace Impedance	90 Ω ±10%

8. Trace loss of FR4 was estimated to have 1 dB of loss per 1 inch of FR4 length with matched impedance and no VIAS.

Typical Layout Practices

- RX and TX pairs should maintain as close to a 90 Ω differential impedance as possible.
- Limit the number of vias used on each data line. It is suggested that 2 or fewer are used.
- Traces should be routed as straight and symmetric as possible.
- RX and TX differential pairs should always be placed and routed on the same layer directly above a ground plane. This will help reduce EMI and noise on the data lines.
- Routing angles should be obtuse angles and kept to 135 degrees or larger.
- To minimize crosstalk, TX and RX data lines should be kept away from other high speed signals.

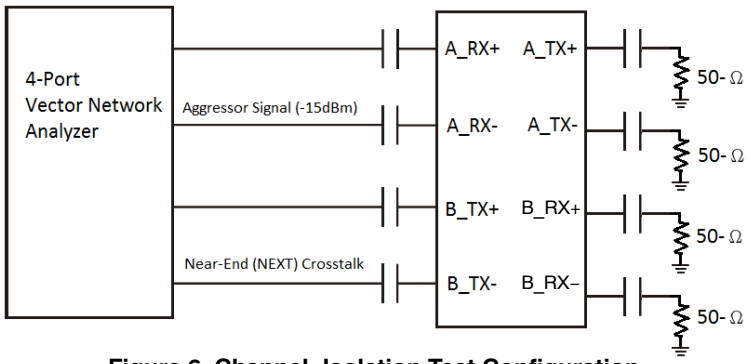


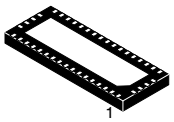
Figure 6. Channel−Isolation Test Configuration

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

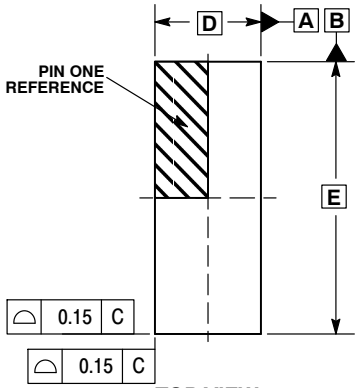
ON Semiconductor®

WQFN42 3.5x9, 0.5P
CASE 510AP−01
ISSUE O

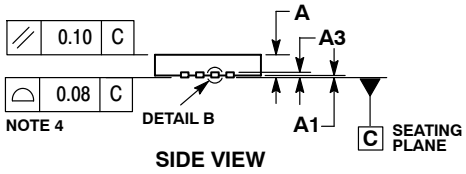
DATE 15 FEB 2010



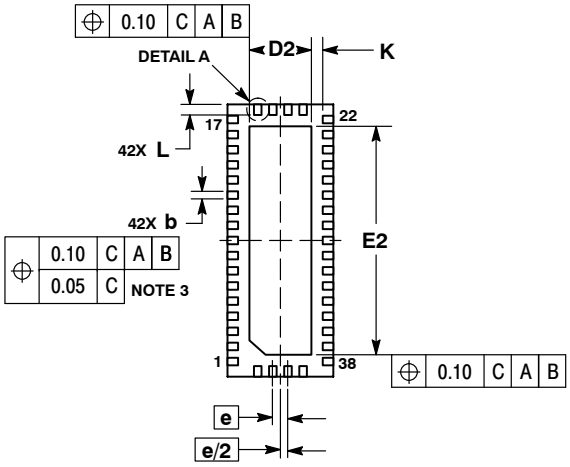
SCALE 2:1



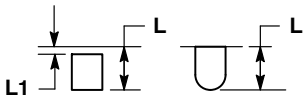
TOP VIEW



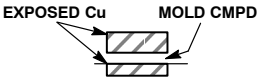
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

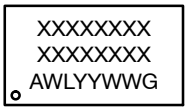


DETAIL B
ALTERNATE CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.50 BSC	
D2	1.95	2.15
E	9.00 BSC	
E2	7.45	7.65
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50
L1	0.00	0.15

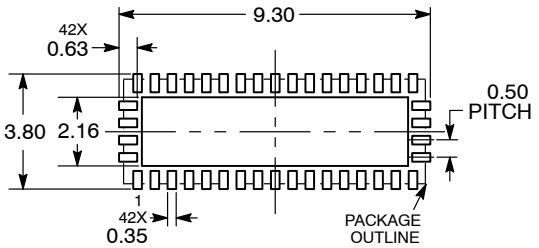
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98AON48316E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	WQFN42 3.5X9, 0.5P	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales