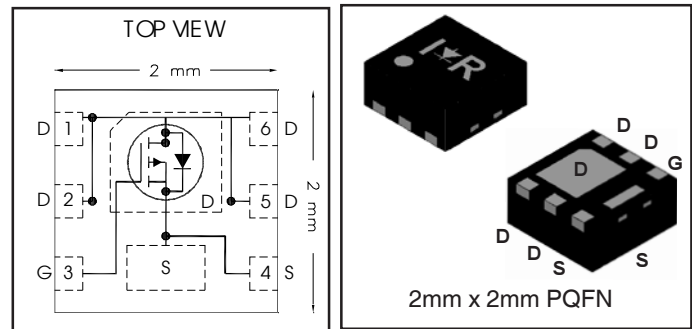


HEXFET® Power MOSFET

V_{DS}	-20	V
$V_{GS\ max}$	±12	V
$R_{DS(on)\ max}$ (@ $V_{GS} = 4.5V$)	31	mΩ
$R_{DS(on)\ max}$ (@ $V_{GS} = 2.5V$)	53	mΩ
$Q_g\ typ$	9.6	nC
I_D (@ $T_{c(Bottom)} = 25^\circ C$)	-8.5 Ⓐ	A



Applications

- Charge and Discharge Switch for Battery Application
- System/load switch

Features and Benefits

Features

Low Thermal Resistance to PCB ($\leq 13^\circ C/W$)
Low Profile ($\leq 1.0mm$)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant Containing no Lead, no Bromide and no Halogen
MSL1, Industrial Qualification

results in
 \Rightarrow

Benefits

Enable better thermal dissipation
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRLHS2242TRPbF	PQFN 2mm x 2mm	Tape and Reel	4000	
IRLHS2242TR2PbF	PQFN 2mm x 2mm	Tape and Reel	400	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	±12	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-7.2	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-5.8	
$I_D @ T_{c(Bottom)} = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-15Ⓐ	
$I_D @ T_{c(Bottom)} = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	-9.8Ⓐ	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$ (Wirebond Limited)	-8.5Ⓐ	
I_{DM}	Pulsed Drain Current ①	-34	
$P_D @ T_A = 25^\circ C$	Power Dissipation ②	2.1	W
$P_D @ T_{c(Bottom)} = 25^\circ C$	Power Dissipation ②	9.6	
	Linear Derating Factor ③	0.02	W/°C
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		

Notes ① through ⑦ are on page 9

Static @ T_J = 25°C (unless otherwise specified)

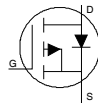
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.01	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	25	31	mΩ	V _{GS} = -4.5V, I _D = -8.5A ③
		—	43	53		V _{GS} = -2.5V, I _D = -6.8A ③
V _{GS(th)}	Gate Threshold Voltage	-0.4	-0.8	-1.1	V	V _{DS} = V _{GS} , I _D = -10μA
ΔV _{GS(th)}	Gate Threshold Voltage Coefficient	—	-3.8	—	mV/°C	
I _{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	V _{DS} = -16V, V _{GS} = 0V
		—	—	-150		V _{DS} = -16V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -12V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 12V
g _{fs}	Forward Transconductance	10	—	—	S	V _{DS} = -10V, I _D = -8.5A
Q _g	Total Gate Charge	—	12	—	nC	V _{GS} = -10V, V _{DS} = -10V, I _D = -8.5A
Q _g	Total Gate Charge	—	9.6	—	nC	V _{DS} = -10V V _{GS} = -4.5V I _D = -8.5A
Q _{gs}	Gate-to-Source Charge	—	1.6	—		
Q _{gd}	Gate-to-Drain Charge	—	3.7	—		
Q _{godr}	Gate Charge Overdrive	—	4.3	—		
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	—	4.8	—		
Q _{oss}	Output Charge	—	6.8	—	nC	V _{DS} = 16V, V _{GS} = 0V
R _G	Gate Resistance	—	17	—	Ω	
t _{d(on)}	Turn-On Delay Time	—	7.9	—	ns	V _{DD} = -10V, V _{GS} = -4.5V I _D = -8.5A R _G = 2.0Ω
t _r	Rise Time	—	54	—		
t _{d(off)}	Turn-Off Delay Time	—	54	—		
t _f	Fall Time	—	66	—		
C _{iss}	Input Capacitance	—	877	—	pF	V _{GS} = 0V V _{DS} = -10V f = 1.0KHz
C _{oss}	Output Capacitance	—	273	—		
C _{riss}	Reverse Transfer Capacitance	—	182	—		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	18	mJ
I _{AR}	Avalanche Current ①	—	-8.5	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-8.5⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-34		
V _{SD}	Diode Forward Voltage	—	—	-1.2	V	T _J = 25°C, I _S = -8.5A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	—	27	41	ns	T _J = 25°C, I _F = -8.5A, V _{DD} = -10V
Q _{rr}	Reverse Recovery Charge	—	20	30	nC	di/dt = 200A/μs ③
t _{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				


Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC} (Bottom)	Junction-to-Case ⑤	—	13	°C/W
R _{θJC} (Top)	Junction-to-Case ⑤	—	90	
R _{θJA}	Junction-to-Ambient ④	—	60	
R _{θJA} (<10s)	Junction-to-Ambient ④	—	42	

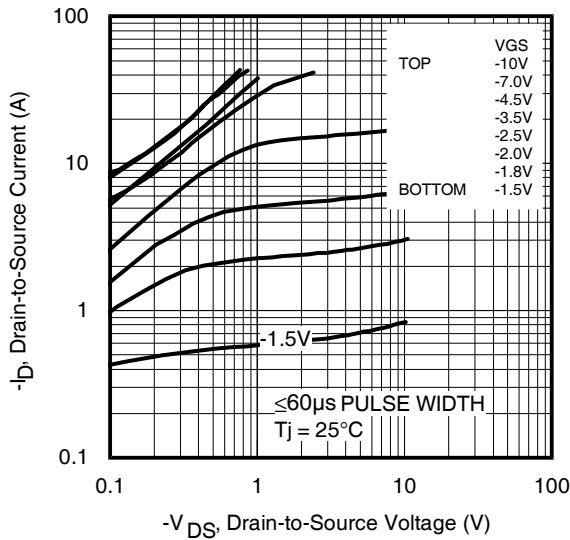


Fig 1. Typical Output Characteristics

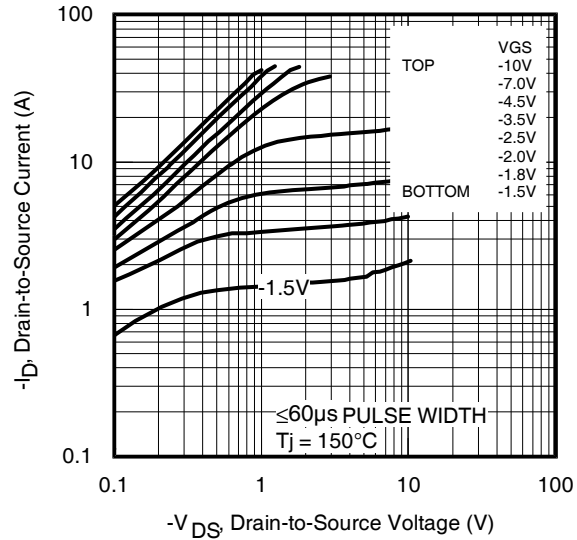


Fig 2. Typical Output Characteristics

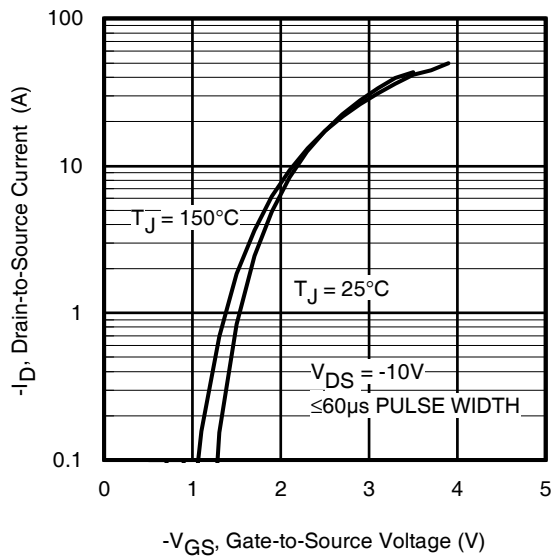


Fig 3. Typical Transfer Characteristics

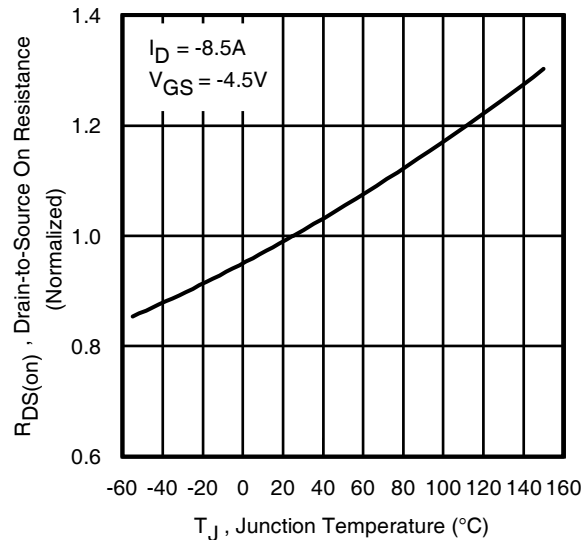


Fig 4. Normalized On-Resistance vs. Temperature

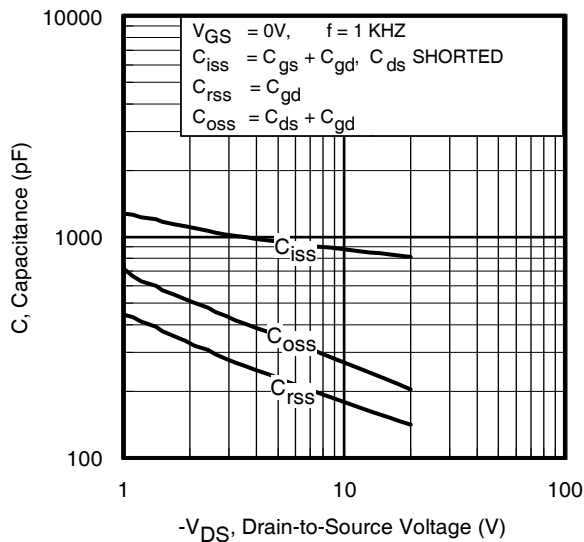


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

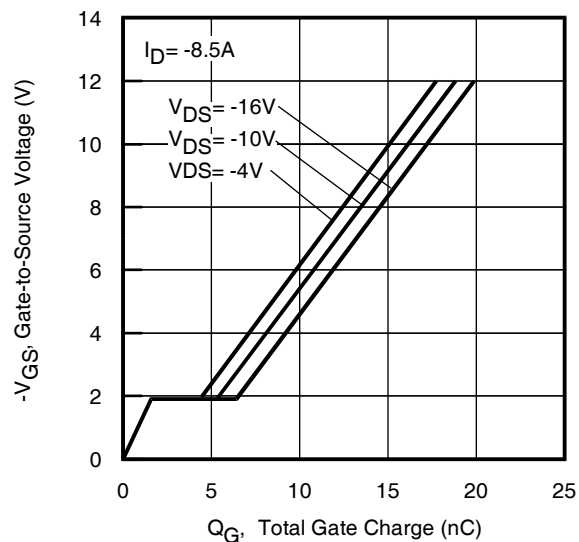
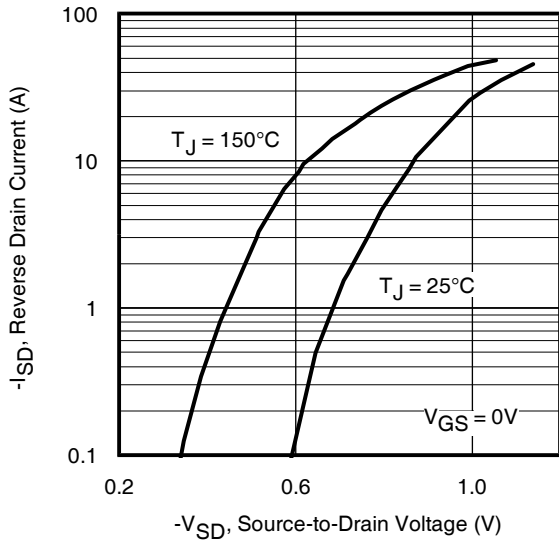
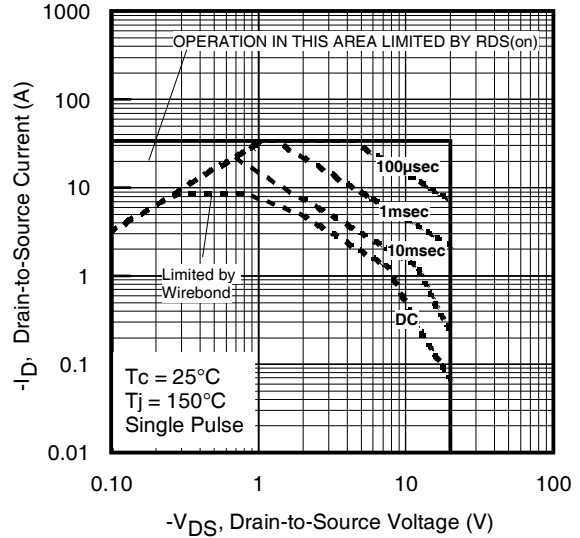
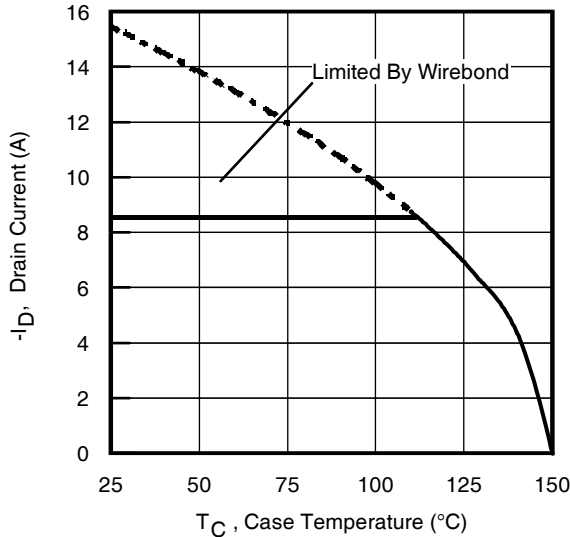
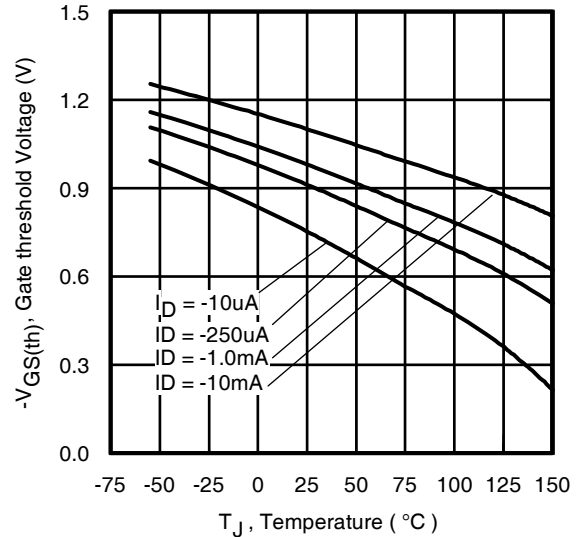
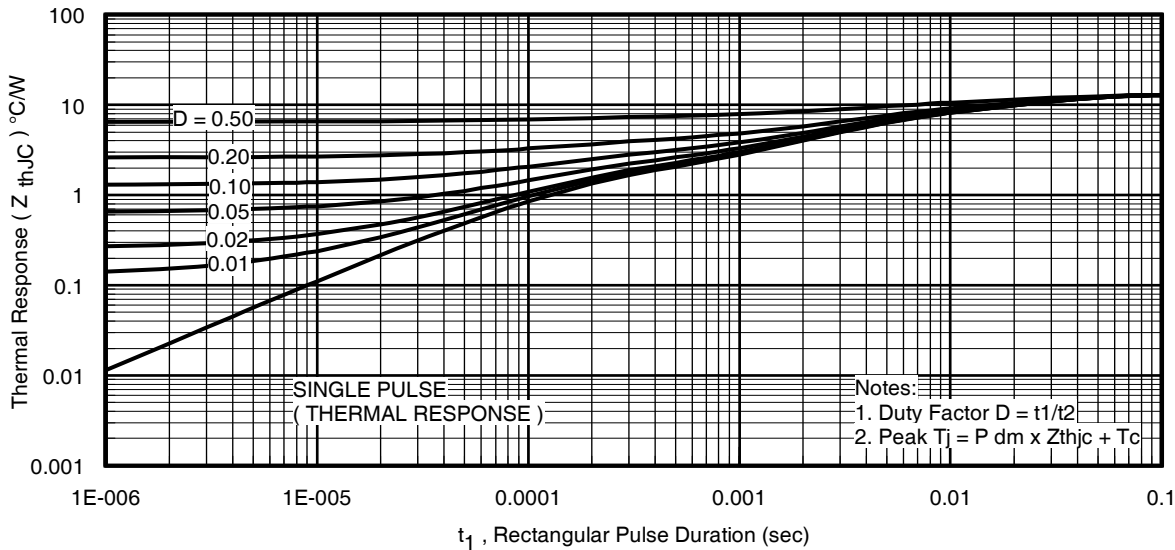


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

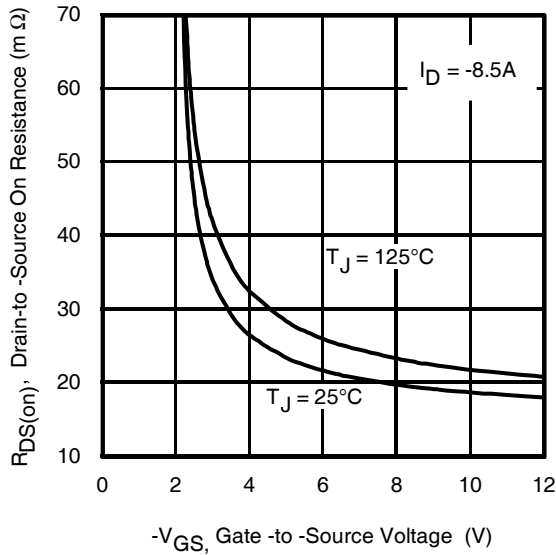


Fig 12. On-Resistance vs. Gate Voltage

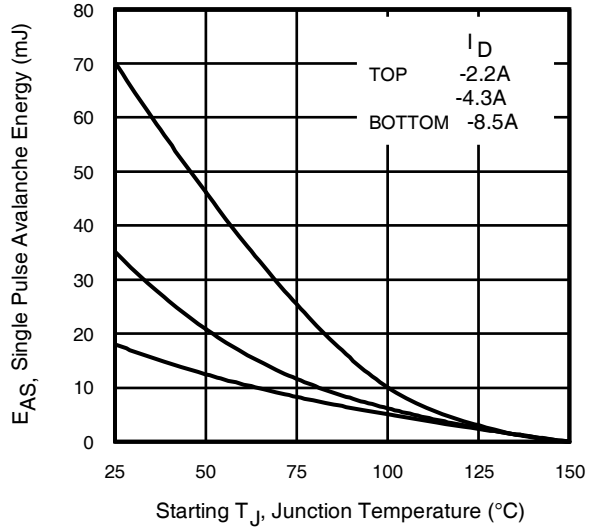


Fig 13. Maximum Avalanche Energy vs. Drain Current

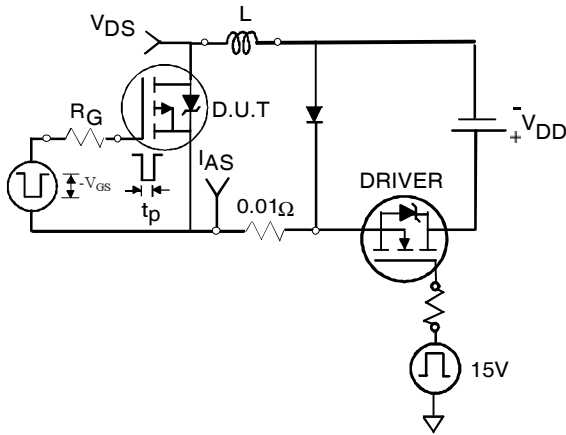


Fig 14a. Unclamped Inductive Test Circuit

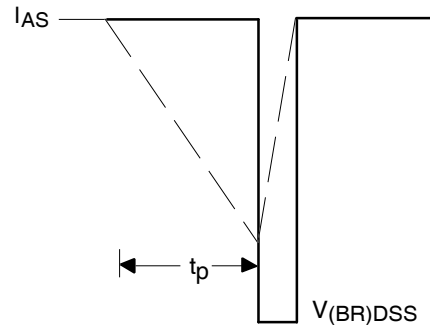


Fig 14b. Unclamped Inductive Waveforms

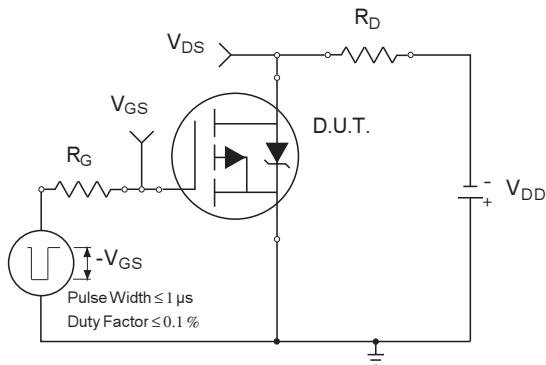


Fig 15a. Switching Time Test Circuit

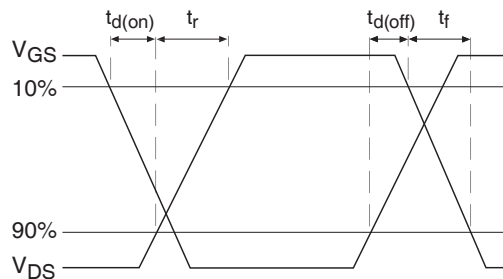


Fig 15b. Switching Time Waveforms

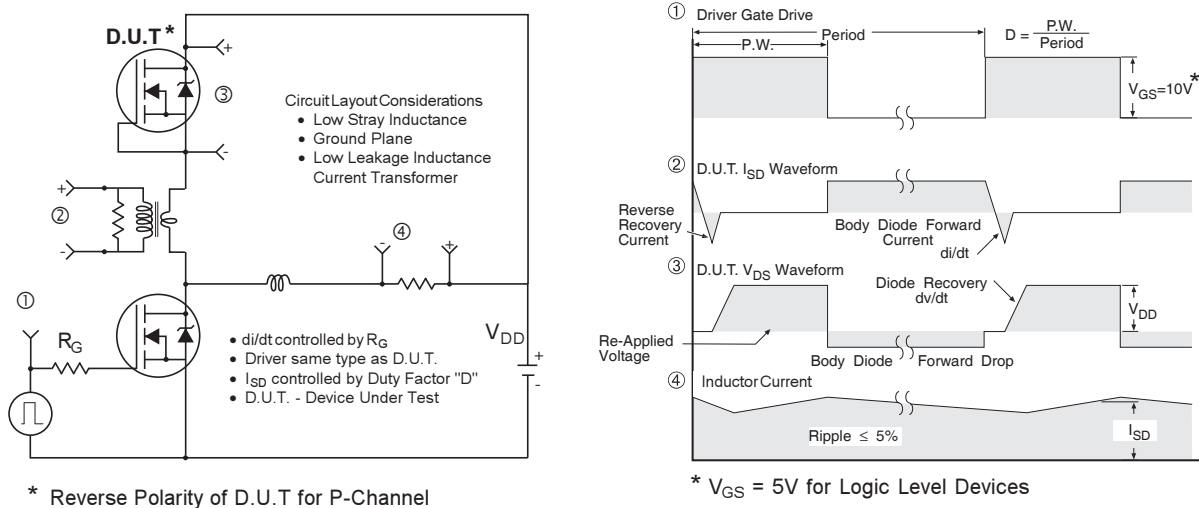


Fig 16. Diode Reverse Recovery Test Circuit for P-Channel HEXFET® Power MOSFETs

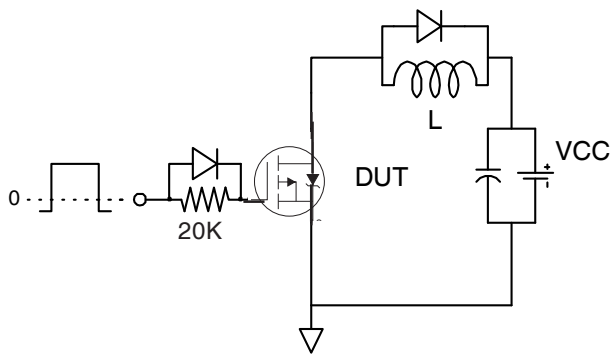


Fig 17a. Gate Charge Test Circuit

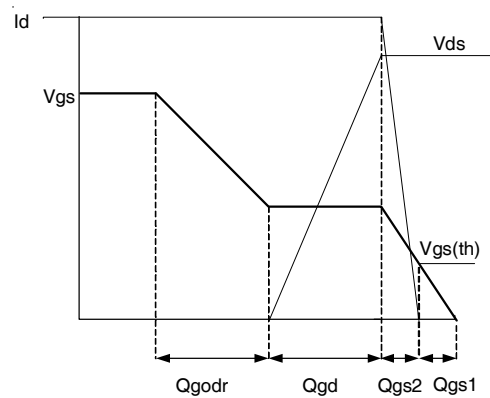
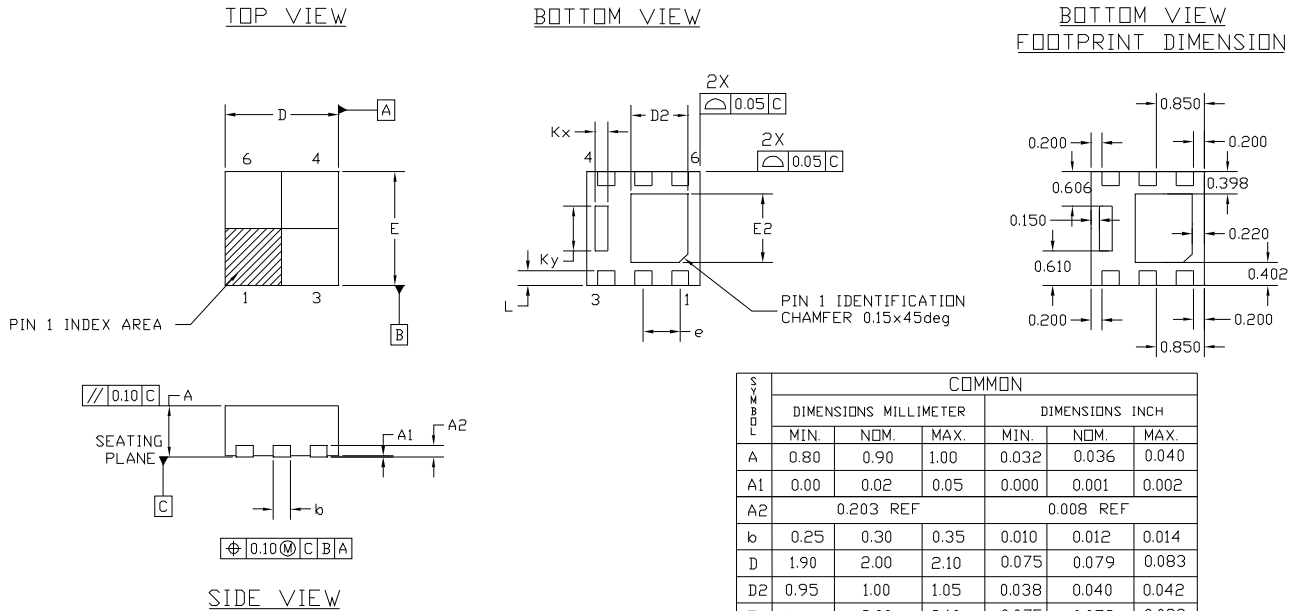


Fig 17b. Gate Charge Waveform

PQFN Package Details

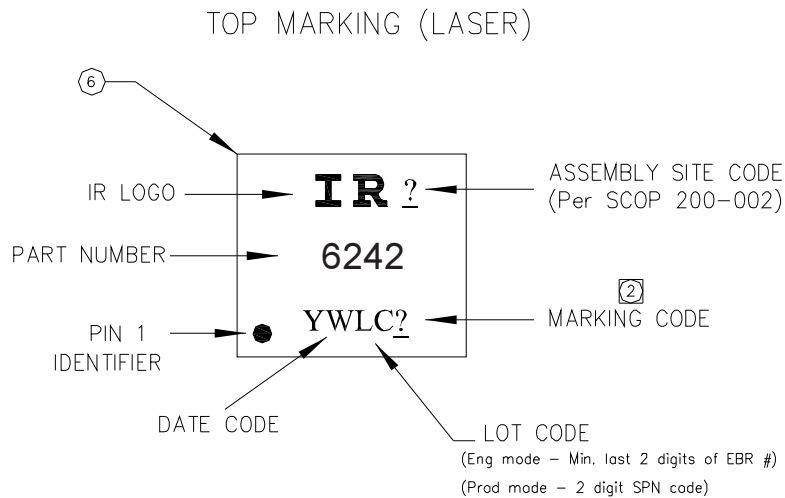


SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.036	0.040
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.203 REF			0.008 REF		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D2	0.95	1.00	1.05	0.038	0.040	0.042
E	1.90	2.00	2.10	0.075	0.079	0.083
E2	1.15	1.20	1.25	0.046	0.048	0.050
e	0.65 BSC			0.026 BSC		
L	0.20	0.25	0.30	0.008	0.010	0.012
Kx	0.23 REF			0.010 REF		
Ky	0.785 REF			0.031 REF		

NOTES :

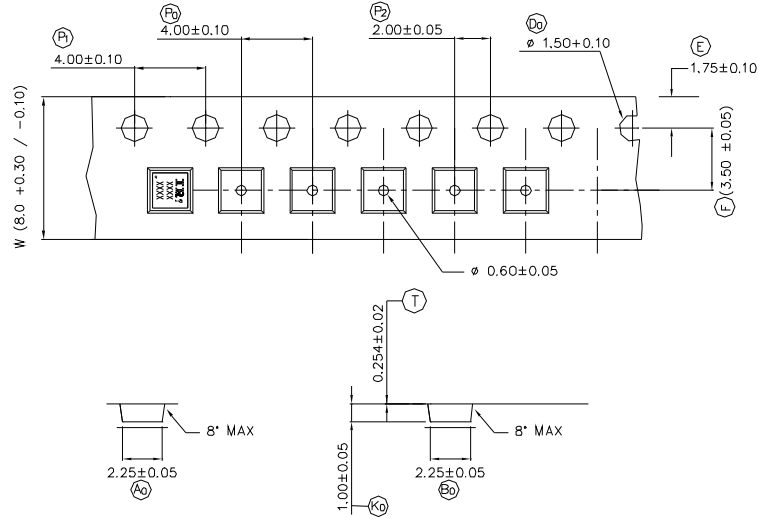
1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER
3. DIMENSION *b* APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm. FROM TERMINAL TIP.

PQFN Part Marking

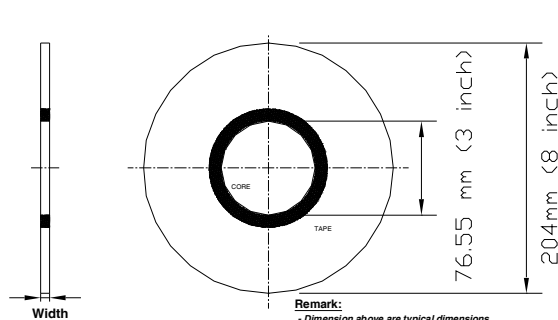


Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

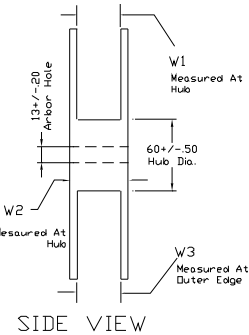
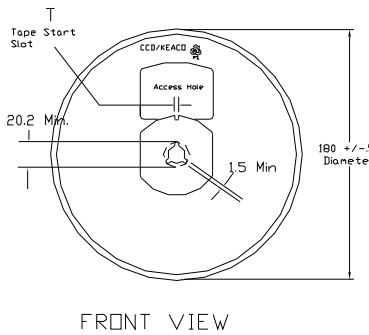
PQFN 2x2 Outline Tape and Reel



NOTE: The Surface Resistivity is $10^4 - 10^8$ OHM/SQ



Remark:
 - Dimension above are typical dimensions.
 - Cover tape thickness is 0.048mm +/- 0.005mm.
 - Surface resistivity $10E5 < R_s < 10E9$.



COVER TAPE (WIDTH)	TOLERANCE
5.4 mm	+/- 0.1 mm
9.5 mm	+/- 0.1 mm

TAPE WIDTH	T	W1	W2	W3	PART NO
8 MM	3 ± 0.50	8.4 ^{+1.5} _{-0.0}	14.4 Max	7.90 Min 10.9 Max	91586-1
12 MM	5 ± 0.50	12.4 ^{+2.0} _{-0.0}	18.4 Max	11.9 Min 15.4 Max	91586-2

Note: Surface resistivity is $\geq 1 \times 10^5$ but $< 1 \times 10^{12}$ ohm/sq.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial [†] (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN 2mm x 2mm	MSL1 (per IPC/JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site
<http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^{\circ}\text{C}$, $L = 0.49\text{mH}$, $R_G = 50\Omega$, $I_{AS} = -8.5\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_{θ} is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.
- ⑥ Calculated continuous current based on maximum allowable junction temperature.
- ⑦ Package is limited to -8.5A by die-source to lead-frame bonding technology

Revision History

Date	Comments
10/10/2013	<ul style="list-style-type: none"> • Corrected Qual level from "Consumer" to "Industrial" on page 1, 9 • Updated data sheet with new IR corporate template
12/16/2013	<ul style="list-style-type: none"> • Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259)

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