

# 100 V, 2.0 A, Low $V_{CE(sat)}$ PNP Transistor

## NSS1C200L, NSV1C200L

onsemi's e<sup>2</sup>PowerEdge family of low  $V_{CE(sat)}$  transistors are miniature surface mount devices featuring ultra low saturation voltage ( $V_{CE(sat)}$ ) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e<sup>2</sup>PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

### Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	$V_{CEO}$	-100	Vdc
Collector-Base Voltage	$V_{CBO}$	-140	Vdc
Emitter-Base Voltage	$V_{EBO}$	-7.0	Vdc
Collector Current - Continuous	$I_C$	-2.0	A
Collector Current - Peak	$I_{CM}$	-3.0	A

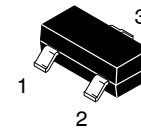
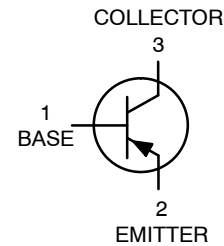
### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 1)	490 3.7	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	255	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$ (Note 2)	710 4.3	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	176	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

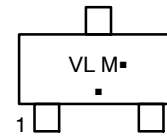
1. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces.
2. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces.

## -100 VOLTS, 2.0 AMPS PNP LOW $V_{CE(sat)}$ TRANSISTOR



SOT-23 (TO-236)  
CASE 318  
STYLE 6

### MARKING DIAGRAM



- VL = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)  
\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NSS1C200LT1G, NSV1C200LT1G	SOT-23 (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NSS1C200L, NSV1C200L

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

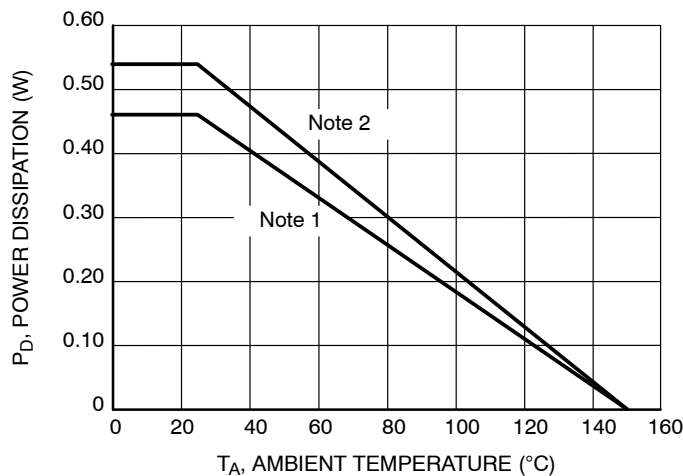
Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector - Emitter Breakdown Voltage ( $I_C = -10 \text{ mAdc}$ , $I_B = 0$ )	$V_{(BR)CEO}$	-100			Vdc
Collector - Base Breakdown Voltage ( $I_C = -0.1 \text{ mAdc}$ , $I_E = 0$ )	$V_{(BR)CBO}$	-140			Vdc
Emitter - Base Breakdown Voltage ( $I_E = -0.1 \text{ mAdc}$ , $I_C = 0$ )	$V_{(BR)EBO}$	-7.0			Vdc
Collector Cutoff Current ( $V_{CB} = -140 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$			-100	nAdc
Emitter Cutoff Current ( $V_{EB} = -6.0 \text{ Vdc}$ )	$I_{EBO}$			-50	nAdc

## ON CHARACTERISTICS

DC Current Gain (Note 3) ( $I_C = -10 \text{ mA}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -500 \text{ mA}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -1.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ ) ( $I_C = -2.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ )	$h_{FE}$	150 120 80 50	240	360	
Collector - Emitter Saturation Voltage (Note 3) ( $I_C = -0.1 \text{ A}$ , $I_B = -0.01 \text{ A}$ ) ( $I_C = -0.5 \text{ A}$ , $I_B = -0.05 \text{ A}$ ) ( $I_C = -1.0 \text{ A}$ , $I_B = -0.100 \text{ A}$ ) ( $I_C = -2.0 \text{ A}$ , $I_B = -0.200 \text{ A}$ )	$V_{CE(sat)}$			-0.040 -0.080 -0.115 -0.250	V
Base - Emitter Saturation Voltage (Note 3) ( $I_C = -1.0 \text{ A}$ , $I_B = -0.100 \text{ A}$ )	$V_{BE(sat)}$			-0.950	V
Base - Emitter Turn-on Voltage (Note 3) ( $I_C = -1.0 \text{ A}$ , $V_{CE} = -2.0 \text{ V}$ )	$V_{BE(on)}$			-0.850	V
Cutoff Frequency ( $I_C = -100 \text{ mA}$ , $V_{CE} = -5.0 \text{ V}$ , $f = 100 \text{ MHz}$ )	$f_T$		120		MHz
Input Capacitance ( $V_{EB} = 2.0 \text{ V}$ , $f = 1.0 \text{ MHz}$ )	$C_{ibo}$		200		pF
Output Capacitance ( $V_{CB} = 10 \text{ V}$ , $f = 1.0 \text{ MHz}$ )	$C_{obo}$		22		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle  $\leq$  2%.



**Figure 1. Power Derating**

# NSS1C200L, NSV1C200L

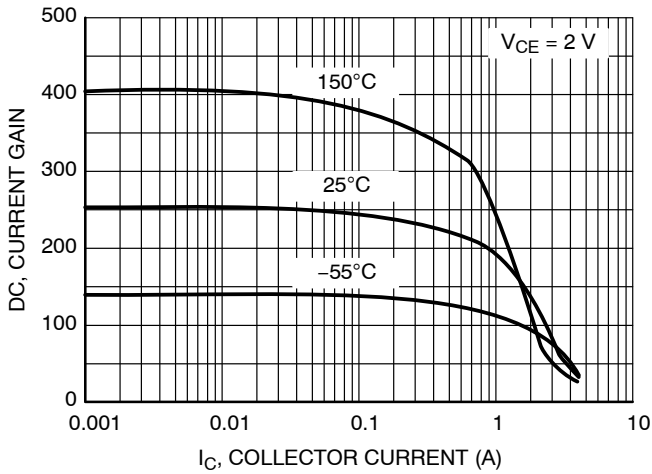


Figure 2. DC Current Gain

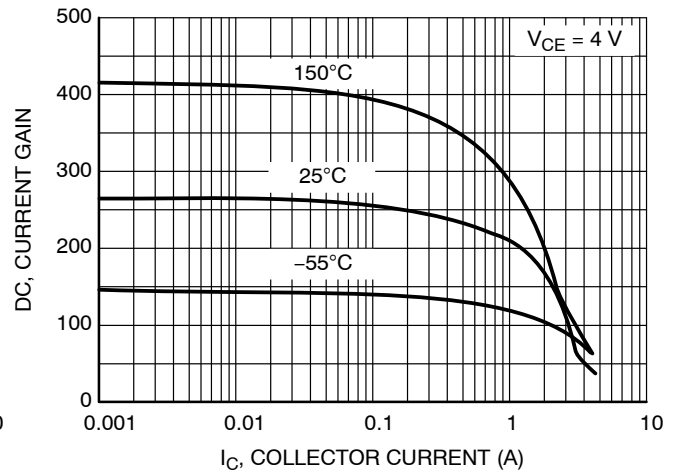


Figure 3. DC Current Gain

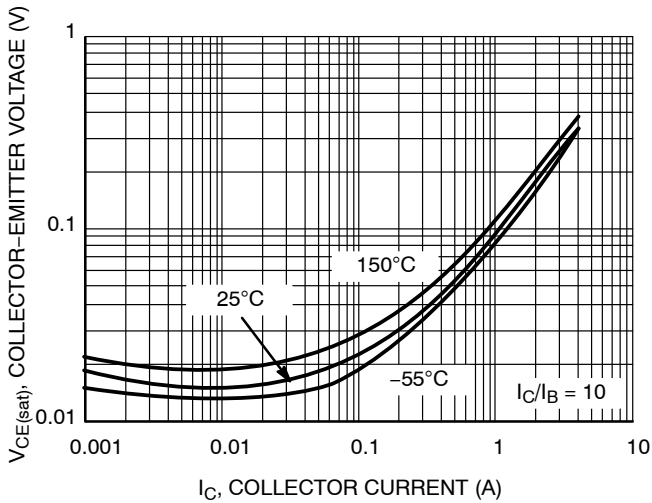


Figure 4. Collector-Emitter Saturation Voltage

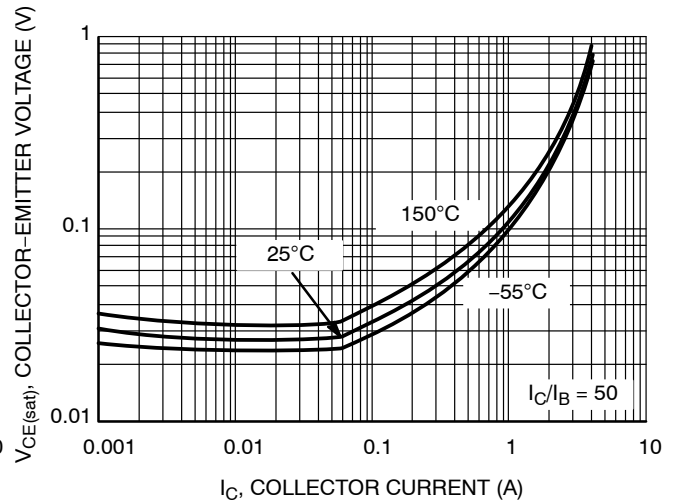


Figure 5. Collector-Emitter Saturation Voltage

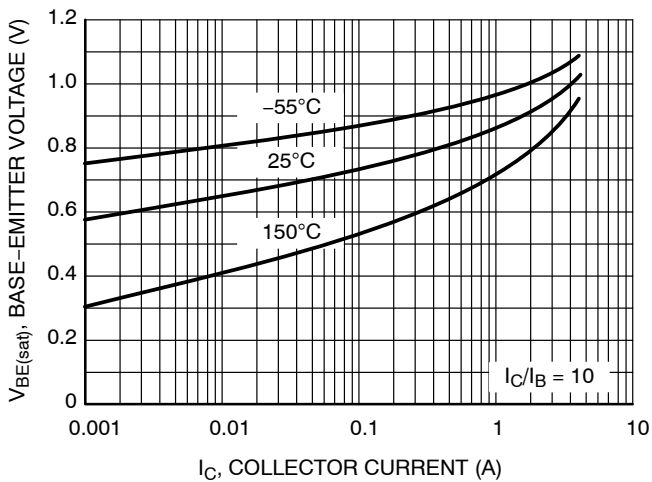


Figure 6. Base-Emitter Saturation Voltage

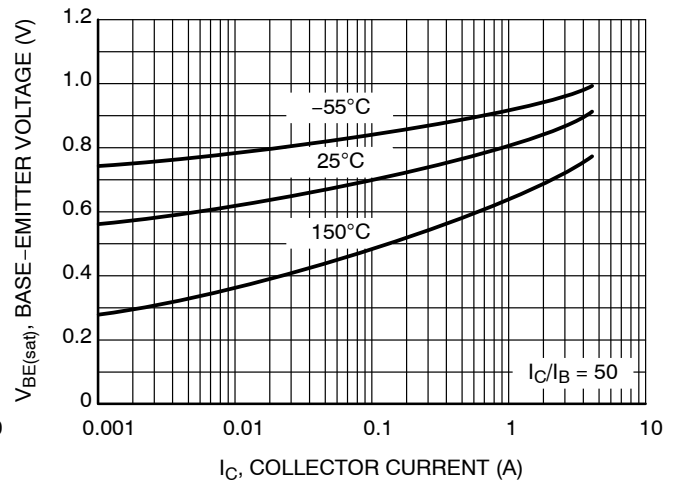
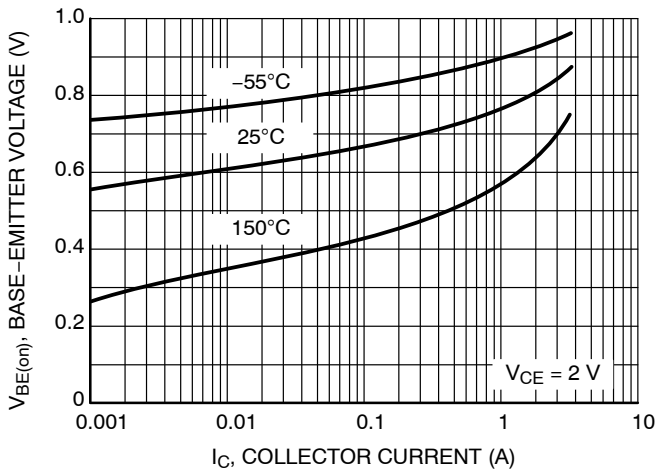
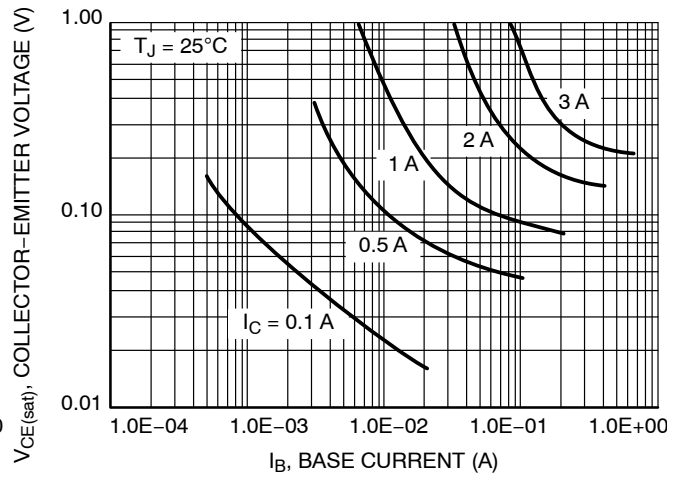


Figure 7. Base-Emitter Saturation Voltage

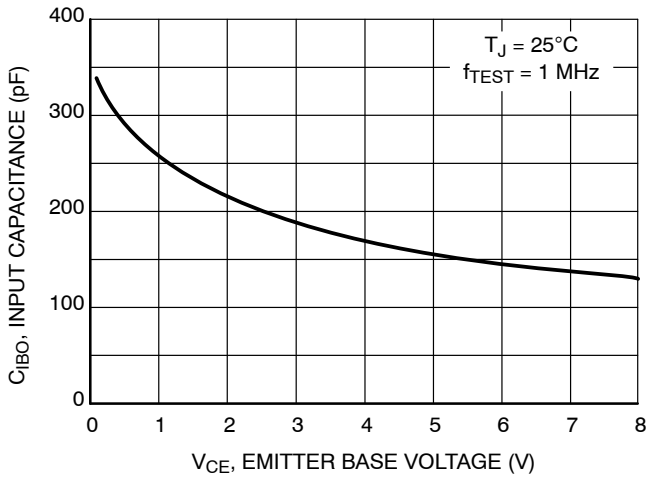
# NSS1C200L, NSV1C200L



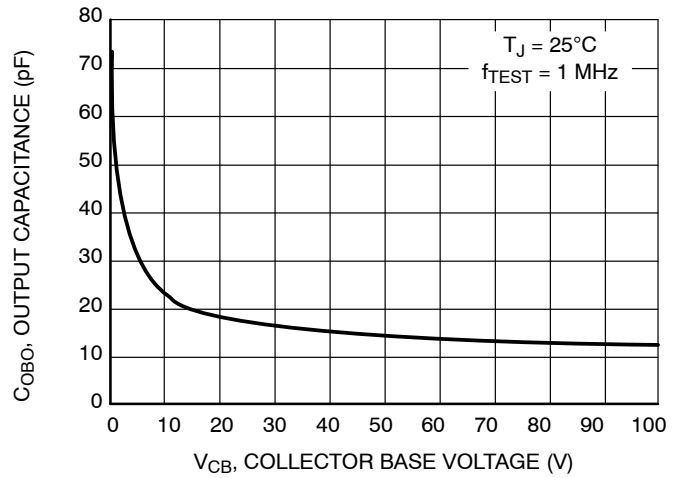
**Figure 8. Base-Emitter Saturation Voltage**



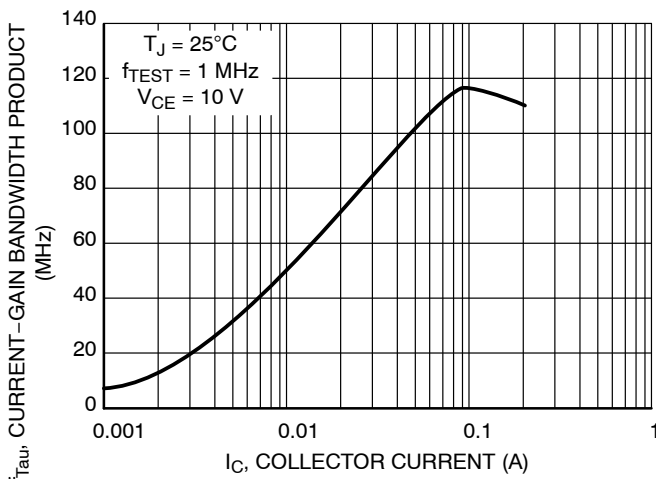
**Figure 9. Collector Saturation Region**



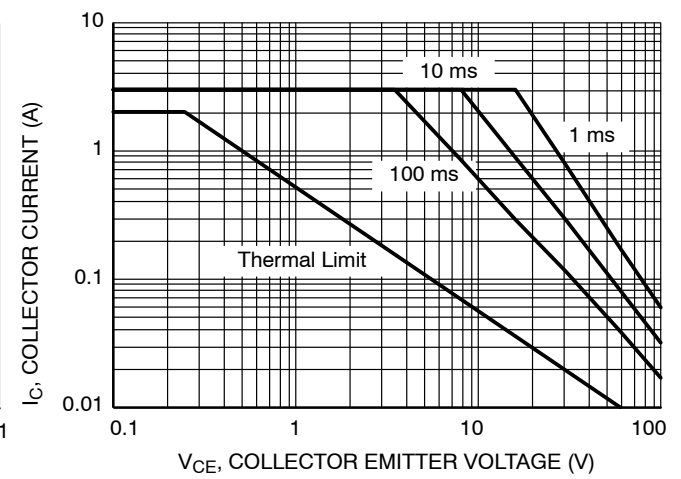
**Figure 10. Input Capacitance**



**Figure 11. Output Capacitance**



**Figure 12. Current-Gain Bandwidth Product**



**Figure 13.**

# NSS1C200L, NSV1C200L

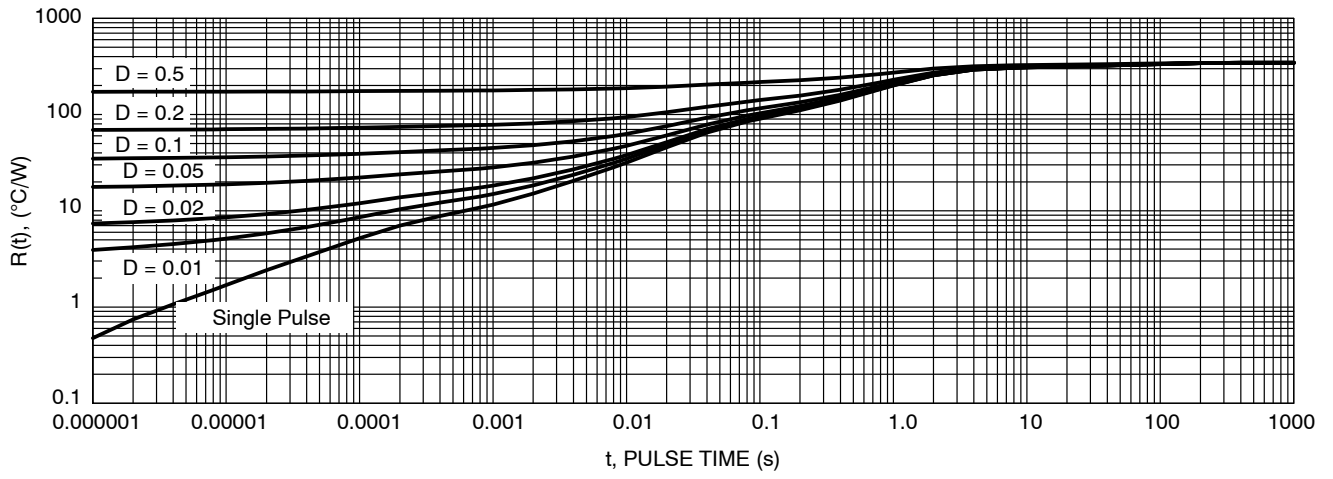


Figure 14. Transient Thermal Resistance

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**SOT-23 (TO-236)**  
CASE 318  
ISSUE AT

DATE 01 MAR 2023

SCALE 4:1



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H <sub>E</sub>	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



**RECOMMENDED MOUNTING FOOTPRINT**

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**STYLES ON PAGE 2**

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**MECHANICAL CASE OUTLINE  
PACKAGE DIMENSIONS**



**SOT-23 (TO-236)  
CASE 318  
ISSUE AT**

DATE 01 MAR 2023

- |   |   |   |   |   |   |
|---|---|---|---|---|---|
| STYLE 1 THRU 5:<br>CANCELLED                            | STYLE 6:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR | STYLE 7:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR       | STYLE 8:<br>PIN 1. ANODE<br>2. NO CONNECTION<br>3. CATHODE  |   |   |
| STYLE 9:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE      | STYLE 10:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE     | STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE-ANODE | STYLE 12:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE       | STYLE 13:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE           | STYLE 14:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 15:<br>PIN 1. GATE<br>2. CATHODE<br>3. ANODE      | STYLE 16:<br>PIN 1. ANODE<br>2. CATHODE<br>3. CATHODE | STYLE 17:<br>PIN 1. NO CONNECTION<br>2. ANODE<br>3. CATHODE | STYLE 18:<br>PIN 1. NO CONNECTION<br>2. CATHODE<br>3. ANODE | STYLE 19:<br>PIN 1. CATHODE<br>2. ANODE<br>3. CATHODE-ANODE | STYLE 20:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE          |
| STYLE 21:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN       | STYLE 22:<br>PIN 1. RETURN<br>2. OUTPUT<br>3. INPUT   | STYLE 23:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE         | STYLE 24:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE           | STYLE 25:<br>PIN 1. ANODE<br>2. CATHODE<br>3. GATE          | STYLE 26:<br>PIN 1. CATHODE<br>2. ANODE<br>3. NO CONNECTION |
| STYLE 27:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. CATHODE | STYLE 28:<br>PIN 1. ANODE<br>2. ANODE<br>3. ANODE     |   |   |   |   |

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