

MOSFET – N-Channel, POWERTRENCH®

150 V, 130 A, 7.5 mΩ

FDP075N15A, FDB075N15A

Description

This N-Channel MOSFET is produced using **onsemi** advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

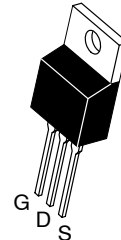
- $R_{DS(on)} = 6.25 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 100 \text{ A}$
- Fast Switching
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Applications

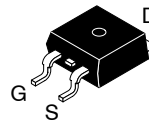
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
150 V	7.5 mΩ @ 10 V	130 A

*Package limitation current is 120 A.

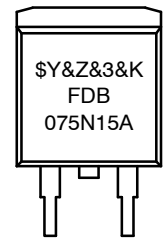
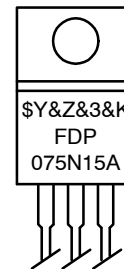


TO-220
 CASE 221A-09

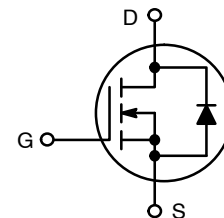


D²PAK-3 (TO-263, 3-LEAD)
 CASE 418AJ

MARKING DIAGRAM



- \$Y = onsemi logo
- FDP075N15A = Device Code
- FDB075N15A = Device Code
- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code Format
- &K = 2-Digits Lot Run Traceability Code



N-Channel

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FDP075N15A, FDB075N15A

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		FDP075N15A-F102 FDB075N15A	Unit
V_{DSS}	Drain to Source Voltage		150	V
V_{GSS}	Gate to Source Voltage	- DC	± 20	V
		- AC ($f > 1$ Hz)	± 30	
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	130*	A
		- Continuous ($T_C = 100^\circ\text{C}$)	92	
I_{DM}	Drain Current	- Pulsed (Note 1)	522	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		588	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	333	W
		- Derate Above 25°C	2.22	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Package limitation current is 120 A.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2. Starting $T_J = 25^\circ\text{C}$, $L = 3$ mH, $I_{AS} = 19.8$ A.

3. $I_{SD} \leq 100$ A, $di/dt \leq 200$ A/ μs , $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP075N15A-F102 FDB075N15A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient, D2-PAK (1 in ² Pad of 2-oz Copper), Max.	40	

FDP075N15A, FDB075N15A

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

B _V DSS	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	150	–	–	V
ΔB _V DSS / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.1	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 120 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 120 V, T _C = 150°C	–	–	500	
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	–	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 100 A	–	6.25	7.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 100 A	–	164	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 75 V, V _{GS} = 0 V, f = 1 MHz	–	5525	7350	pF
C _{oss}	Output Capacitance		–	516	685	pF
C _{rss}	Reverse Transfer Capacitance		–	21	–	pF
C _{oss(er)}	Energy Related Output Capacitance	V _{DS} = 75 V, V _{GS} = 0 V	–	909	–	pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 75 V, I _D = 100 A, V _{GS} = 10 V (Note 4)	–	77	100	nC
Q _{gs}	Gate to Source Gate Charge		–	26	–	nC
Q _{gs2}	Gate Charge Threshold to Plateau		–	11	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	16	–	nC
ESR	Equivalent Series Resistance (G–S)	f = 1 MHz	–	2.29	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 75 V, I _D = 100 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	28	66	ns
t _r	Turn-On Rise Time		–	37	84	ns
t _{d(off)}	Turn-Off Delay Time		–	62	134	ns
t _f	Turn-Off Fall Time		–	21	52	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

I _S	Maximum Continuous Drain to Source Diode Forward Current	–	–	130*	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	–	–	520	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 100 A	–	–	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 75 V, I _{SD} = 100 A, dI _F /dt = 100 A/μs	–	97	–	ns
Q _{rr}	Reverse Recovery Charge		–	264	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

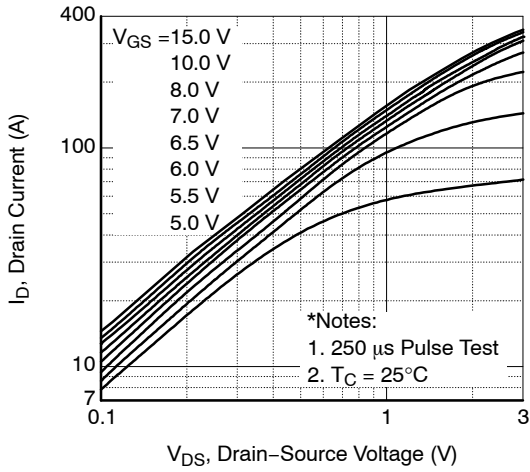


Figure 1. On-Region Characteristics

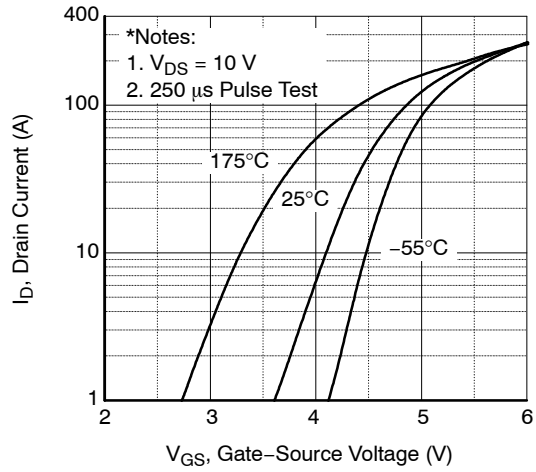


Figure 2. Transfer Characteristics

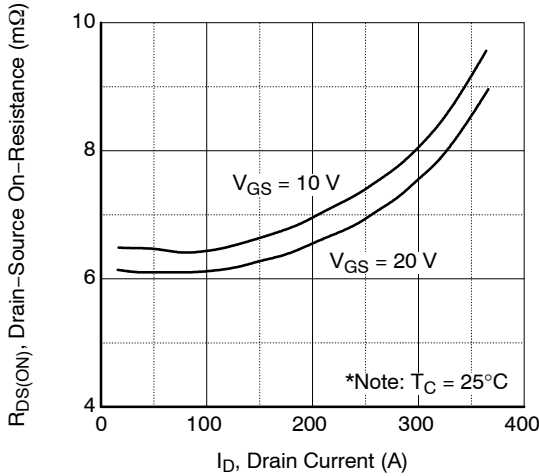


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

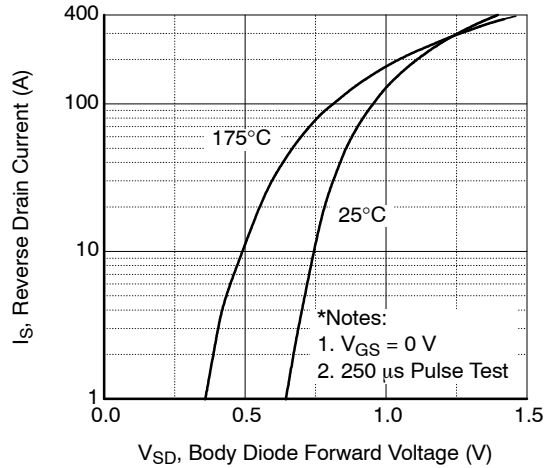


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

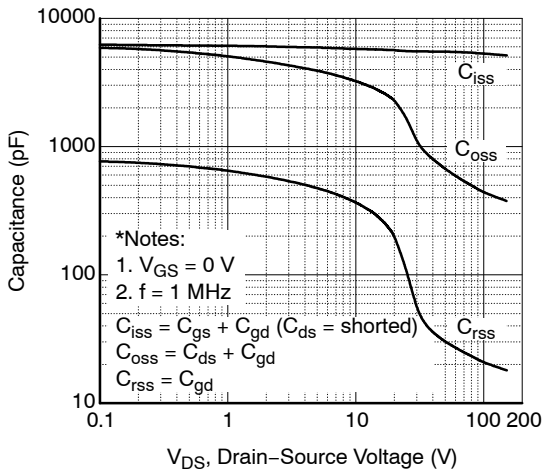


Figure 5. Capacitance Characteristics

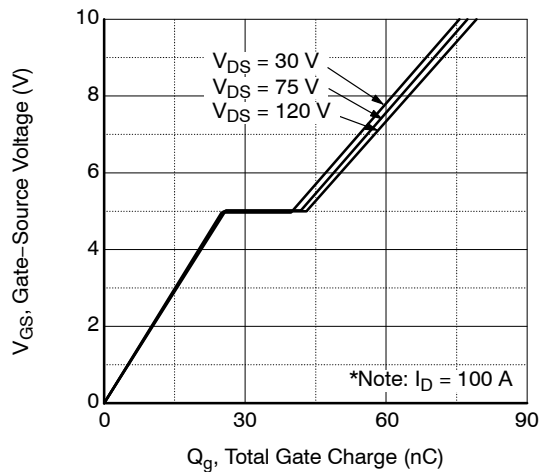
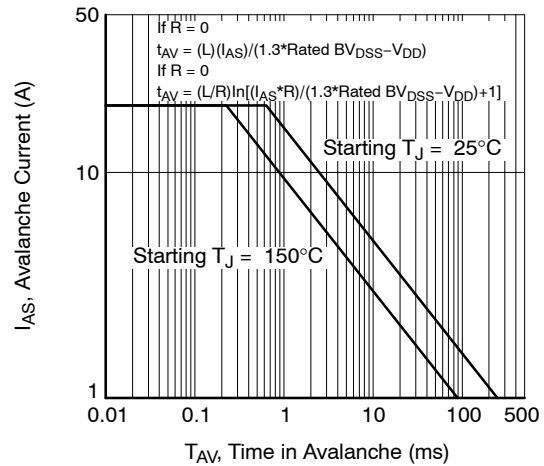
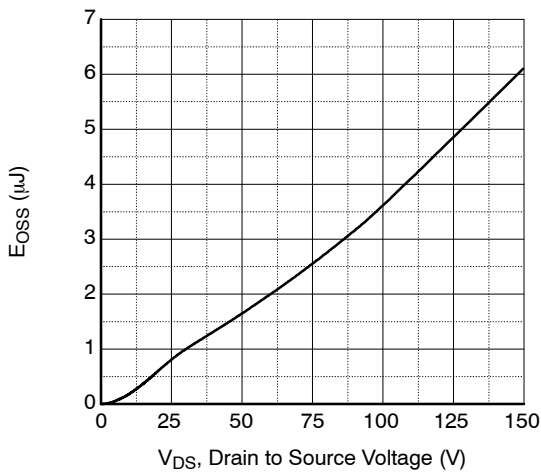
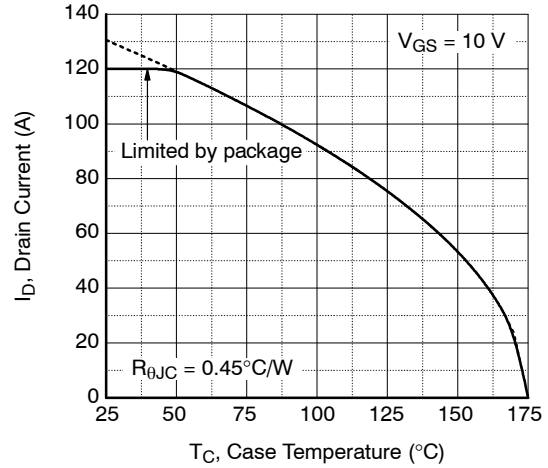
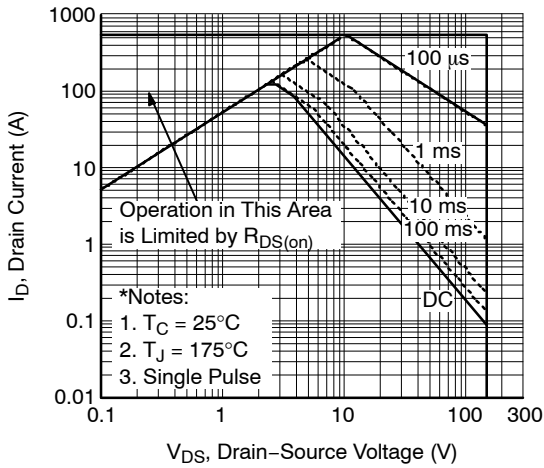
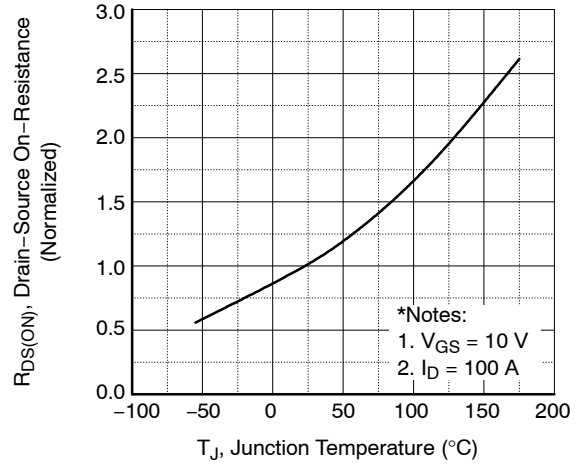
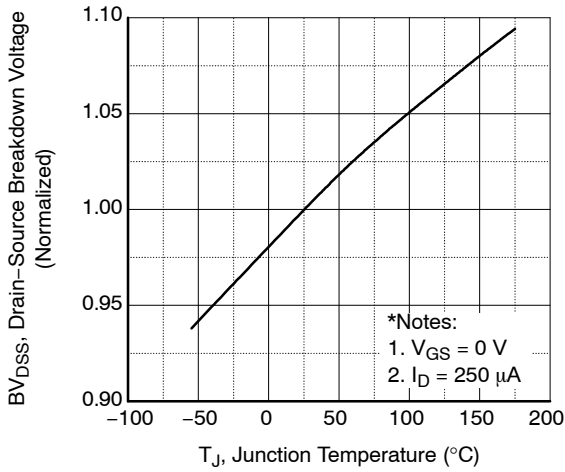


Figure 6. Gate Charge Characteristics

FDP075N15A, FDB075N15A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



FDP075N15A, FDB075N15A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

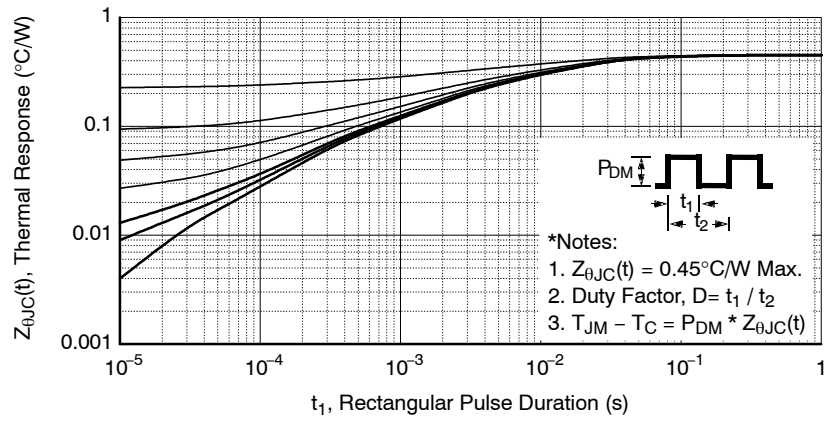


Figure 13. Transient Thermal Response Curve

FDP075N15A, FDB075N15A

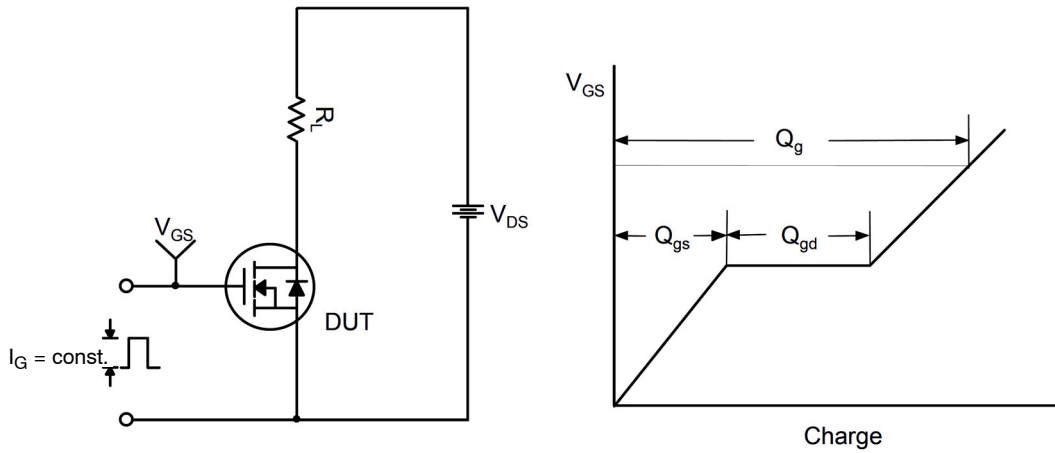


Figure 14. Gate Charge Test Circuit & Waveform

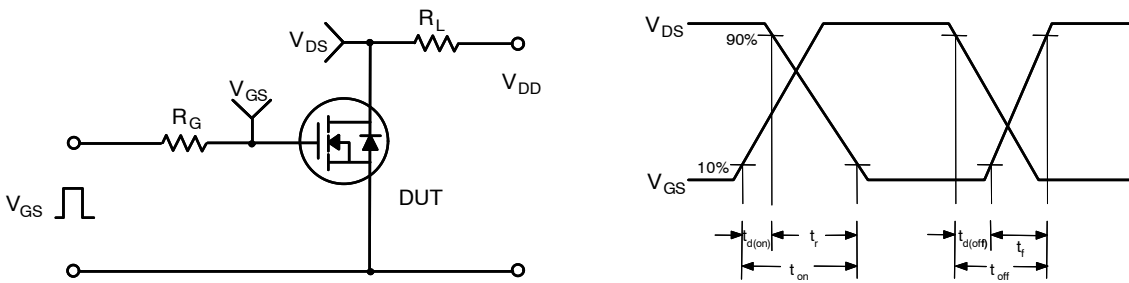


Figure 15. Resistive Switching Test Circuit & Waveforms

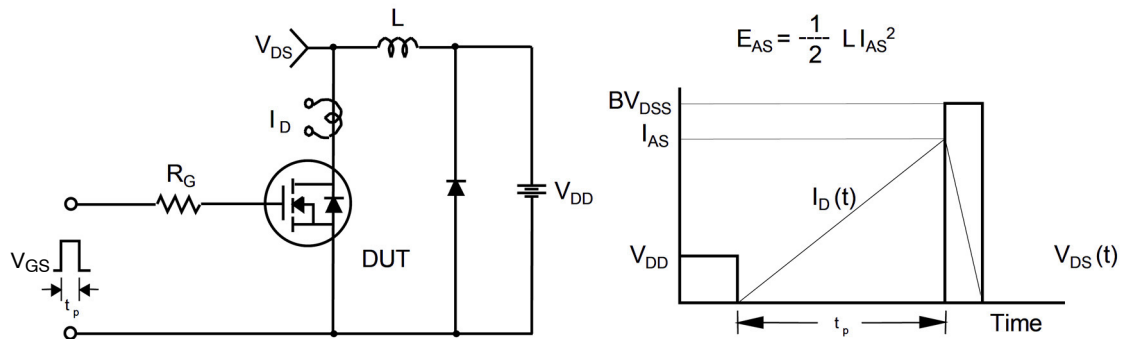


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

FDP075N15A, FDB075N15A

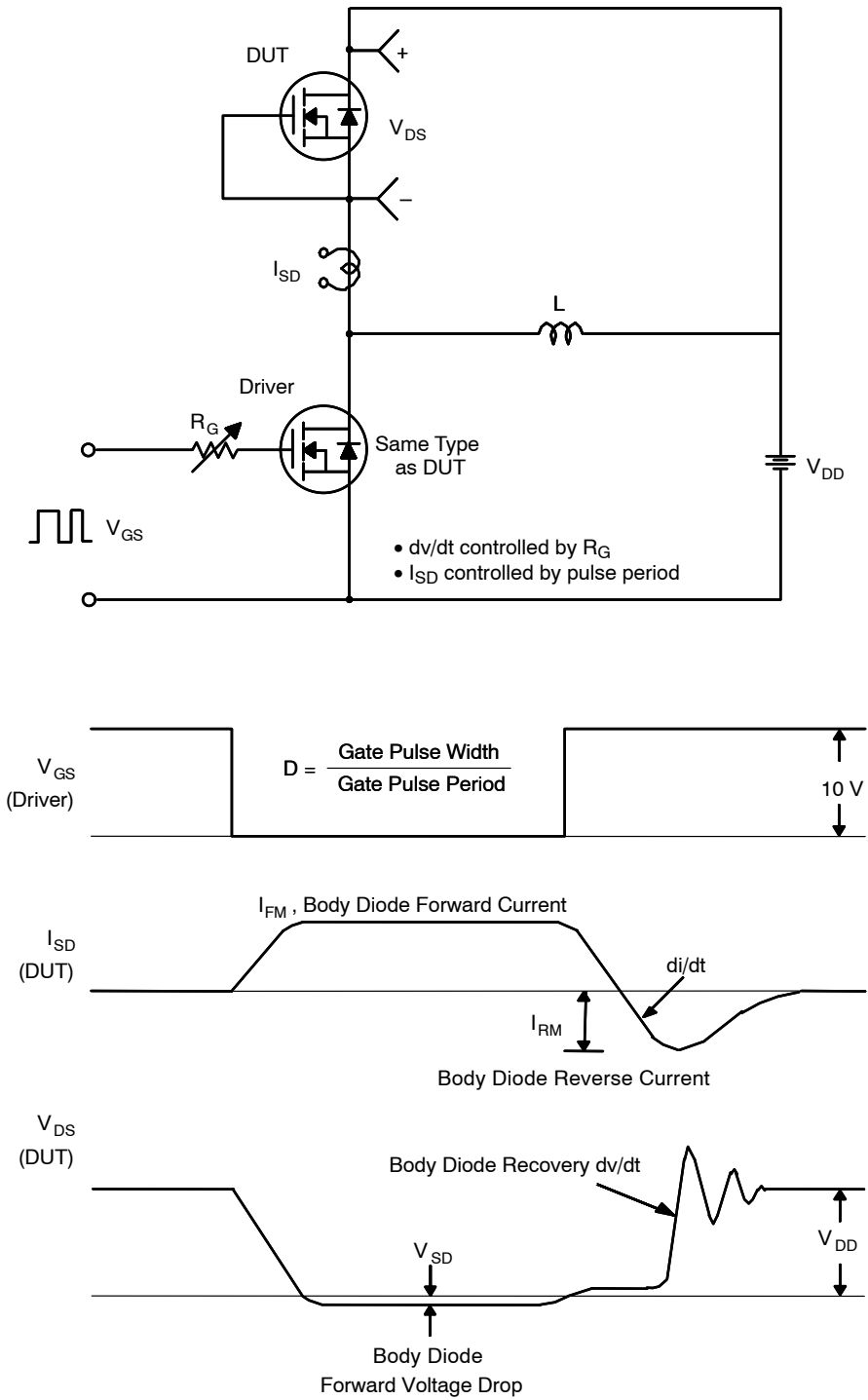


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FDP075N15A, FDB075N15A

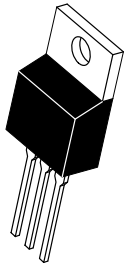
PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping†
FDP075N15A-F102	FDP075N15A	TO-220	N/A	N/A	50 units / Tube
FDB075N15A	FDB075N15A	D ² -PAK	330 mm	24 mm	800 units / Tape & Reel

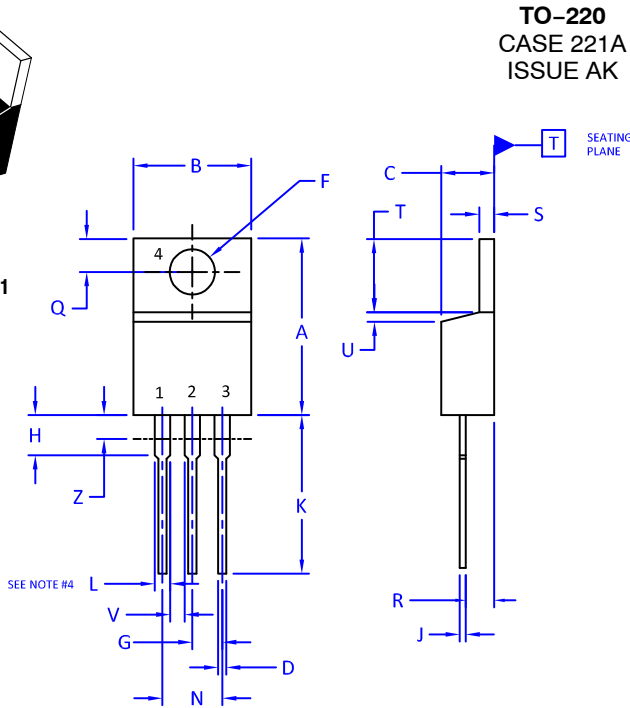
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

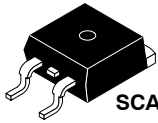
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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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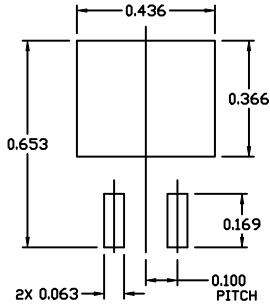
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D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

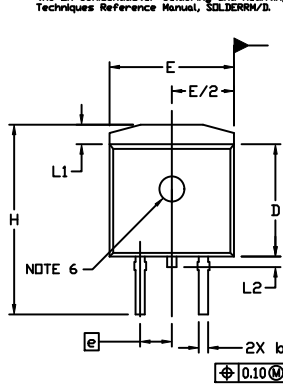
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

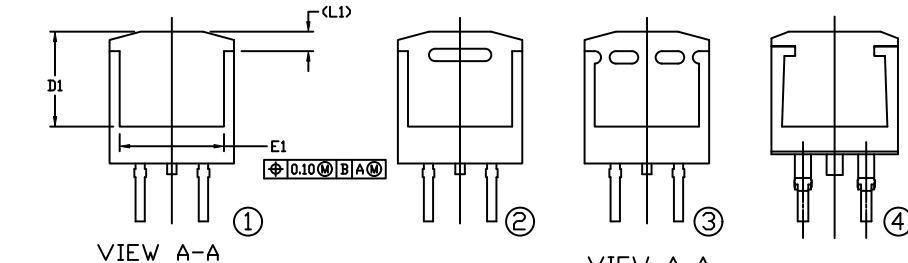
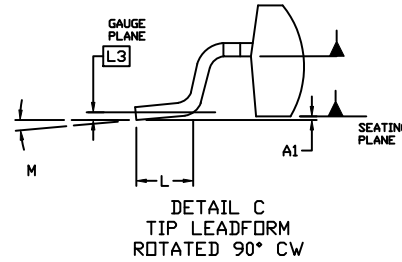
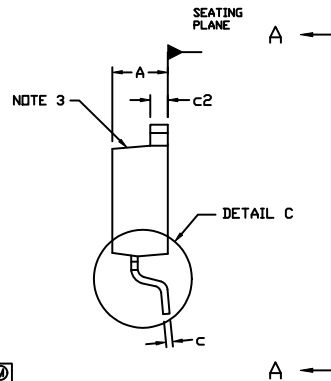
■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

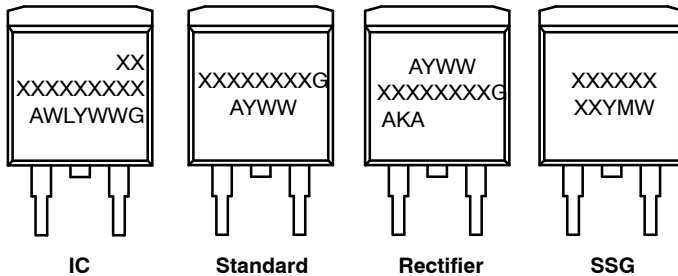
DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*



VIEW A-A

VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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