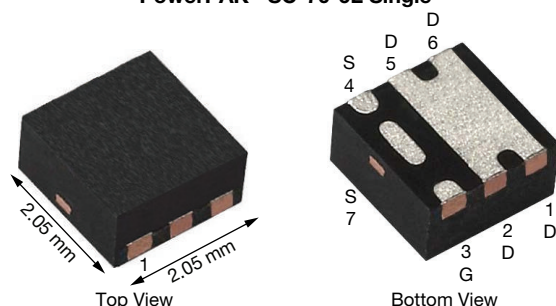


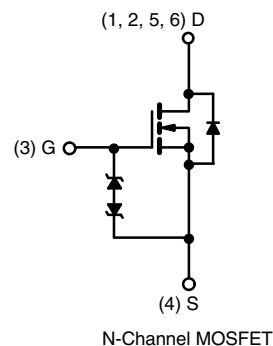
Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PowerPAK® SC-70-6L Single

Marking Code: QHXXXX

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5$ V	0.056
$R_{DS(on)}$ (Ω) at $V_{GS} = 2.5$ V	0.070
I_D (A)	2.25
Configuration	Single
Package	PowerPAK SC-70

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE


ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	30	V
Gate-source voltage		V_{GS}	± 12	
Continuous drain current ^a	$T_C = 25$ °C	I_D	2.25	A
	$T_C = 125$ °C		2.25	
Continuous source current (diode conduction) ^a		I_S	2.25	
Pulsed drain current ^a		I_{DM}	9	
Single pulse avalanche current	$L = 0.1$ mH	I_{AS}	9	mJ
		E_{AS}	4	
Maximum power dissipation ^b	$T_C = 25$ °C	P_D	13.6	W
	$T_C = 125$ °C		4.5	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount ^c	R_{thJA}	90	°C/W
Junction-to-case (drain)		R_{thJC}	11	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

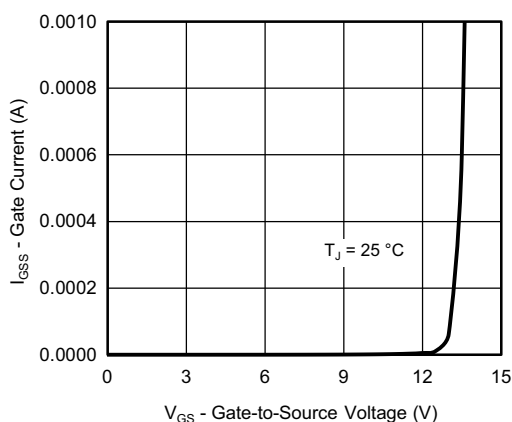
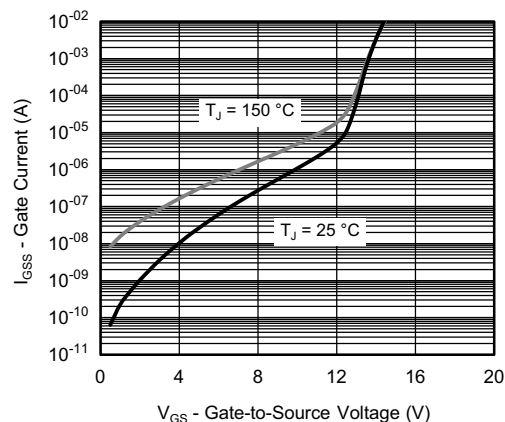
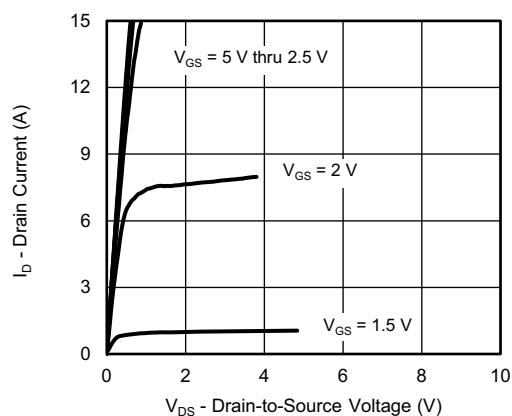
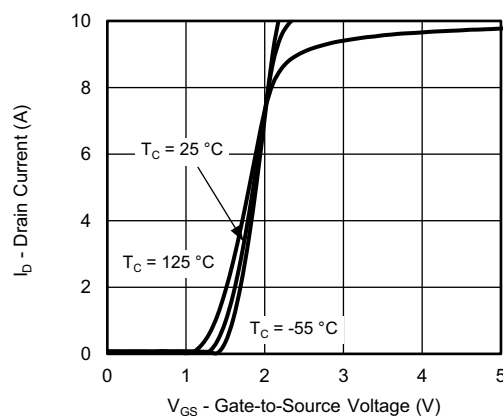
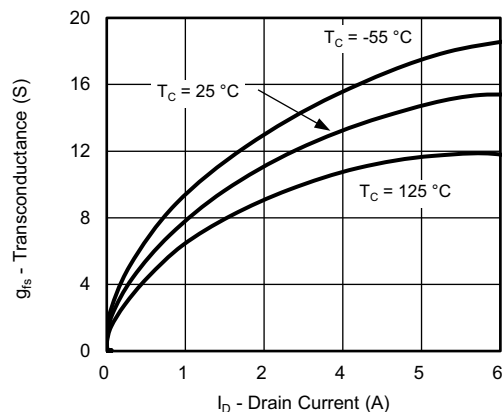
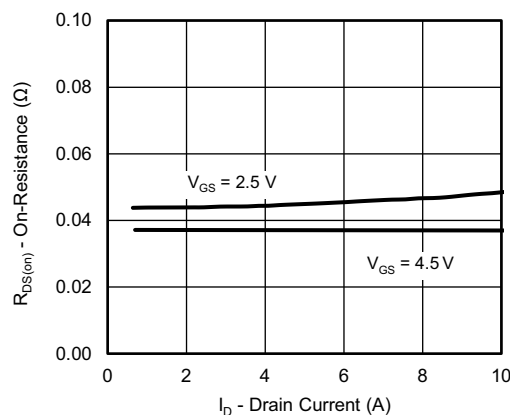


SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		0.6	1	1.6	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 3 V		-	-	± 100	nA
		V _{DS} = 0 V, V _{GS} = ± 12 V		-	-	± 15	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 30 V	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V	V _{DS} = 30 V, T _J = 175 °C	-	-	250	
On-state drain current ^a	I _{D(on)}	V _{GS} = 4.5 V	V _{DS} ≥ 5 V	10	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V	I _D = 2 A	-	0.038	0.056	Ω
		V _{GS} = 4.5 V	I _D = 2 A, T _J = 125 °C	-	-	0.084	
		V _{GS} = 4.5 V	I _D = 2 A, T _J = 175 °C	-	-	0.099	
		V _{GS} = 2.5 V	I _D = 2 A	-	0.044	0.070	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3 A		-	13	-	S
Dynamic ^b							
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 20 V, f = 1 MHz	-	362	453	pF
Output capacitance	C _{oss}			-	66	83	
Reverse transfer capacitance	C _{rss}			-	38	48	
Total gate charge ^c	Q _g	V _{GS} = 4.5 V	V _{DS} = 15 V, I _D = 4.2 A	-	4.1	5.2	nC
Gate-source charge ^c	Q _{gs}			-	0.58	-	
Gate-drain charge ^c	Q _{gd}			-	1.1	-	
Gate resistance	R _g	f = 1 MHz		1.9	3.2	5.1	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω		-	8.2	10.3	ns
Rise time ^c	t _r			-	22	28	
Turn-off delay time ^c	t _{d(off)}			-	21	26	
Fall time ^c	t _f			-	26	32	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}			-	-	9	A
Forward voltage	V _{SD}	I _F = 4.5 A, V _{GS} = 0 V		-	0.75	1.2	V

Notes

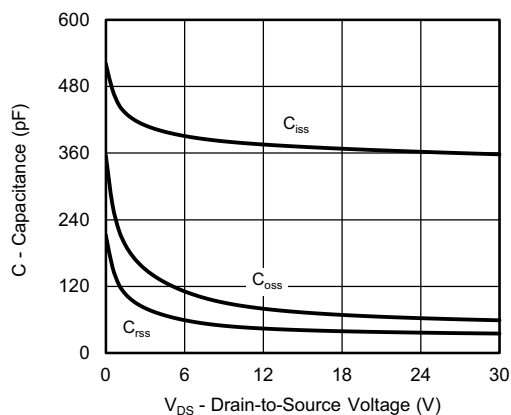
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

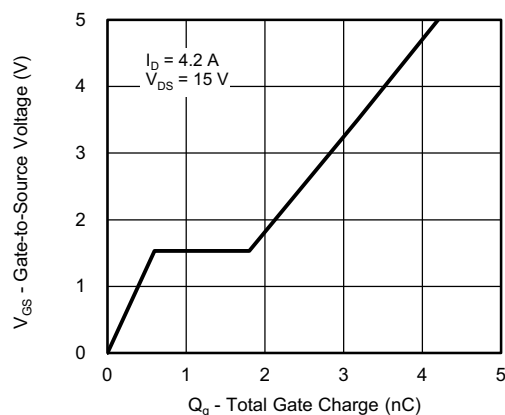
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current



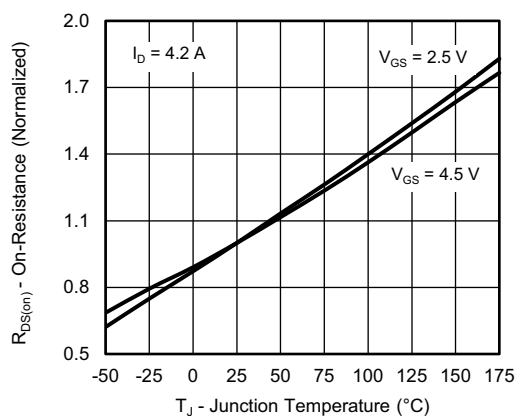
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



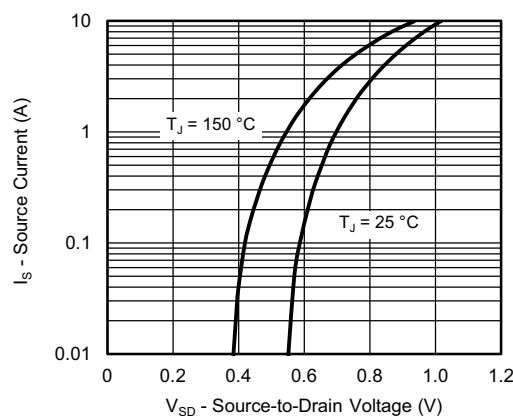
Capacitance



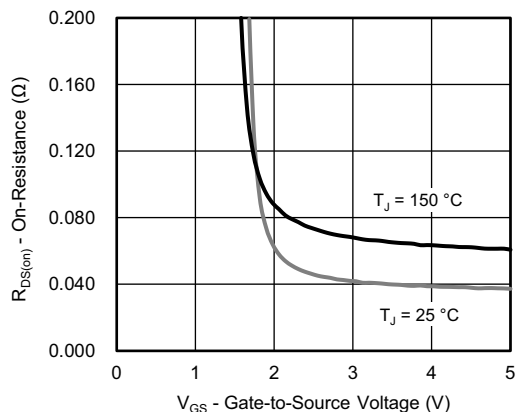
Gate Charge



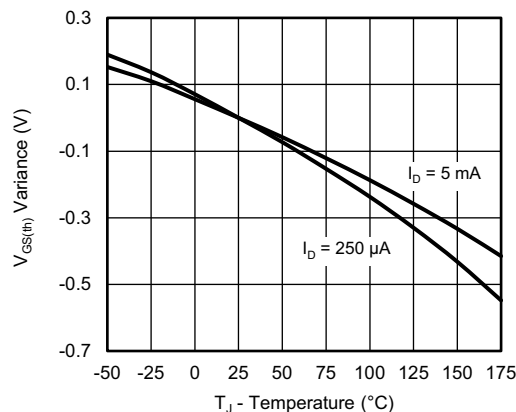
On-Resistance vs. Junction Temperature



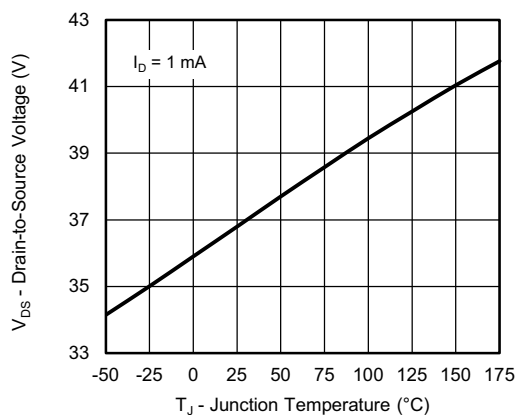
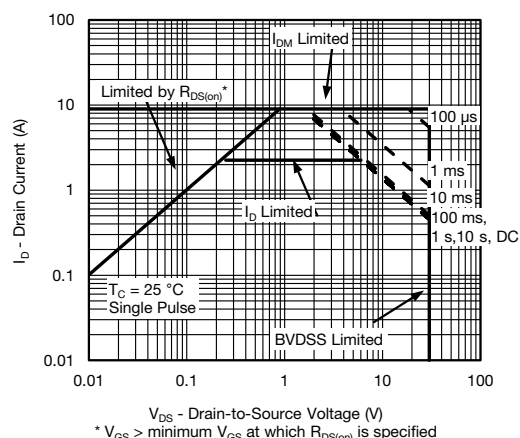
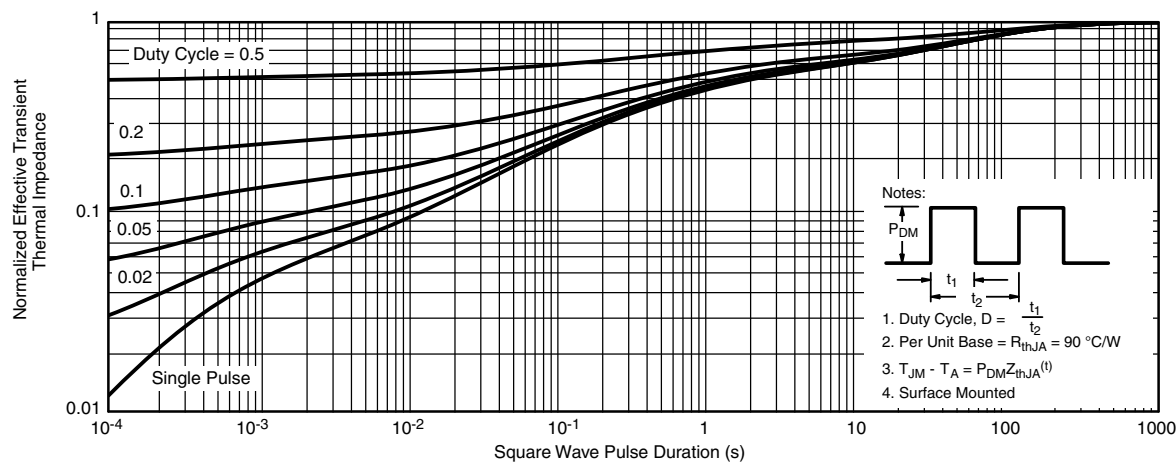
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

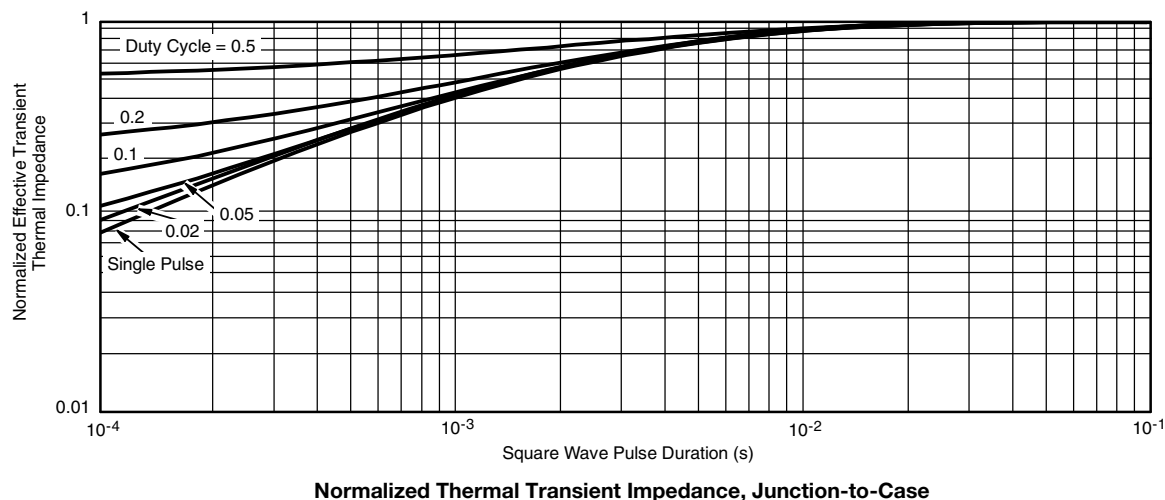


Threshold Voltage

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area
THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76236.



PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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