OPTIREG™ linear voltage regulator TLS820F3ELVxx demoboard

Z8F68163446

Family overview

Support

Preface

Scope and purpose

This document describes the usage of the OPTIREG™ linear voltage regulator TLS820F3ELVxx demoboard for the TLS820F3ELV33 and TLS820F3ELV50 from Infineon Technologies AG. Please also refer to the corresponding datasheets.

Intended audience

This document is intended for engineers who develop applications.

Table of contents

1 Introduction

1.1 General description

The TLS820F3ELV33 and TLS820F3ELV50 are monolithic integrated low drop out voltage regulators for loads up to 200 mA in a PG-SSOP-14 package. With an input voltage range of 3 V to 42 V and very low quiescent current of only 26 µA, these devices are perfectly suitable for automotive or other supply systems connected to the battery permanently. Both variants provide an output voltage accuracy of ±2%.

The loop concept combines fast regulation and very good stability while requiring only one small ceramic capacitor of 1 µF at the output. The operating range starts already at an input voltage of only 3 V (extended operating range). This makes the devices also suitable to supply automotive systems that need to operate during cranking condition.

Additional features include:

- switching the device on and off via enable
- reset circuit to supervise the output voltage and delay the reset at power-on with an adjustable lower reset threshold
- watchdog circuit to monitor a microcontroller
- shared external delay capacitor to set both reset timing and watchdog timing
- output current limitation
- thermal shutdown

1.2 TLS820F3ELV33 and TLS820F3ELV50 features

- Output voltage 5 V and 3.3 V ±2%
- Current capability 200 mA
- Input voltage range from 3 V to 42 V
- Stable with 1 µF ceramic output capacitor
- Ultra low current consumption: typically 26 µA
- Very low drop out voltage: typically 100 mV at 100 mA
- Watchdog circuit for monitoring a microprocessor
- Watchdog inhibit
- Reset circuit supervises the output voltage
  - Programmable undervoltage reset threshold: minimum 2.5 V
  - Programmable delay time
- Separate outputs for reset and watchdog
- Enable
- Output current limitation
- Overtemperature shutdown
- Automotive temperature range T_j = -40°C to 150°C
- Green Product (RoHS compliant)

1.3 Block diagram

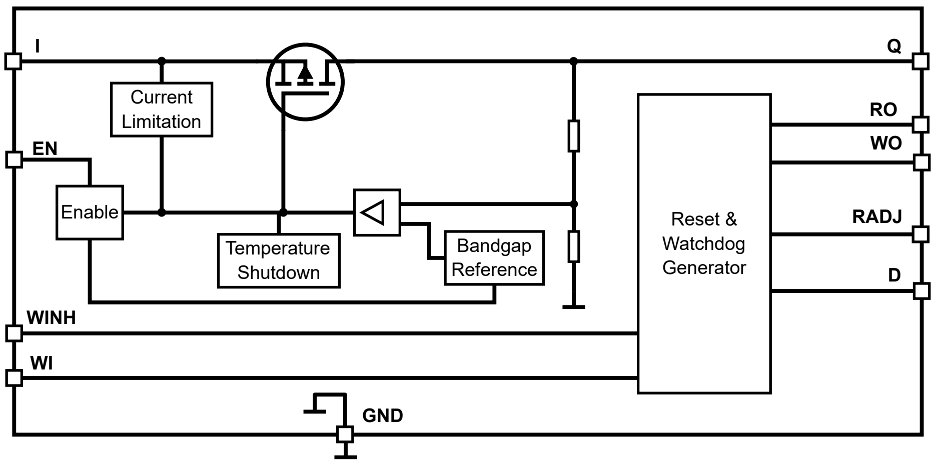

Figure 1 Block diagram TLS820F3ELVxx

2 Demoboard

2.1 Assembly

There are two different demoboard assemblies available. One for the TLS820F3ELV33 and one for the TLS820F3ELV50. They differ only by the resistor divider values on the RADJ pin, see Table 2.

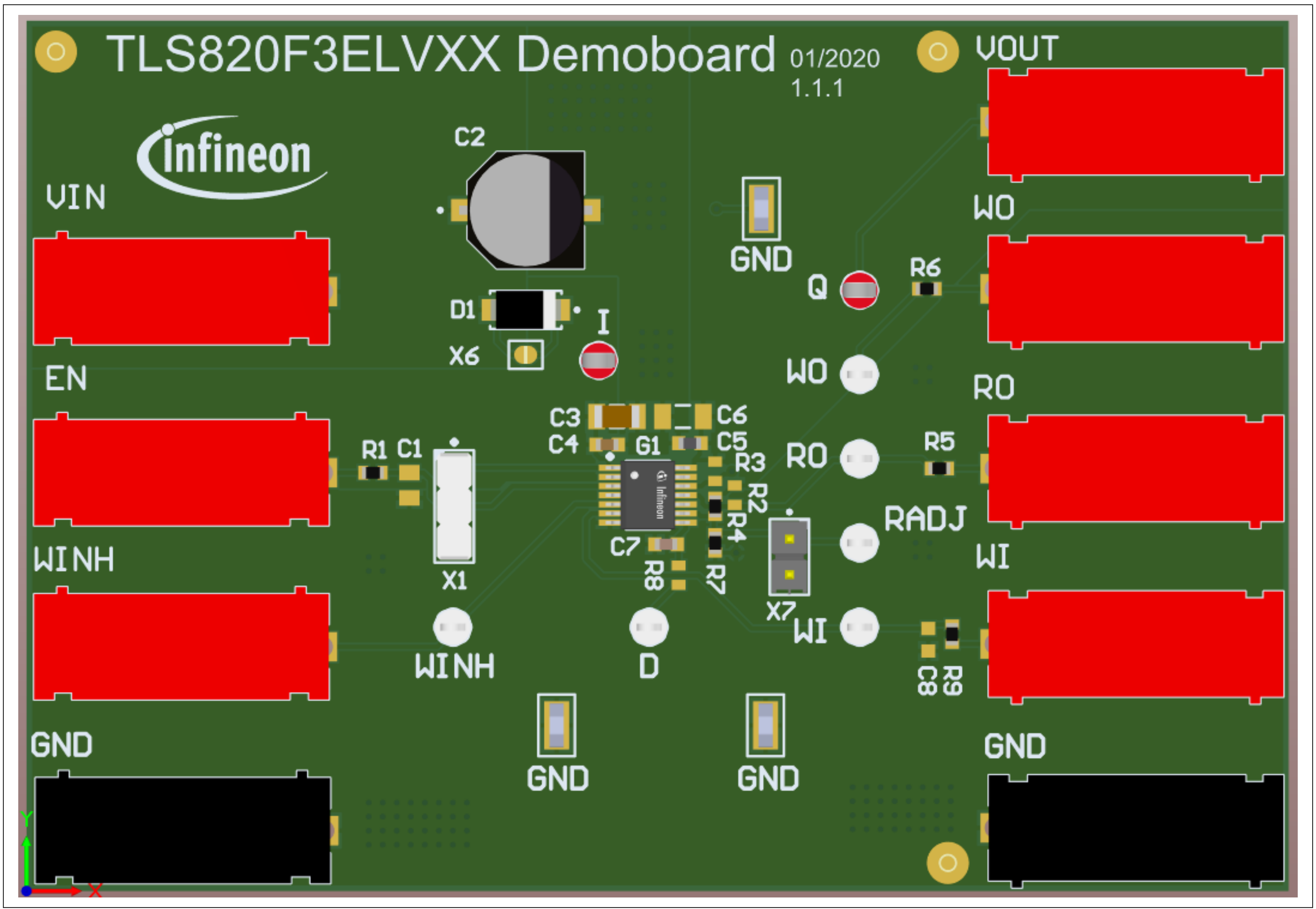

Figure 2 **Assembly TLS820F3ELVxx demoboard**

2.2 Operating conditions

To avoid electrical damage of the demoboard, the values in Table 1 must be maintained.

Table 1 Limit values for operation[1)]

Parameter	Symbol[2)]	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Board supply voltage	V_{IN}	0	–	42	V	–
Output voltage	V_{Q}	-0.3	–	7	V	[3)]
Output current	I_{Q}	0	–	200	mA	Limited by overcurrent protection
Enable	V_{EN}	0	–	42	V	[3)]
Watchdog inhibit	V_{WINH}	-0.3	–	7	V	[3)]
Watchdog output	V_{WO}	-0.3	–	7	V	[3)]
Watchdog input	V_{WI}	-0.3	–	7	V	[3)]
Reset output	V_{RO}	-0.3	–	7	V	[3)]
Ground voltage	V_{GND}	0	–	0	V	–

1) T_A = 25°C.
2) Symbols refer to the connectors of the demoboard.
3) Absolute maximum rating.

2.3 Configuration

The demoboard can be easily configured via jumpers on the board.

The demoboard provides the following configuration options:

- connect the enable signal EN to VIN or to GND with a jumper
- connect the RADJ pin to GND with a jumper to select the default reset thresholds

2.3.1 EN selection

The EN pin can be connected to either GND or to VIN by placing a jumper as shown in Figure 3. The EN pin is always connected to the external banana-plug. If the jumper is placed, then do not connect an external signal to EN.

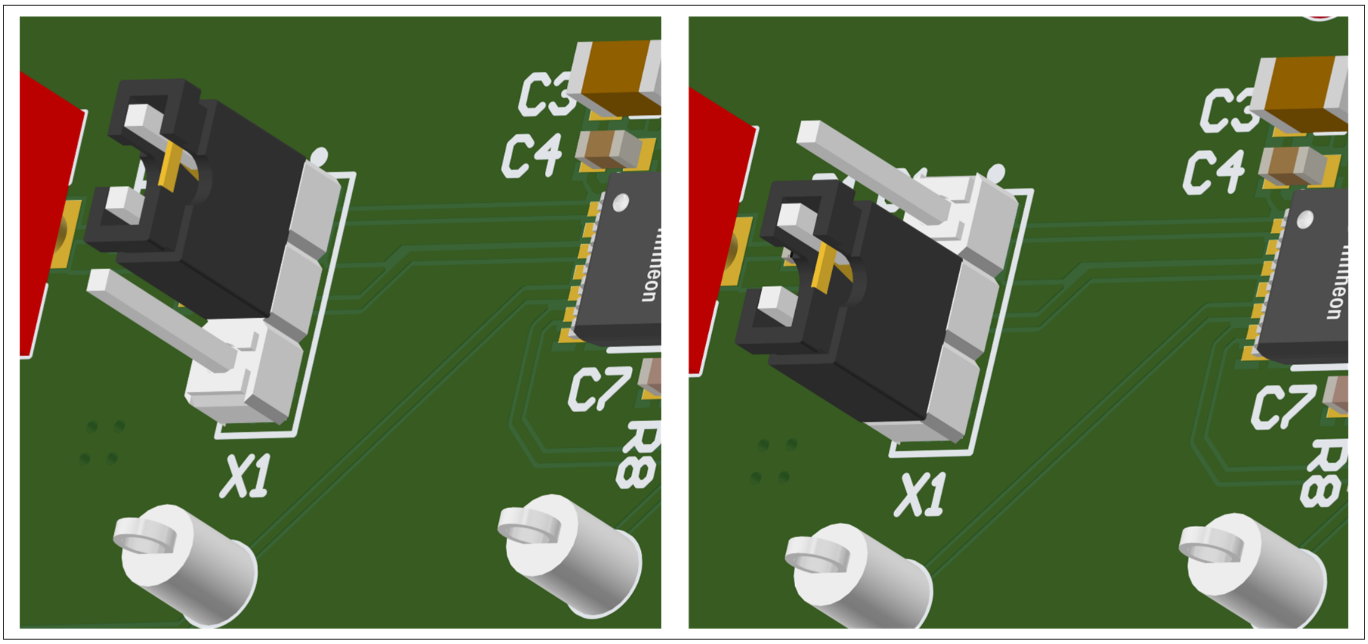

Figure 3 EN jumper (left: EN to VIN; right: EN to GND)

2.3.2 RADJ selection

The TLS820F3ELVxx demoboard features adjustable reset thresholds by applying a voltage divider between the Q pin and the RADJ-pin. The demoboard resistors R4 and R7 set the reset adjust threshold, see Figure 4. There are two different assemblies of these resistors, one for the TLS820F3ELV33 and one for the TLS820F3ELV50, see Table 2. The formula for calculating the reset threshold is given in Equation 1. Placing the jumper as shown in Figure 5 connects the RADJ to GND and sets the default reset thresholds as shown in the datasheet. The jumper shorts resistor R7 and causes a small permanent current through R4.

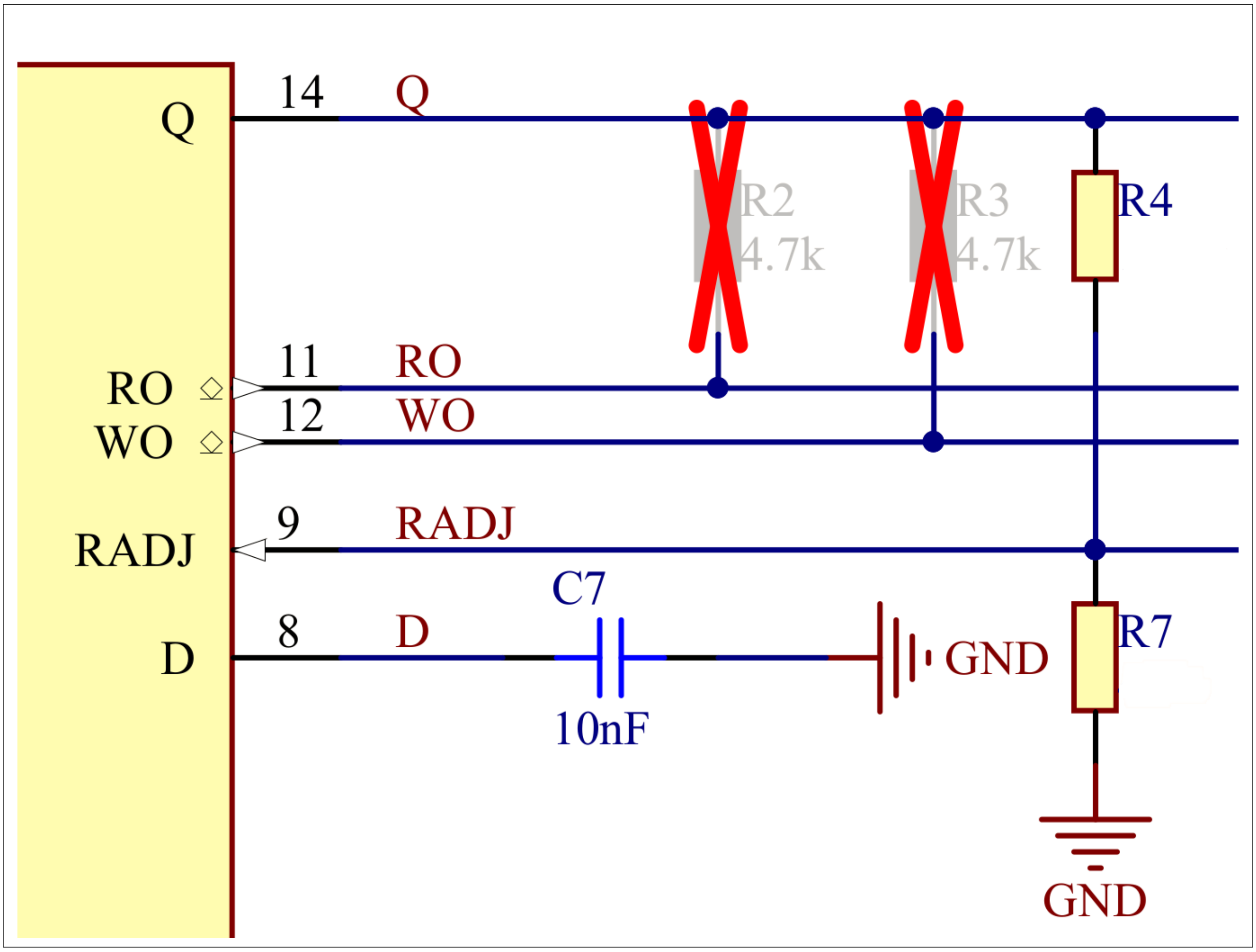

Figure 4 **RADJ resistor divider schematic**

Table 2 **RADJ resistor divider assembly**

Variant	R4	R7	$V_{RT,lo}$
TLS820F3ELV33	9.4 kΩ	4.7 kΩ	2.7 V
TLS820F3ELV50	16.2 kΩ	4.7 kΩ	4 V

$$V_{\mathrm{RT,lo}} = V_{\mathrm{RADJ,th}} \times \frac{R_4 + R_7}{R_7} \approx 0.9 \times \frac{R_4 + R_7}{R_7}$$

Equation 1 **$V_{RT,lo}$ calculation**

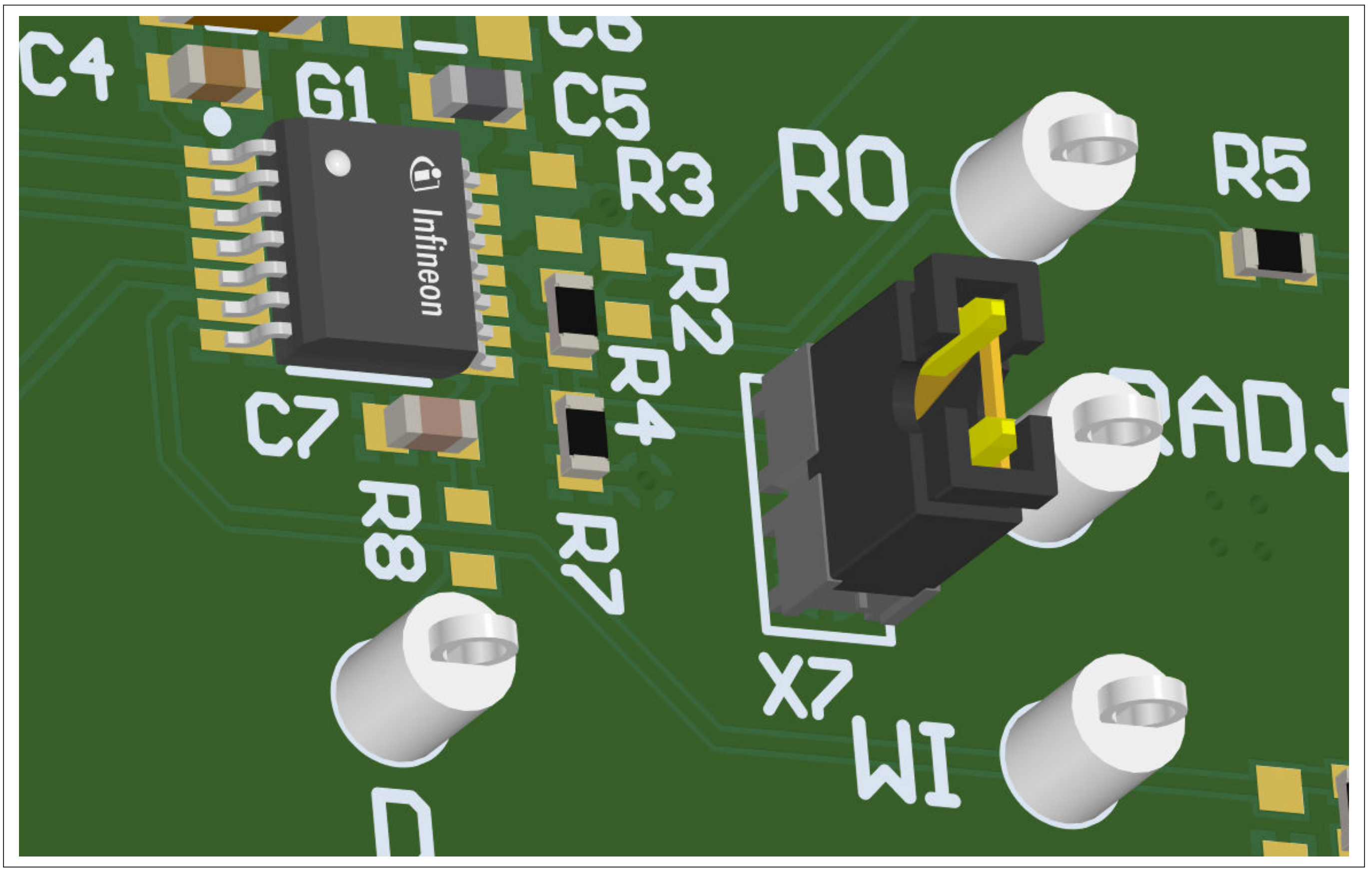

Figure 5 RADJ jumper

2.3.3 Signal adaption

For easy signal adaption, for example connecting probes of an oscilloscope, test points are scattered across the PCB. The label of each test point indicates the probed signal. For further information on the mapping between test points and signals see Figure 7. The GND clip of the probe can be attached to one of several ground hooks as shown in Figure 6.

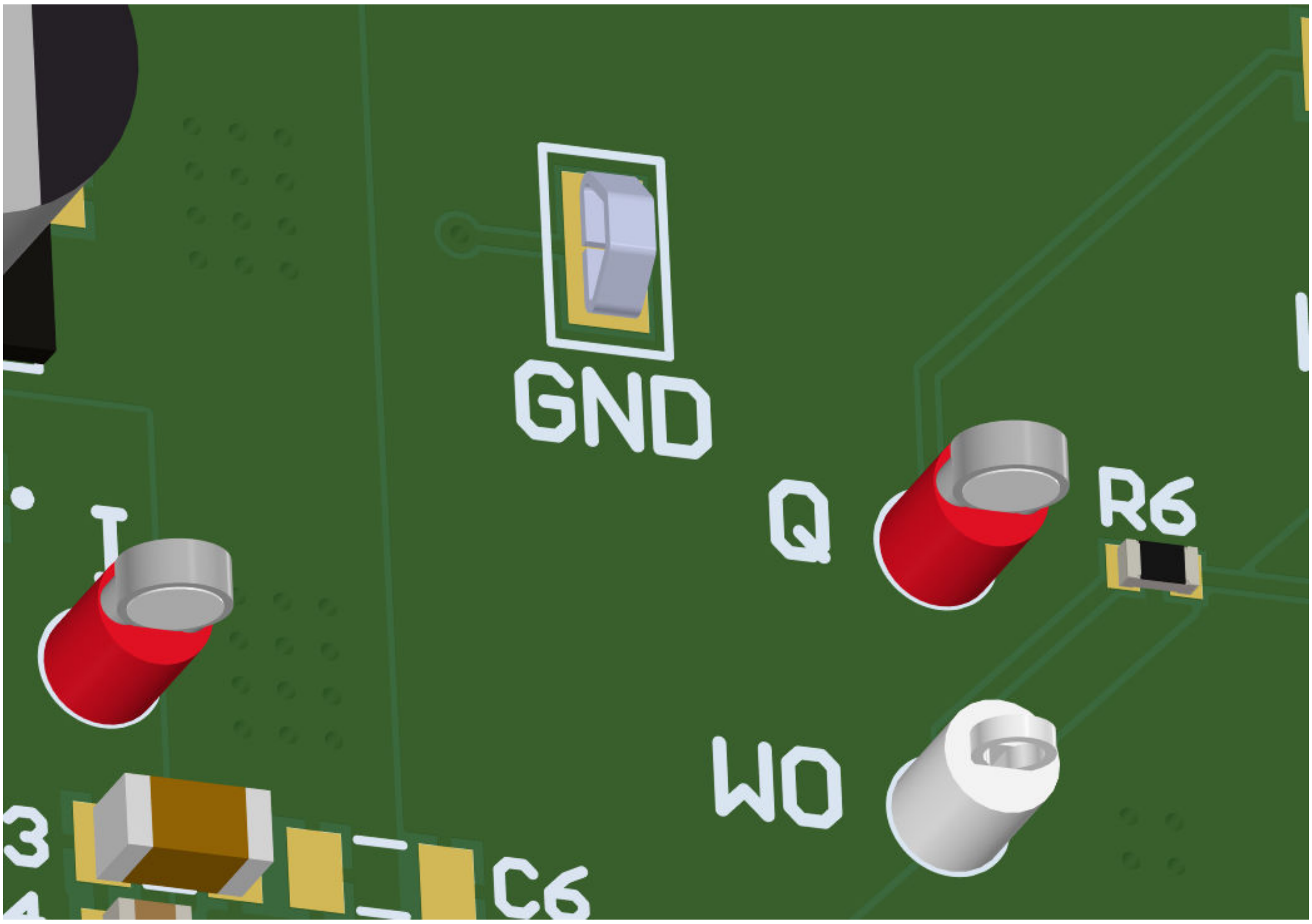

Figure 6 Testpoint and GND hook example

2.4 Connectors

Table 3 Connectors and device pin mapping

Label	PIN	Function
VIN	I	Regulator input
EN	EN	Enable input: "High" enables the IC. "Low" disables the IC. This pin has an integrated pull-down resistor.
WINH	WINH	Watchdog inhibit input: "Low" activates the watchdog function. "High" deactivates the watchdog function. This pin has an integrated pull-down resistor.
VOUT	Q	Regulator output
WO	WO	Watchdog output: This pin has an integrated pull-up resistor to Q. It is an open collector output. If the watchdog function is not needed, then leave this pin open.
RO	RO	Reset output: This pin has an integrated pull-up resistor to Q. It is an open collector output. If the reset function is not needed, then leave this pin open.
WI	WI	Watchdog input: Serve watchdog with trigger input signal. This pin has an integrated pull-down resistor.
GND_VOUT, GND_VIN	GND	Ground

3 Schematic and layout

3.1 Schematic

The schematic in Figure 7 is assembled with two different configurations for the resistors R4 and R7, depending on whether the TLS820F3ELV33 or TLS820F3ELV50 is mounted, see Table 2 for details. Not mounted parts are optional and marked with a red cross.

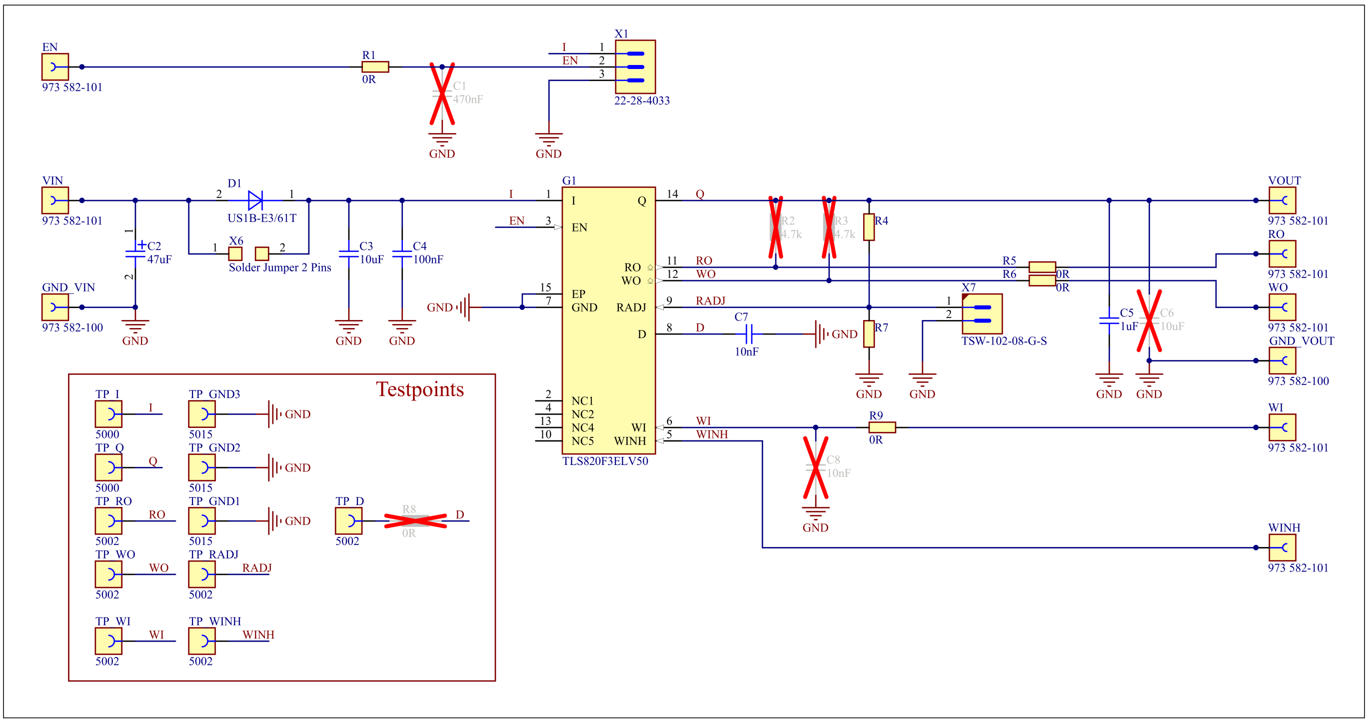

Figure 7 Schematic TLS820F3ELVxx demoboard

3.2 Layout

The PCB uses a four layer standard stack-up. The product can also be soldered to double layer boards. However, four layers offer better thermal characteristics. The configuration on this demoboard is comparable to the 2s2p thermal interface situation.

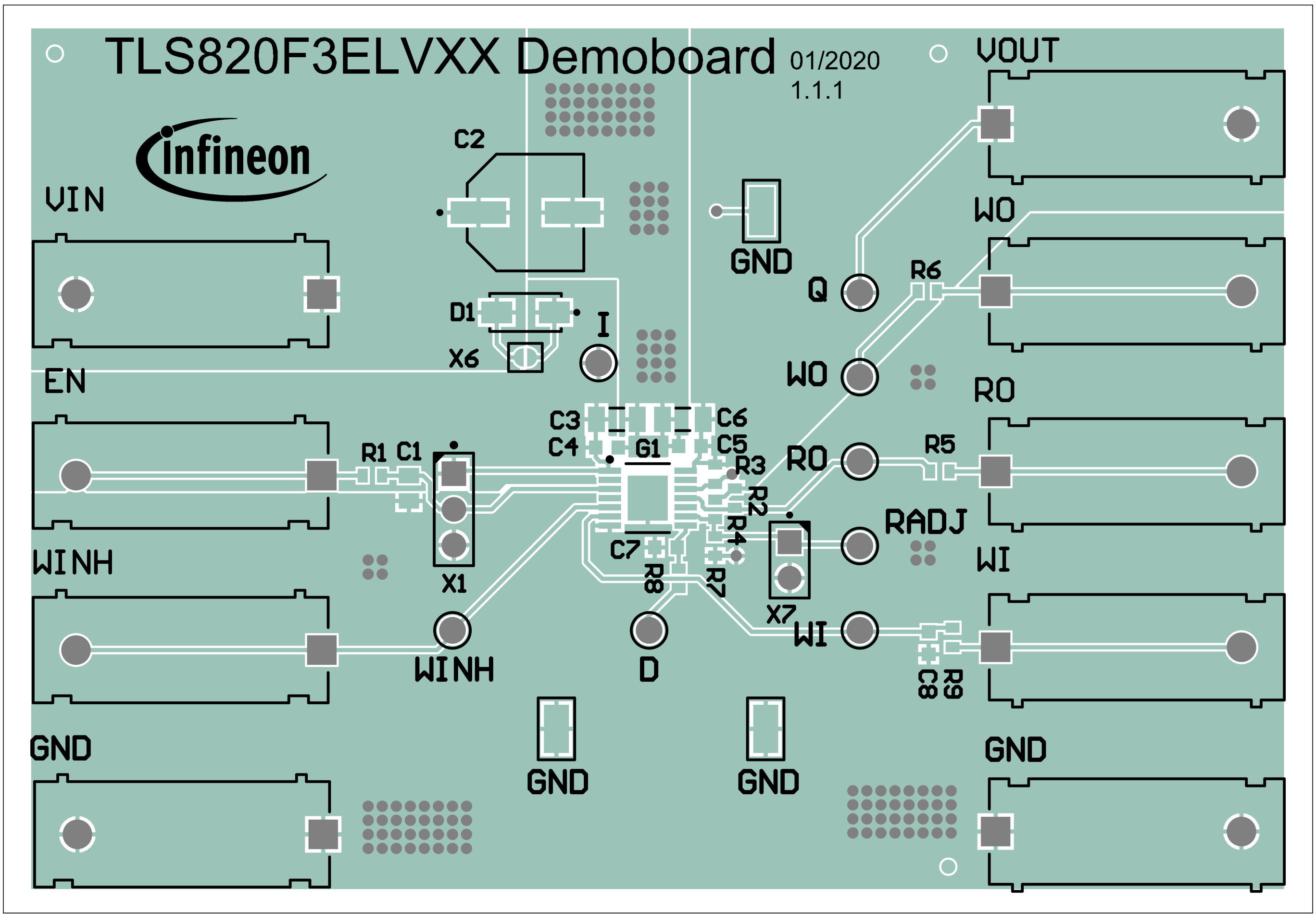

Figure 8 **Top layer and components TLS820F3ELVxx demoboard**

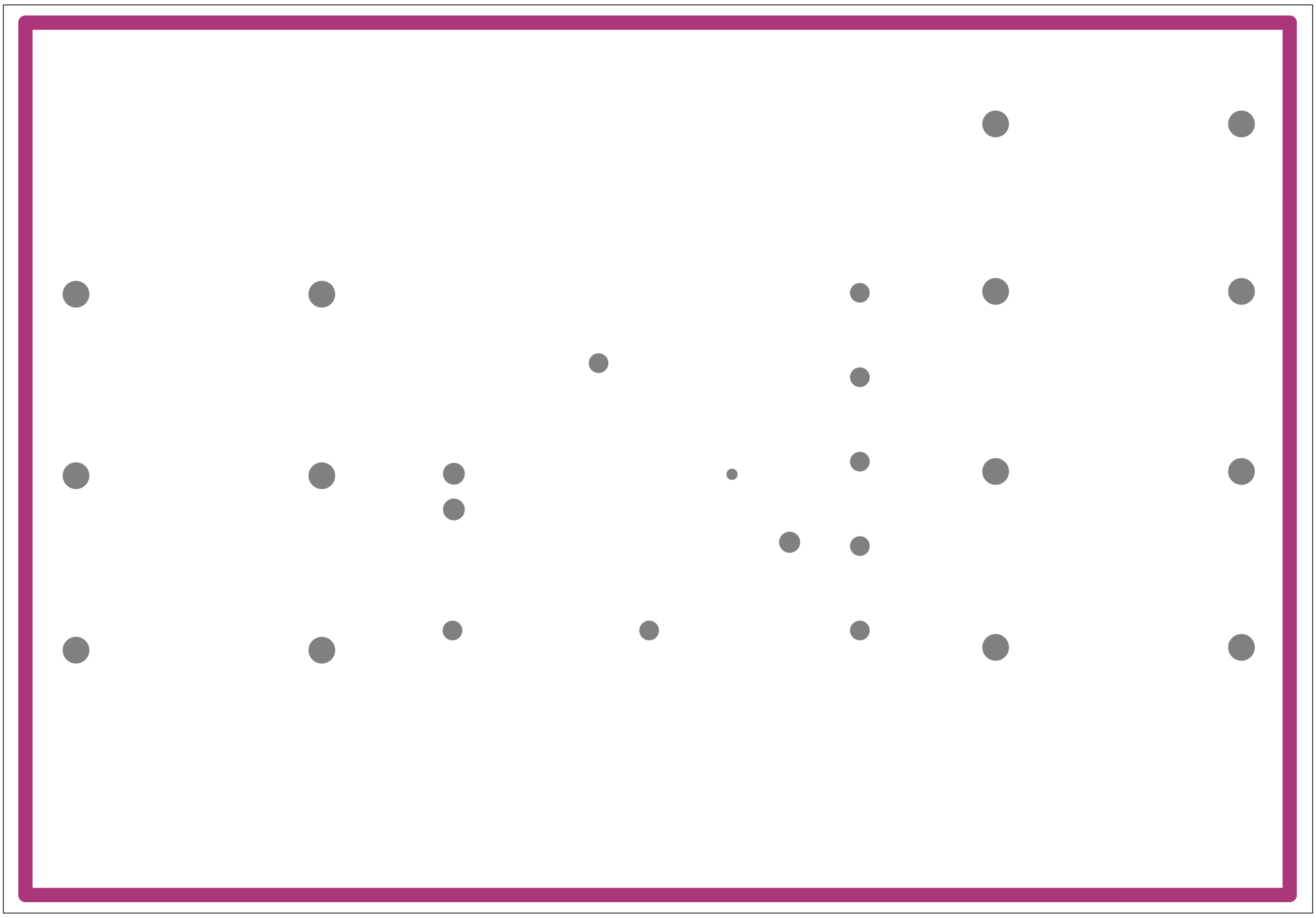

Figure 9 **Internal layer 1 TLS820F3ELVxx demoboard**

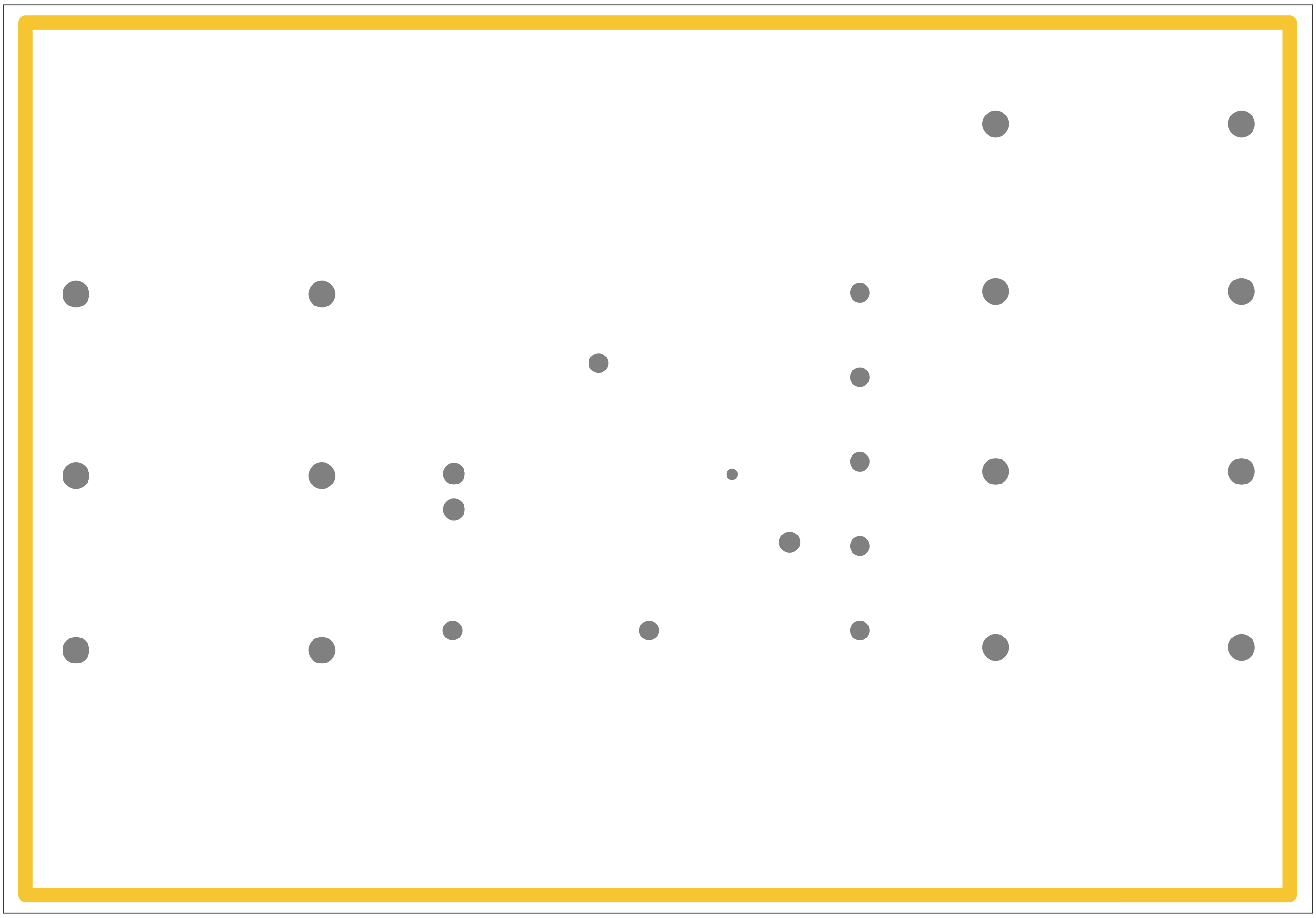

Figure 10 **Internal layer 2 TLS820F3ELVxx demoboard**

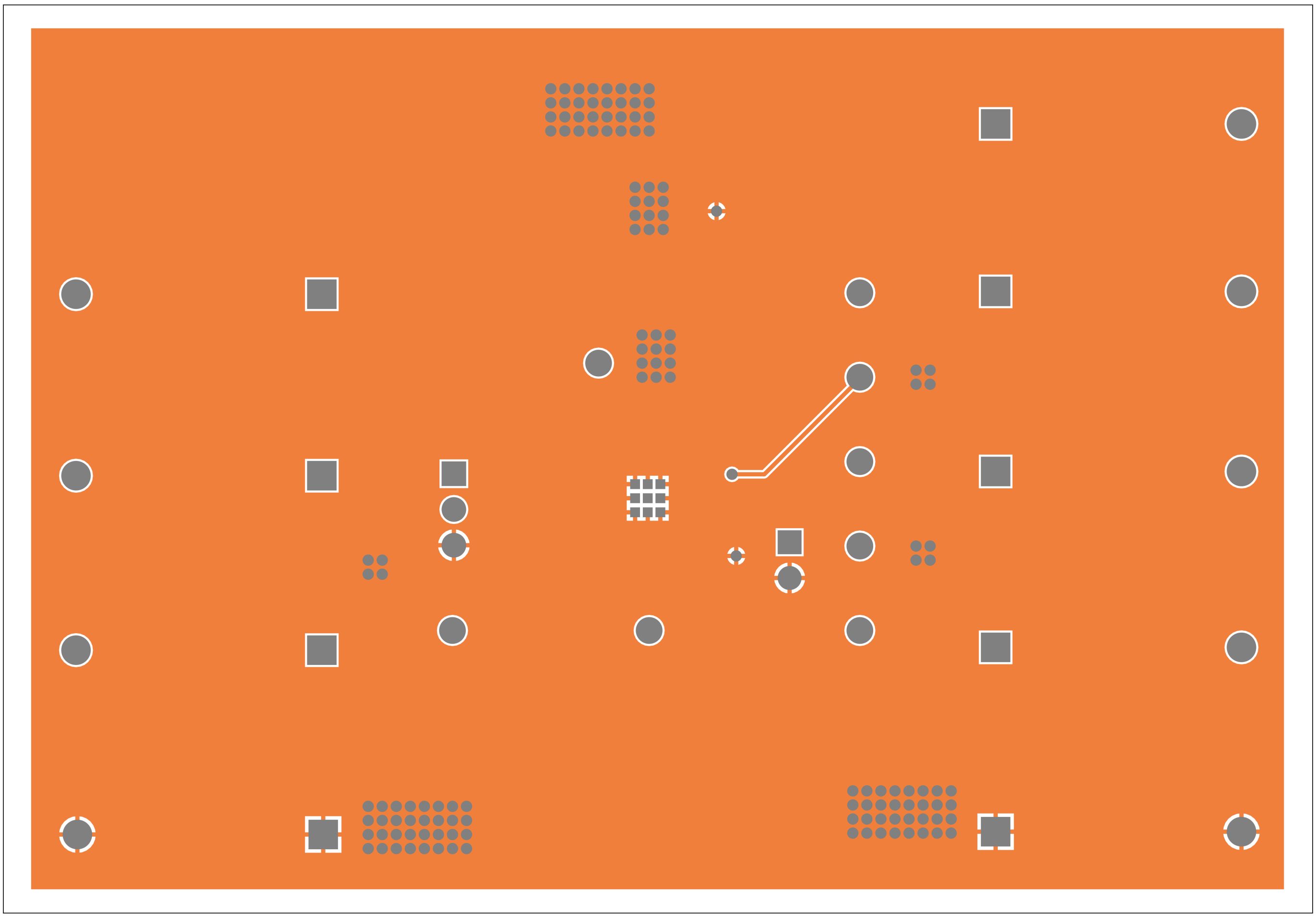

Figure 11 **Bottom layer TLS820F3ELVxx demoboard**

4 Bill of materials

The bill of materials shows the components on the TLS820F3ELVxx demoboard. For the mounting condition of each component see Figure 7 and Figure 8. Mechanical parts, such as connectors or test-points are not mentioned. Table 2 shows the configuration for resistors R4 and R7.

Table 4 Bill of materials TLS820F3ELVxx demoboard

Part	Value	Package
D1	US1B-E3/61T	DO-214
C2	47 µF / 50 V	n.a.
C3	10 µF / 50 V	1206
C4	100 nF / 50 V	0603
C5	1 µF / 16 V	0603
C7	10 nF / 50 V	0603
R1, R5, R6, R9	0 Ω	0603

5 Restrictions

This demoboard offers limited features only for evaluation and testing of Infineon products. The demoboard is not an end product or finished appliance, nor is it intended or authorized by Infineon to be integrated into end products. The demoboard may not be used in any production system.

For further information please visit www.infineon.com.

6 Revision history

Revision	Date	Changes
1.02	2024-05-08	Document updated • Additional connector details • Editorial changes
1.01	2022-12-01	Document updated • Editorial changes
1.0	2020-02-26	Document created.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-05-08

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-xju1645616949554 Z8F68163446