MP4865A

64-Channel, High-Voltage Analog Switch with Output Bleed Resistors and 5V Bias

DESCRIPTION

The MP4865A is a 64-channel, high-voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors. The device can multiplex the transmit and receive voltages to and from multiple piezoelectric transducers (PZTs), and is designed for medical ultrasound imaging applications

The output switches are controlled by a 64-bit serial shift register, followed by a 64-bit data latch. The data out pin (DOUT) allows for multiple devices to be cascaded together. This helps to minimize the number of input/output (I/O) control lines. When the data latch is logic high, the corresponding analog switch turns on; when the data latch is low, the corresponding switch turns off.

The MP4865A does not require any high-voltage supplies. It only requires two low-voltage supplies (3.3V and 5V). The analog switch can block or pass analog voltages up to ±90V with peak currents up to ±1.8A.

The MP4865A is available in a BGA-144 (10mmx10mm) package.

FEATURES

- No High-Voltage Supplies Required
- 64 Channels
- Up to ±90V Analog Signals
- 14Ω Typical Switch Resistance
- ±1.8A Typical Switch Peak Current
- Off-Isolation of -66dB at 5MHz
- Integrated Output Bleed Resistor
- 60MHz Clock Frequency
- 5V Bias
- Available in a BGA-144 (10mmx10mm) Package

APPLICATIONS

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT)

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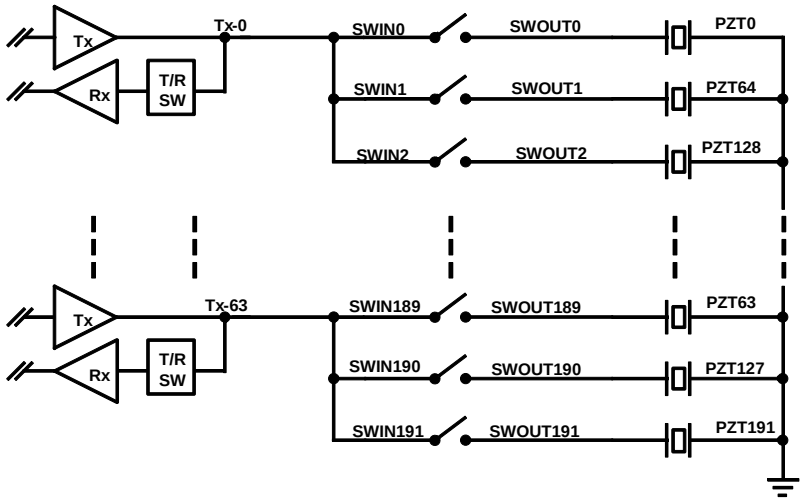
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4865AGBD	BGA-144 (10mmx10mm)	*See Below*	3

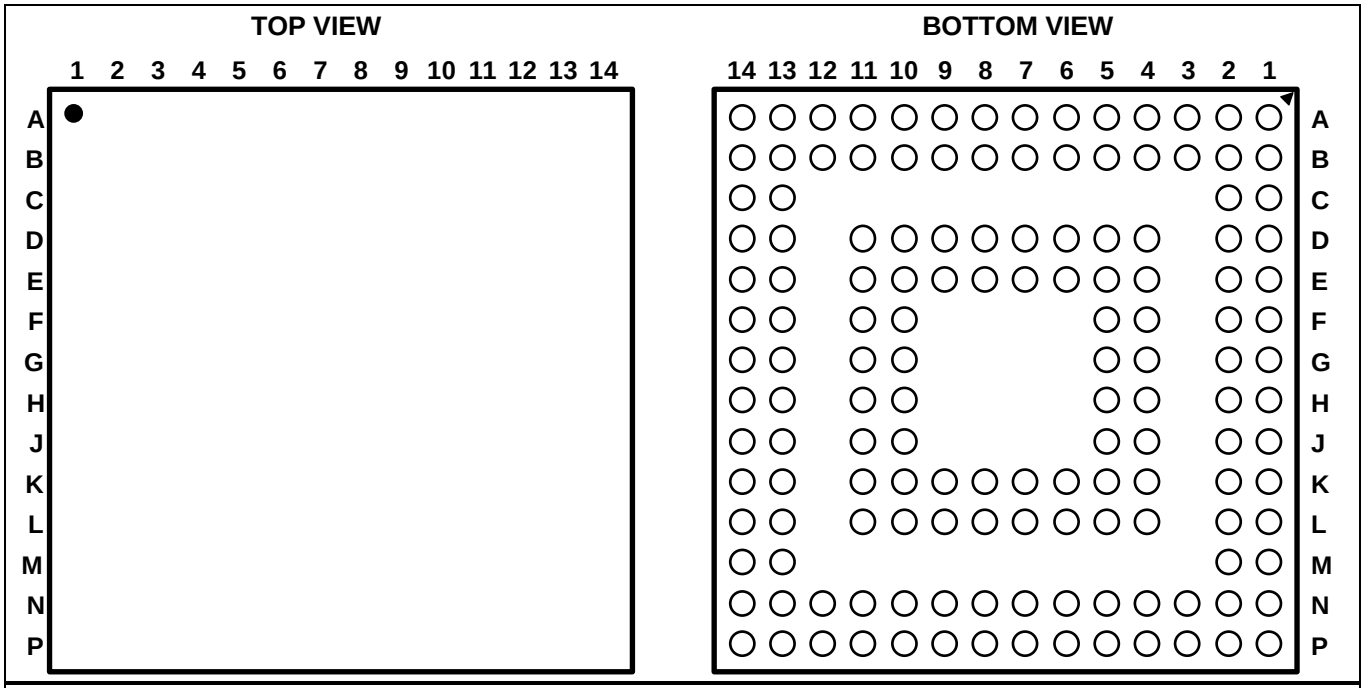
* For Tray, add suffix -T (e.g. MP4865AGBD-T).

TOP MARKING

MPSYYWW
MP4865A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4865A: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



BGA-144 (10mmx10mm)

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PIN FUNCTIONS

Pin #	Name	Description
A1	GND	**Device ground.**
A2	SWIN3	**Analog switch input 3.** Connect SWIN3 to the high-voltage pulse/transmitter.
A3	SWOUT3	**Analog switch output 3.** Connect SWOUT3 to the piezoelectric transducer.
A4	SWIN5	**Analog switch input 5.** Connect SWIN5 to the high-voltage pulse/transmitter.
A5	SWOUT5	**Analog switch output 5.** Connect SWOUT5 to the piezoelectric transducer.
A6	SWIN6	**Analog switch input 6.** Connect SWIN6 to the high-voltage pulse/transmitter.
A7	SWOUT6	**Analog switch output 6.** Connect SWOUT6 to the piezoelectric transducer.
A8	SWIN8	**Analog switch input 8.** Connect SWIN8 to the high-voltage pulse/transmitter.
A9	SWOUT8	**Analog switch output 8.** Connect SWOUT8 to the piezoelectric transducer.
A10	SWIN9	**Analog switch input 9.** Connect SWIN9 to the high-voltage pulse/transmitter.
A11	SWOUT9	**Analog switch output 9.** Connect SWOUT9 to the piezoelectric transducer.
A12	SWIN11	**Analog switch input 11.** Connect SWIN11 to the high-voltage pulse/transmitter.
A13	SWOUT11	**Analog switch output 11.** Connect SWOUT11 to the piezoelectric transducer.
A14	GND	**Device ground.**
B1	SWOUT1	**Analog switch output 1.** Connect SWOUT1 to the piezoelectric transducer.
B2	SWIN4	**Analog switch input 4.** Connect SWIN4 to the high-voltage pulse/transmitter.
B3	SWOUT4	**Analog switch output 4.** Connect SWOUT4 to the piezoelectric transducer.
B4	SWIN35	**Analog switch input 35.** Connect SWIN35 to the high-voltage pulse/transmitter.
B5	SWOUT35	**Analog switch output 35.** Connect SWOUT35 to the piezoelectric transducer.
B6	SWIN7	**Analog switch input 7.** Connect SWIN7 to the high-voltage pulse/transmitter.
B7	SWOUT7	**Analog switch output 7.** Connect SWOUT7 to the piezoelectric transducer.
B8	SWIN40	**Analog switch input 40.** Connect SWIN40 to the high-voltage pulse/transmitter.
B9	SWOUT40	**Analog switch output 40.** Connect SWOUT40 to the piezoelectric transducer.
B10	SWIN10	**Analog switch input 10.** Connect SWIN10 to the high-voltage pulse/transmitter.
B11	SWOUT10	**Analog switch output 10.** Connect SWOUT10 to the piezoelectric transducer.
B12	SWIN43	**Analog switch input 43.** Connect SWIN43 to the high-voltage pulse/transmitter.
B13	SWOUT43	**Analog switch output 43.** Connect SWOUT43 to the piezoelectric transducer.
B14	SWIN12	**Analog switch input 12.** Connect SWIN12 to the high-voltage pulse/transmitter.
C1	SWIN1	**Analog switch input 1.** Connect SWIN1 to the high-voltage pulse/transmitter.
C2	SWOUT2	**Analog switch output 2.** Connect SWOUT2 to the piezoelectric transducer.
C13	SWIN14	**Analog switch input 14.** Connect SWIN14 to the high-voltage pulse/transmitter.
C14	SWOUT12	**Analog switch output 12.** Connect SWOUT12 to the piezoelectric transducer.
D1	SWOUT0	**Analog switch output 0.** Connect SWOUT0 to the piezoelectric transducer.
D2	SWIN2	**Analog switch input 2.** Connect SWIN2 to the high-voltage pulse/transmitter.
D4	SWIN36	**Analog switch input 36.** Connect SWIN36 to the high-voltage pulse/transmitter.
D5	SWOUT36	**Analog switch output 36.** Connect SWOUT36 to the piezoelectric transducer.
D6	SWIN38	**Analog switch input 38.** Connect SWIN38 to the high-voltage pulse/transmitter.
D7	SWOUT38	**Analog switch output 38.** Connect SWOUT38 to the piezoelectric transducer.
D8	SWIN41	**Analog switch input 41.** Connect SWIN41 to the high-voltage pulse/transmitter.
D9	SWOUT41	**Analog switch output 41.** Connect SWOUT41 to the piezoelectric transducer.
D10	SWIN45	**Analog switch input 45.** Connect SWIN45 to the high-voltage pulse/transmitter.
D11	SWIN44	**Analog switch input 44.** Connect SWIN44 to the high-voltage pulse/transmitter.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
D13	SWOUT14	**Analog switch output 14.** Connect SWout14 to the piezoelectric transducer.
D14	SWIN13	**Analog switch input 13.** Connect SWIN13 to the high-voltage pulse/transmitter.
E1	SWIN0	**Analog switch input 0.** Connect SWIN0 to the high-voltage pulse/transmitter.
E2	GND	**Device ground.**
E4	SWIN37	**Analog switch input 37.** Connect SWIN37 to the high-voltage pulse/transmitter.
E5	SWOUT37	**Analog switch output 37.** Connect SWOUT37 to the piezoelectric transducer.
E6	SWIN39	**Analog switch input 39.** Connect SWIN39 to the high-voltage pulse/transmitter.
E7	SWOUT39	**Analog switch output 39.** Connect SWOUT39 to the piezoelectric transducer.
E8	SWIN42	**Analog switch input 42.** Connect SWIN42 to the high-voltage pulse/transmitter.
E9	SWOUT42	**Analog switch output 42.** Connect SWOUT42 to the piezoelectric transducer.
E10	SWOUT45	**Analog switch output 45**. Connect SWOUT45 to the piezoelectric transducer.
E11	SWOUT44	**Analog switch output 44.** Connect SWOUT44 to the piezoelectric transducer.
E13	SWIN46	**Analog switch input 46.** Connect SWIN46 to the high-voltage pulse/transmitter.
E14	SWOUT13	**Analog switch output 13.** Connect SWOUT13 to the piezoelectric transducer.
F1	VLL	**Logic supply voltage.** VLL has a 2.7V to 5.5V operating range.
F2	VDD	**Translator supply voltage.** VDD has a 4.5V to 5.5V operating range.
F4	SWOUT34	**Analog switch output 34.** Connect SWOUT34 to the piezoelectric transducer.
F5	GND	**Device ground.**
F10	SWIN48	**Analog switch input 48.** Connect SWIN48 to the high-voltage pulse/transmitter.
F11	SWIN47	**Analog switch input 47.** Connect SWIN47 to the high-voltage pulse/transmitter.
F13	SWOUT46	**Analog switch output 46.** Connect SWOUT46 to the piezoelectric transducer.
F14	SWIN15	**Analog switch input 15.** Connect SWIN15 to the high-voltage pulse/transmitter.
G1	DIN	**Logic input.** DIN is the data input for the 64-bit serial shift register.
G2	GND	**Device ground.**
G4	SWIN34	**Analog switch input 34.** Connect SWIN34 to the high-voltage pulse/transmitter.
G5	SWOUT33	**Analog switch output 33.** Connect SWOUT33 to the piezoelectric transducer.
G10	SWOUT48	**Analog switch output 48.** Connect SWOUT48 to the piezoelectric transducer.
G11	SWOUT47	**Analog switch output 47.** Connect SWOUT47 to the piezoelectric transducer.
G13	SWIN17	**Analog switch input 17.** Connect SWIN17 to the high-voltage pulse/transmitter.
G14	SWOUT15	**Analog switch output 15.** Connect SWOUT15 to the piezoelectric transducer.
H1	CLK	**Logic input.** CLK is the clock input for the 64-bit serial shift register. Data is loaded into the register during the rising edge of the clock.
H2	GND	**Device ground.**
H4	SWOUT32	**Analog switch output 32.** Connect SWOUT32 to the piezoelectric transducer.
H5	SWIN33	**Analog switch input 33.** Connect SWIN33 to the high-voltage pulse/transmitter.
H10	SWIN50	**Analog switch input 50.** Connect SWIN50 to the high-voltage pulse/transmitter.
H11	SWIN49	**Analog switch input 49.** Connect SWIN49 to the high-voltage pulse/transmitter.
H13	SWOUT17	**Analog switch output 17.** Connect SWOUT17 to the piezoelectric transducer.
H14	SWIN16	**Analog switch input 16.** Connect SWIN16 to the high-voltage pulse/transmitter.
J1	LEB	**Logic input.** LEB is the latch enable bar for the 64-bit latch. Pull this pin logic low to transfer data from the serial shift registers to the latches; pull it high to hold the data in the latches. See the Logic Truth Table on page 11 for more details.
J2	GND	**Device ground**.
J4	SWIN32	**Analog switch input 32.** Connect SWIN32 to the high-voltage pulse/transmitter.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
J5	GND	**Device ground.**
J10	SWOUT50	**Analog switch output 50.** Connect SWOUT50 to the piezoelectric transducer.
J11	SWOUT49	**Analog switch output 49.** Connect SWOUT49 to the piezoelectric transducer.
J13	SWIN20	**Analog switch input 20.** Connect SWIN20 to the high-voltage pulse/transmitter.
J14	SWOUT16	**Analog switch output 16.** Connect SWOUT16 to the piezoelectric transducer.
K1	SWOUT31	**Analog switch output 31.** Connect SWOUT31 to the piezoelectric transducer.
K2	DOUT	**Logic output.** DOUT is the data output from the 64-bit serial shift register.
K4	SWOUT61	**Analog switch output 61.** Connect SWOUT61 to the piezoelectric transducer.
K5	SWIN61	**Analog switch input 61.** Connect SWIN61 to the high-voltage pulse/transmitter.
K6	SWOUT59	**Analog switch output 59.** Connect SWOUT59 to the piezoelectric transducer.
K7	SWIN59	**Analog switch input 59.** Connect SWIN59 to the high-voltage pulse/transmitter.
K8	SWOUT57	**Analog switch output 57.** Connect SWOUT57 to the piezoelectric transducer.
K9	SWIN57	**Analog switch input 57.** Connect SWIN57 to the high-voltage pulse/transmitter.
K10	SWOUT55	**Analog switch output 55.** Connect SWOUT55 to the piezoelectric transducer.
K11	SWIN55	**Analog switch input 55.** Connect SWIN55 to the high-voltage pulse/transmitter.
K13	SWOUT20	**Analog switch output 20.** Connect SWOUT20 to the piezoelectric transducer.
K14	SWIN18	**Analog switch input 18.** Connect SWIN18 to the high-voltage pulse/transmitter.
L1	SWIN31	**Analog switch input 31.** Connect SWIN31 to the high-voltage pulse/transmitter.
L2	SWOUT63	**Analog switch output 63.** Connect SWOUT63 to the piezoelectric transducer.
L4	SWOUT60	**Analog switch output 60.** Connect SWOUT60 to the piezoelectric transducer.
L5	SWIN60	**Analog switch input 60.** Connect SWIN60 to the high-voltage pulse/transmitter.
L6	SWOUT58	**Analog switch output 58.** Connect SWOUT58 to the piezoelectric transducer.
L7	SWIN58	**Analog switch input 58.** Connect SWIN58 to the high-voltage pulse/transmitter.
L8	SWOUT56	**Analog switch output 56.** Connect SWOUT56 to the piezoelectric transducer.
L9	SWIN56	**Analog switch input 56.** Connect SWIN56 to the high-voltage pulse/transmitter.
L10	SWOUT54	**Analog switch output 54.** Connect SWOUT54 to the piezoelectric transducer.
L11	SWIN54	**Analog switch input 54.** Connect SWIN54 to the high-voltage pulse/transmitter.
L13	SWIN51	**Analog switch input 51.** Connect SWIN51 to the high-voltage pulse/transmitter.
L14	SWOUT18	**Analog switch output 18.** Connect SWOUT18 to the piezoelectric transducer.
M1	SWOUT30	**Analog switch output 30.** Connect SWOUT30 to the piezoelectric transducer.
M2	SWIN63	**Analog switch input 63.** Connect SWIN63 to the high-voltage pulse/transmitter.
M13	SWOUT51	**Analog switch output 51.** Connect SWOUT51 to the piezoelectric transducer.
M14	SWIN19	**Analog switch input 19.** Connect SWIN19 to the high-voltage pulse/transmitter.
N1	SWIN30	**Analog switch input 30.** Connect SWIN30 to the high-voltage pulse/transmitter.
N2	SWOUT62	**Analog switch output 62.** Connect SWOUT62 to the piezoelectric transducer.
N3	SWOUT29	**Analog switch output 29.** Connect SWOUT29 to the piezoelectric transducer.
N4	SWIN29	**Analog switch input 29.** Connect SWIN29 to the high-voltage pulse/transmitter.
N5	SWOUT27	**Analog switch output 27.** Connect SWOUT27 to the piezoelectric transducer.
N6	SWIN27	**Analog switch input 27.** Connect SWIN27 to the high-voltage pulse/transmitter.
N7	SWOUT25	**Analog switch output 25.** Connect SWOUT25 to the piezoelectric transducer.
N8	SWIN25	**Analog switch input 25.** Connect SWIN25 to the high-voltage pulse/transmitter.
N9	SWOUT23	**Analog switch output 23.** Connect SWOUT23 to the piezoelectric transducer.
N10	SWIN23	**Analog switch input 23.** Connect SWIN23 to the high-voltage pulse/transmitter.
N11	SWOUT53	**Analog switch output 53.** Connect SWOUT53 to the piezoelectric transducer.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
N12	SWIN53	**Analog switch input 53.** Connect SWIN53 to the high-voltage pulse/transmitter.
N13	SWIN52	**Analog switch input 52.** Connect SWIN52 to the high-voltage pulse/transmitter.
N14	SWOUT19	**Analog switch output 19.** Connect SWOUT19 to the piezoelectric transducer.
P1	GND	**Device ground.**
P2	SWIN62	**Analog switch input 62.** Connect SWIN62 to the high-voltage pulse/transmitter.
P3	SWOUT28	**Analog switch output 28.** Connect SWOUT28 to the piezoelectric transducer.
P4	SWIN28	**Analog switch input 28.** Connect SWIN28 to the high-voltage pulse/transmitter.
P5	SWOUT26	**Analog switch output 26.** Connect SWOUT26 to the piezoelectric transducer.
P6	SWIN26	**Analog switch input 26.** Connect SWIN26 to the high-voltage pulse/transmitter.
P7	SWOUT24	**Analog switch output 24**. Connect SWOUT24 to the piezoelectric transducer.
P8	SWIN24	**Analog switch input 24.** Connect SWIN24 to the high-voltage pulse/transmitter.
P9	SWOUT22	**Analog switch output 22.** Connect SWOUT22 to the piezoelectric transducer.
P10	SWIN22	**Analog switch input 22.** Connect SWIN22 to the high-voltage pulse/transmitter.
P11	SWOUT21	**Analog switch output 21.** Connect SWOUT21 to the piezoelectric transducer.
P12	SWIN21	**Analog switch input 21.** Connect SWIN21 to the high-voltage pulse/transmitter.
P13	SWOUT52	**Analog switch output 52.** Connect SWOUT52 to the piezoelectric transducer.
P14	GND	**Device ground.**

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ABSOLUTE MAXIMUM RATINGS (1)

Logic supply (V_{LL}).....-0.5V to +6.6V
Translator supply (V_{DD}) .....-0.5V to +6.6V
Analog signal range (V_{SIG}) .....0V to ±105V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)……
……..4.8W
Storage temperature..... -55°C to +150°C

ESD Ratings

Human body model (HBM) .....JEDEC standard
SWOUTx..... Class 1B
SWINx..... Class 1C
Other pins .....Class 2

Recommended Operating Conditions (3)

Logic supply voltage (V_{LL}).....2.7V to 5.5V
Translator supply voltage (V_{DD}).....4.5V to 5.5V
Analog signal range (V_{SIG}) .....0V to ±90V
Junction temperature (T_J) ..... -25°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

BGA-144 (10mmx10mm)……..21…….4….°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature and result in permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-9, 4-layer PCB.

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DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{LL} = 5V, unless otherwise noted. (5)

Parameter	Sym	Conditions	T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Analog signal range	V_{SIG}	Applied to SWINx	0	±90	0		±90	0	±90	V
On resistance	R_{ON}	I_{SIG} = ±5mA, SWOUTx = 0V, see Figure 2 on page 12		20		14	24		30	Ω
		I_{SIG} = ±200mA, SWOUTx = 0V, see Figure 2 on page 12		16		13.5	19		24	
Small signal on-resistance matching	R_{ON}	I_{SIG} = ±5mA, SWOUTx = 0V				5.0				%
Large signal on resistance (6)	R_{ONL}	I_{SIG} = ±1.0A, t_{PW} ≤ 500ns, duty cycle ≤ 1%, SWOUTx = 0V, see Figure 3 on page 12				13				Ω
Switch output peak current	I_{SWPK}	t_{PW} ≤ 100ns, duty cycle ≤ 1%				±1.8				A
Output bleed resistor	R_{BLEED}	I_{SIG} = ±50µA			20	30	50			kΩ
Switch-off DC offset	V_{DC-OFF}	No load, no V_{SIG}, see Figure 4 on page 12		±50			±50		±50	mV
Switch-on DC offset	V_{DC-ON}	No load, no V_{SIG}, see Figure 4 on page 12		±50			±50		±50	mV
VLL quiescent current	I_{LLQ}	All logic inputs are static		100			100		100	µA
VDD quiescent current	I_{DDQ}	All switches on or off, SWINx = SWOUTx = ground		1			1		1	µA
VLL average dynamic current	I_{LL}	f_{CLK} = 30MHz, D_{IN} = 15MHz				9	11			mA
		f_{CLK} = 60MHz, D_{IN} = 30MHz				11				mA
V_{DD} average dynamic current	I_{DD}	All output switches are turning on and off at 50kHz				6.6	8.5			mA
Input voltage logic low	V_{IL}		0	0.2 x V_{LL}	0		0.2 x V_{LL}	0	0.2 x V_{LL}	V
Input voltage logic high	V_{IH}		0.8 x V_{LL}	V_{LL}	0.8 x V_{LL}		V_{LL}	0.8 x V_{LL}	V_{LL}	V
Input current logic low	I_{IL}		-1.0		-1.0			-1.0		µA
Input current logic high	I_{IH}			1.0			1.0		1.0	µA
Data out logic low voltage	V_{OL}	I_{SINK} = 10mA		1.0			1.0		1.0	V
Data out logic high voltage	V_{OH}	I_{SOURCE} = 10mA	V_{LL} - 1.0		V_{LL} - 1.0			V_{LL} - 1.0		V
Logic input capacitance	C_{IN}			10			10		10	pF

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AC ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{LL} = 5V, unless otherwise noted. (5)

Parameter	Sym	Conditions		T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
Clock frequency (6)	f_{CLK}	50% duty cycle	V_{LL} = 3.3V	0	30	0		30	0	30	MHz
			V_{LL} = 5V	0	60	0		60	0	60	
Clock rising time (6)	t_r				50			50		50	ns
Clock falling time (6)	t_f				50			50		50	ns
Set-up time from data to the rising edge of the clock (6)	t_{SU}			3		3			3		ns
Hold time from the rising edge of the clock to data (6)	t_H			3		3			3		ns
Set-up time before the LE bar rises (6)	t_{SD}			6.0		6.0			6		ns
LE\ pulse width (6)	$t_{WLE\ BAR}$			6.0		6.0			6		ns
Data out propagation delay time from the rising edge of clock (6)	t_{DOHL}, t_{DOLH}	20pF on DOUT to ground		8.5	13	8.5	11	13	8.5	13	ns
Output switch turn-on time	t_{ON}	SWIN = 2V, SWOUT = 50Ω to ground, see Figure 5 on page 13			2.0			2.0		2.0	µs
Output switch turn-off time	t_{OFF}				2.0			2.0		2.0	µs
Analog signal slew rate (6)	dV/dt				20			20		20	V/ns
Off isolation (6)	K_O	f_{SW} = 5MHz, R_{LOAD} = 50Ω, see Figure 6 on page 13					-66				dB
Switch crosstalk (6)	K_{CR}	f_{SW} = 5MHz, R_{LOAD} = 50Ω, see Figure 7 on page 13					-60				dB
SWIN Switch-off capacitance (6)	$C_{SWIN-OFF}$						26				pF
SWIN Switch-on capacitance (6)	$C_{SWIN-ON}$						35				pF
SWOUT switch-off capacitance (6)	$C_{SWOUT-OFF}$						9				pF
SWOUT switch-on capacitance (6)	$C_{SWOUT-ON}$						35				pF
Positive output voltage spike (6)	$+V_{SPK}$	SWINx = 1kΩ to ground, SWOUTx = 50Ω to ground, see Figure 8 on page 14					78				mV
Negative output voltage spike (6)	$-V_{SPK}$						-5				mV
Output charge injection (6)	Q_{INJ}	C_{LOAD} = 1000pF, see Figure 9 on page 14					18				pC

Notes:

5) Production testing is at 25°C only. 0°C and 70°C limits are guaranteed by design and characterization.
6) Parameters are not tested in mass production. Only guaranteed by design or bench characterization.

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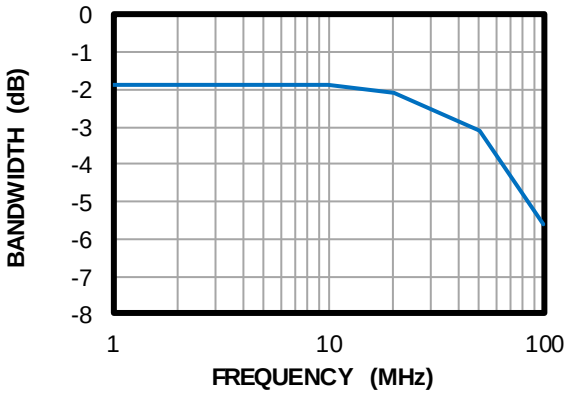
TYPICAL PERFORMANCE CHARACTERISTICS

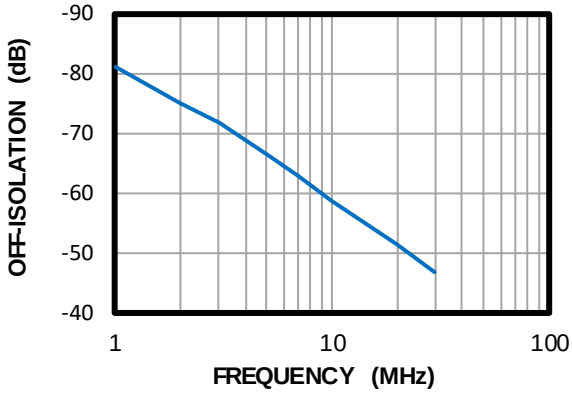
Bandwidth vs. Frequency

R_{LOAD} = 50Ω



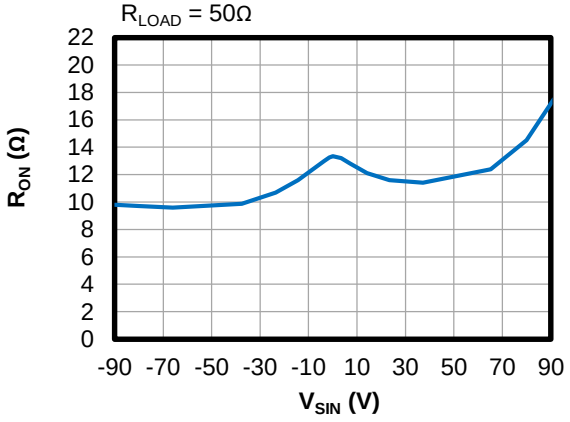
Off-Isolation vs. Frequency

R_{LOAD} = 50Ω



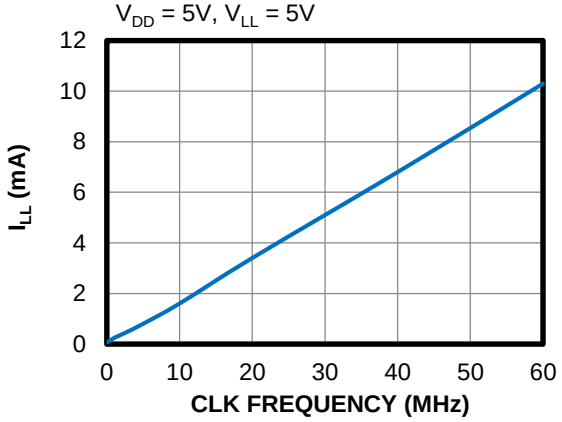
Switch On Resistance vs. Switch Input Voltage

R_{LOAD} = 50Ω



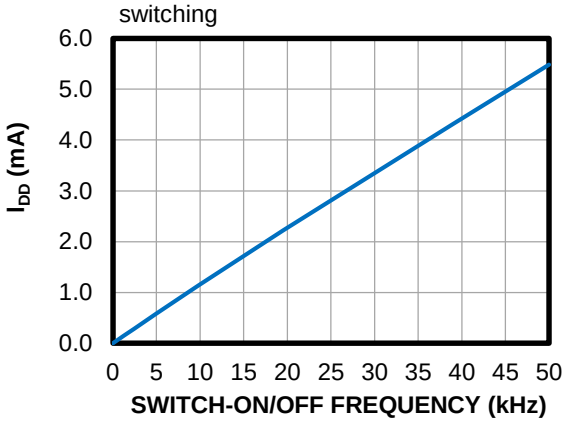
I_{LL} vs. CLK Frequency

V_{DD} = 5V, V_{LL} = 5V



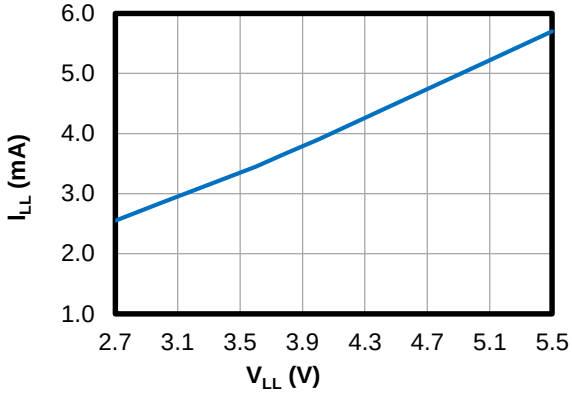
I_{DD} vs. Switch-On/Off Frequency

V_{DD} = 5V, V_{LL} = 5V, all 64 channels switching



I_{LL} vs. V_{LL}

CLK = 30MHz, DIN = 15MHz



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TIMING DIAGRAM

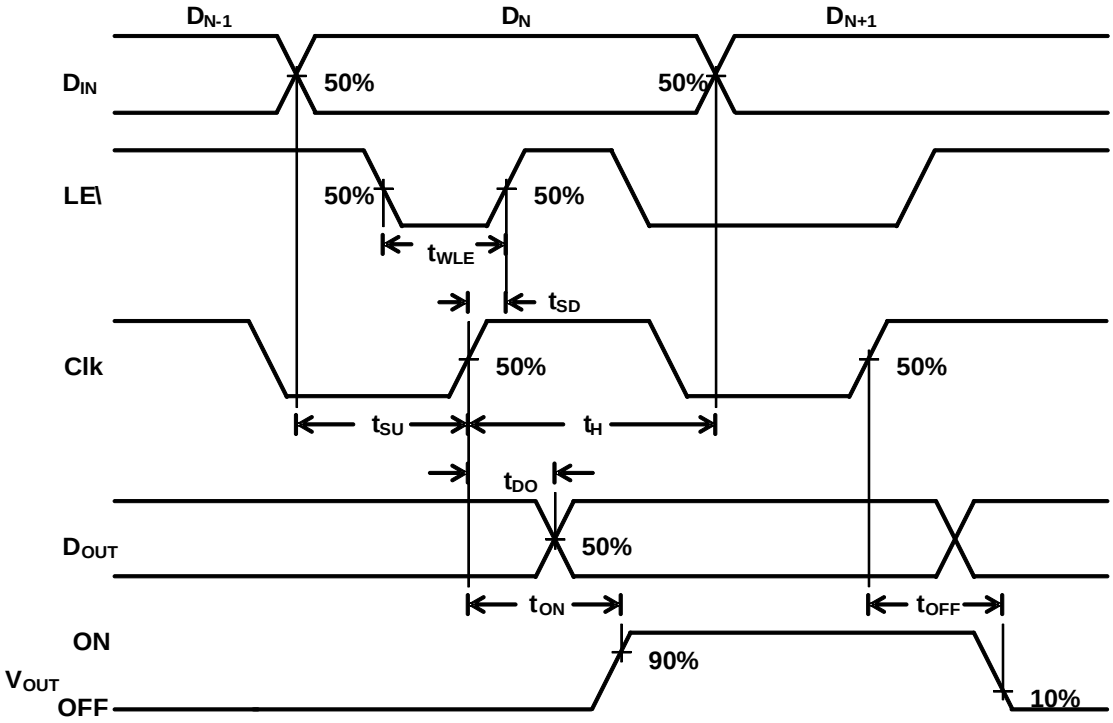

Figure 1: Timing Diagrams

LOGIC TRUTH TABLE (7)

Logic Input							Switch State				
D0	D1	D2	- - -	D63	Din	LE Bar	SW0	SW1	SW2	- - -	SW63
L	-	-		-	x	L	Off	-	-		-
H	-	-		-	x	L	On	-	-		-
-	L	-		-	x	L	-	Off	-		-
-	H	-		-	x	L	-	On	-		-
-	-	L		-	x	L	-	-	Off		-
-	-	H		-	x	L	-	-	On		-
⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮		⋮
-	-	-		L		L	-	-	-		Off
-	-	-		H	x	L	-	-	-		On
x	x	x		x	x	H	Hold previous state				

Note:

7) "L" denotes logic level low, "H" denotes logic level high, and "x" denotes not applicable.

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TEST CIRCUITS

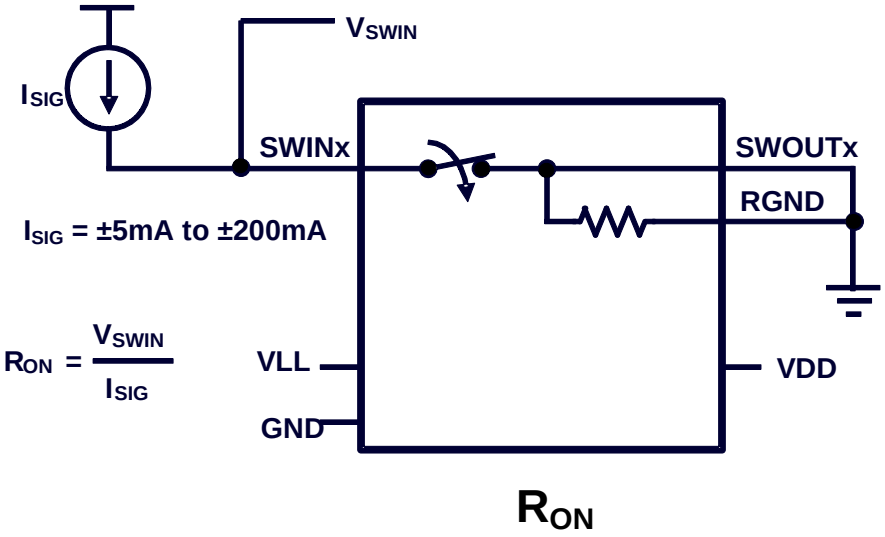

Figure 2: Test Circuit 1

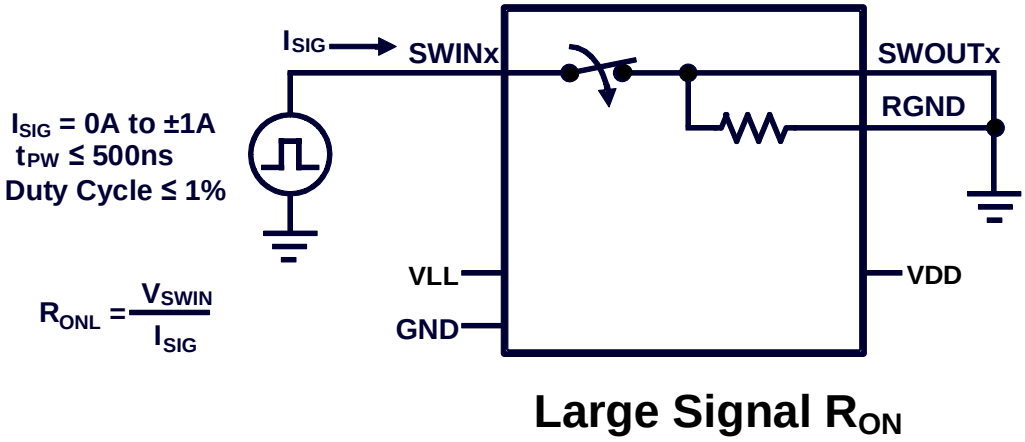

Figure 3: Test Circuit 2

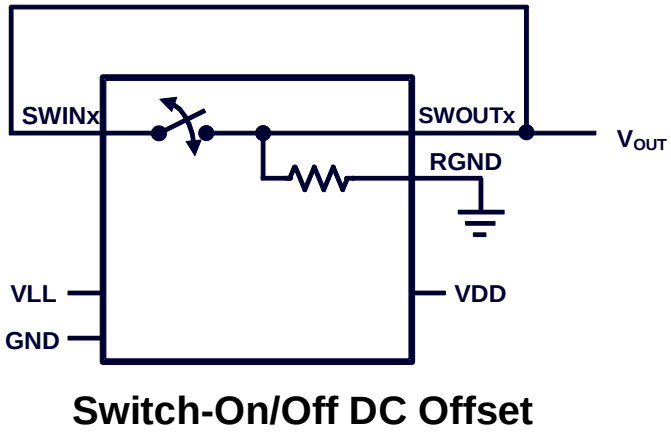

Figure 4: Test Circuit 3

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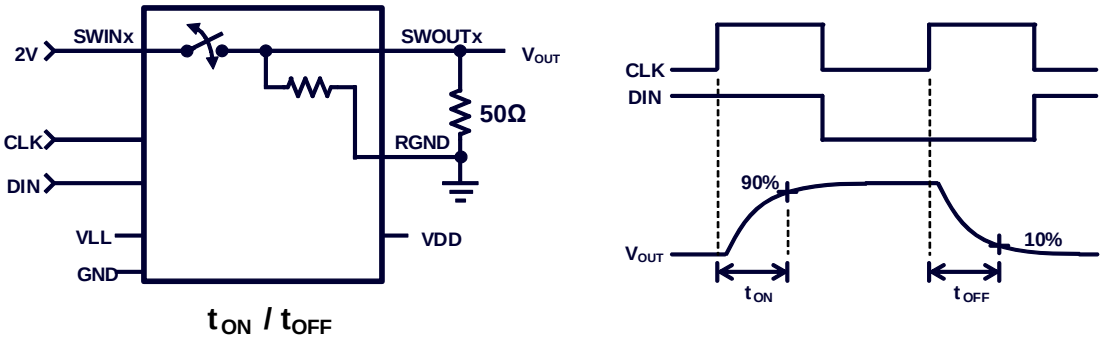
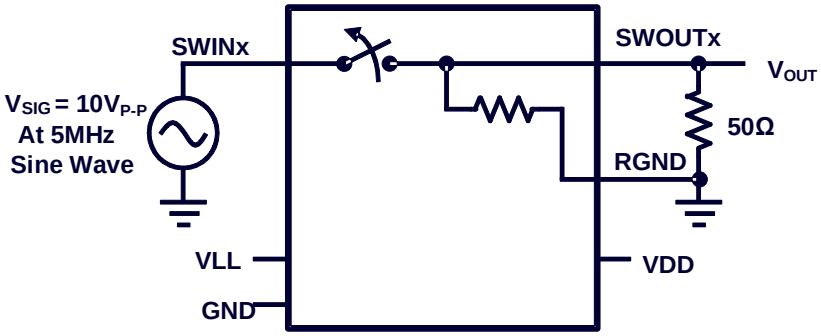
TEST CIRCUITS *(continued)*



t_{ON} / t_{OFF}

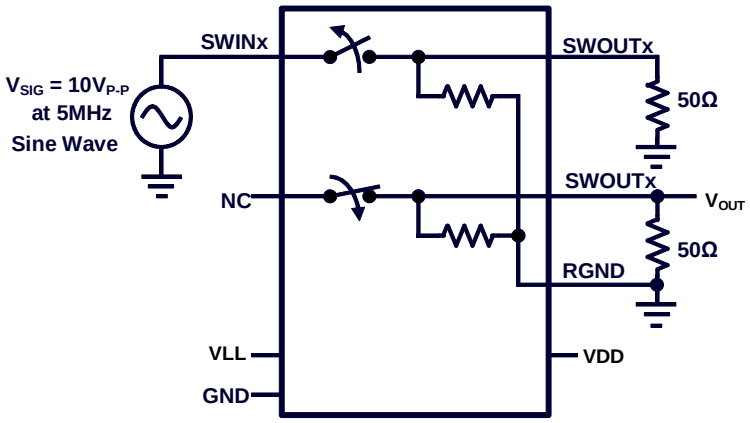
Figure 5: Test Circuit 4



$$K_O = 20Log\left|\frac{V_{OUT}}{V_{SIG}}\right|$$

Switch-Off Isolation

Figure 6: Test Circuit 5



Switch Crosstalk $K_{CR} = 20Log\left|\frac{V_{OUT}}{V_{SIG}}\right|$

Figure 7: Test Circuit 6

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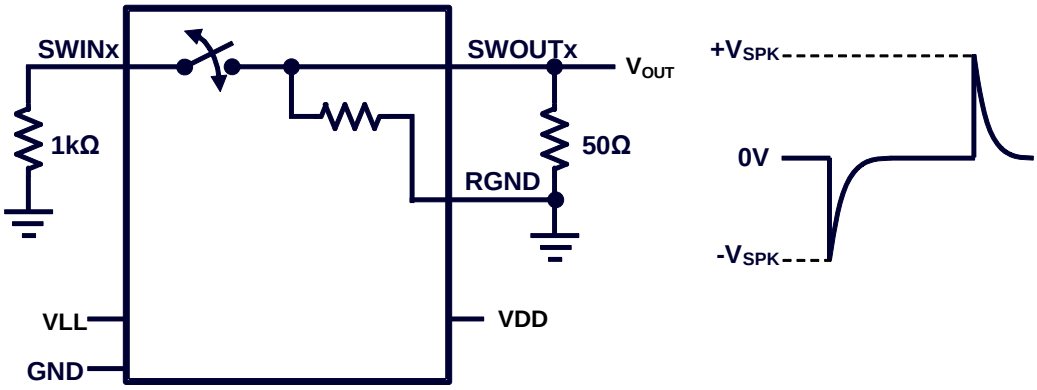
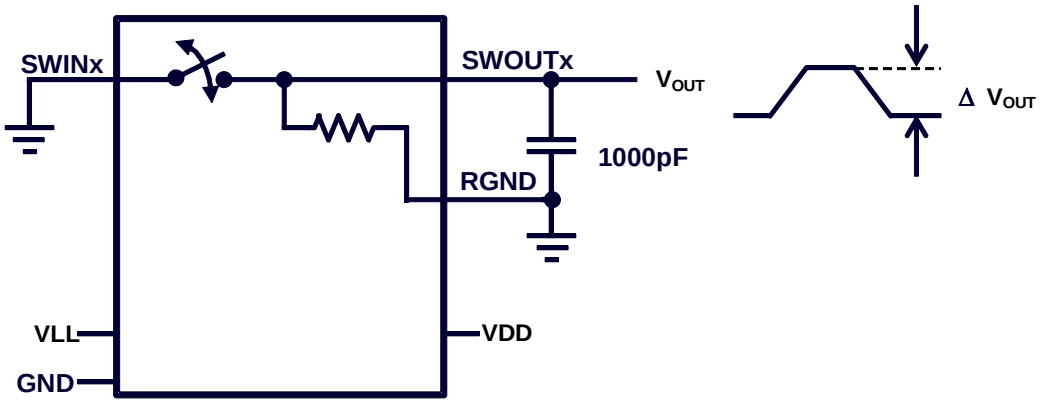
TEST CIRCUITS *(continued)*



Output Voltage Spike

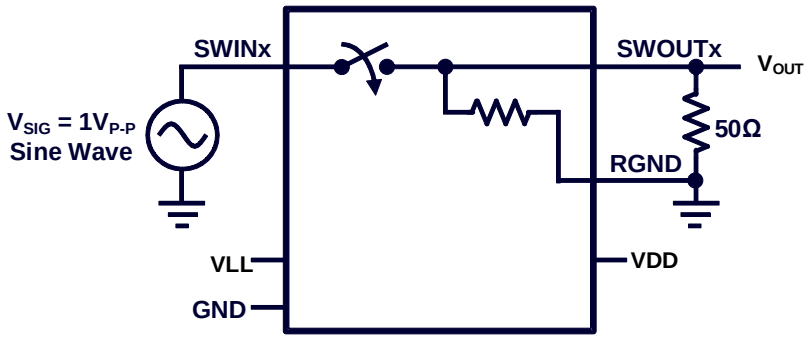
Figure 8: Test Circuit 7



$Q_{INJ} = 1000pF \times \Delta V_{OUT}$

Charge Injection

Figure 9: Test Circuit 8



Small Signal Bandwidth

Figure 10: Test Circuit 9

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FUNCTIONAL BLOCK DIAGRAM

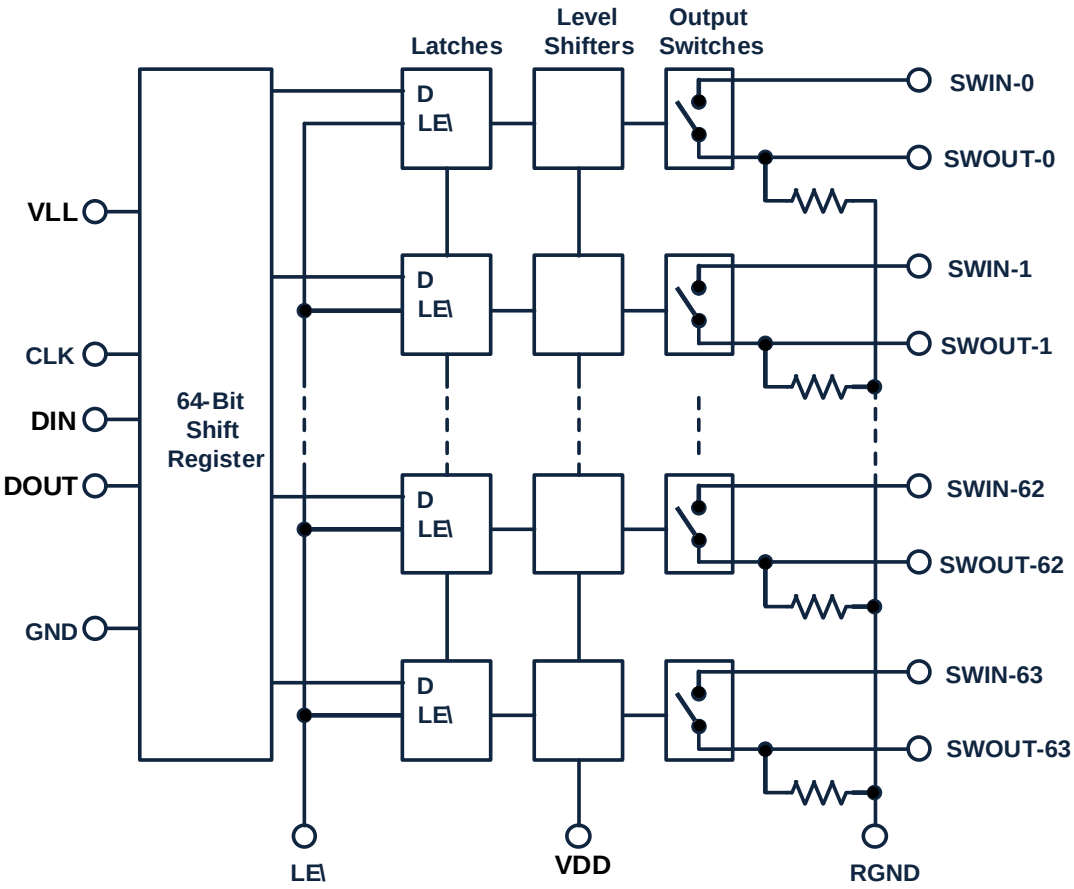

Figure 11: Functional Block Diagram

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OPERATION

The MP4865A is a 64-channel, high-voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors. It is designed for medical ultrasound imaging and non-destructive testing (NDT) applications. The MP4865A is designed to multiplex high transmission voltages to the selected piezoelectric transducers (PZTs), and to multiplex small analog echo signals to the selected receivers

The output switches are controlled by a 64-bit serial shift register followed by a 64-bit data latch. A data out (DOUT) pin allows for multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high signal in the data latch turns on the corresponding analog switch; a logic low signal turns off the corresponding analog switch.

The MP4865A has a unique patented design that does not require any high-voltage negative or positive supplies. As a result, the MP4865A eliminates:

- The need to generate high-voltage positive and negative supplies
- The need to place high-voltage bypass capacitors next to each device
- Safety concerns regarding the high-voltage buses
- Concerns related to start-up and/or shutdown fault conditions

Analog Switch

The analog switches have a typical switch on resistance (R_{ON}) of 14Ω. When turned on, the MP4865A can pass transmission voltages up to ±90V, with peak currents of up to ±1.8A. When turned off, the device can block voltages up to ±90V.

Each switch has a dedicated input and output pin (SWINx and SWOUTx). The transmission voltages must be connected to the SWINx pins, and the PZT load must be connected to the SWOUTx pins. The SWINx and SWOUTx pins are not interchangeable.

Typically, high-voltage transmission waves are caused by short bursts of high-voltage pulses. The burst can consist of a single cycle or multiple cycles with 1MHz to 15MHz pulses, starting and ending at 0V (see Figure 12).

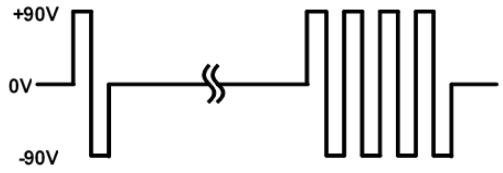

Figure 12: Typical High Voltage Burst

The SWINx input must be close to ground before sending the high-voltage pulses. This allows the internal circuitry to properly drive the output switches. Transmission voltages above ±5V require frequencies above 500kHz. There is no restriction when receiving echo signals in which the voltages are below ±0.5V. The switch can pass low-voltage DC signals.

Logic Interface

The MP4865A is controlled by a 64-bit serial shift register, followed by a 64-bit latch. Data is loaded into the shift register during the rising edge of the clock. No data is transferred during the falling edge. Data is shifted into register 0, then data is shifted out of register 63.

Figure 13 shows the logic interface details. During the first clock cycle, the first data bit enters shift register 0. After 63 more clocked cycles, the first bit is in register 63.

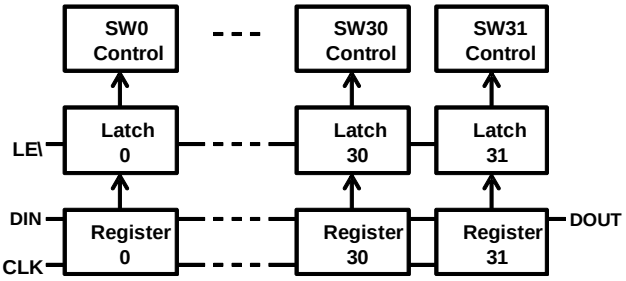

Figure 13: Logic Interface Details

When the latch enable bar (LE\) is low, the data in the shift registers are transferred to the 64-bit latch. When LE\ is high, the data in the latches are held. When LE\ is high, new data can be shifted to the 64-bit serial shift register without affecting the data in the 64-bit latch. The output switches states by following the data in the 64-bit latch.

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APPLICATION INFORMATION

The MP4865A's maximum clock frequency is 60MHz. The front-end logic control is designed to minimize the number of I/O control lines. For example, a system requiring 192 channels would require three devices (192 / 64). Figure 14 shows three MP4865A devices in a single daisy chain configuration. With a 60MHz clock, all three devices can be updated in 3.2µs. Only three control lines are required: clock, data in, and latch enable bar.

For systems requiring a faster update, multiple data input lines can be used (see Figure 15). Figure 15 shows a 192-channel system incorporating three data input lines: D_{INA}, D_{INB}, and D_{INC}. Each MP4865A has its own data input line, which makes a total of five control lines. With a 60MHz clock, all 192 channels can be updated in 1.07µs.

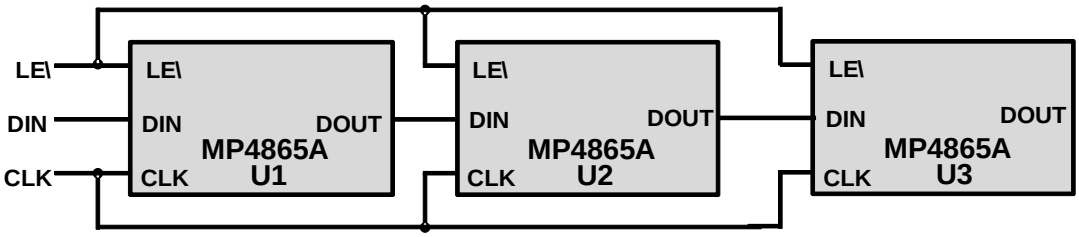

Figure 14: Daisy-Chaining Three MP4865A Devices with a Single Data Input Line

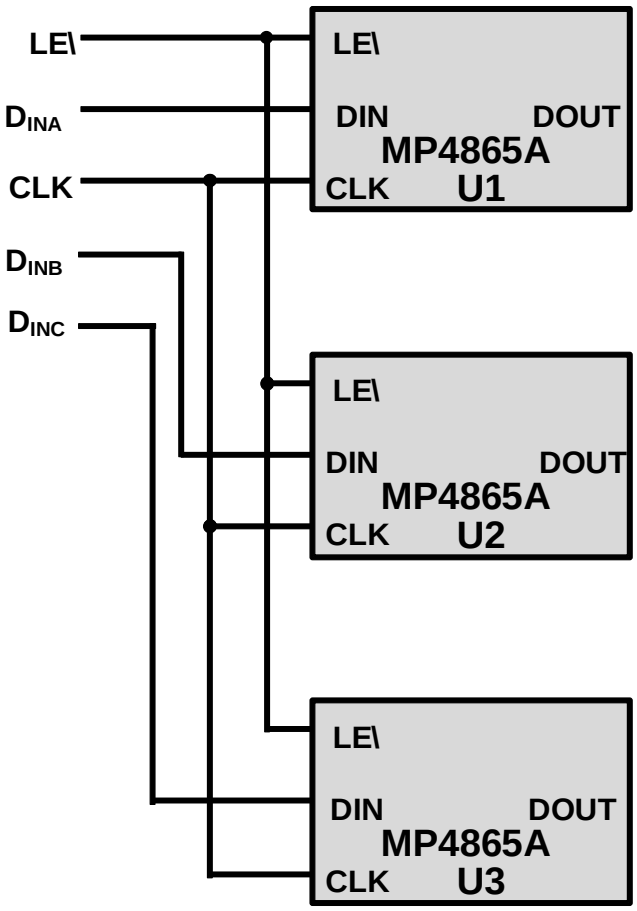

Figure 15: Daisy Chaining MP4865A Devices with Multiple Data Input Lines

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Figure 16 shows where the MP4865A analog switches reside in an ultrasound system. A 1:3 multiplexing configuration is shown as an example. Multiplexing configurations can range from 1:2 to 1:8 or higher. 1:8 or higher ratios have slower image frame rates and/or lower quality images, which are generally used in the lower-end, lower-cost ultrasound market. The MP4865A can be used in any ratio.

The main advantage of using the MP4865A is to simplify the transmitter and receiver circuitry. Without any analog switches, the ultrasound console requires 192 transmitters and receivers to drive an ultrasound probe with 192 PZT elements. With analog switches, only 64 transmitters and receivers are required. This reduction saves board space, power, and cost, since the transmitter and receiver circuitry can be quite complex. These benefits are especially important for portable ultrasound systems in which space, battery life, and weight are all at a premium.

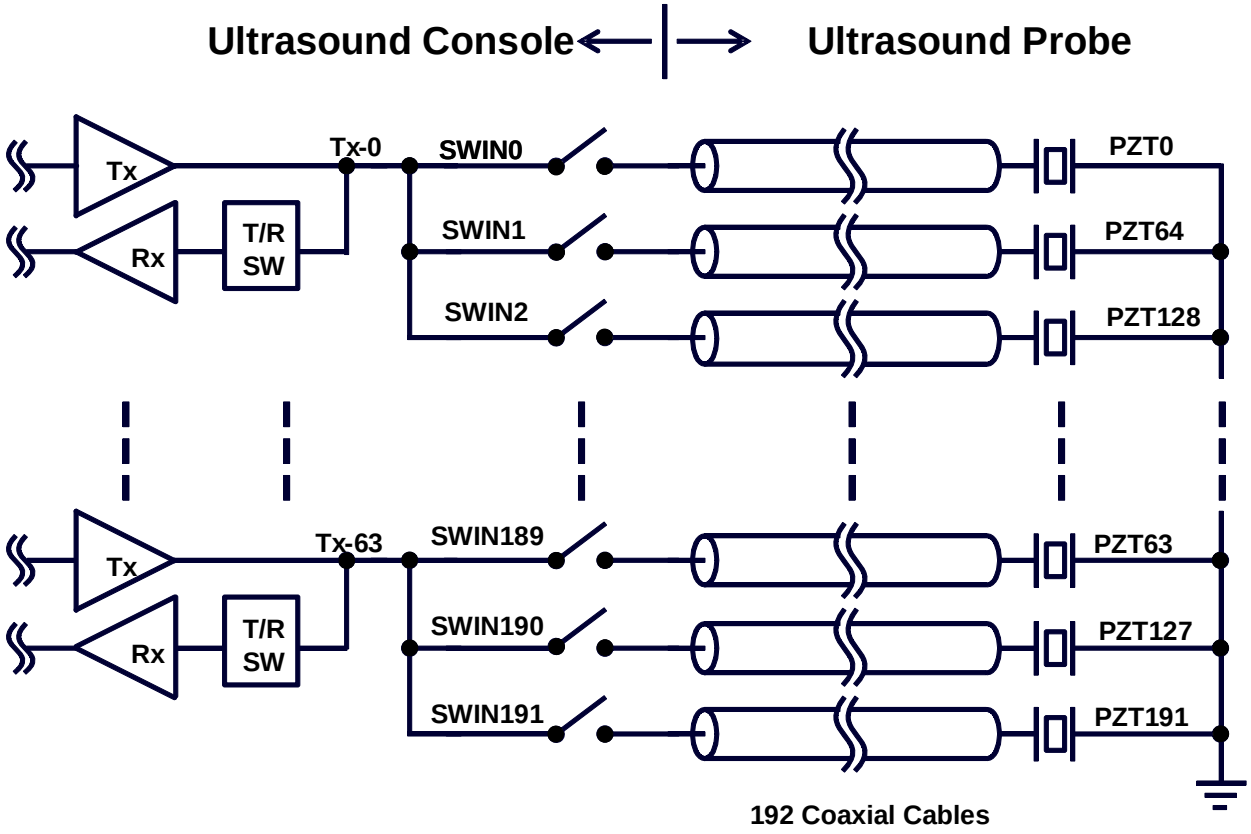

Figure 16: The MP4865A in an Ultrasound Console

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Figure 17 shows the advantages of placing analog switches inside the probe head, which is called an active probe. Typically, the probe head is severely space-limited and thermally limited. The housing is waterproof since it must be submersed in alcohol for sterilization. By employing analog switches inside the probe head, the number of coaxial cables can be reduced. Instead of 192 coaxial cables, only 64 coaxial cables are required for the PZT elements, plus 10 or fewer additional coaxial cables for the supply lines and logic interface.

The reduced number of coaxial cables provides significant cost savings for the probe head, as the coaxial cable is by far the most expensive item. Aside from the material cost, the labor to connect the coaxial cables is also typically quite costly. An added user benefit is the increased maneuverability of the probe head. The sonographer undergoes less fatigue using an active probe. Because it does not require high-voltage supplies, the MP4865A eliminates safety concerns about running high-voltage DC lines on the coaxial cables. The minimal power dissipation design also minimizes thermal constraints inside the probe head, and the higher clock speed helps reduce the number of data lines.

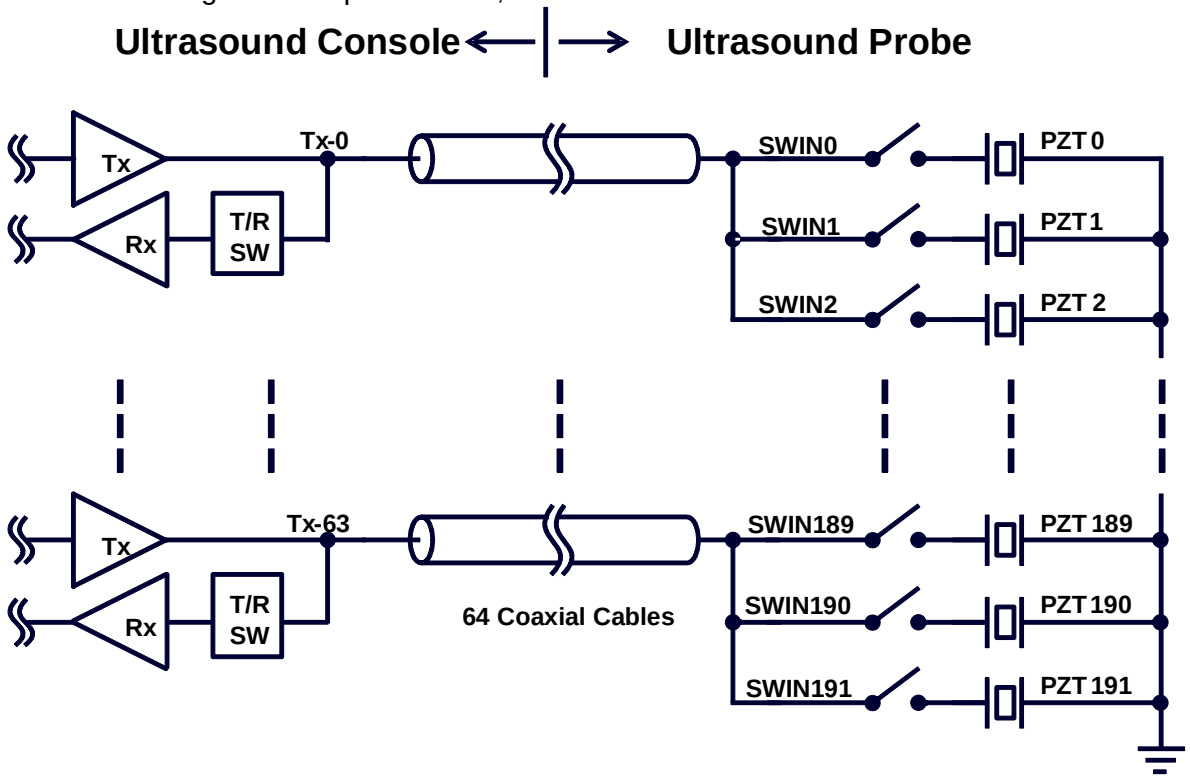

Figure 17: The MP4865A inside the Ultrasound Probe Head

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TYPICAL APPLICATION CIRCUIT

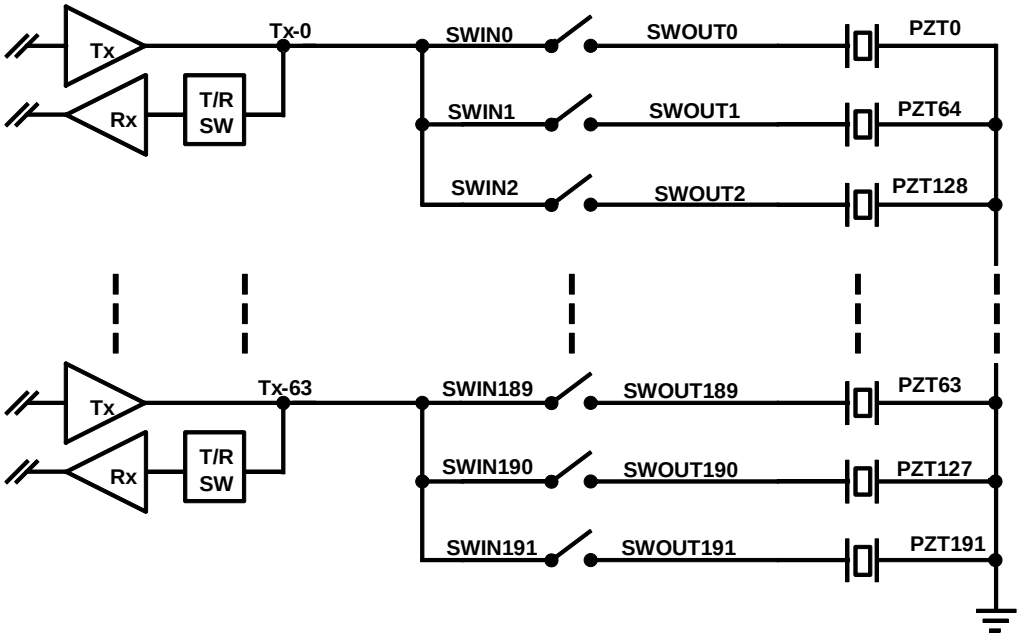

Figure 18: Typical Application Circuit

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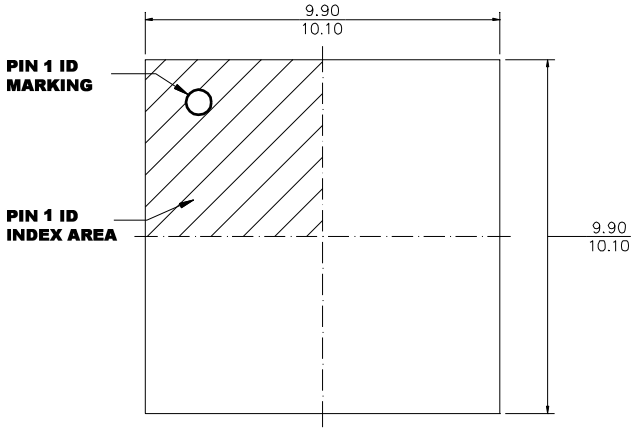
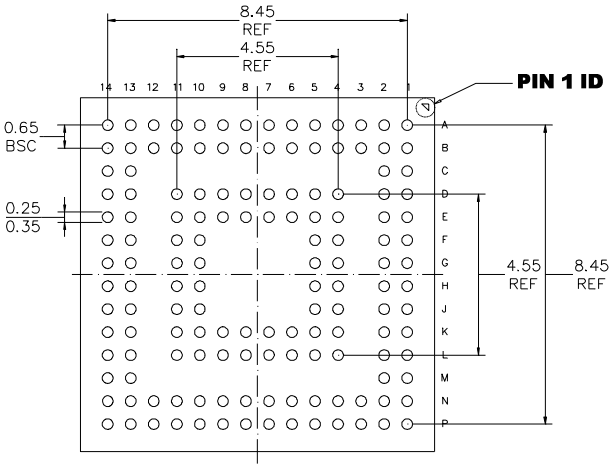
PACKAGE INFORMATION

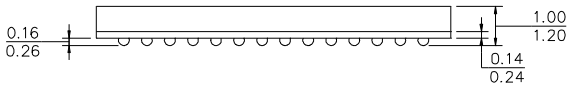
BGA-144 (10mmx10mm)



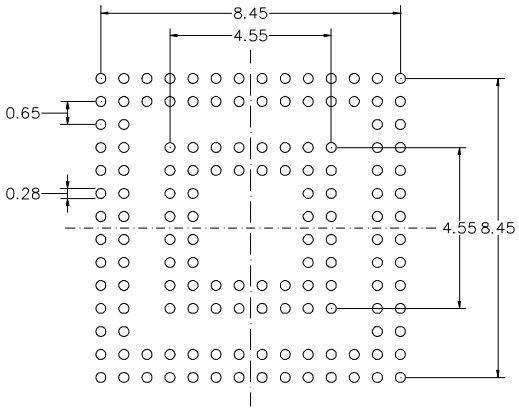
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

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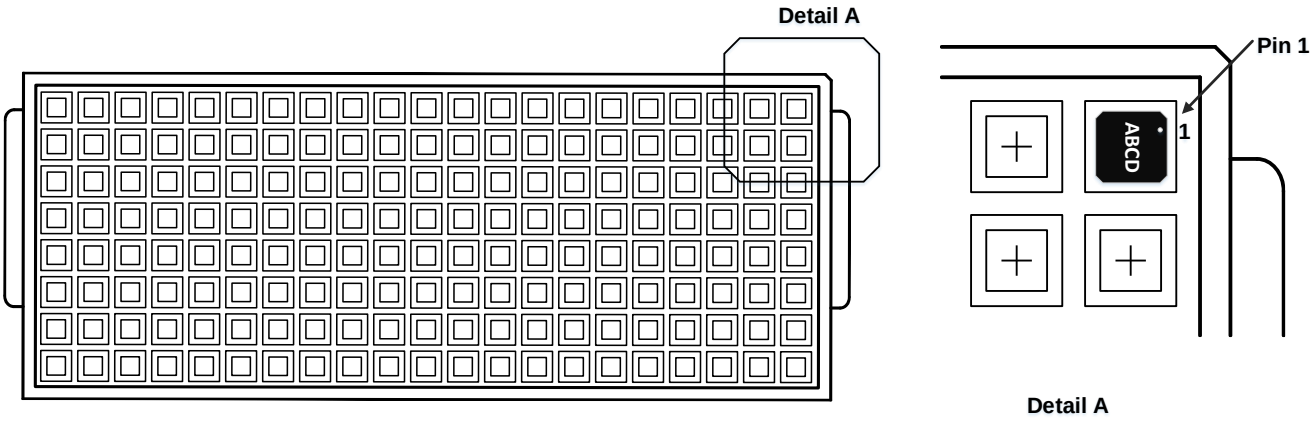
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4865AGBD-T	BGA-144 (10mmx10mm)	N/A	N/A	240	N/A	N/A	N/A

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/21/2022	Initial Release	-

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