# ESD Protection Diode

## Ultra−Low Capacitance Micro−Packaged Diodes for ESD Protection

# ESD7462, SZESD7462



The ESD7462 is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

### Features

- Industry Leading Capacitance Linearity Over Voltage
- Ultra−Low Capacitance: 0.3 pF Typ
- Insertion Loss: 0.05 dB at 1 GHz; 0.10 dB at 3 GHz
- Low Leakage: < 1 nA Typ
- Protection for the following IEC Standards:
  - IEC61000−4−2 (ESD): Level 4
  - IEC61000−4−4 (EFT): 40 A −5/50 ns
  - IEC61000−4−5 (Lightning): 1 A (8/20 μs)
- Protection for ISO 10605 (ESD)
- SZESD7462MXWT5G − Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications
- USB 2.0, USB 3.0

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Total Power Dissipation (Note 2) @ $T_A$ = 25°C<br>Thermal Resistance, Junction−to−Ambient | $P_D$<br>$R_{\theta JA}$ | 300<br>400 | mW<br>°C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Second Duration) | $T_L$ | 260 | °C |
| IEC 61000−4−2 Contact (Note 1)<br>IEC 61000−4−2 Air<br>ISO 10605 Contact (330 pF / 330 Ω)<br>ISO 10605 Contact (330 pF / 2 kΩ)<br>ISO 10605 Contact (150 pF / 2 kΩ)<br>Human Body Model (HBM) | ESD | ±18<br>±18<br>±13<br>±29<br>±30<br>±8 | kV |

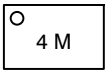
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse at $T_A$ = 25°C, per IEC61000−4−2 waveform.
2. Mounted with recommended minimum pad size, DC board FR−4

### MARKING DIAGRAM



**X2DFN2**
**CASE 714AB**




4 = Specific Device Code
M = Date Code



**X2DFNW2**
**CASE 711BG**




E = Specific Device Code
M = Date Code

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| ESD7462N2T5G | X2DFN2 (Pb−Free) | 8000 / Tape & Reel |
| SZESD7462N2T5G | X2DFN2 (Pb−Free) | 8000 / Tape & Reel |
| SZESD7462MXWT5G | X2DFNW2 (Pb−Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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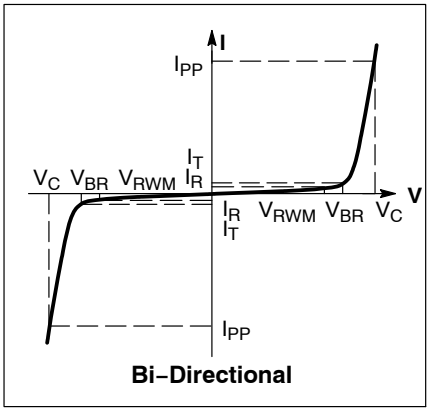
## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $I_{PP}$ | Maximum Reverse Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$ |
| $V_{RWM}$ | Working Peak Reverse Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.




## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse Working Voltage | | | | 16 | V |
| $V_{BR}$ | Breakdown Voltage | $I_T$ = 1 mA (Note 3) | 16.5 | 22 | 28 | V |
| $I_R$ | Reverse Leakage Current | $V_{RWM}$ = 16 V | | | 100 | nA |
| $V_C$ | Clamping Voltage | IEC 61000−4−2, ±8 kV Contact | See Figures 7 and 8 | | | V |
| $V_C$ | Clamping Voltage, TLP (Note 4) | $I_{PP}$ = ±8 A<br>$I_{PP}$ = ±16 A | | ±34<br>±47 | | V |
| $R_{DYN}$ | Dynamic Resistance | TLP Pulse | | 1.6 | | Ω |
| $C_J$ | Junction Capacitance | $V_R$ = 0 V, f = 1 MHz<br>$V_R$ = 0 V, f = 1 GHz | | 0.30<br>0.25 | 0.55<br>0.55 | pF |
| | Insertion Loss | f = 1 GHz<br>f = 3 GHz | | 0.05<br>0.10 | | dB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
4. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 4 ns, averaging window; $t_1$ = 30 ns to $t_2$ = 60 ns.

## TYPICAL CHARACTERISTICS

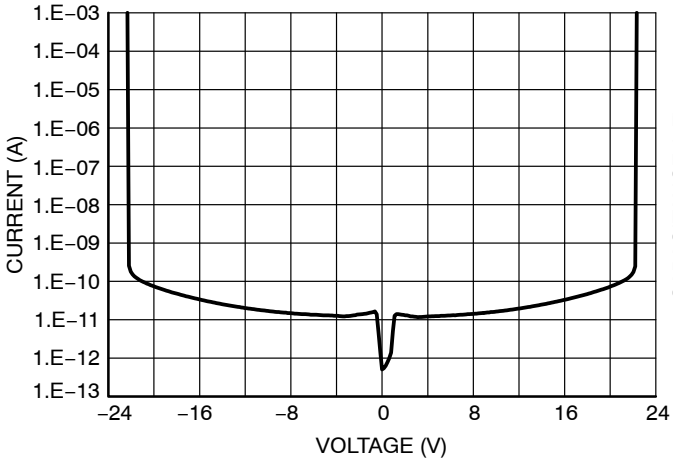



**Figure 1. Typical IV Characteristic Curve**

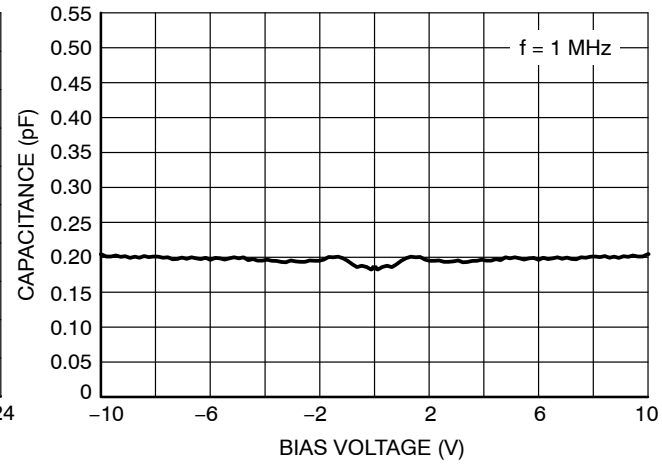



**Figure 2. Typical CV Characteristic Curve**

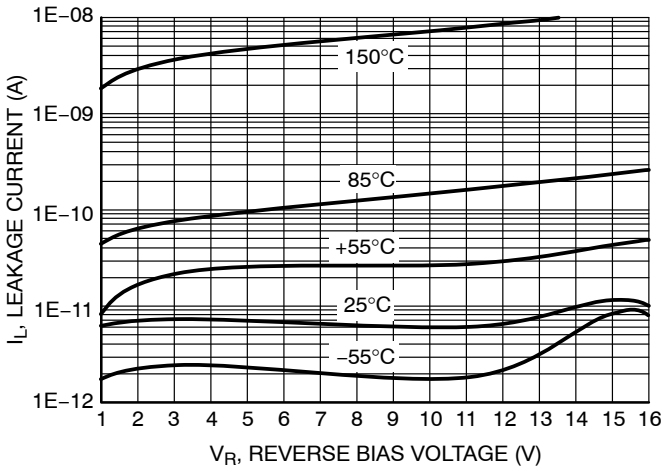



**Figure 3. $I_R$ vs. Temperature Characteristics**

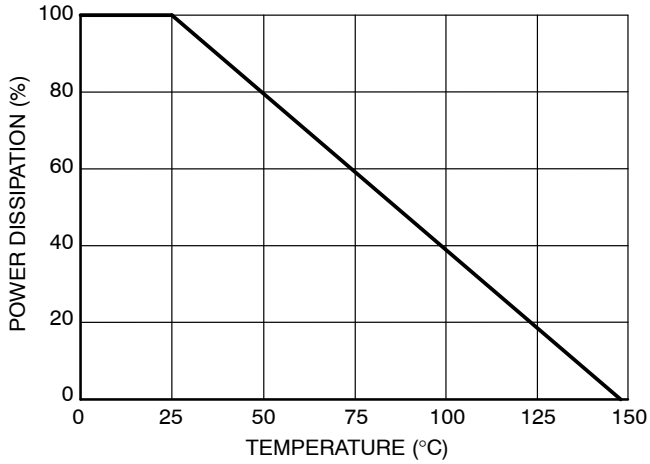



**Figure 4. Steady State Power Derating**

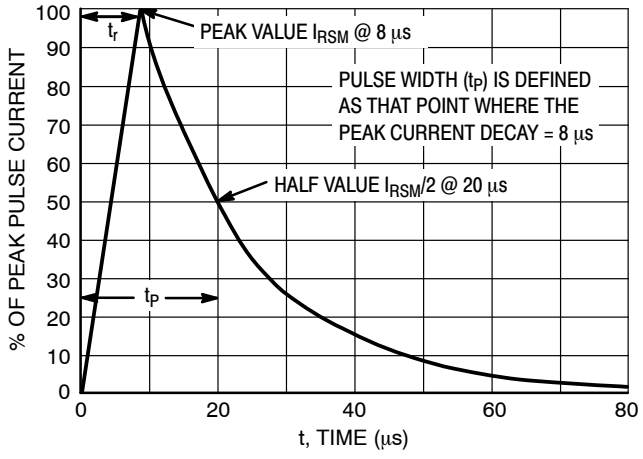



**Figure 5. 8 X 20 μs Pulse Waveform**

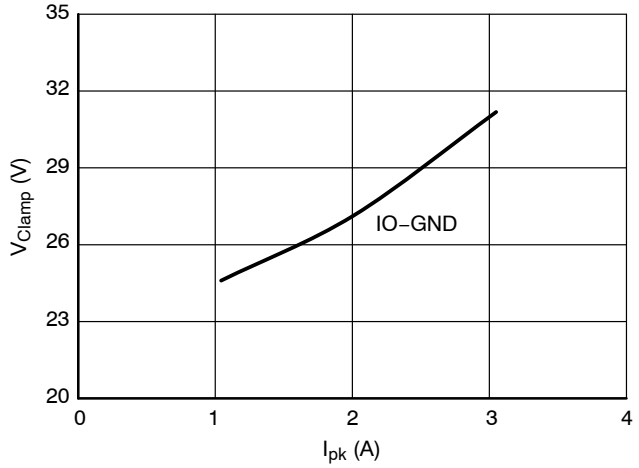



**Figure 6. Clamping Voltage vs. Peak Pulse Current (8/20 μs)**

## TYPICAL CHARACTERISTICS

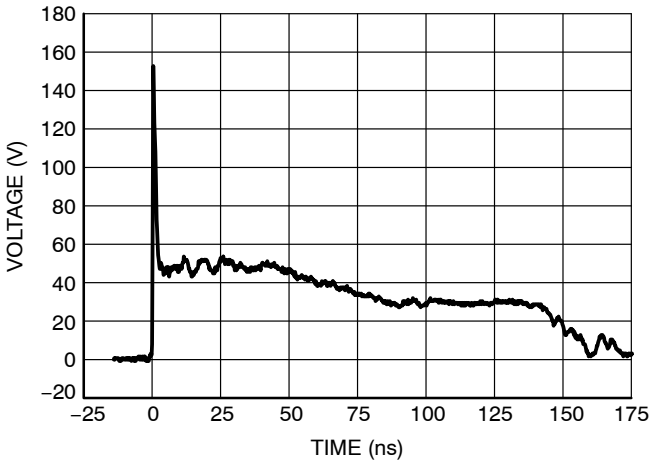



**Figure 7. Typical IEC61000−4−2 +8 kV Contact ESD Clamping Voltage**

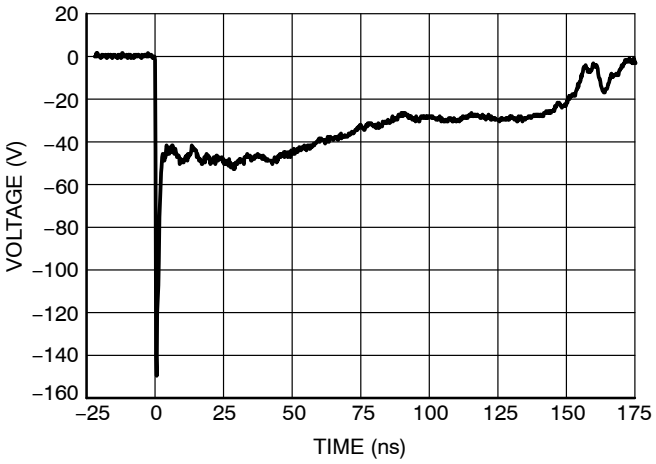



**Figure 8. Typical IEC61000−4−2 −8 kV Contact ESD Clamping Voltage**

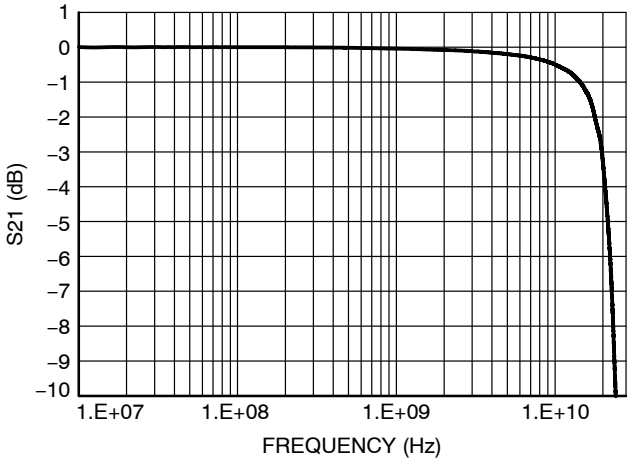



**Figure 9. Typical Insertion Loss**

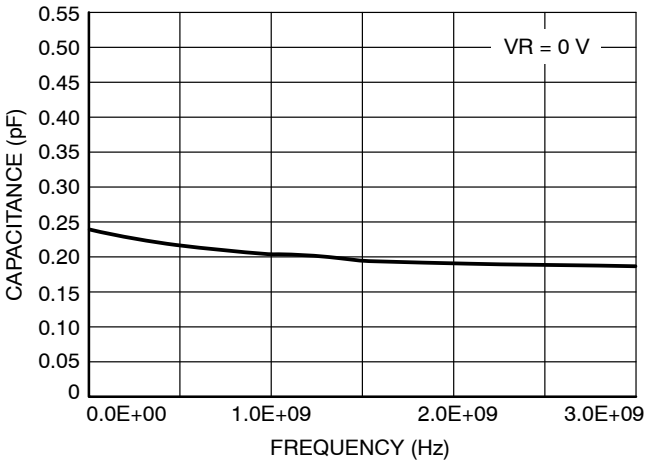



**Figure 10. Typical Capacitance Over Frequency**

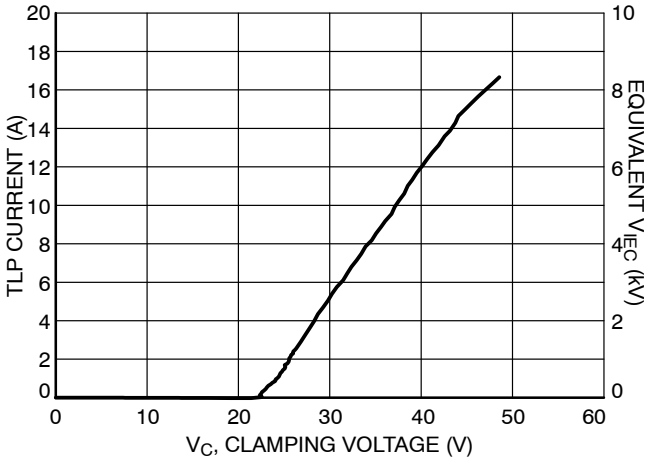



**Figure 11. Typical Positive TLP IV Curve**

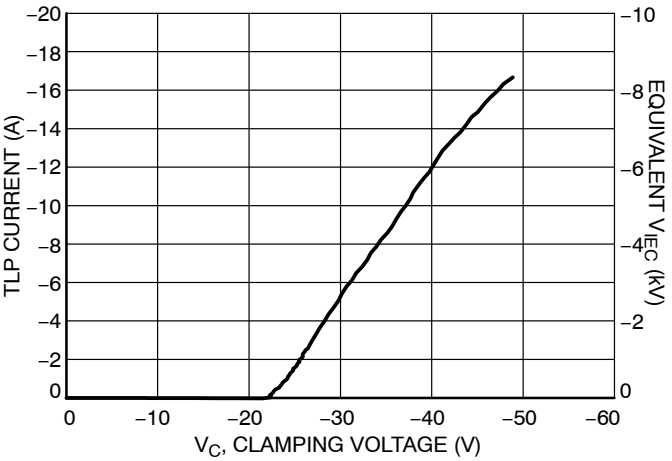



**Figure 12. Typical Negative TLP IV Curve**

NOTE: TLP parameter: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 300 ps, averaging window: $t_1$ = 30 ns to $t_2$ = 60 ns. $V_{IEC}$ is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

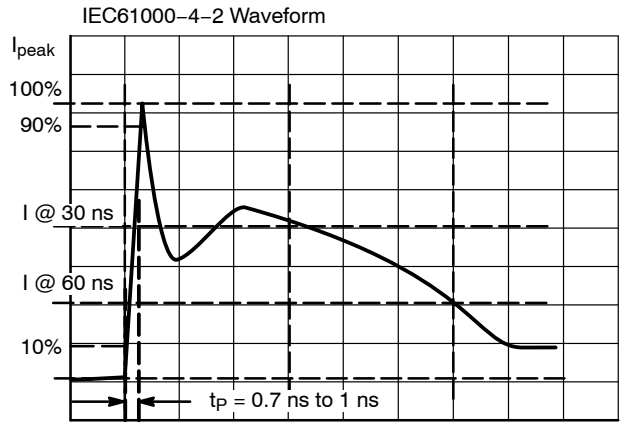



**Figure 13. IEC61000−4−2 Spec**

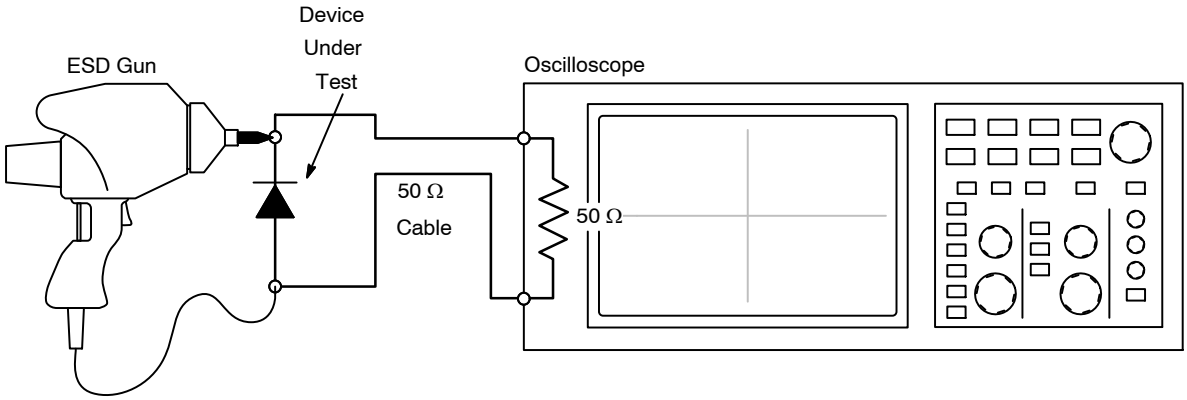



**Figure 14. Diagram of ESD Clamping Voltage Test Setup**

**The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.**

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 15. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 16 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

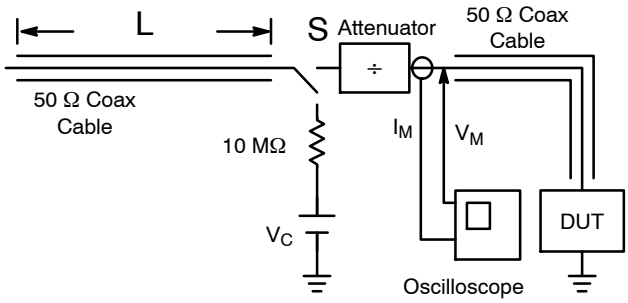



**Figure 15. Simplified Schematic of a Typical TLP System**

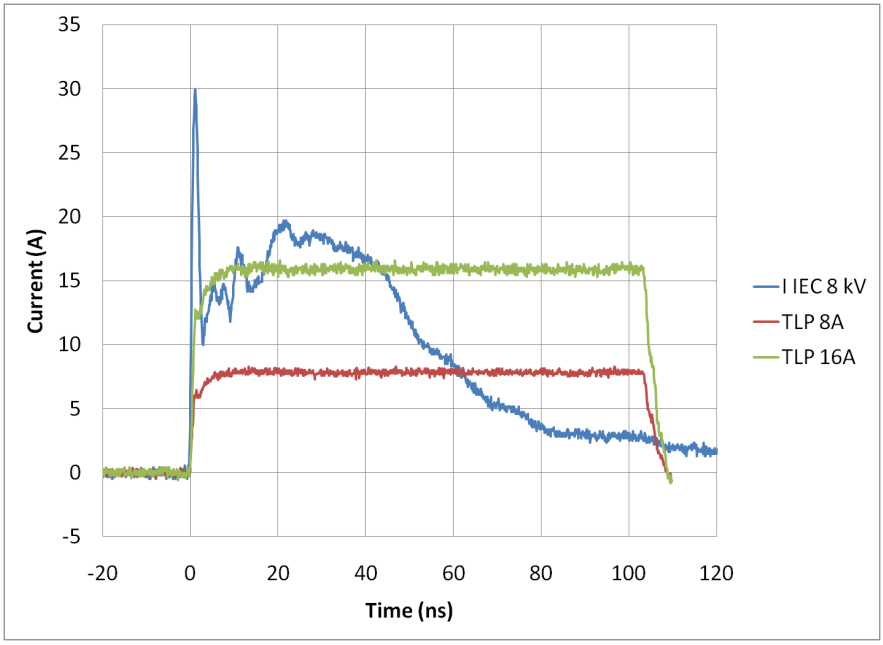
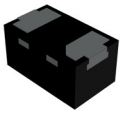


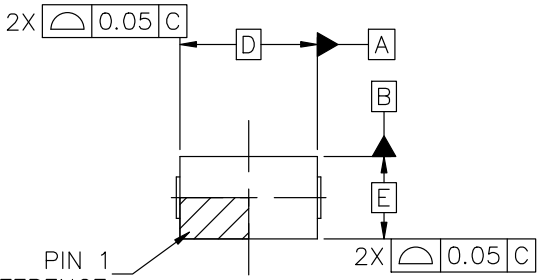

**Figure 16. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

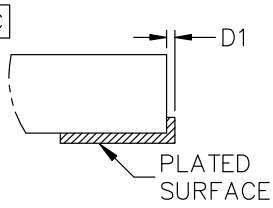


**X2DFNW2 1.00x0.60x0.37, 0.65P**
CASE 711BG
ISSUE D

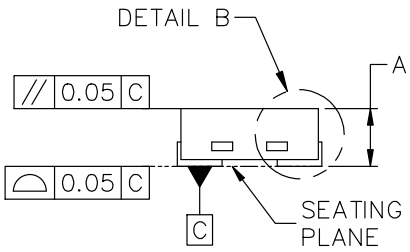
DATE 29 FEB 2024



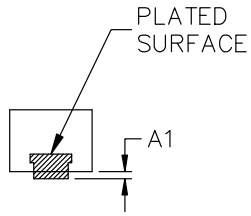

TOP VIEW



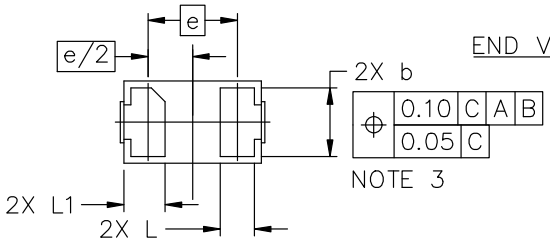

DETAIL "B"
SCALE 2:1




SIDE VIEW




END VIEW

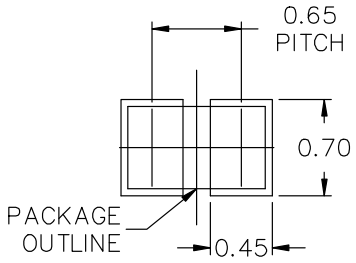



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| A1 | −−− | −−− | 0.05 |
| b | 0.45 | 0.50 | 0.55 |
| D | 1.00 BSC | | |
| D1 | −−− | −−− | 0.05 |
| E | 0.60 BSC | | |
| e | 0.65 BSC | | |
| L | 0.22 REF | | |
| L1 | 0.24 | 0.28 | 0.34 |

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* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***




XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **X2DFNW2 1.00x0.60x0.37, 0.65P** | **PAGE 1 OF 1** |

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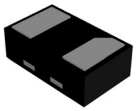
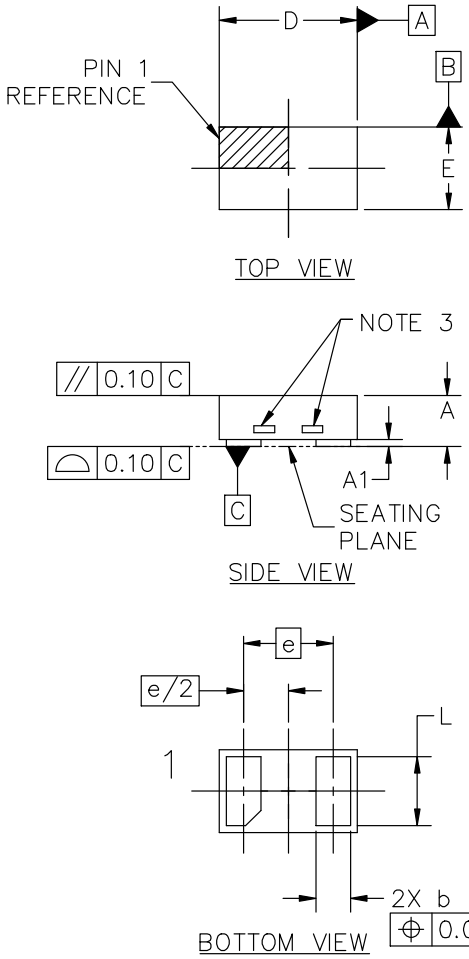


**X2DFN2 1.00x0.60x0.37, 0.65P**
CASE 714AB
ISSUE C

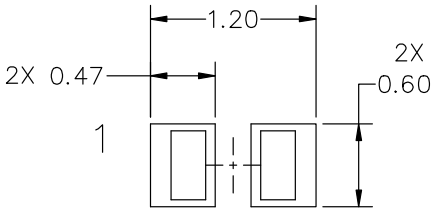
DATE 21 FEB 2024




NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOW.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| A1 | −−− | 0.03 | 0.050 |
| b | 0.20 | 0.25 | 0.30 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.55 | 0.60 | 0.65 |
| e | 0.65 BSC | | |
| L | 0.45 | 0.50 | 0.55 |

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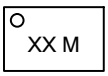
**GENERIC MARKING DIAGRAM***




XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **X2DFN2 1.00x0.60x0.37, 0.65P** | **PAGE 1 OF 1** |

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