3.3 V, 2.5 Gb/s Multi Level Clock/Data Input to CML Receiver/Buffer/Translator

NB4N11M



TSSOP−8
DT SUFFIX
CASE 948R

Description

The NB4N11M is a differential 1−to−2 clock/data distribution/translation chip with CML output structure, targeted for high−speed clock/data applications. The device is functionally equivalent to the EP11, LVEP11, SG11 or 7L11M devices. Device produces two identical differential output copies of clock or data signal operating up to 2.5 GHz or 2.5 Gb/s, respectively. As such, NB4N11M is ideal for SONET, GigE, Fiber Channel, Backplane and other clock/data distribution applications.

Inputs accept LVPECL, CML, LVCMOS, LVTTL, or LVDS (See Table 5). The CML outputs are 16 mA open collector (See Figure 18) which requires resistor (R_L) load path to V_{TT} termination voltage. The open collector CML outputs must be terminated to V_{TT} at power up. Differential outputs produces current−mode logic (CML) compatible levels when receiver loaded with 50 Ω or 25 Ω loads connected to 1.8 V, 2.5 V or 3.3 V supplies (see Figure 19). This simplifies device interface by eliminating a need for coupling capacitors.

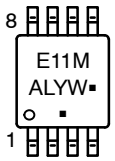
The device is offered in a small 8−pin TSSOP package.

Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency > 2.5 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- Typically 1 ps of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter @ 2.5 Gb/s, R_L = 25 Ω
- 420 ps Typical Propagation Delay
- 150 ps Typical Rise and Fall Times
- Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V and V_{TT} = 1.8 V to 3.6 V
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

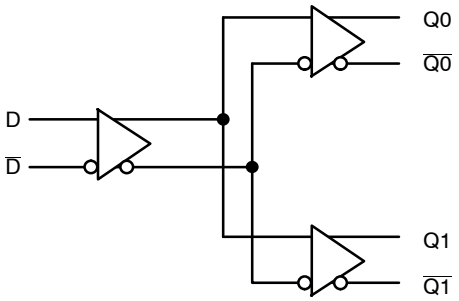


Figure 1. Functional Block Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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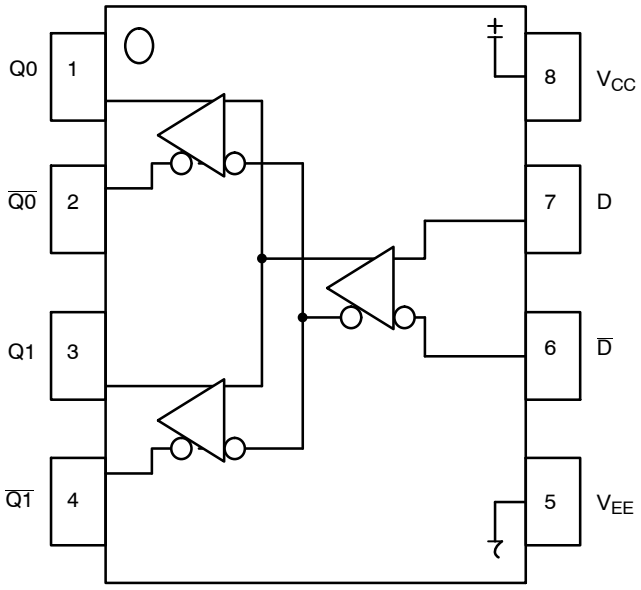


Figure 2. Pinout (Top View) and Logic Diagram

Table 1. Pin Description

Pin	Name	I/O	Description
1	Q0	CML Output	Noninverted differential output. Typically receiver terminated with 50 Ω resistor to V_{TT}. Open collector CML outputs must be terminated to V_{TT} at powerup.
2	$\overline{Q0}$	CML Output	Inverted differential output. Typically receiver terminated with 50 Ω resistor to V_{TT}. Open collector CML outputs must be terminated to V_{TT} at powerup.
3	Q1	CML Output	Noninverted differential output. Typically receiver terminated with 50 Ω resistor to V_{TT}. Open collector CML outputs must be terminated to V_{TT} at powerup.
4	$\overline{Q1}$	CML Output	Inverted differential output. Typically receiver terminated with 50 Ω resistor to V_{TT}. Open collector CML outputs must be terminated to V_{TT} at powerup.
5	V_{EE}	–	Negative supply voltage.
6	$\overline{D}$	LVPECL, CML, HSTL, LVCMOS, LVDS, LVTTL Input	Inverted differential input.
7	D	LVPECL, CML, HSTL, LVCMOS, LVDS, LVTTL Input	Noninverted differential input.
8	V_{CC}	–	Positive supply voltage.

Table 2. ATTRIBUTES

Characteristics	Value
ESD Protection Human Body Model Machine Model	 > 1000 V > 70 V
Moisture Sensitivity (Note 1) 8−TSSOP	 Level 3
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V−0 @ 0.125 in
Transistor Count	197
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	V_{EE} = −0.5 V		4	V
V_{EE}	Negative Power Supply	V_{CC} = +0.5 V		−4	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	V_I = V_{CC} +0.4 V V_I = V_{EE} −0.4 V	4 −4	V V
V_O	Output Voltage Minimum Maximum			V_{EE} + 600 V_{CC} + 400	mV mV
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 2)	0 lfpm 500 lfpm	TSSOP−8 TSSOP−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	1S2P (Note 2)	TSSOP−8	41 to 44	°C/W
T_{sol}	Wave Solder	< 3 Sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board − 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS, CLOCK Inputs, CML Outputs V_{CC} = 3.0 V to 3.6 V, V_{EE} = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open)		25	35	mA
R_L = 50 Ω, V_{TT} = 3.6 V to 2.5 V					
V_{OH}	Output HIGH Voltage (Note 3)	V_{TT} − 60	V_{TT} − 10	V_{TT}	mV
V_{OL}	Output LOW Voltage (Note 3)	V_{TT} − 1100	V_{TT} − 800	V_{TT} − 640	mV
$\|V_{OD}\|$	Differential Output Voltage Magnitude	640	780	1000	mV
R_L = 25 Ω, V_{TT} = 3.6 V to 2.5 V ±5%					
V_{OH}	Output HIGH Voltage (Note 3)	V_{TT} − 60	V_{TT} − 10	V_{TT}	mV
V_{OL}	Output LOW Voltage (Note 3)	V_{TT} − 550	V_{TT} − 400	V_{TT} − 320	mV
$\|V_{OD}\|$	Differential Output Voltage Magnitude	320	390	500	mV
R_L = 50 Ω, V_{TT} = 1.8 V ±5%					
V_{OH}	Output HIGH Voltage (Note 3)	V_{TT} − 170	V_{TT} − 10	V_{TT}	mV
V_{OL}	Output LOW Voltage (Note 3)	V_{TT} − 1100	V_{TT} − 800	V_{TT} − 640	mV
$\|V_{OD}\|$	Differential Output Voltage Magnitude	570	780	1000	mV
R_L = 25 Ω, V_{TT} = 1.8 V ±5%					
V_{OH}	Output HIGH Voltage (Note 3)	V_{TT} − 85	V_{TT} − 10	V_{TT}	mV
V_{OL}	Output LOW Voltage (Note 3)	V_{TT} − 500	V_{TT} − 400	V_{TT} − 320	mV
$\|V_{OD}\|$	Differential Output Voltage Magnitude	285	390	500	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 14 and 16)					
V_{th}	Input Threshold Reference Voltage Range (Note 5)	V_{EE}		V_{CC}	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC} + 400	mV
V_{IL}	Single−ended Input LOW Voltage	V_{EE} − 400		V_{th} − 100	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 15 and 17)					
V_{IHD}	Differential Input HIGH Voltage	V_{EE}		V_{CC} + 400	mV
V_{ILD}	Differential Input LOW Voltage	V_{EE} − 400		V_{CC} − 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	V_{EE}		V_{CC}	mV
$\|V_{ID}\|$	Differential Input Voltage Magnitude ($\|V_{IHD} - V_{ILD}\|$) (Note 7)	100		$V_{CC} - V_{EE}$	mV
C_{IN}	Input Capacitance (Note 7)		1.5		pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. CML outputs require R_L receiver termination resistors to V_{TT} for proper operation. Outputs must be connected through R_L to V_{TT} at power up. The output parameters vary 1:1 with V_{TT}.
4. Input parameters vary 1:1 with V_{CC}.
5. V_{th} is applied to the complementary input when operating in single−ended mode.
6. V_{CMR} (MIN) varies 1:1 with V_{EE}, V_{CMR} max varies 1:1 with V_{CC}.
7. Parameter guaranteed by design and evaluation but not tested in production.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, V_{EE} = 0 V; (Note 8)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (R_L = 50 Ω)										mV
	$f_{in} \le$ 1 GHz	550	660		550	660		550	660		
	(See Figure 12) $f_{in} \le$ 1.5 GHz	400	640		400	640		400	640		
	$f_{in} \le$ 2.5GHz	150	400		150	400		150	400		
V_{OUTPP}	Output Voltage Amplitude (R_L = 25 Ω)										mV
	$f_{in} \le$ 1 GHz	280	370		280	370		280	370		
	(See Figure 12) $f_{in} \le$ 1.5 GHz	280	360		280	360		280	360		
	$f_{in} \le$ 2.5GHz	100	300		100	400		100	400		
f_{DATA}	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential @ 0.5 GHz	300	420	600	300	420	600	300	420	600	ps
t_{SKEW}	Duty Cycle Skew (Note 9)		2	20		2	20		2	20	ps
	Within Device Skew		5	25		5	25		5	25	
	Device to Device Skew (Note 13)		20	100		20	100		20	100	
t_{JITTER}	RMS Random Clock Jitter R_L = 50 Ω and										ps
	R_L = 25 Ω (Note 11) f_{in} = 750 MHz		1	3		1	3		1	3	
	f_{in} = 1.5 GHz		1	3		1	3		1	3	
	f_{in} = 2.5 GHz		1	3		1	3		1	3	
	Peak–to–Peak Data Dependent Jitter R_L = 50 Ω										
	f_{DATA} = 1.5 Gb/s		15	55		15	55		15	55	
	(Note 12) f_{DATA} = 2.5 Gb/s		20	85		20	85		20	85	
	Peak–to–Peak Data Dependent Jitter R_L = 25 Ω										
	f_{DATA} = 1.5 Gb/s		5	35		5	35		5	35	
	(Note 12) f_{DATA} = 2.5 Gb/s		10	35		10	35		10	35	
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)	100			100			100			mV
t_r t_f	Output Rise/Fall Times @ 0.5 GHz (20% – 80%) Q, $\overline{Q}$		150	300		150	300		150	300	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. All output loaded with an external R_L = 50 Ω and R_L = 25 Ω to V_{TT}. Outputs must be connected through R_L to V_{TT} at power up. Input edge rates 150 ps (20% – 80%).
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 0.5 GHz.
10. V_{INPP} (MAX) cannot exceed V_{CC} – V_{EE}. Input voltage swing is a single–ended measurement operating in differential mode.
11. Additive RMS jitter with 50% duty cycle clock signal.
12. Additive peak–to–peak data dependent jitter with input NRZ data signal (PRBS 2^{23}–1).
13. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.

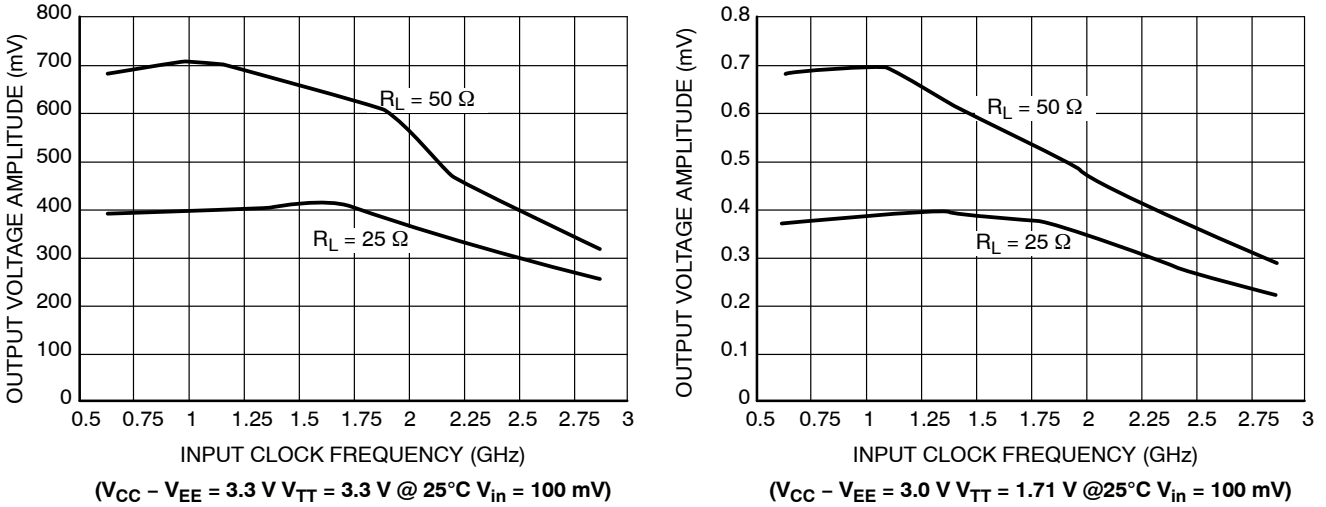


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{IN}) at Ambient Temperature (Typical)

NB4N11M

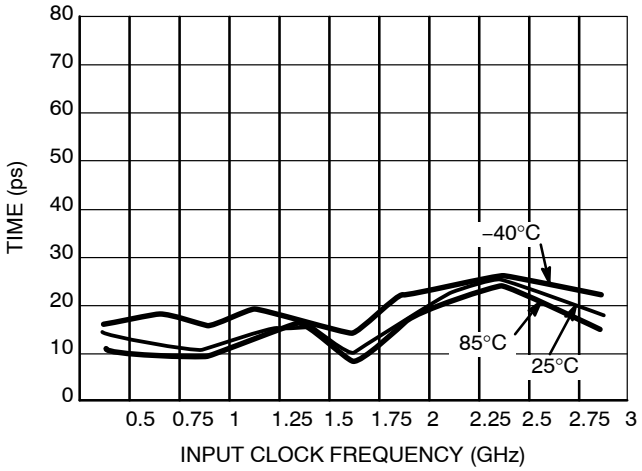


Figure 4. Data Dependent Jitter vs. Frequency and Temperature (V_{CC} − V_{EE} = 3.3 V; V_{TT} = 3.3 V @ 25°C; V_{IN} = 100 mV; PRBS 2^{23}−1; R_L = 50 Ω)

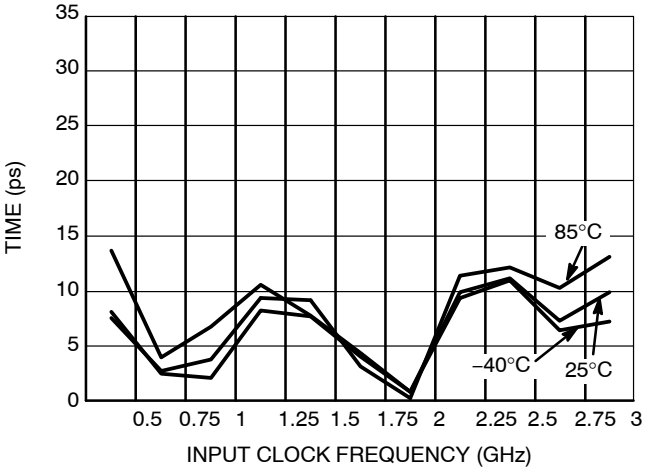


Figure 5. Data Dependent Jitter vs. Frequency and Temperature (V_{CC} − V_{EE} = 3.3 V; V_{TT} = 3.3 V @ 25°C; V_{IN} = 100 mV; PRBS 2^{23}−1; R_L = 25 Ω)

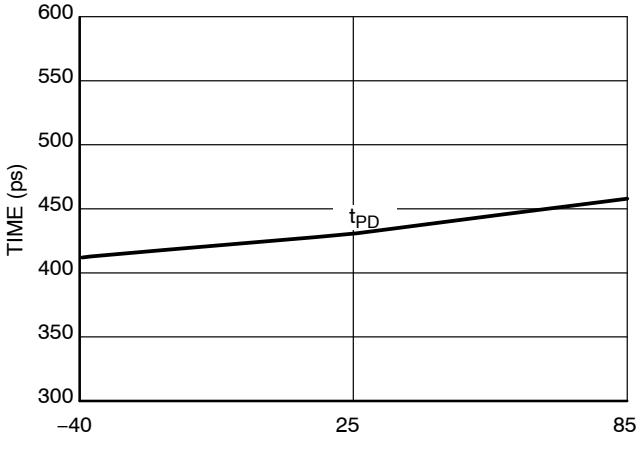


Figure 6. Typical Propagation Delay vs. Temperature (V_{CC} − V_{EE} = 3.3 V; V_{TT} = 3.3 V @ 25°C; V_{in} = 100 mV; R_L = 50 Ω)

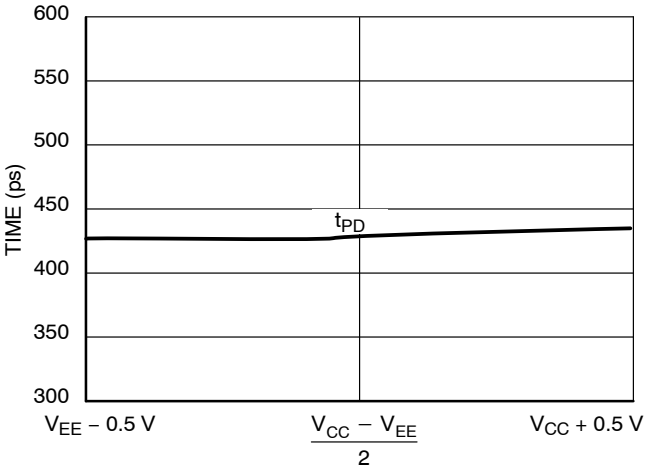


Figure 7. Typical Propagation Delay vs. Input Offset Voltage (V_{CC} − V_{EE} = 3.3 V; V_{TT} = 3.3 V @ 25°C; V_{in} = 100 mV R_L = 50 Ω)

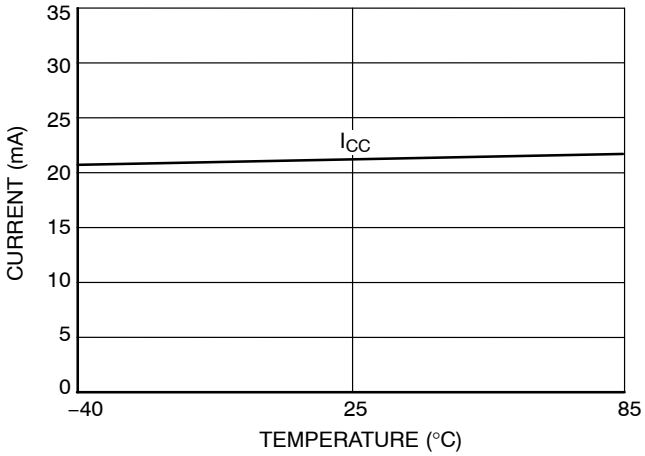


Figure 8. Supply Current vs. Temperature

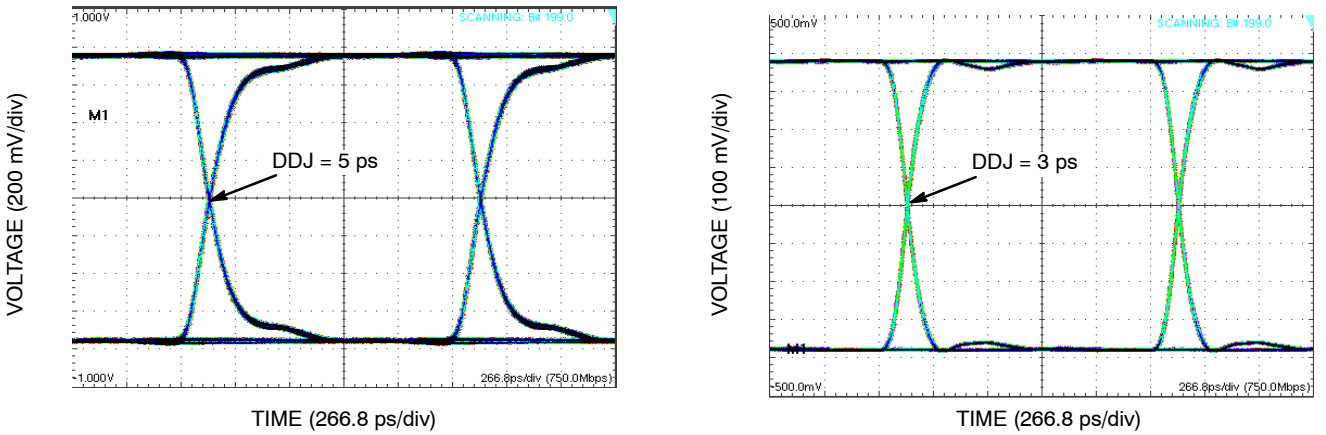


Figure 9. Typical Differential Output Waveform at 750 Mb/s
(R_L = 50 Ω Left Plot, R_L = 25 Ω Right Plot, V_{in} = 100 mV, System DDJ = 24 ps)

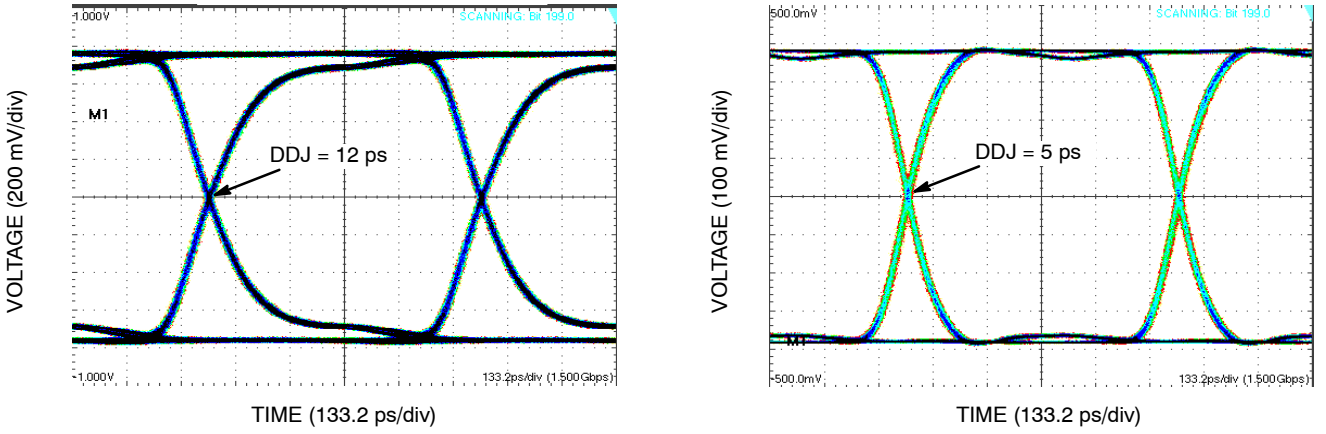


Figure 10. Typical Differential Output Waveform 1.5 Gb/s
(R_L = 50 Ω Left Plot, R_L = 25 Ω Right Plot, V_{in} = 100 mV, System DDJ = 25 ps)

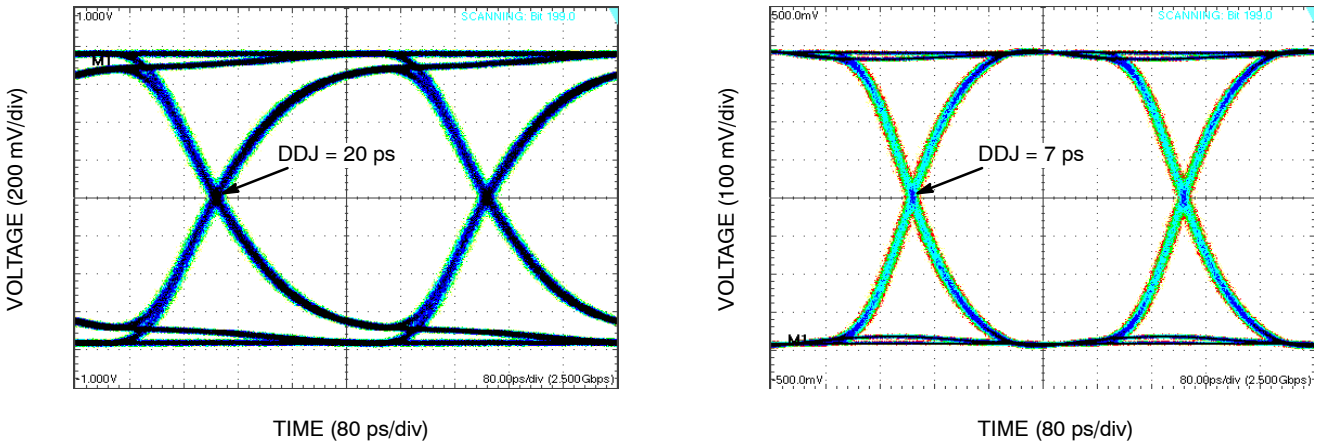


Figure 11. Typical Differential Output Waveform 2.5 Gb/s
(R_L = 50 Ω Left Plot, R_L = 25 Ω Right Plot, V_{in} = 100 mV, System DDJ = 24 ps)

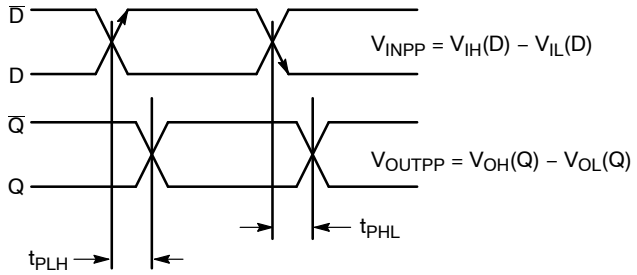


Figure 12. AC Reference Measurement

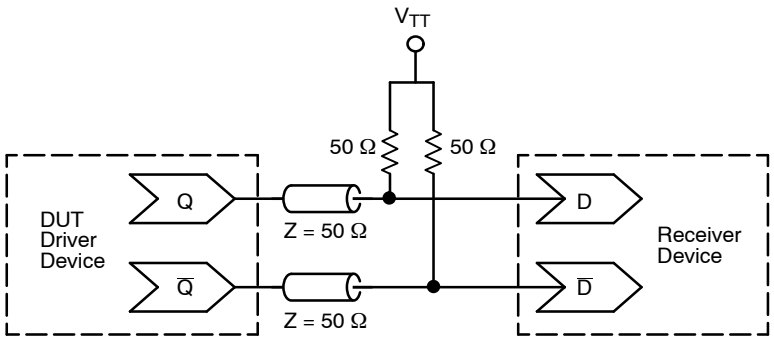


Figure 13. Typical Termination for Output Driver and Device Evaluation

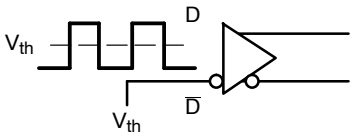


Figure 14. Differential Input Driven Single−Ended

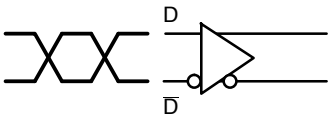


Figure 15. Differential Inputs Driven Differentially

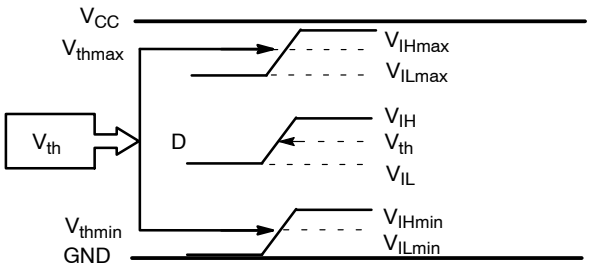


Figure 16. V_{th} Diagram

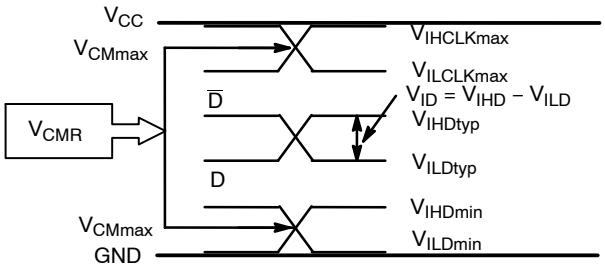


Figure 17. V_{CMR} Diagram

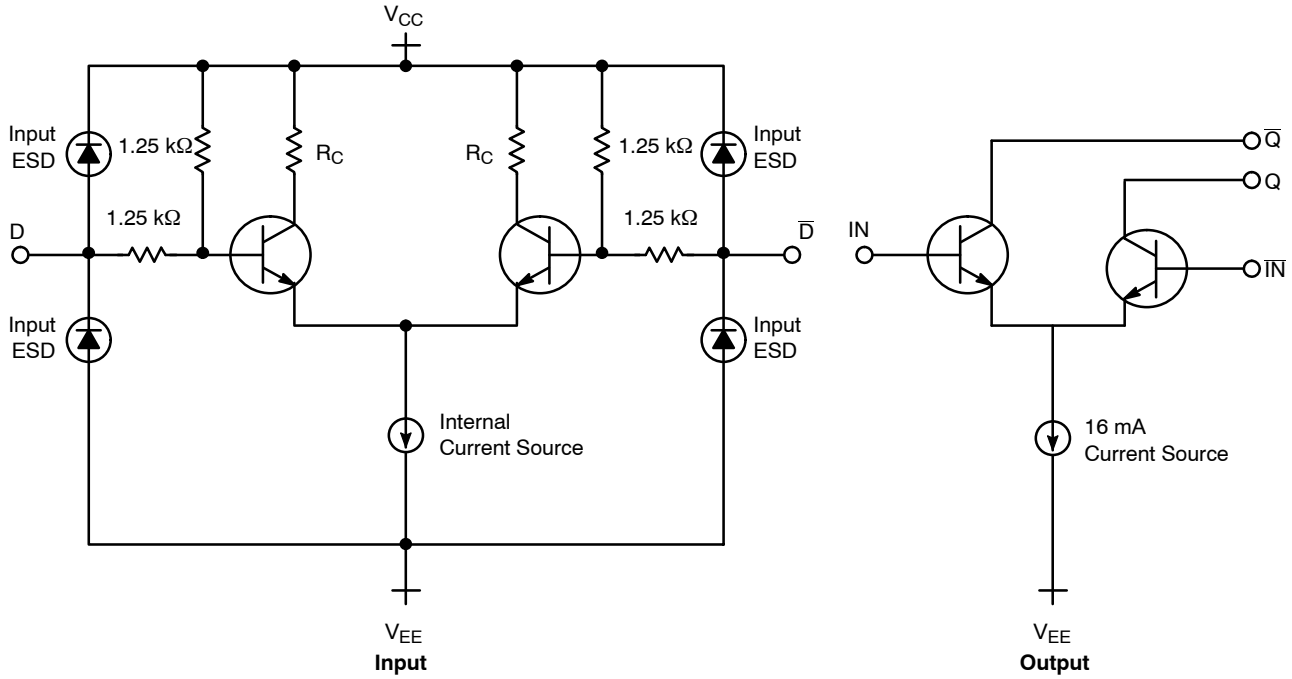


Figure 18. CML Input and Output Structure

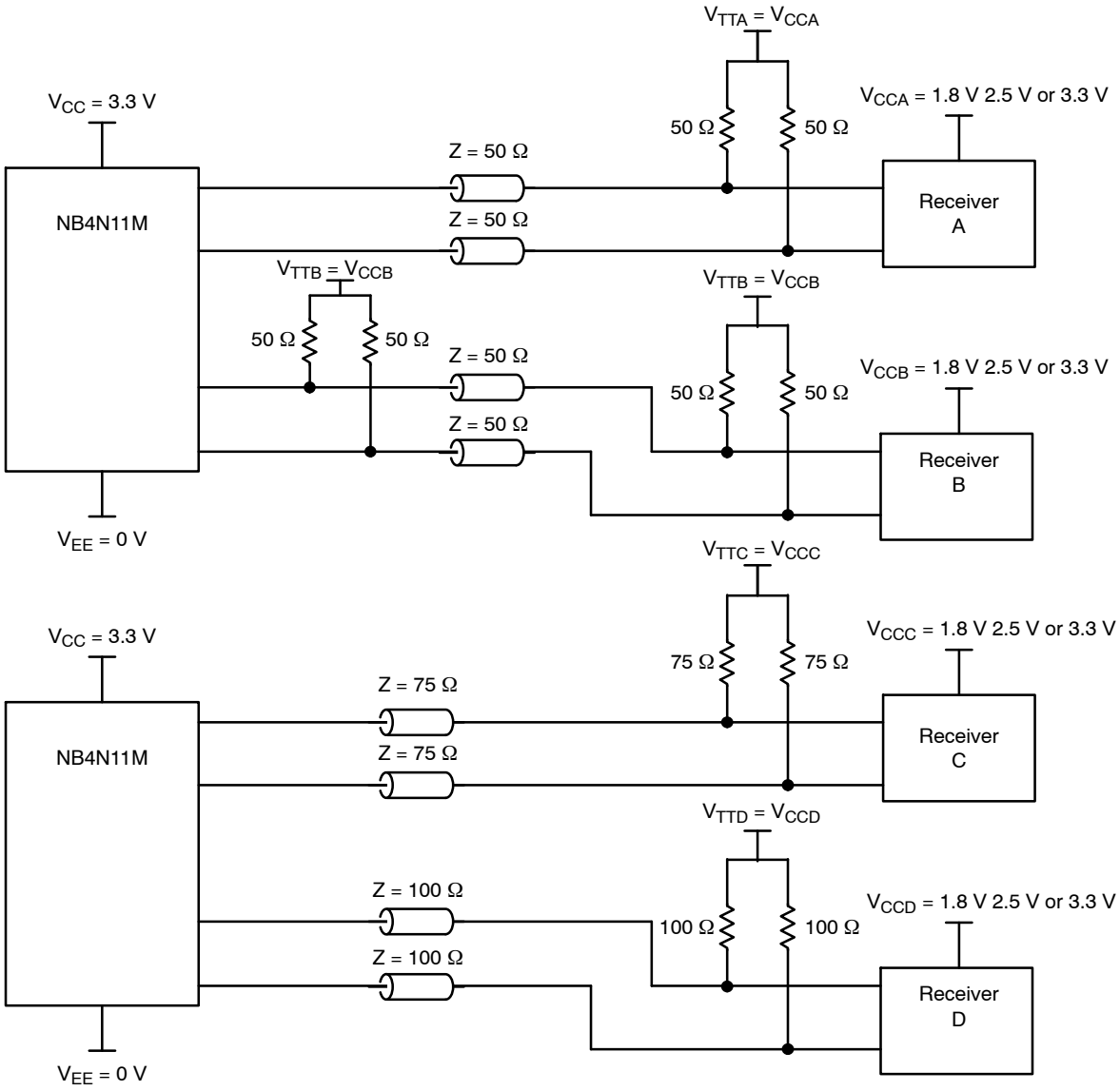


Figure 19. Typical Examples of the Application Interface

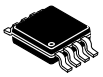
ORDERING INFORMATION

Device	Package	Shipping†
NB4N11MDTR2G	TSSOP−8 (Pb−Free)	2500 / Tape & Reel

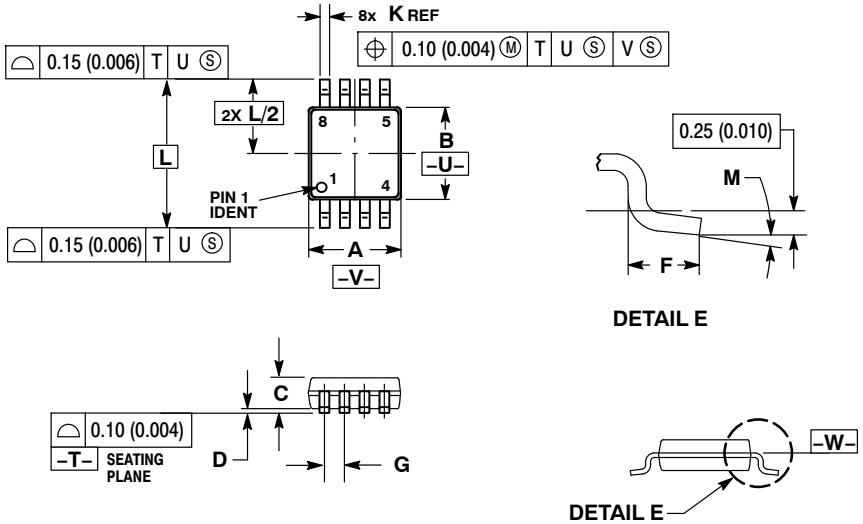
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TSSOP 8
CASE 948R–02
ISSUE A

DATE 04/07/2000



SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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