MPQ4316A

45V, 6A, Low-I_Q, Synchronous Step-Down Converter with Frequency Spread Spectrum, AEC-Q100 Qualified

DESCRIPTION

The MPQ4316A is a configurable-frequency, synchronous, step-down switching converter with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). The device provides up to 6A of highly efficient output current (I_{OUT}) with current mode control for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A low 1.7µA quiescent current (I_Q) in shutdown mode allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation.

A high duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4316A is available in a QFN-20 (4mmx4mm) package, and is AEC-Q100 qualified.

FEATURES

- Designed for Automotive Applications:
  - Wide 3.3V to 45V Operating Input Voltage (V_{IN}) Range
  - 6A Continuous Output Current (I_{OUT})
  - 100ns Minimum On Time (t_{ON_MIN})
  - Junction Temperature (T_J) Operation from -40°C to +150°C
- Increases Battery Life:
  - 1.7µA Low Shutdown Supply Current
  - 18µA Sleep Mode Quiescent Current
  - AAM Mode Increases Efficiency under Light Loads
- High Performance for Improved Thermals:
  - Internal 48mΩ HS-FET and 20mΩ LS-FET
- Optimized for EMC and EMI:
  - 350kHz to 1000kHz Configurable f_{SW} for Car Battery Applications
  - Synchronize to External Clock
  - Out-of-Phase Synchronized Clock Output
  - FSS Modulation
  - Symmetric VIN Pinout
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Power Good (PG) Output
  - External Soft Start (SS)
  - Selectable AAM Mode or FCCM
  - Low-Dropout Mode
  - Hiccup Over-Current Protection (OCP)
  - Available in a QFN-20 (4mmx4mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

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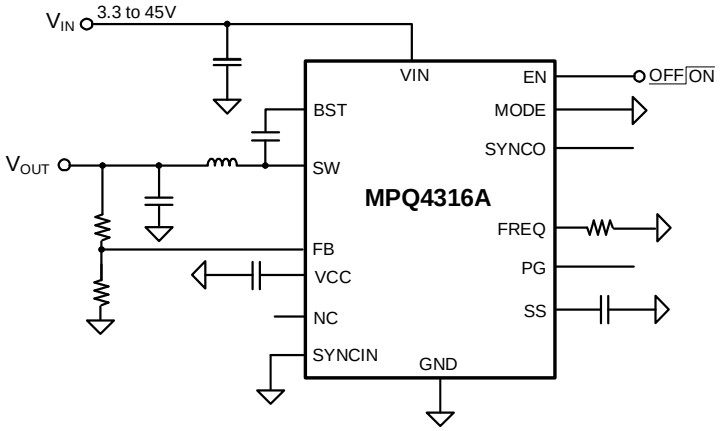
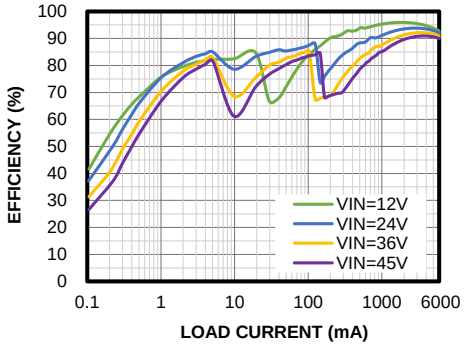
TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7µH (DCR = 15mΩ), AAM mode



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4316AGRE-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4316AGRE-AEC1-Z).

** Moisture Sensitivity Level Rating

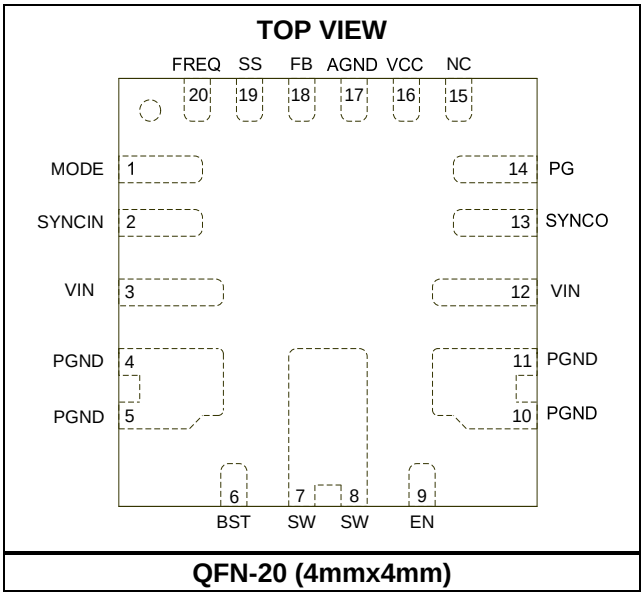
*** Wettable Flank

TOP MARKING

MPSYWW
M4316A
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
M4316A: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**Advanced asynchronous modulation (AAM) mode or forced continuous conduction mode (FCCM) selection pin.** Pull this pin high to force the device to operate in FCCM; pull it low to force the device to operate in AAM mode under light loads. Do not float this pin.
2	SYNCIN	**SYNC input.** Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. SYNCIN has an internal high impedance. Do not float SYNCIN. If using SYNCIN, ensure that the external sync clock has adequate pull-up and pull-down capability. It is recommended to place a ≤51kΩ resistor between SYNCIN and ground if the external sync clock's pull-down capability is not sufficient, or if SYNCIN enters a high-impedance (Hi-Z) state.
3, 12	VIN	**Input supply.** This pin supplies power to all the internal control circuitry, as well as the power switch connected to SW. To minimize switching spikes, it is recommended to connect a decoupling capacitor from VIN to ground, placed as close to VIN as possible.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap (BST).** This pin is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between the BST and SW pins. To calculate the capacitor size, see the Selecting the External Bootstrap (BST) Diode and Resistor section on page 32.
7, 8	SW	**Switch node.** This pin is the internal power MOSFET's output.
9	EN	**Enable.** Pull this pin below the specified threshold (0.85V) to shut down the chip; pull EN above the specified threshold (1V) to enable the chip.
13	SYNCO	**SYNC output.** The SYNCO pin outputs a clock signal that is 180° out of phase with the internal oscillator signal. SYNCO can also output a signal that is opposite to the clock signal applied at SYNCIN. If not being used, float SYNCO.
14	PG	**Power good indicator.** This pin's output is an open drain. Connect PG to a power source using a pull-up resistor. PG goes high if the output voltage (V_{OUT}) is within 95% to 105% of the nominal voltage. PG goes low if V_{OUT} is above 106.5% or below 93% of the nominal voltage.
15	NC	**Not connected.** If not being used, float this pin.
16	VCC	**Bias supply.** The VCC pin supplies 4.9V to power the internal control circuit and gate drivers. Connect a decoupling capacitor from VCC to ground, and placed close to VCC. To calculate the capacitor size, see the Selecting the VCC Capacitor (C_{VCC}) section on page 33.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** To set V_{OUT}, connect the FB pin to the center point between the external resistor divider from the output and AGND. The feedback threshold voltage (V_{FB}) is about 0.815V. Place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
19	SS	**Soft-start (SS) input.** Place a capacitor from the SS pin to ground to set the SS time (t_{SS}). The MPQ4316A sources 13µA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the feedback voltage (V_{FB}) increases to limit the inrush current during start-up.
20	FREQ	**Switching frequency (f_{SW}) configuration.** Connect a resistor from the FREQ pin to ground to set f_{SW}. See the f_{SW} vs. R_{FREQ} curves on page 15 to set the frequency.

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ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .....-0.3V to +50V
SW ..... -0.3V to $V_{IN(MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
All other pins .....-0.3V to + 5.5V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-20 (4mmx4mm) 5.4W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (3)
Charged device model (CDM) ..... Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN}) .....3.3V to 45V
Output voltage (V_{OUT}).....0.815V to 0.95 x V_{IN}
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)			
JESD51-7	44	9	°C/W (5)
EVQ4316A-R-00A	23	2.5	°C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on JESD51-7, a 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The θ_{JC} value shows the thermal resistance from the junction-to-case bottom.
6) Measured on a standard EVB: a 4-layer, 2oz copper thickness PCB (9cmx9cm). The θ_{JC} value shows the thermal resistance from the junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$		2.5	2.7	2.9	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
V_{IN} quiescent current	I_Q	FB = 0.85V, no load, sleep mode		18	26	µA
V_{IN} switching quiescent current (7)	$I_{Q_SWITCHING}$	MODE = GND (AAM mode), switching, no load, R_{FB_UP} = 1MΩ, R_{FB_DOWN} = 324kΩ		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
V_{IN} shutdown current	I_{SHDN}	EN=0V		1.7	3.5	µA
FB reference voltage	V_{FB}	V_{IN} = 3.3V to 45V, T_J = 25°C	0.807	0.815	0.823	V
		V_{IN} = 3.3V to 45V	0.799	0.815	0.831	V
FB current	I_{FB}	V_{FB} = 0.85V	-50	0	+50	nA
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (7)	t_{ON_MIN}			100		ns
Minimum off time (7)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		Deg
High-side (HS) current limit	I_{LIMIT_HS}	Duty cycle = 30%	10	13	16	A
Low-side (LS) valley current limit	I_{LIMIT_VALLEY}		8	10	12	A
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	-0.15	0.1	+0.35	A
LS reverse current limit	$I_{LIMIT_REVERSE}$	FCCM	2	4.5	7	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST} - V_{SW} = 5V		48	80	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	8	13	19	µA
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			190		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising	92	95	98	% of V_{REF}
		V_{FB} falling	102	105	108	
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling	90.5	93.5	96.5	
		V_{FB} rising	103.5	106.5	109.5	
PG low output voltage	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	$t_{PG_R_DELAY}$			35		µs
PG falling deglitch time	$t_{PG_F_DELAY}$			35		µs
Thermal shutdown (7)	T_{SD}			170		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C

Note:

7) Derived from bench characterization. Not tested in production.

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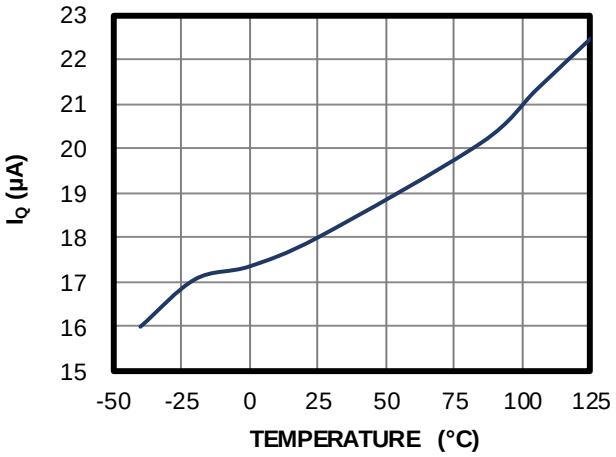
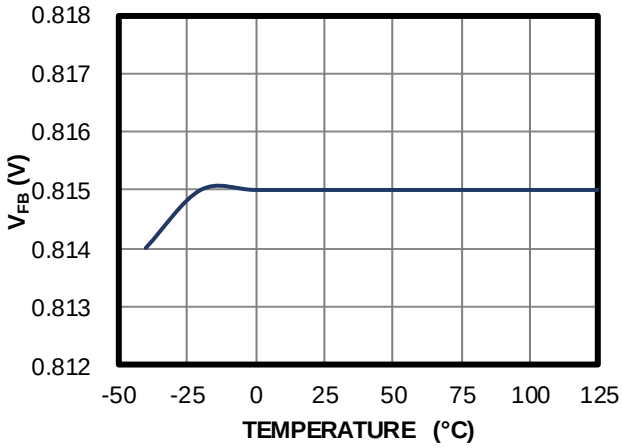
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

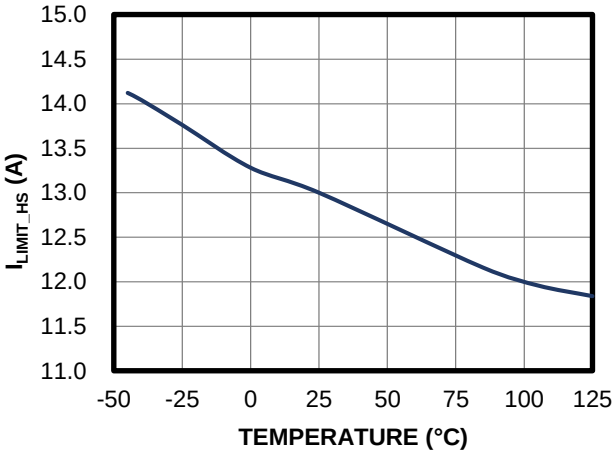
V_{IN} Quiescent Current vs. Temperature



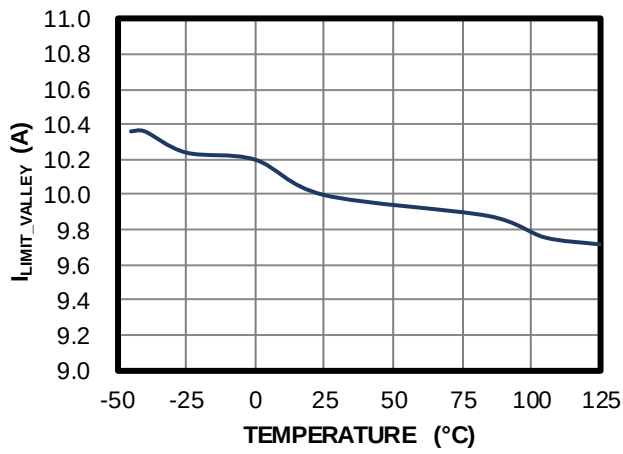
FB Voltage vs. Temperature



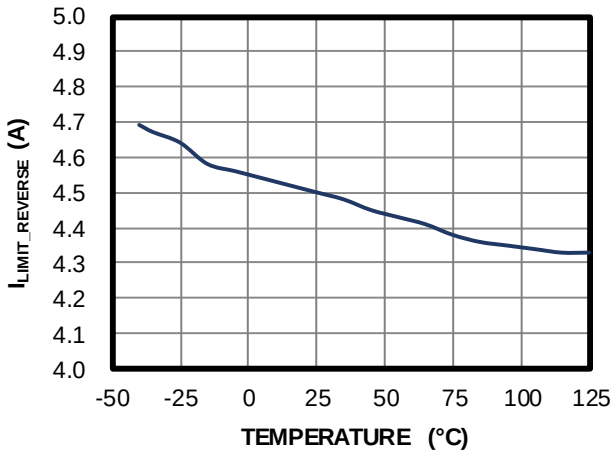
HS Current Limit vs. Temperature



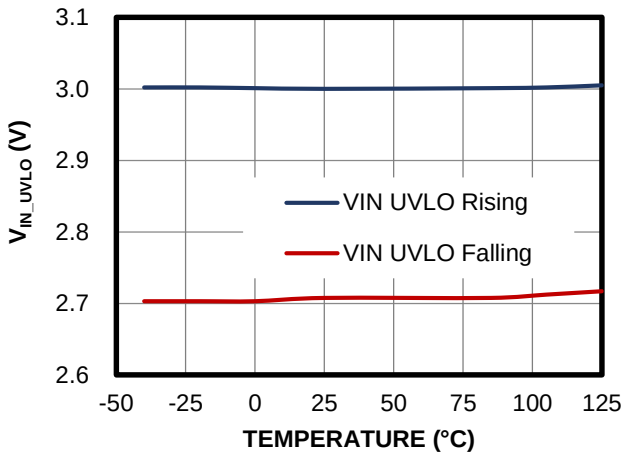
LS Valley Current Limit vs. Temperature



LS Reverse Current Limit vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



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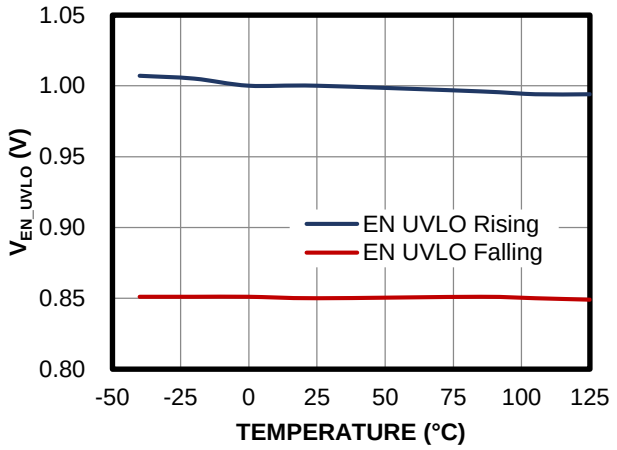
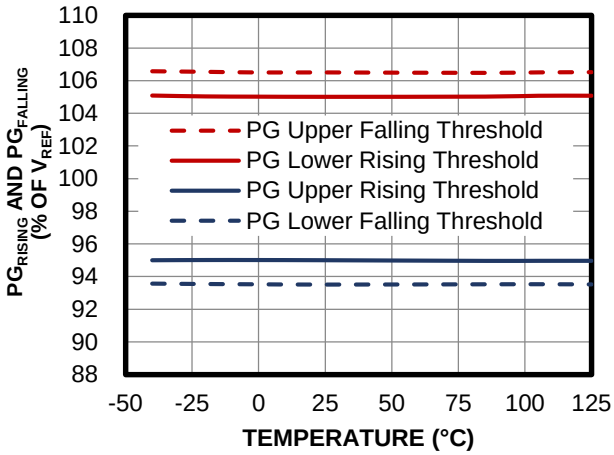
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

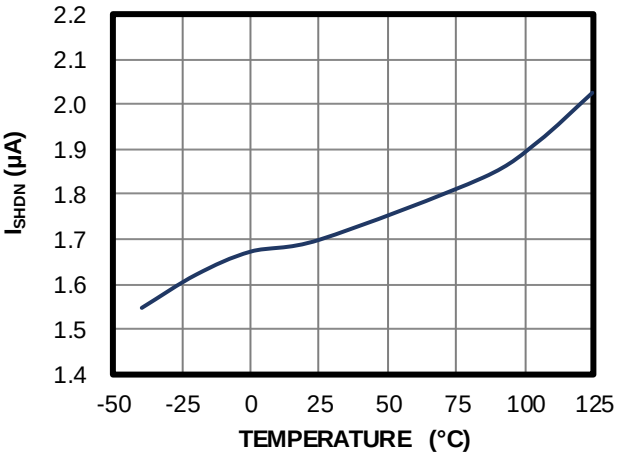
EN UVLO Threshold vs. Temperature



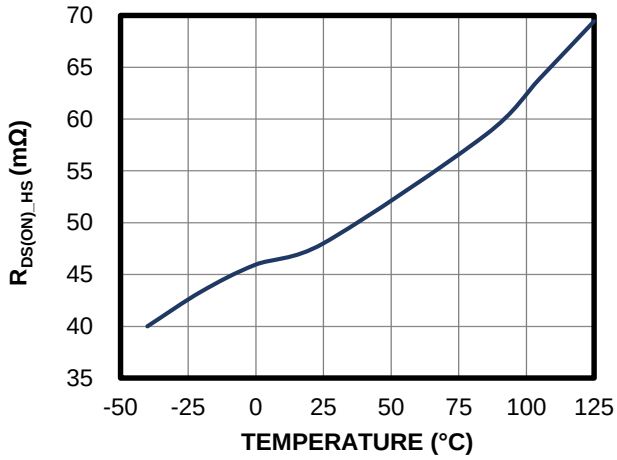
PG Rising and Falling Threshold vs. Temperature



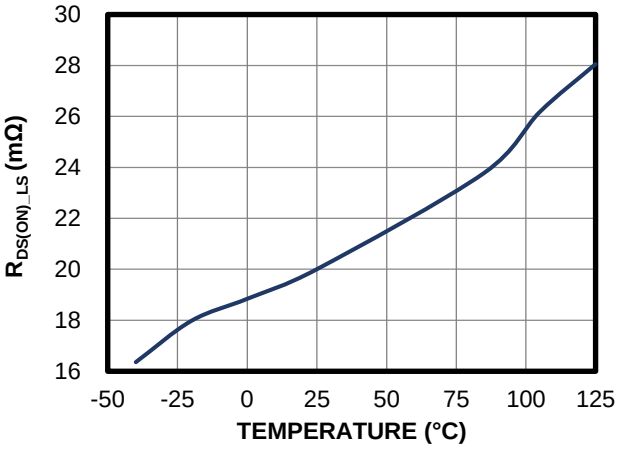
V_{IN} Shutdown Current vs. Temperature



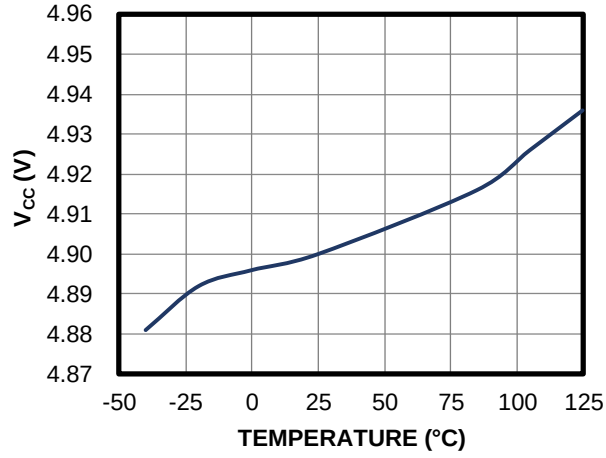
HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature



V_{CC} vs. Temperature



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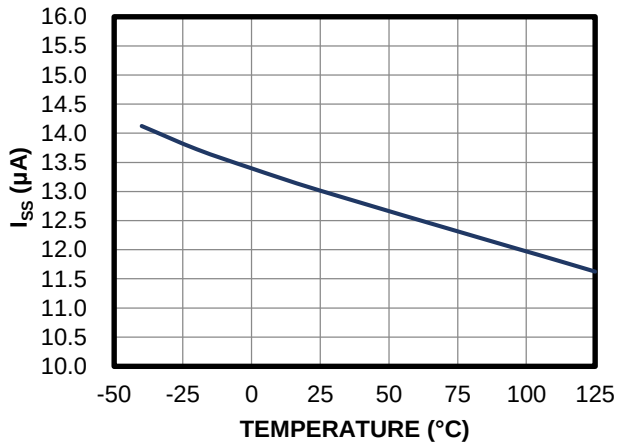
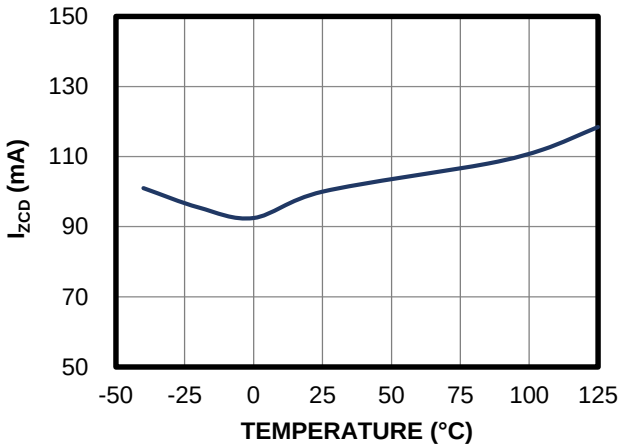
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Soft-Start Current vs. Temperature

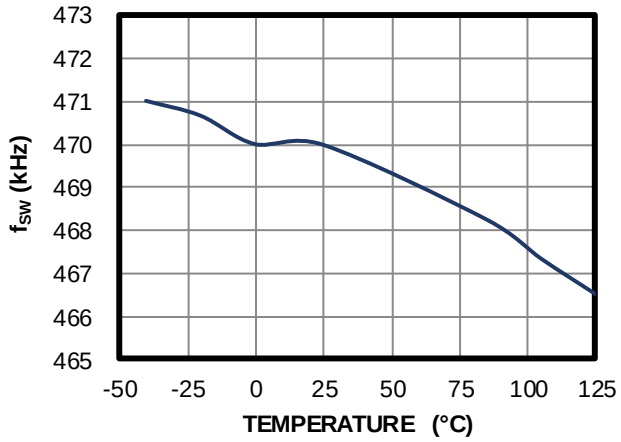


ZCD Current vs. Temperature



Switching Frequency vs. Temperature

R_{FREQ} = 62kΩ



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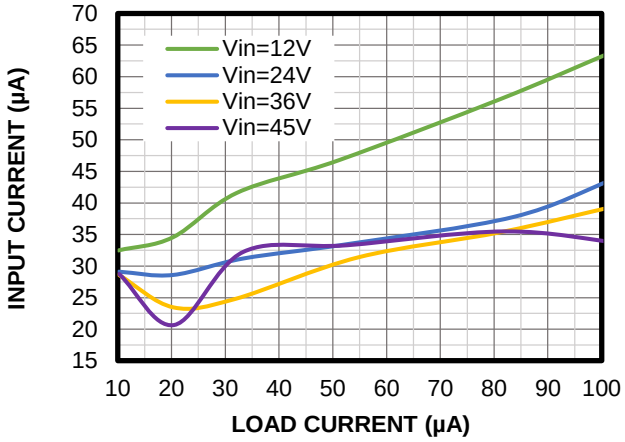
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

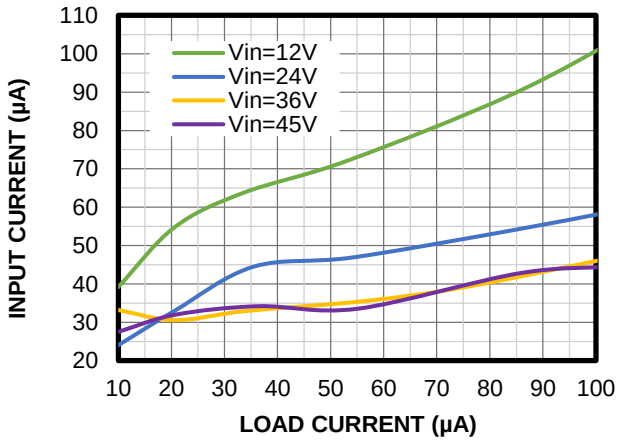
Input Current vs. Load Current

AAM mode, V_{OUT} = 3.3V



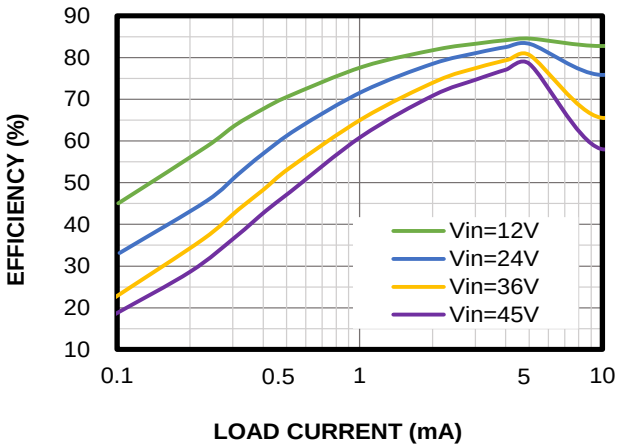
Input Current vs. Load Current

AAM mode, V_{OUT} = 5V



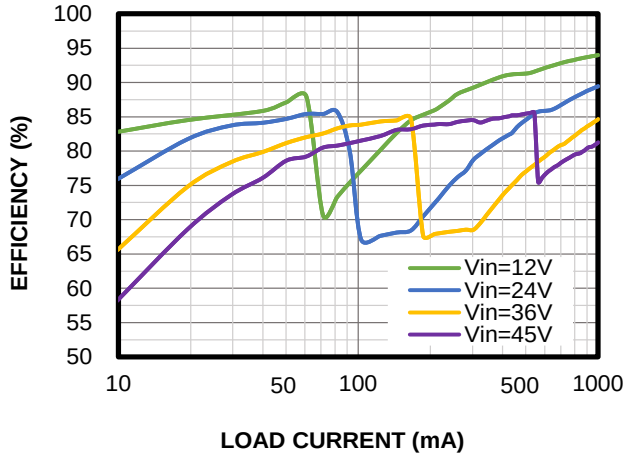
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



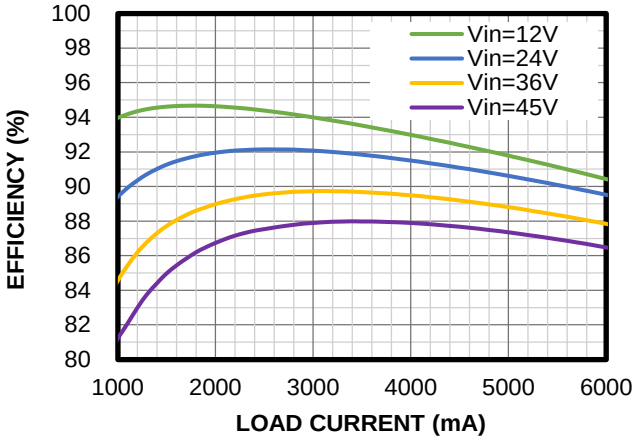
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



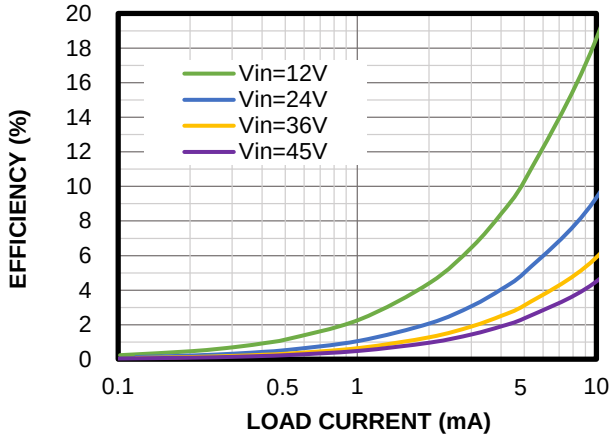
Efficiency vs. Load Current

AAM mode, V_{OUT} = 3.3V



Efficiency vs. Load Current

FCCM, V_{OUT} = 3.3V



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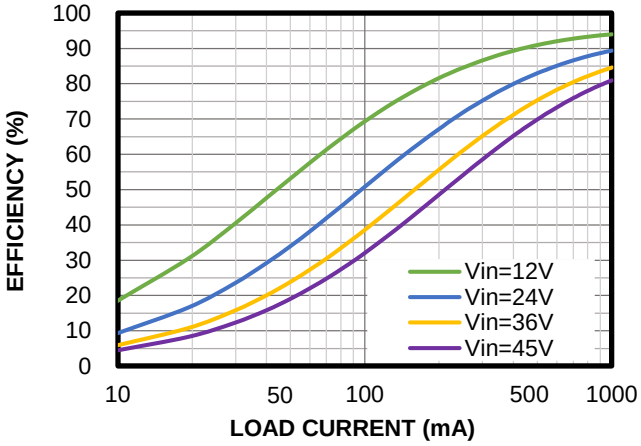
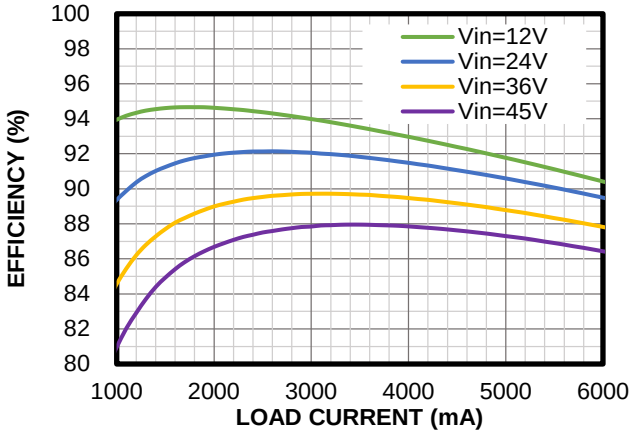
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (8), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

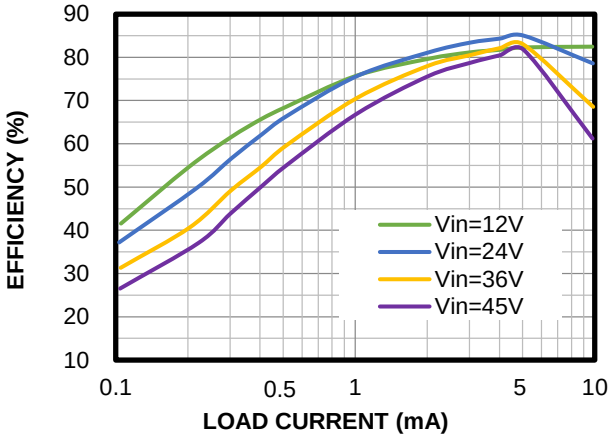
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



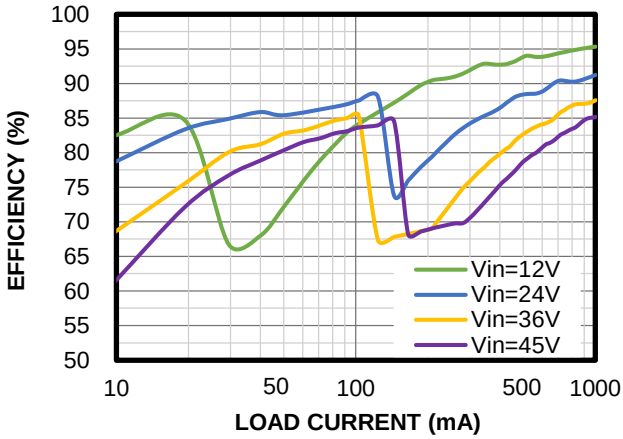
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



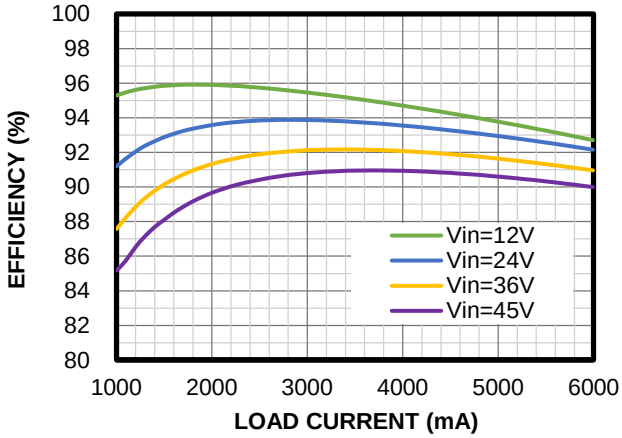
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



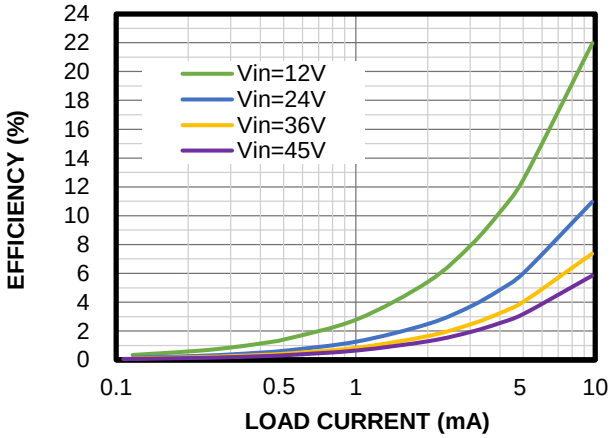
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V



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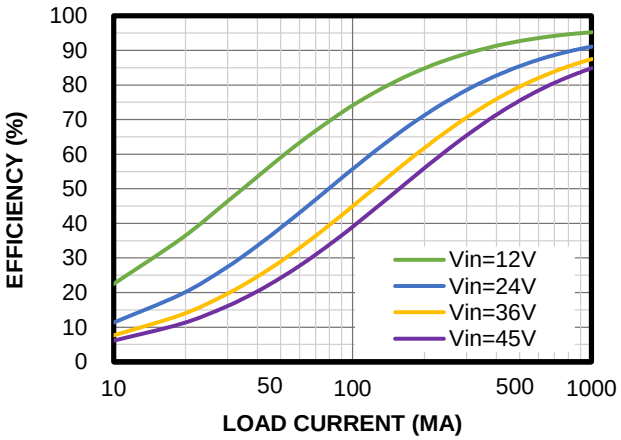
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

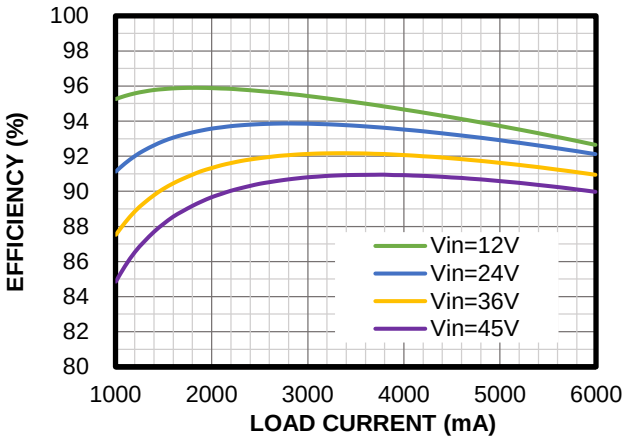
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



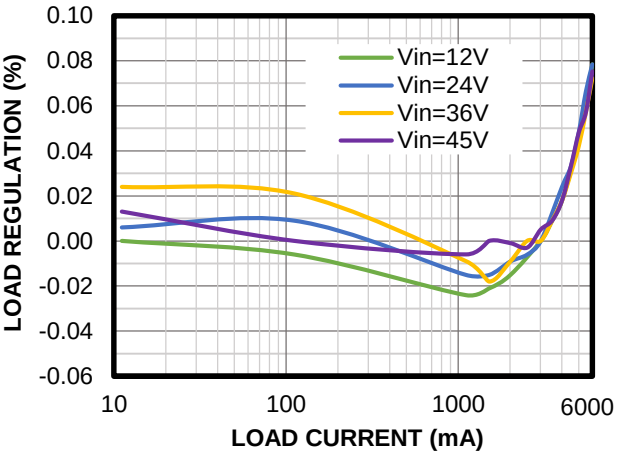
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



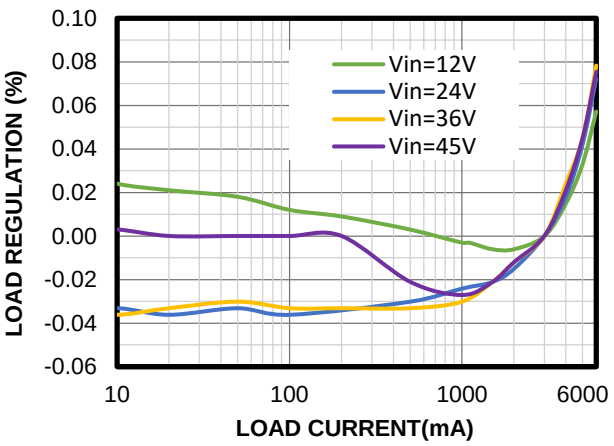
Load Regulation

AAM mode, V_{OUT} = 3.3V



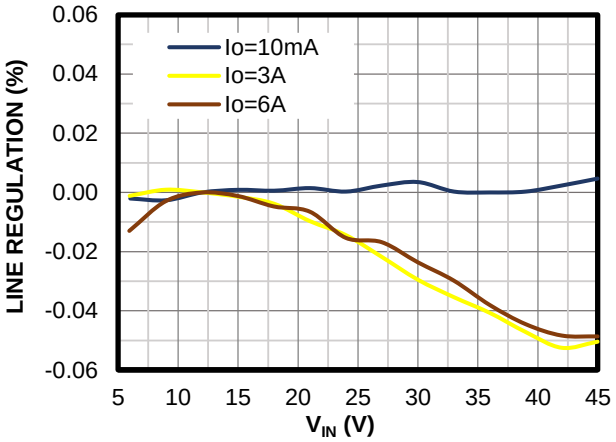
Load Regulation

FCCM, V_{OUT} = 3.3V



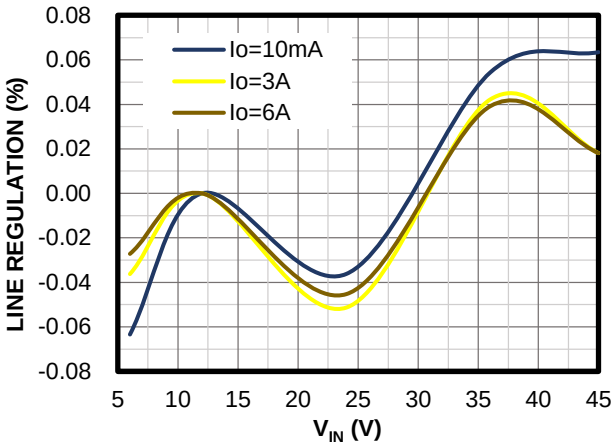
Line Regulation

AAM mode, V_{OUT} = 3.3V



Line Regulation

FCCM, V_{OUT} = 3.3V



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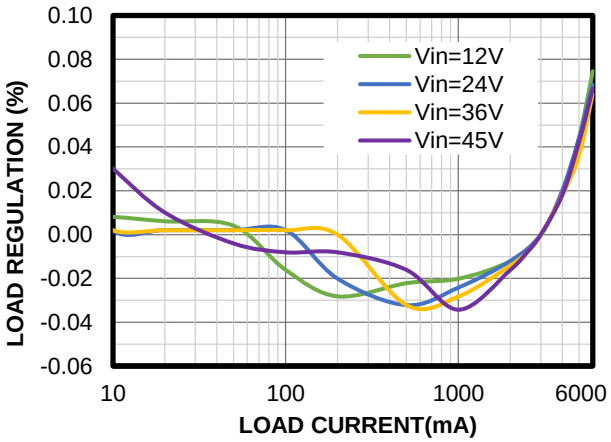
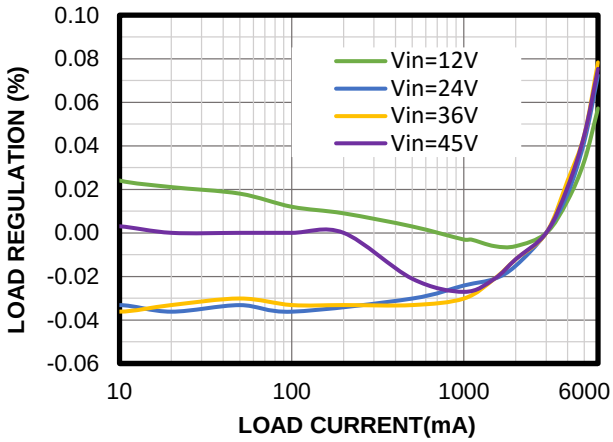
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [8], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

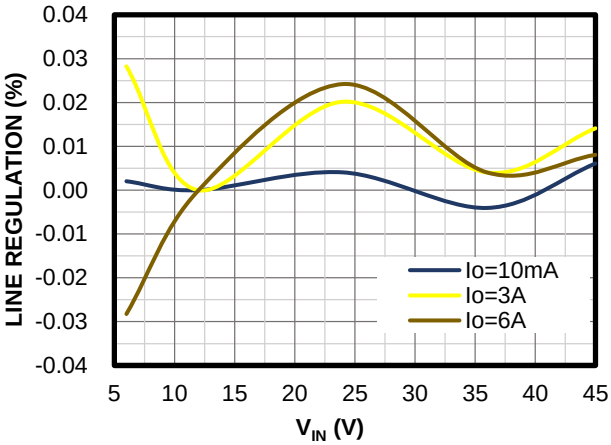
Load Regulation
AAM mode, V_{OUT} = 5V



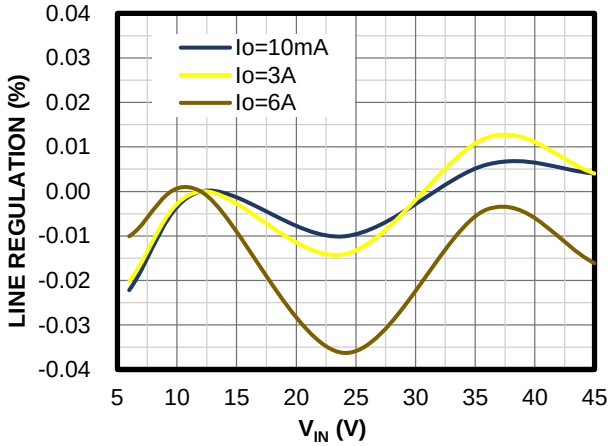
Load Regulation
FCCM, V_{OUT} = 5V



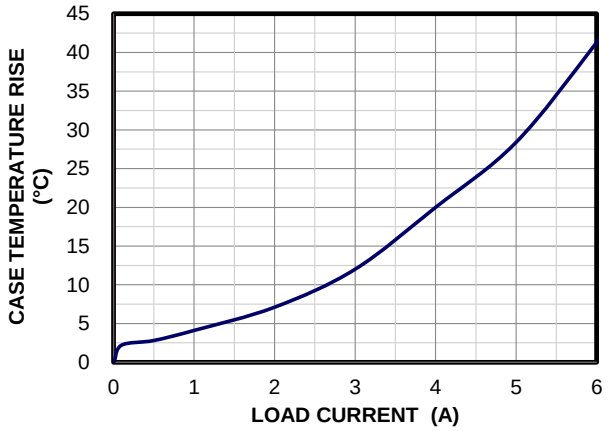
Line Regulation
AAM mode, V_{OUT} = 5V



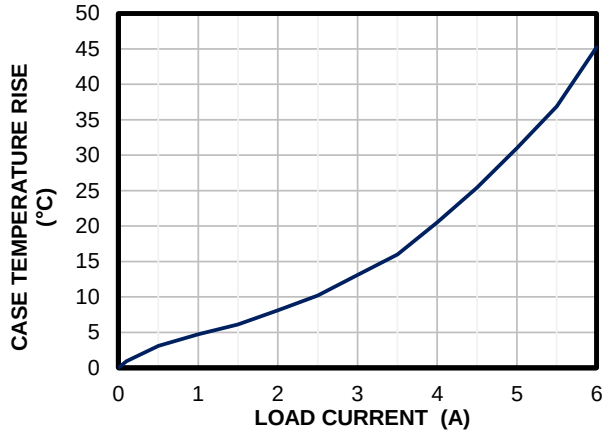
Line Regulation
FCCM, V_{OUT} = 5V



Case Temperature Rise
V_{OUT} = 3.3V



Case Temperature Rise
V_{OUT} = 5V



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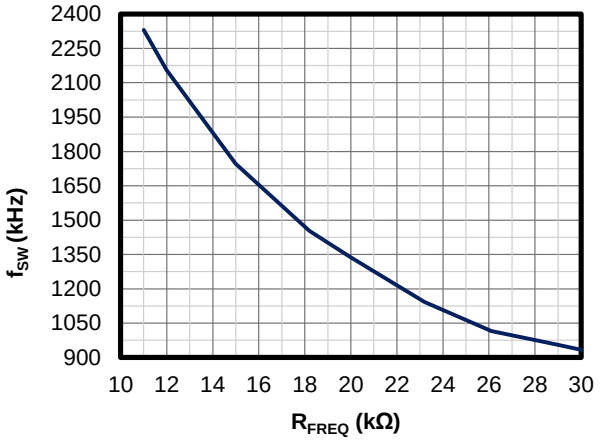
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (8), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

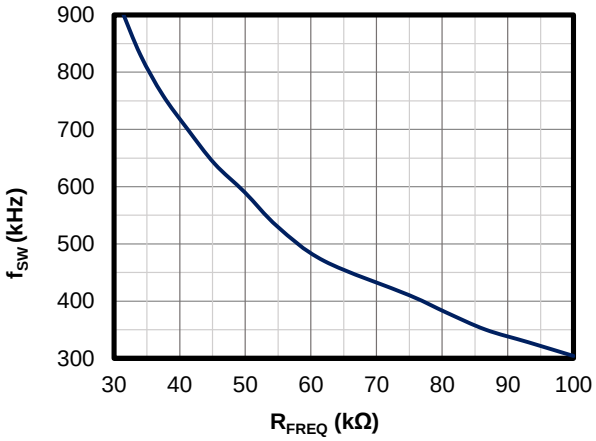
f_{SW} vs. R_{FREQ}

R_{FREQ} = 10kΩ to 30kΩ

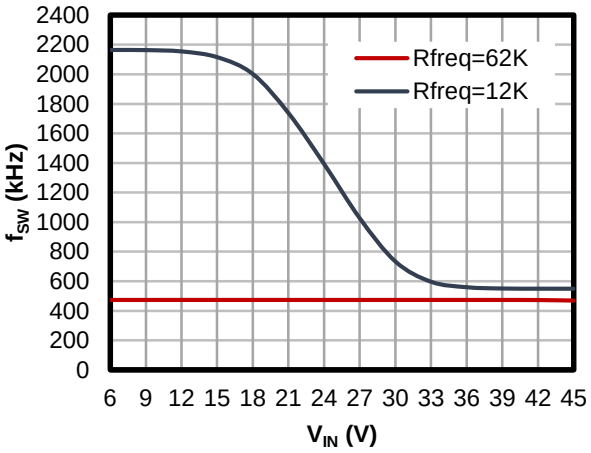


f_{SW} vs. R_{FREQ}

R_{FREQ} = 30kΩ to 100kΩ

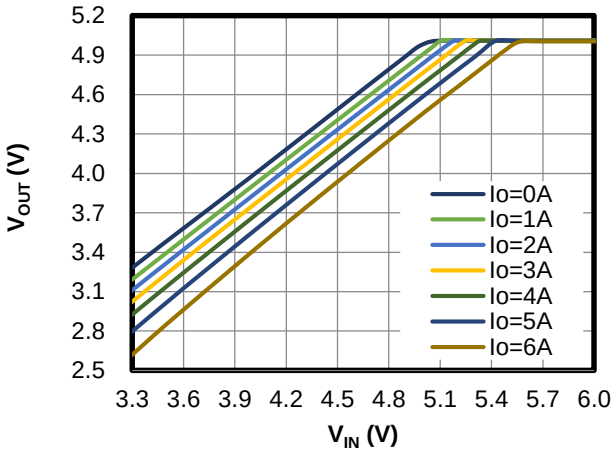


f_{SW} vs. V_{IN}



Low-Dropout Mode

V_{OUT} = 5V



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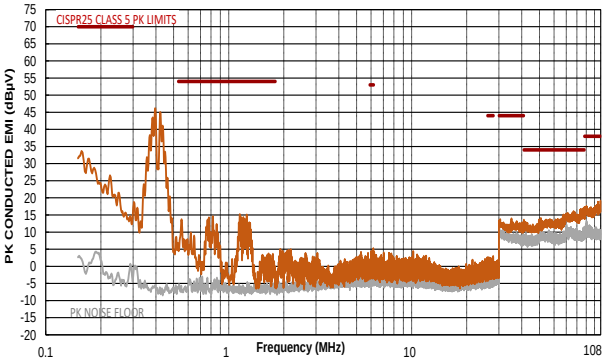
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH [8], f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. [9]

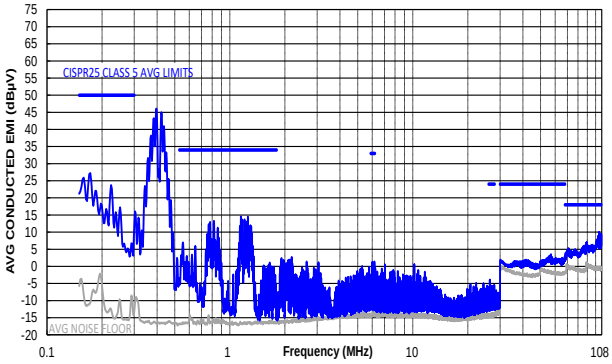
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



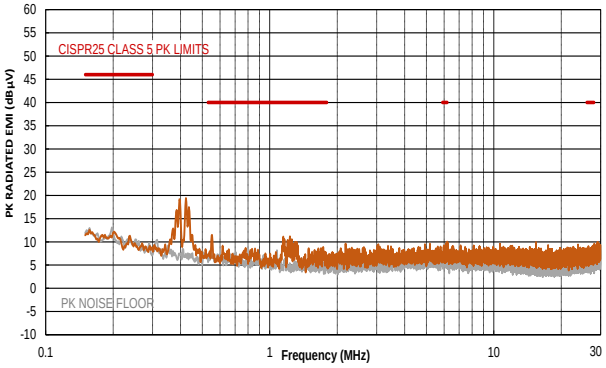
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



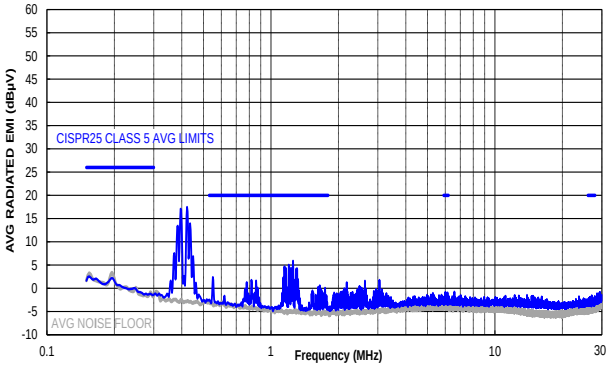
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



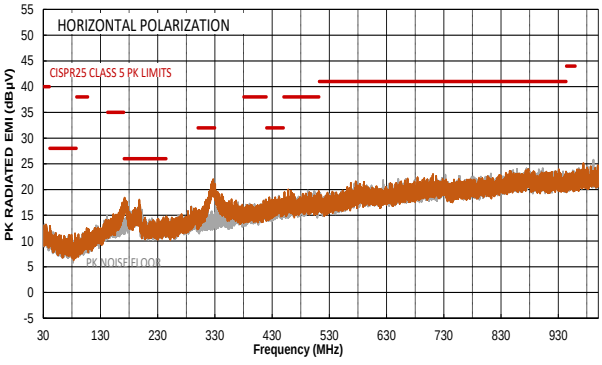
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



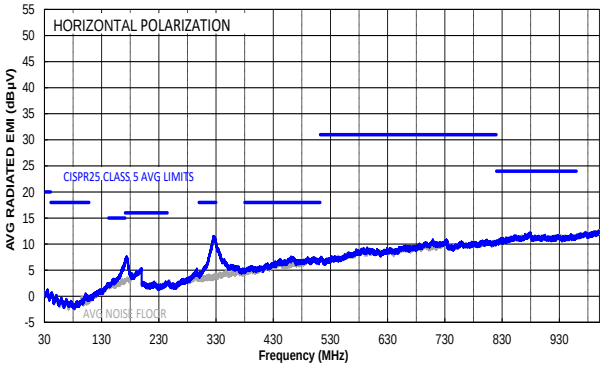
CISPR25 Class 5 Peak Radiated Horizontal

30MHz to 1GHz



CISPR25 Class 5 Average Radiated Horizontal

30MHz to 1GHz



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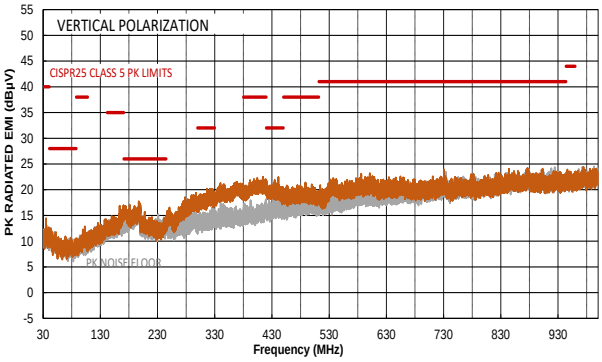
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (8), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted. (9)

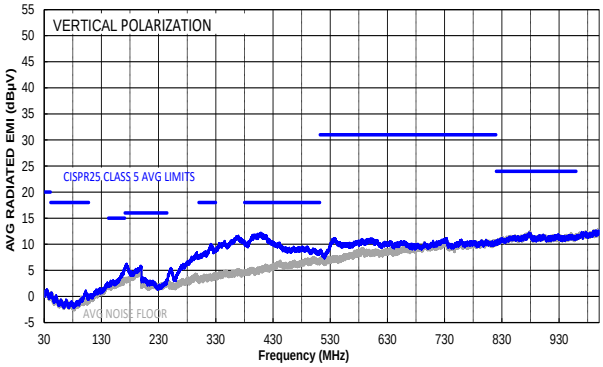
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

8) Inductor PN: XAL6060-472MEC. DCR = 15mΩ.
9) The EMC test results are based on the application circuit with EMI filters (see Figure 11 on page 34).

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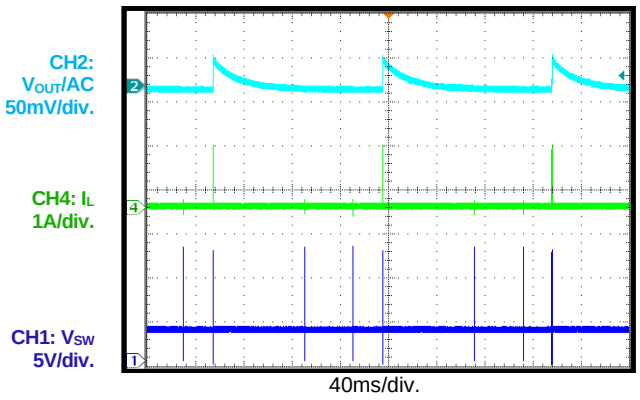
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

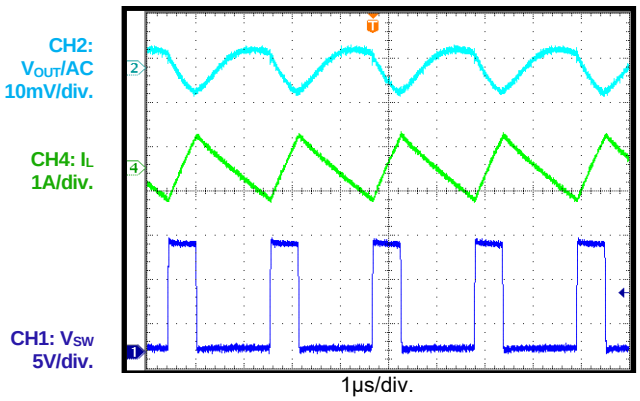
Steady State

I_{OUT} = 0A, AAM mode



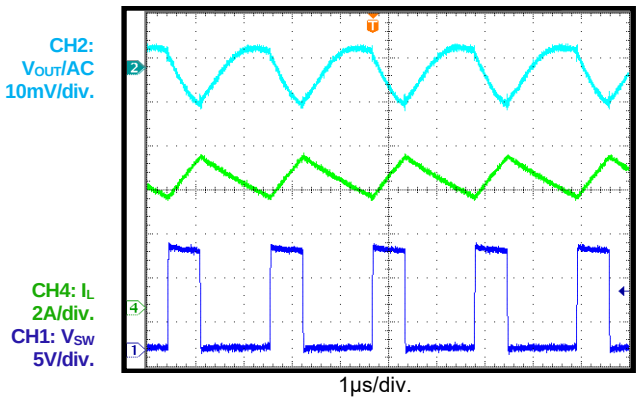
Steady State

I_{OUT} = 0A, FCCM



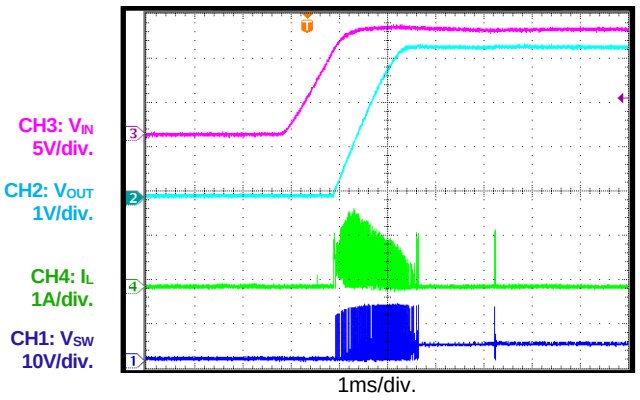
Steady State

I_{OUT} = 6A



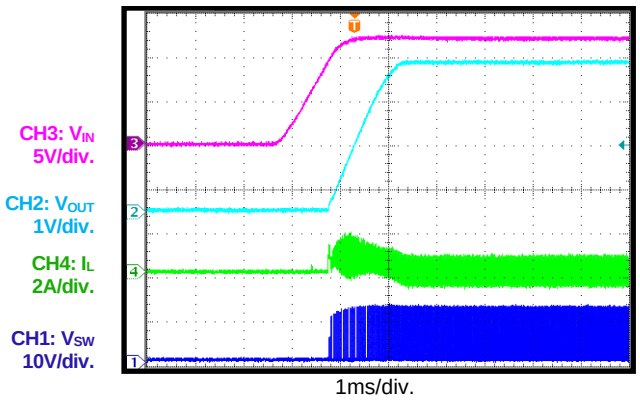
Start-Up through VIN

I_{OUT} = 0A, AAM mode



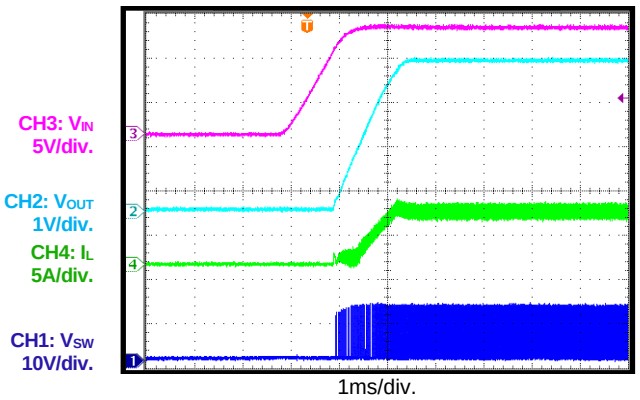
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 6A



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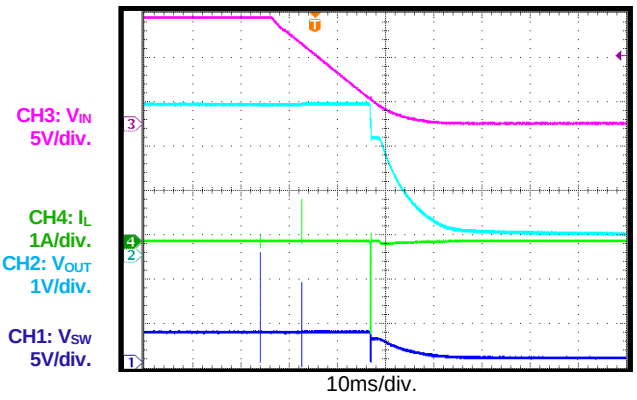
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

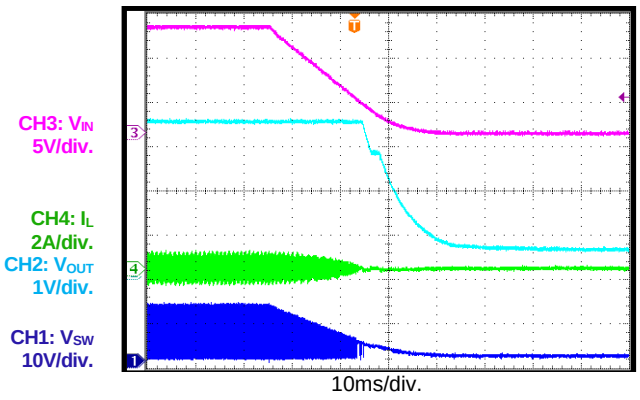
Shutdown through VIN

I_{OUT} = 0A, AAM mode



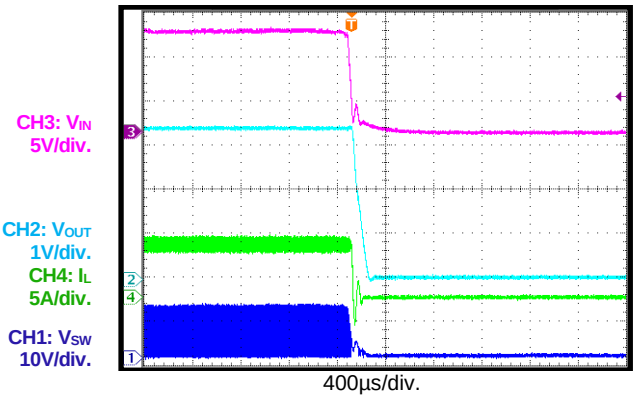
Shutdown through VIN

I_{OUT} = 0A, FCCM



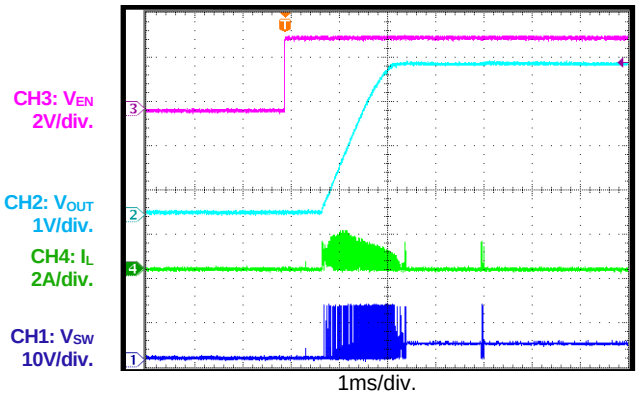
Shutdown through VIN

I_{OUT} = 6A



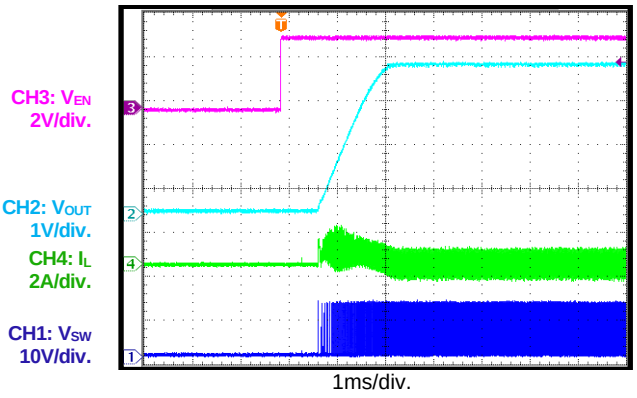
Start-Up through EN

I_{OUT} = 0A, AAM mode



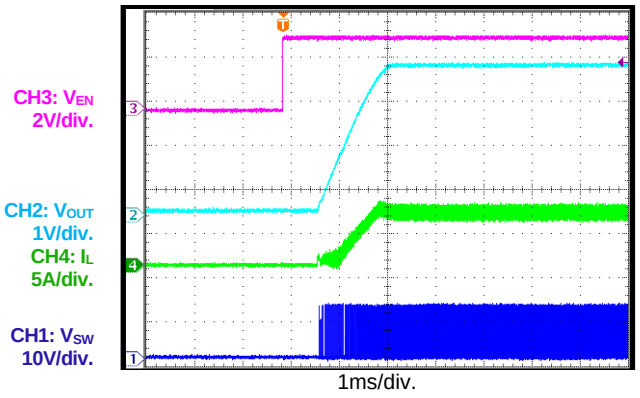
Start-Up through EN

I_{OUT} = 0A, FCCM



Start-Up through EN

I_{OUT} = 6A



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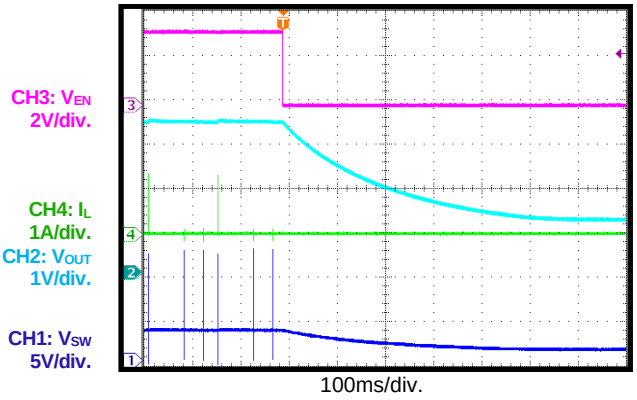
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

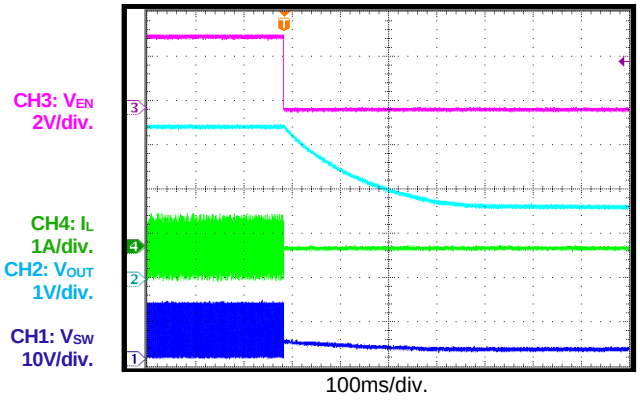
Shutdown through EN

I_{OUT} = 0A, AAM mode



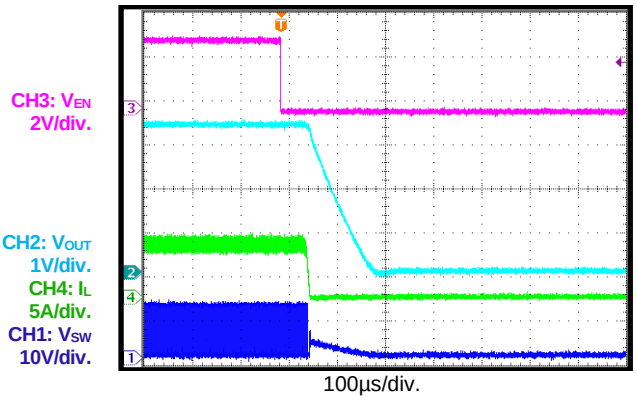
Shutdown through EN

I_{OUT} = 0A, FCCM



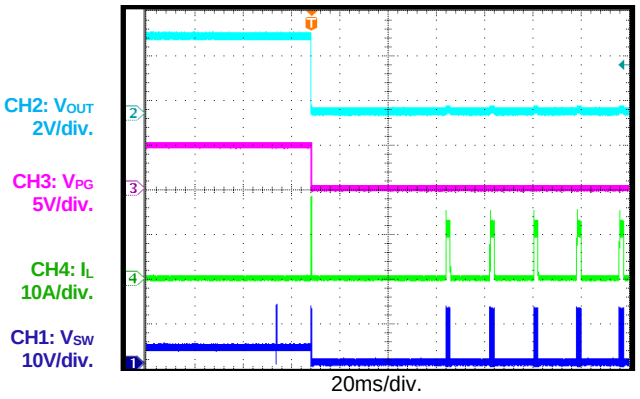
Shutdown through EN

I_{OUT} = 6A



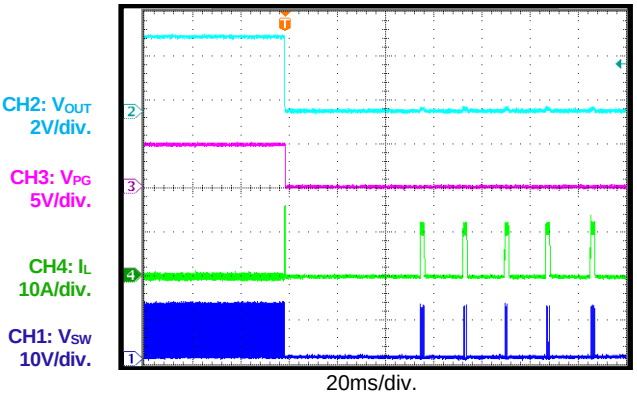
SCP Entry

I_{OUT} = 0A, AAM mode



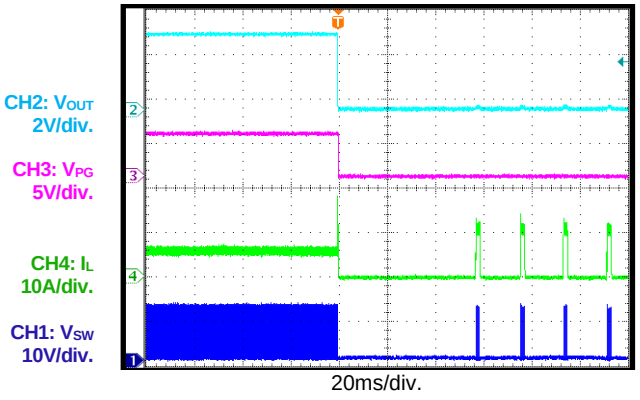
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 6A



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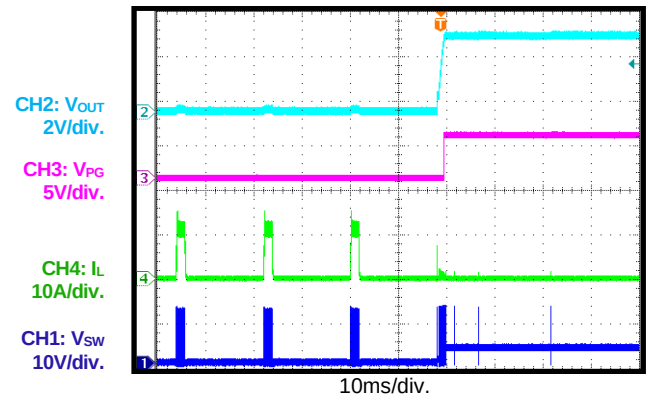
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

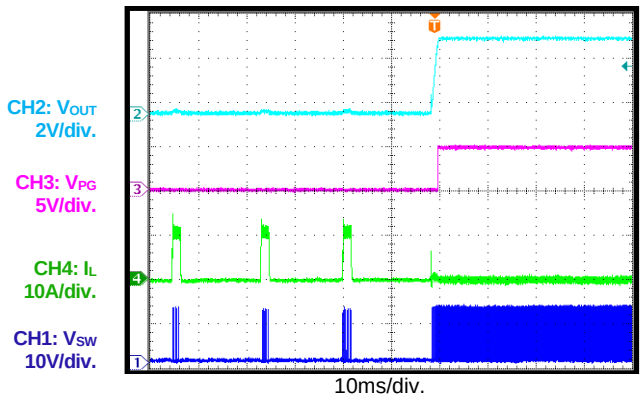
SCP Recovery

I_{OUT} = 0A, AAM mode



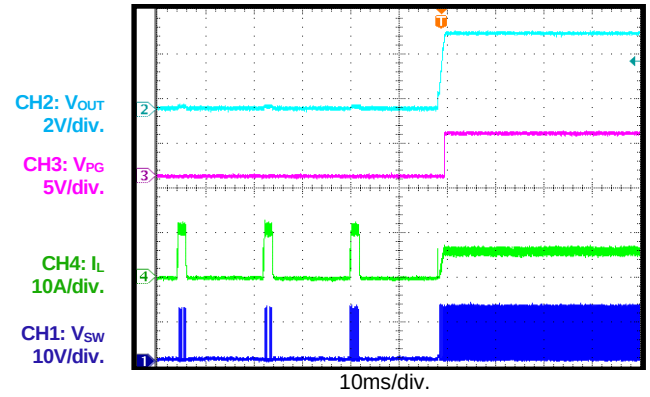
SCP Recovery

I_{OUT} = 0A, FCCM

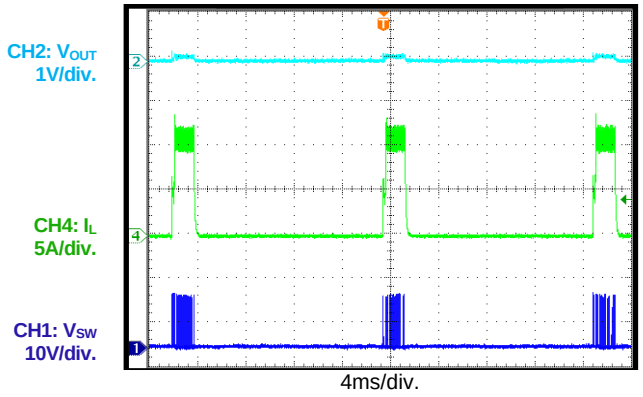


SCP Recovery

I_{OUT} = 6A

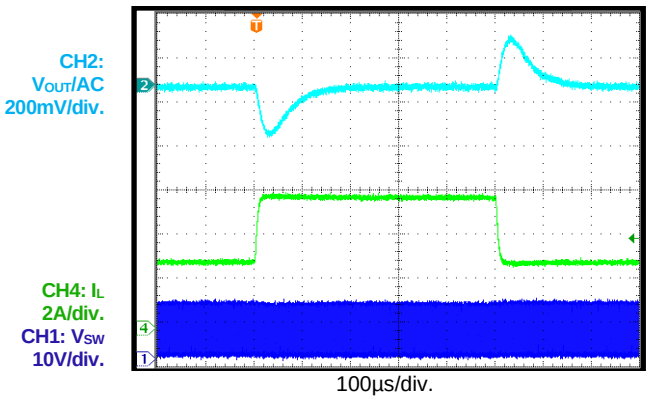


SCP Steady State



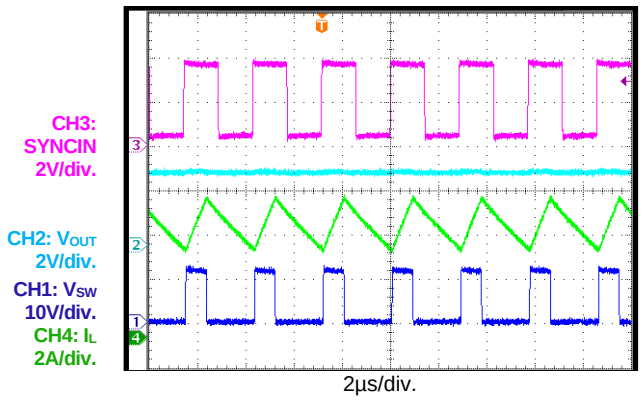
Load Transient

I_{OUT} = 3A to 6A, 1.6A/µs



SYNC Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



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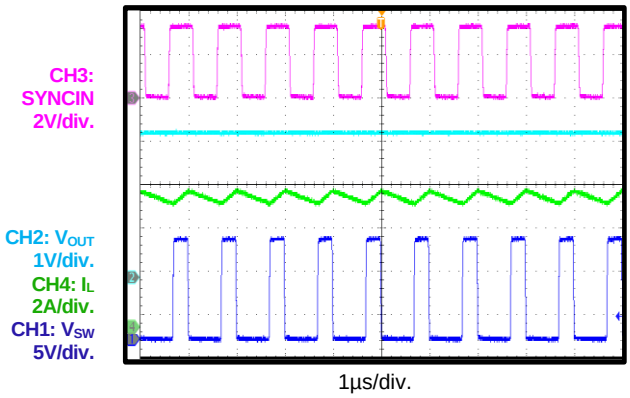
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

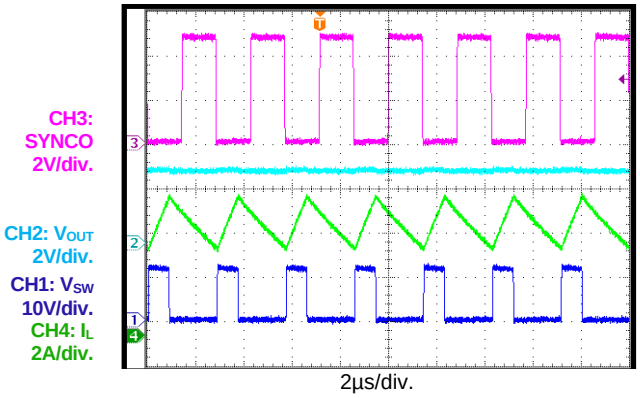
SYNC Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



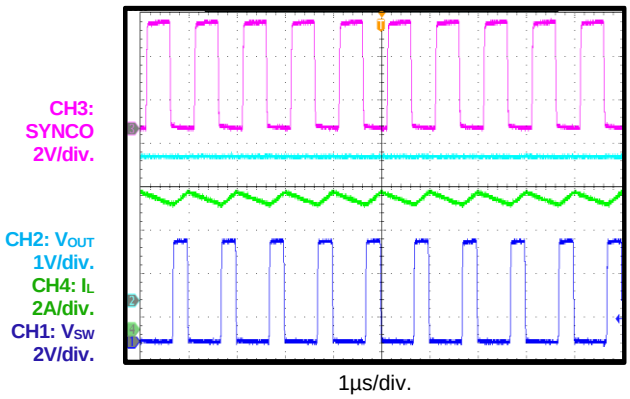
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



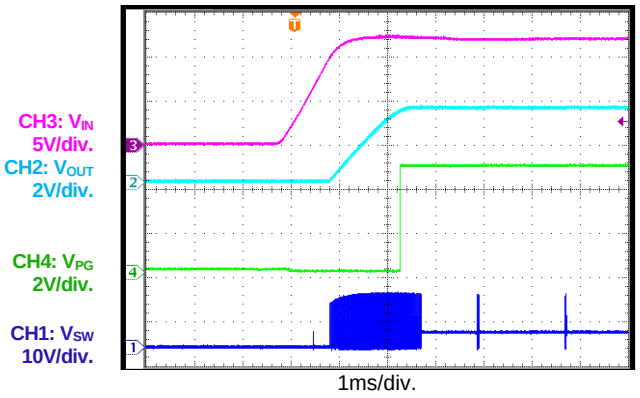
SYNCO Operation

I_{OUT} = 6A, SYNC frequency = 1000kHz



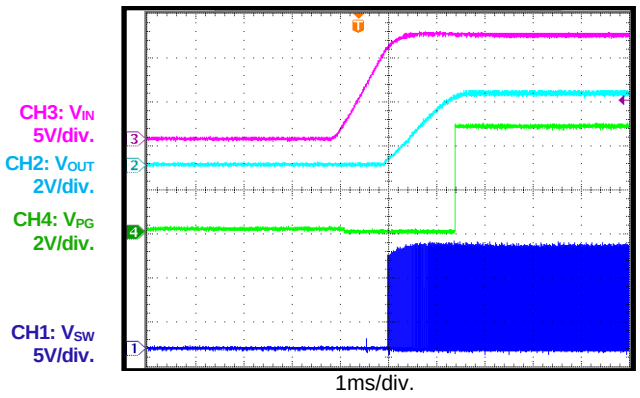
PG in Start-Up through VIN

I_{OUT} = 0A



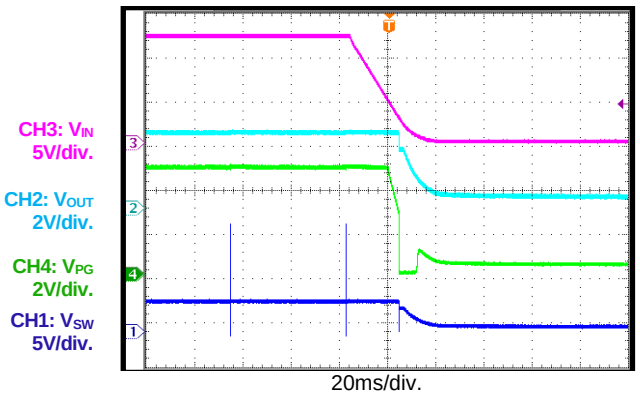
PG in Start-Up through VIN

I_{OUT} = 6A



PG in Shutdown through VIN

I_{OUT} = 0A



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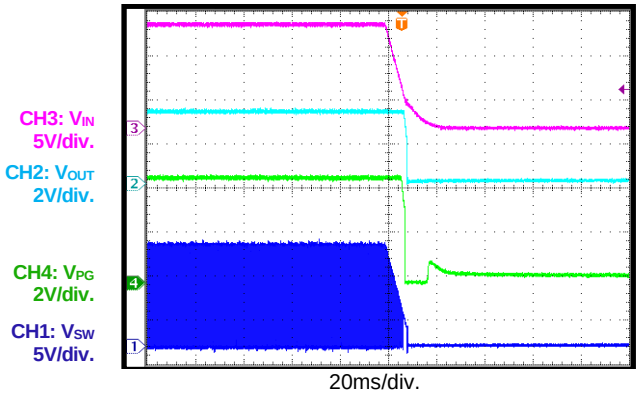
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

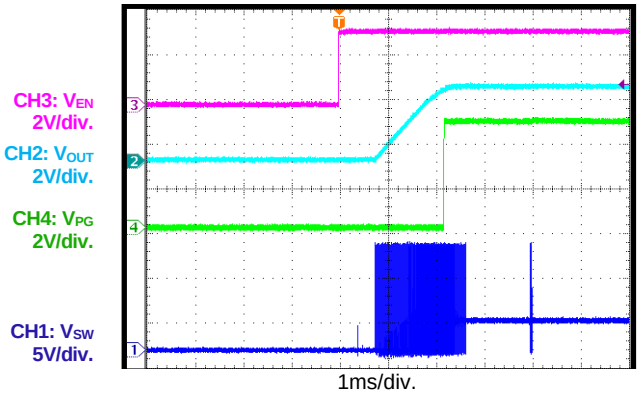
PG in Shutdown through VIN

I_{OUT} = 6A



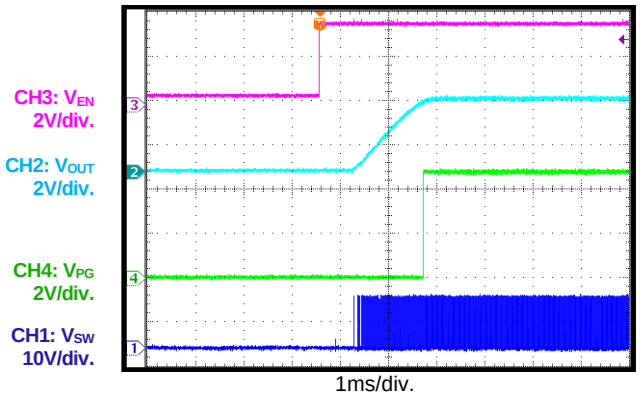
PG in Start-Up through EN

I_{OUT} = 0A



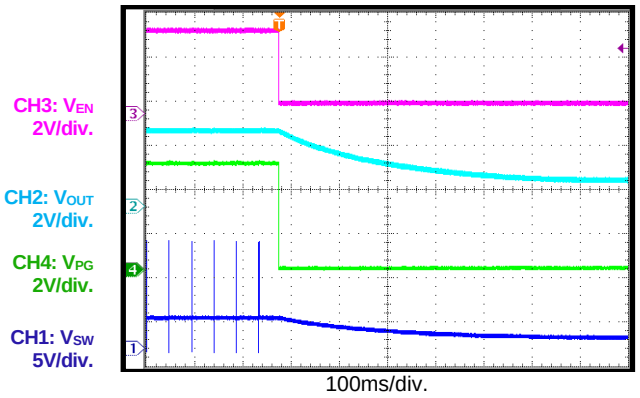
PG in Start-Up through EN

I_{OUT} = 6A



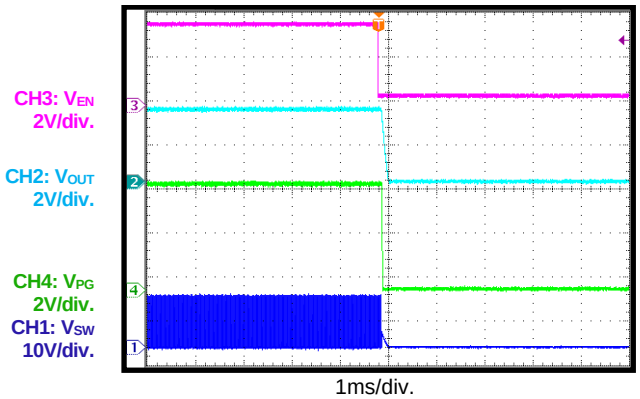
PG in Shutdown through EN

I_{OUT} = 0A



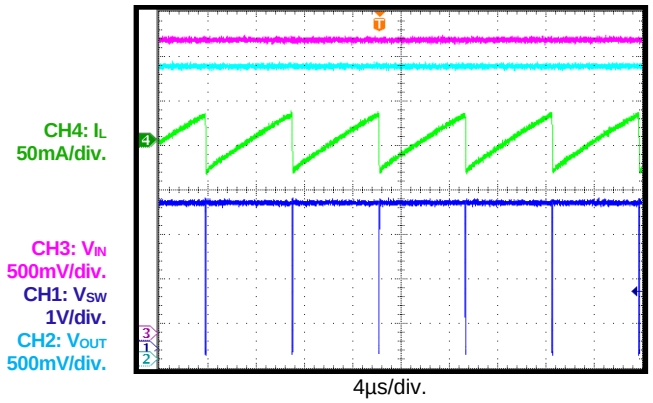
PG in Shutdown through EN

I_{OUT} = 6A



Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



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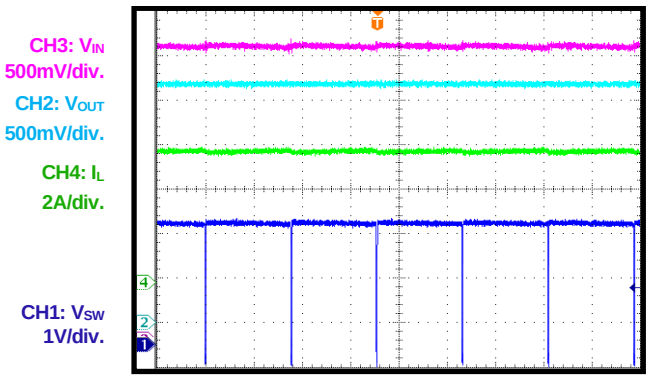
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

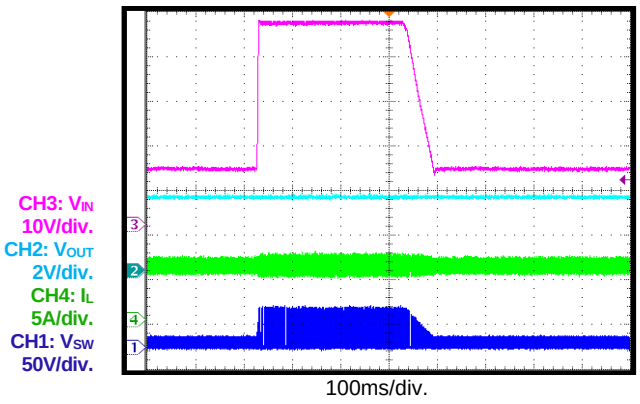
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



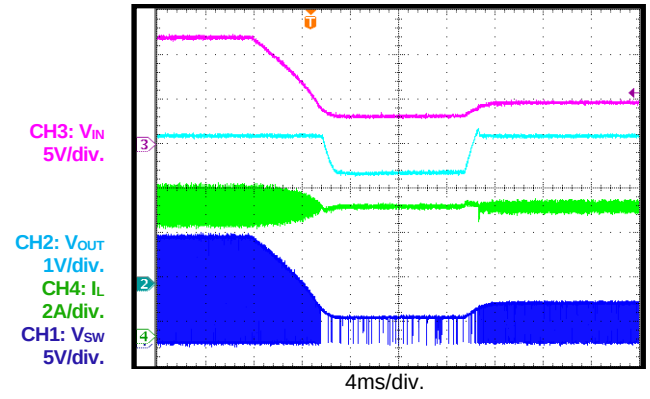
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



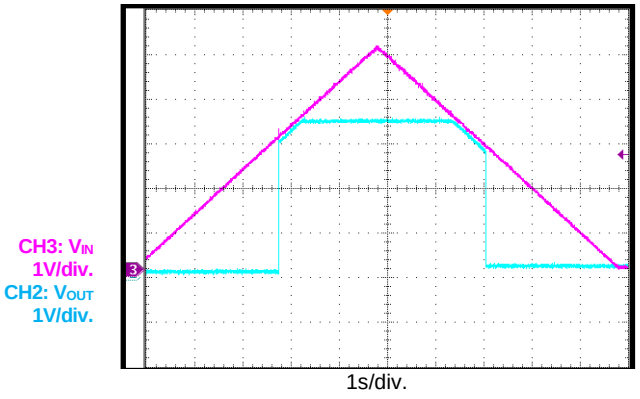
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



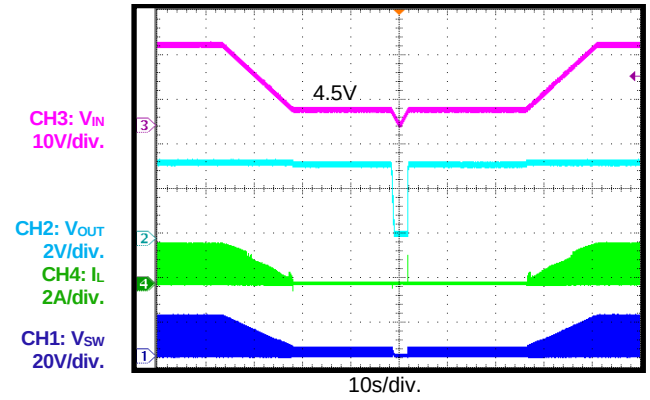
V_{IN} Ramping Up and Down

I_{OUT} = 0.1A



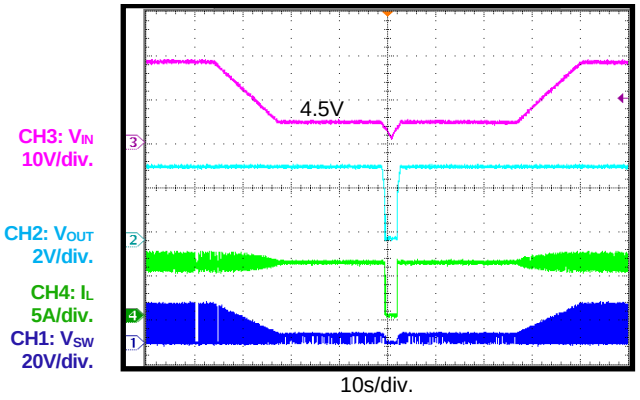
V_{IN} Ramping Down and Up

I_{OUT} = 1mA



V_{IN} Ramping Down and Up

I_{OUT} = 6A



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FUNCTIONAL BLOCK DIAGRAM

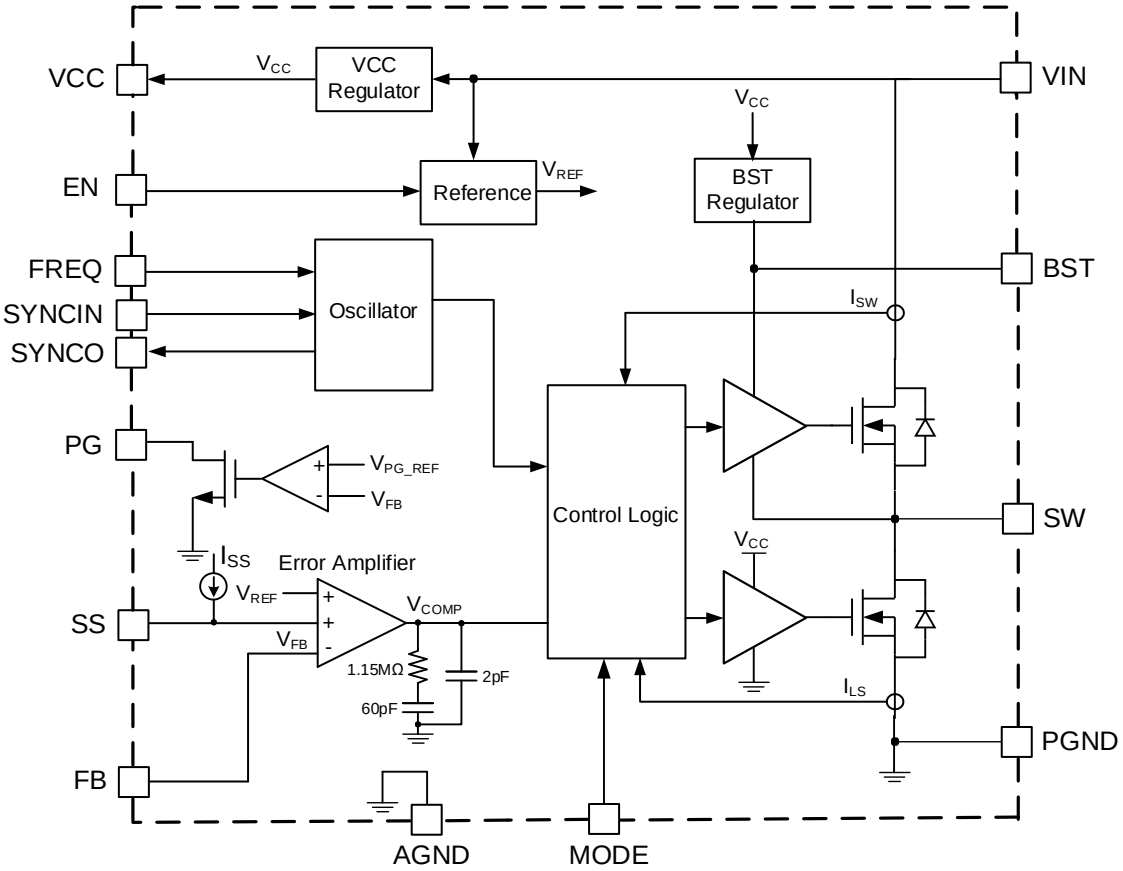

Figure 1: Functional Block Diagram

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TIMING DIAGRAM

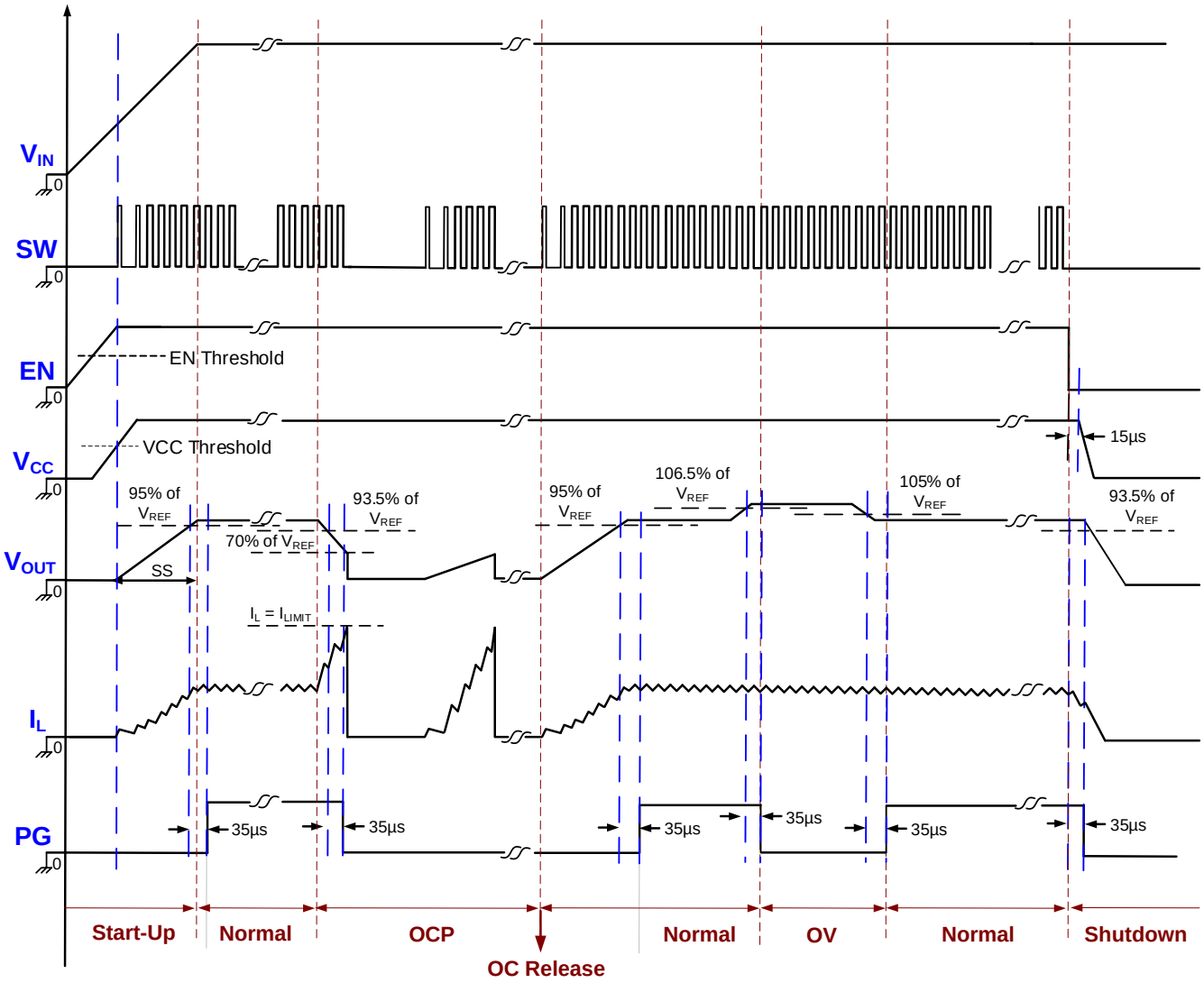

Figure 2: Timing Diagram

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OPERATION

The MPQ4316A is a synchronous, step-down switching converter with an integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). The device provides 6A of highly efficient output current (I_{OUT}) with current mode control.

The MPQ4316A features a wide input voltage (V_{IN}) range, configurable switching frequency (f_{SW}), external soft start (SS), and a precise current limit. The device's low operational quiescent current (I_Q) makes it well-suited for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4316A operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A pulse-width modulation (PWM) cycle is initiated by the internal clock. At the clock's rising edge, the HS-FET turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). The HS-FET stays on for at least 100ns.

When the HS-FET is off, the LS-FET turns on immediately and remains on for at least 80ns until the next cycle starts.

If the current in the HS-FET cannot reach the value set by COMP within one PWM period, the HS-FET remains on and saves a turn-off operation. If it remains on for about 10µs, then the HS-FET is forced off even if it has not reached the value set by COMP.

Light-Load Operation

Under light-load conditions, the MPQ4316A works in two different modes based on the MODE pin: forced continuous conduction mode (FCCM) and advanced asynchronous modulation (AAM) mode.

When MODE is pulled above 1.8V, the MPQ4316A works in FCCM. In FCCM, the device operates with a fixed frequency during no-load to full-load conditions. The advantages of FCCM include its controllable frequency and lower output ripple under light loads.

When MODE is pulled below 0.4V, the MPQ4316A works AAM mode. AAM mode optimizes efficiency during light-load and no-load conditions.

When AAM mode is enabled, the MPQ4316A enters asynchronous operation while the inductor current (I_L) approaches 0A under light loads (see Figure 3).

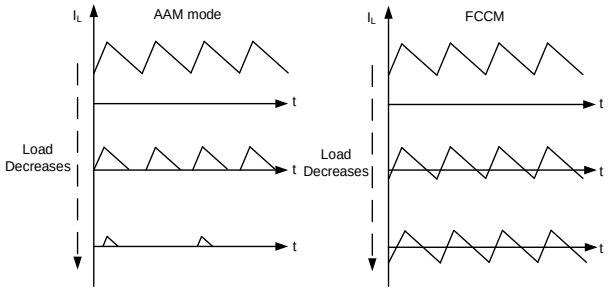

Figure 3: AAM Mode and FCCM

If the load further decreases or there is no load, then V_{COMP} drops to the set value and the MPQ4316A enters AAM mode.

In AAM mode, the internal clock is reset every time V_{COMP} crosses the set value, and the crossover time is used as a benchmark for the next clock. When the load increases and V_{COMP} exceeds the set value, the device operates in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with a constant switching frequency (f_{SW}).

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) to the internal reference voltage (V_{REF}, typically 0.815V) and outputs a current (I_{OUT}) that is proportional to the difference between these voltages. This I_{OUT} is then used to charge the compensation network to form V_{COMP}, which controls the power MOSFET's current.

During normal operation, the minimum V_{COMP} is clamped to 0.9V, and its maximum is clamped to 2V. In shutdown mode, COMP is internally pulled down to ground.

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Internal Regulator (VCC)

The internal 4.9V regulator (VCC) powers most of the internal circuitry. This regulator uses V_{IN} as the input and operates across the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is fully regulated. When V_{IN} drops below 4.9V, the VCC output degrades.

Bootstrap (BST) Charging

The bootstrap (BST) capacitor (C_{BST}) is charged and regulated to about 5V by the dedicated internal BST regulator. When the voltage between the BST and SW nodes drops below its regulated value, a N-channel MOSFET pass transistor connected from VCC to BST turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate charging. When the HS-FET is on, BST exceeds VCC, meaning C_{BST} cannot be charged.

Under higher duty cycles, C_{BST} has less time to charge, so it may not be charged sufficiently. If the external circuit has an insufficient voltage or not enough time to charge C_{BST}, then use additional external circuitry to ensure that the BST voltage (V_{BST}) remains in the normal operation range.

Low-Dropout Operation and Refreshing Bootstrap (BST)

To improve dropout, the MPQ4316A is designed to operate at close to 100% duty cycle when the difference between the voltages on the BST and SW pins exceed 2.5V. If the voltage from BST to SW drops below 2.5V, the HS-FET turns off using an under-voltage lockout (UVLO) circuit. This allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. As a result, the switching regulator's effective duty cycle is high.

The regulator's effective duty cycle during dropout is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side (LS) diode, and PCB resistance.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off.

Enabled by an External Logic (High/Low) Signal

When EN is pulled below its falling threshold voltage (about 0.85V), the chip operates in the lowest shutdown current mode. To turn on the MPQ4316A, EN must be pulled above its rising threshold voltage (about 1V).

Configurable V_{IN} Under-Voltage Lockout (UVLO)

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. With an internal current source, the circuit can generate a configurable V_{IN} UVLO threshold and hysteresis. Resistor dividers can be used to set the EN voltage (V_{EN}) (see Figure 4).

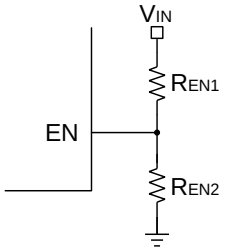

Figure 4: Enable Divider Circuit

Configurable Frequency and Foldback

The MPQ4316A's oscillating frequency can be configured via an external resistor (R_{FREQ}) connected from FREQ to ground, or by a logic-level SYNC signal.

To set f_{SW}, select R_{FREQ} using the f_{SW} vs. R_{FREQ} curves on page 15. Note that when f_{SW} is set high, it may fold back at high V_{IN} values to avoid triggering a minimum on time (t_{ON_MIN}) and forcing the output out of regulation.

For car battery applications, f_{SW} is between 350kHz and 1000kHz. Table 1 on page 29 lists the recommended R_{FREQ} values for common frequencies. Higher frequencies can be used in applications that do not have a critical f_{SW} limit, as well as applications with a low and stable V_{IN}.

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Table 1: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

Frequency Spread Spectrum (FSS)

The MPQ4316A uses a 12kHz modulation frequency with a fixed 128-step triangular profile to spread the internal oscillator frequency across a 20% (±10%) window. The steps are fixed and independent of the set oscillator frequency, which optimizes the frequency spread spectrum (FSS) performance (see Figure 5).

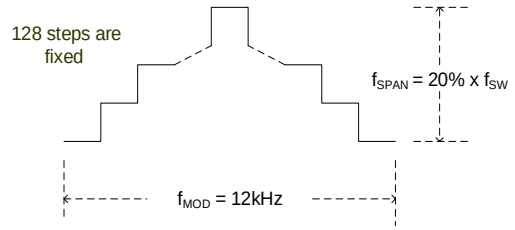

Figure 5: Spread Spectrum Scheme

Side bands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is reduced. This significantly reduces the peak EMI noise.

Soft Start (SS)

SS is implemented to prevent V_{OUT} from overshooting during start-up. When SS begins, an internal current source begins charging the external C_{SS}. When the soft-start voltage (V_{SS}) is below V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

C_{SS} can be calculated using Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 13.5 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} – 150mV during start-up, this means that the output has a pre-biased voltage. In the scenario, the HS-FET and LS-FET do not turn on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds upper threshold (170°C), then the device shuts down the power MOSFETs. Once the temperature drops below the lower threshold (150°C), the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET's current is accurately sensed via a current-sense MOSFET. This current is then fed to the high-speed current comparator for current mode control. The current comparator uses this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to mitigate noise. The comparator compares the power MOSFET's current to the value set by V_{COMP}. When the sensed current exceeds the value set by COMP, the comparator outputs low to turn off the HS-FET. The internal power MOSFET's maximum current is internally limited cycle by cycle.

Hiccup Protection

If the output is shorted to ground, then V_{OUT} may drop below 70% of its nominal output. When this occurs, the MPQ4316A shuts down momentarily and begins discharging C_{SS}. Once C_{SS} is fully discharged, the device restarts with a full SS. This process repeats until the fault is removed.

Start-Up and Shutdown

If both V_{IN} and EN exceed their appropriate thresholds, the chip starts up. The reference block starts first, generating a stable V_{REF} and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank any start-up glitches.

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When the SS block is enabled, the SS output stays low to ensure that the remaining circuitries are ready before slowly ramping up.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. When shutdown is initiated, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4316A includes an open-drain power good (PG) output. If using PG, connect the pin to a power source using a pull-up resistor. If V_{OUT} is within 95% to 105% of the nominal voltage, then PG goes high. If V_{OUT} is above 106.5% or below 93.5% of the nominal voltage, then PG goes low.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is between 350kHz and 1000kHz. Ensure that SYNCIN's off time is shorter than the internal oscillator period. Otherwise, the internal clock may turn on the HS-FET before SYNCIN's rising edge.

There is no limit for the SYNCIN pulse width, but there is often parasitic capacitance on the pad. If the pulse width is too short, then a clear rising and falling edge may not be achieved due to the parasitic capacitance. It is recommended to make the pulse longer than 100ns.

When using SYNCIN in AAM mode, drive SYNCIN below its specified threshold (about 0.4V), or float SYNCIN before starting up the MPQ4316A. Then add the external SYNCIN clock. Connect a resistor from SYNCIN to ground to avoid floating SYNCIN when using this function. It recommended to use a 10kΩ to 51kΩ resistor.

SYNCO provides a default 180° phase-shifted clock for the internal oscillator. If there is no external SYNCIN clock, SYNCO can provide a 180° phase-shift clock that is compared to the internal clock.

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APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider connected to FB sets V_{OUT} (see Figure 6).

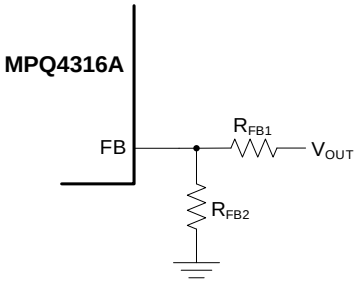

Figure 6: Feedback Network

R_{FB2} can be calculated using Equation (2):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.815V} - 1} \quad (2)$$

Table 2 lists the recommended feedback resistor values for common V_{OUT} values.

Table 2: Resistor Selection for V_{OUT} Values

V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)
3.3	100 (1%)	32.4 (1%)
5	100 (1%)	19.6 (1%)

Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current (I_{IN}), and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, it is recommended to use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating.

The RMS current in the input capacitor (I_{CIN}) can be estimated using Equation (3):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (4):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (4)$$

For simplification, choose C_{IN} with an RMS current rating that exceeds half of the maximum load current. C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the device as possible.

When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge, which prevents an excessive voltage ripple at the input.

The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated using Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. It is recommended to use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple (ΔV_{OUT}) low.

ΔV_{OUT} can be calculated using Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

Where L is the inductance, and R_{ESR} is C_{OUT}'s equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}.

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For simplification, ΔV_{OUT} can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be calculated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

C_{OUT} characteristics also affect the stability of the regulation system. The MPQ4316A can be optimized for a wide range of capacitances and ESR values.

Selecting the Inductor

For most applications, a 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in reduced ripple current and ΔV_{OUT}; however, it also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance (L) is to allow the inductor ripple current to be approximately 30% of the maximum load current. L can be estimated using Equation (9):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated using Equation (10):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MPQ4316A has an internal, fixed UVLO threshold. The rising threshold is 3V, while the falling threshold is about 2.7V. For applications that require a higher UVLO, place an external resistor divider between VIN and EN to raise the relevant UVLO threshold (see Figure 7).

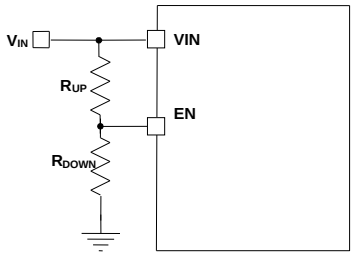

Figure 7: Adjustable UVLO Using EN Divider

The UVLO rising threshold ($V_{IN_UVLO_RISING}$) can be calculated using Equation (11):

$$V_{IN_UVLO_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_RISING} \quad (11)$$

The UVLO falling threshold ($V_{IN_UVLO_FALLING}$) can be calculated using Equation (12):

$$V_{IN_UVLO_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN_FALLING} \quad (12)$$

Where V_{EN_RISING} is 1V, and $V_{EN_FALLING}$ is 0.85V.

Selecting the External Bootstrap (BST) Diode and Resistor

An external BST diode can enhance the regulator's efficiency when the duty cycle is high. A power supply between 2.5V and 5V can power the external BST diode. It is recommended to use the VCC voltage (V_{CC}) or V_{OUT} to the power supply in the circuit (see Figure 8).

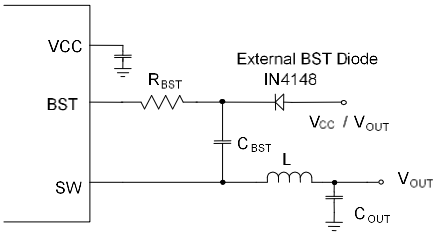

Figure 8: Optional External BST Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} is between 0.1µF and 1µF. Connect a resistor (R_{BST}) in series with C_{BST} to reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at higher V_{IN} values. A higher resistance reduces SW spikes, but compromises efficiency. R_{BST} is recommended to be ≤20Ω.

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Selecting the VCC Capacitor (C_{VCC})

The VCC capacitor (C_{VCC}) should have a capacitance that 10 times greater than C_{BST}. It is not recommended for C_{VCC} to exceed 68µF.

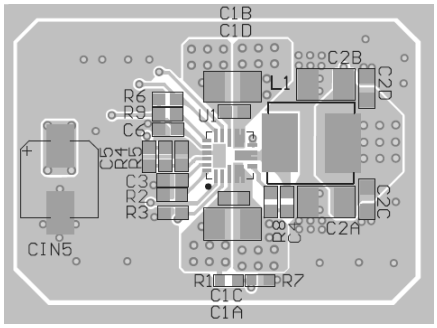
PCB Layout Guidelines (10)

Efficient PCB layout, especially C_{IN} placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

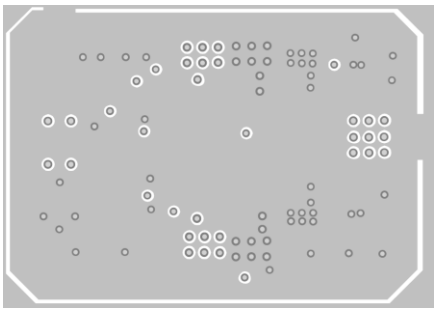
1. Place the symmetric input capacitors as close to VIN and ground as possible.
2. Use a large copper plane to connect directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at ground and VIN have short, direct, and wide traces.
5. Place the ceramic C_{IN}, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place C_{VCC} as close to VCC and ground as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip, and ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

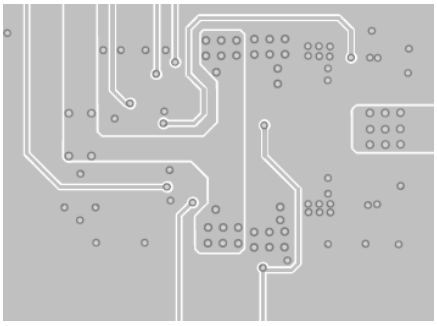
10) The recommended PCB layout is based on Figure 10 on page 34.



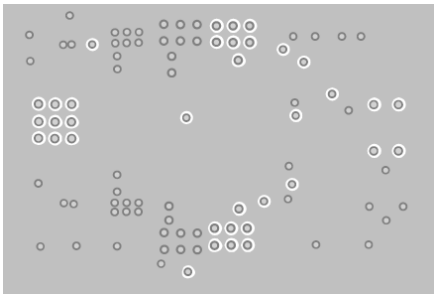
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout

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TYPICAL APPLICATION CIRUITS

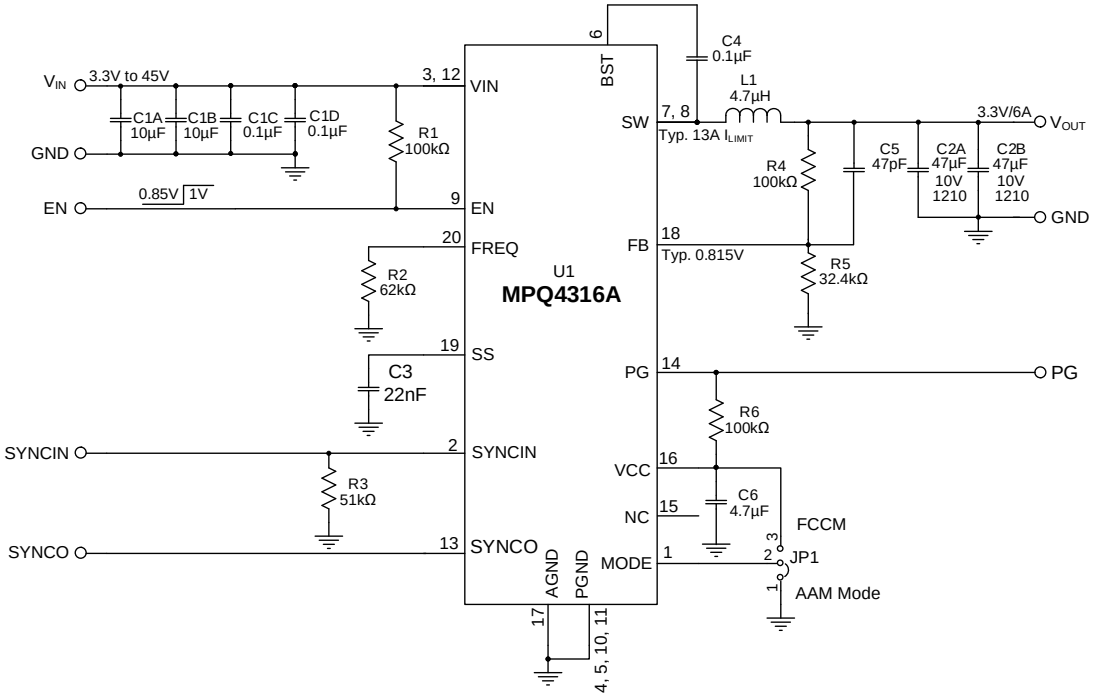

Figure 10: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 470kHz)

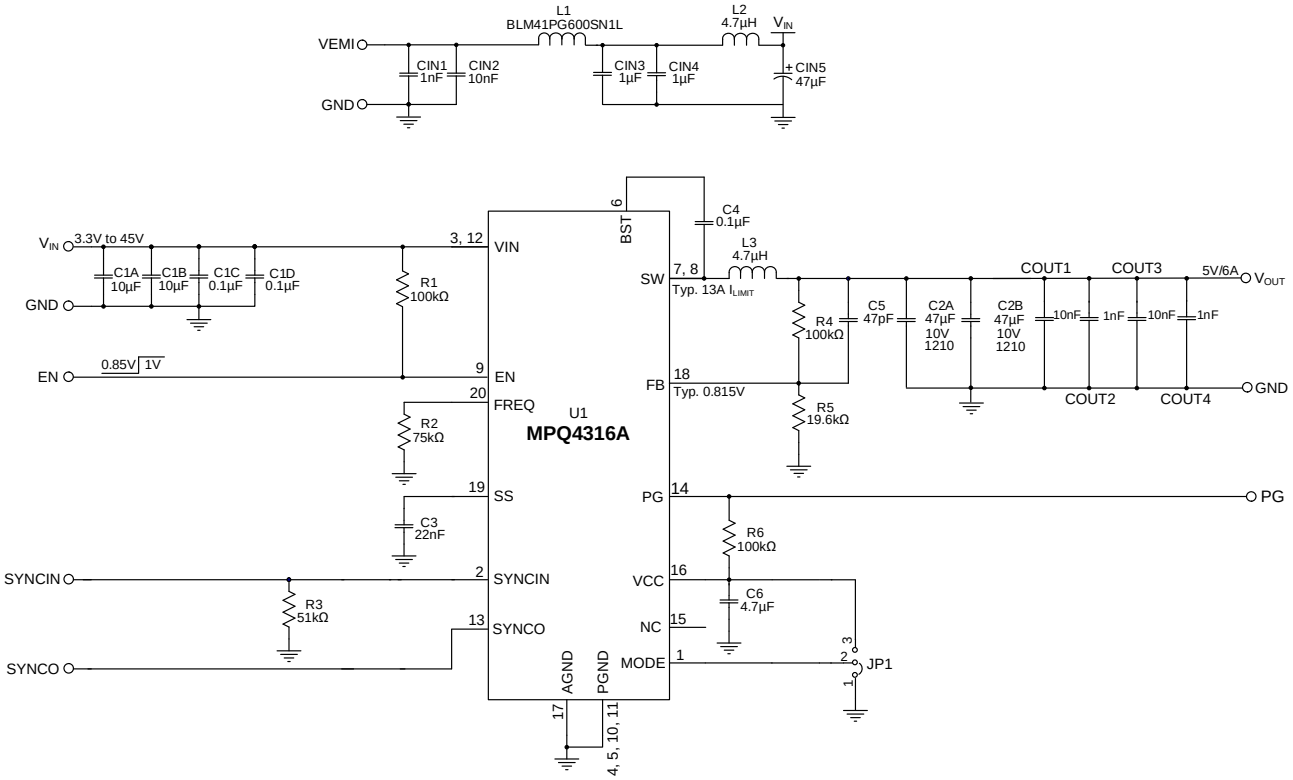

Figure 11: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters)

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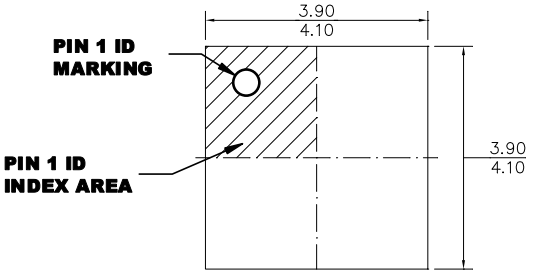
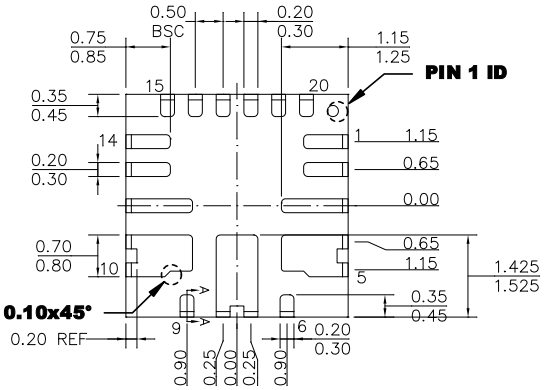
PACKAGE INFORMATION

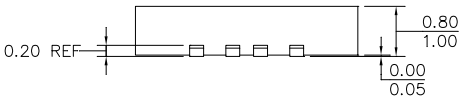
QFN-20 (4mmx4mm)
Wettable Flank



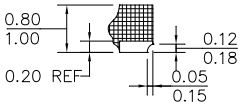
TOP VIEW



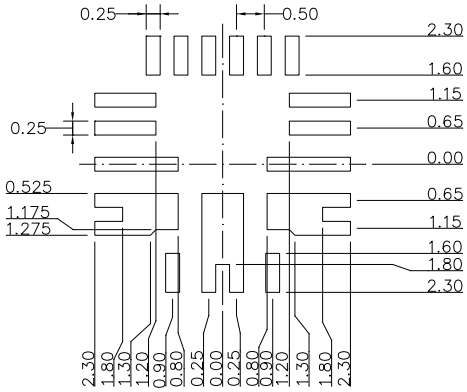
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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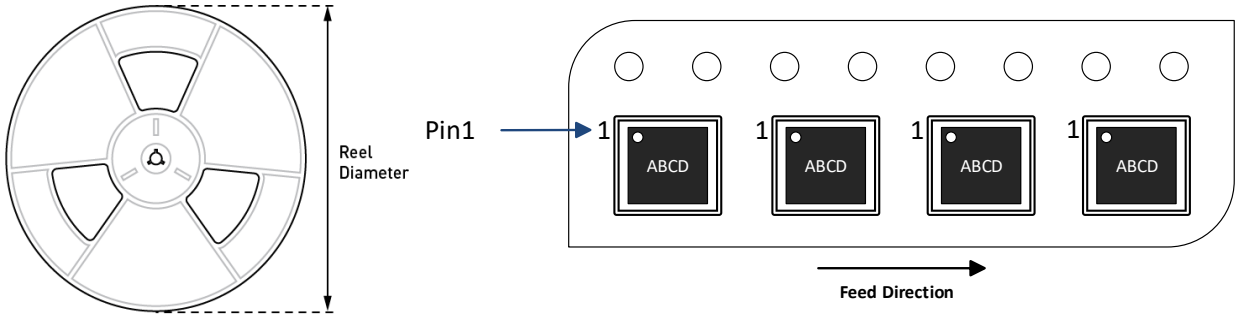
CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube (11)	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4316AGRE-AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

11) "N/A" indicates not available tubes. For 500-piece tape & reel prototype quantities, contact the factory. (Order code for a 500-piece partial reel order is "-P". Tape & reel dimensions are the same as the full reel.)

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	6/17/2022	Initial Release	-

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