MPQ4348/4348J

36V, 5A, Ultra-Low Quiescent Current, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4348/4348J is a configurable frequency (350kHz to 2.5MHz), synchronous step-down switching converter with integrated internal high-side and low side power MOSFETs (HS-FET and LS-FET, respectively). It can achieve up to 5A of highly efficient output (I_{OUT}) with fixed-frequency, zero-delay pulse-width modulation (PWM) control to optimize transient response.

The wide 3.3V to 36V input voltage (V_{IN}) range and 42V load dump tolerance can accommodate a variety of step-down applications in automotive input environments. A 1µA shutdown current (I_{SD}) allows the device to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output is within 94% to 106% of its nominal voltage.

Thermal shutdown provides reliable, fault-tolerant operation. A high-duty cycle and low-dropout (LDO) mode are provided for the automotive cold crank conditions.

The MPQ4348 is available in a QFN-17 (3mmx4mm) package. The MPQ4348J is available in a QFN-19 (3mmx4mm) package.

FEATURES

- Designed for Automotive Applications:
  - 42V Load Dump Tolerance
  - Supports 3.1V Cold Crank
  - Low-Dropout (LDO) Mode
  - 5A Continuous Output Current (I_{OUT})
  - Continuous Operation Up to 36V
  - Zero-Delay Pulse-Width Modulation (PWM) Control
  - 20ns Minimum On Time (t_{ON_MIN})
  - -40°C to +150°C Operating Junction Temperature (T_J) Range
  - Available in AEC-Q100 Grade 1
- Increases Battery Life:
  - 1µA Low Shutdown Current (I_{SD})
  - 3µA Sleep Mode Quiescent Current (I_Q)
  - Advanced Asynchronous Modulation (AAM) Mode for Light-Load Efficiency
- High Performance for Improved Thermals:
  - Internal 60mΩ HS-FET and 35mΩ LS-FET
- Optimized for EMC and EMI Reduction:
  - 350kHz to 2.5MHz Configurable Switching Frequency (f_{SW})
  - Symmetric VIN Pinout
  - Frequency Spread Spectrum (FSS) Modulation
  - CISPR25 Class 5 Compliant
  - MeshConnect™ Flip-Chip Package
- Additional Features:
  - Fixed Output Options (1): 1V, 1.1V, 1.8V, 2.5V, 3.0V, 3.3V, 3.8V, and 5V
  - Power Good (PG) Output
  - Synchronizable to an External Clock
  - Synchronized Clock Output
  - External Soft Start (SS)
  - Over-Current Protection (OCP) with Hiccup Mode
  - Available in a QFN-17 (3mmx4mm) Package for the MPQ4348 and a QFN-19 (3mmx4mm) Package for the MPQ4348J
  - Available in a Wettable Flank Package

Note:

1) See the Ordering Information section for more details regarding additional fixed output voltage (V_{OUT}) options.

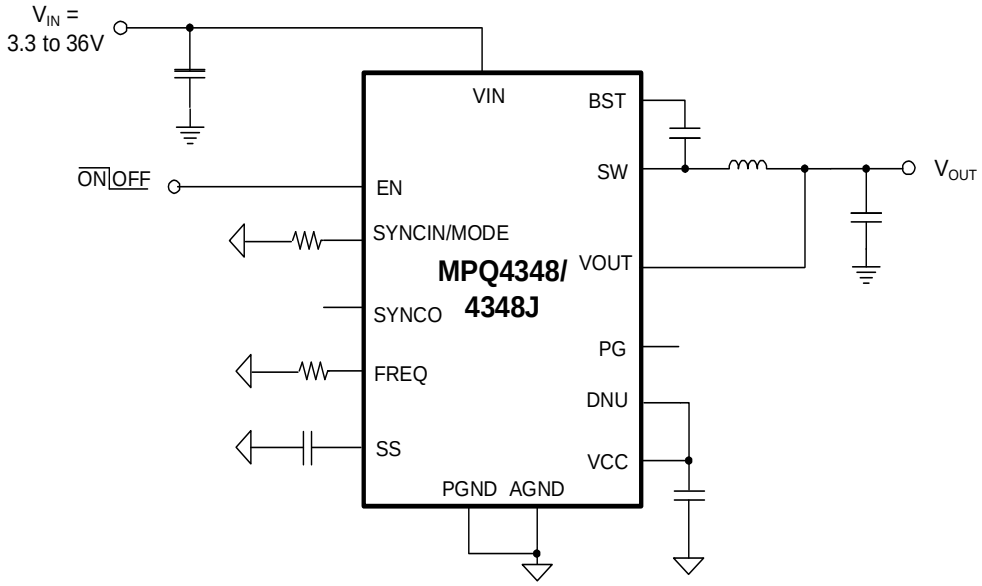
APPLICATIONS

- Automotive Clusters
- Automotive Infotainment
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

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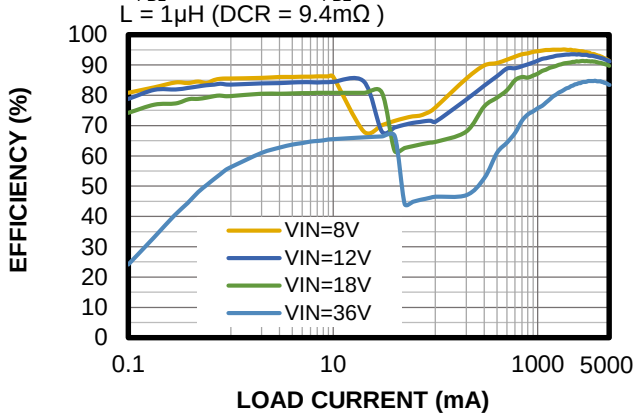
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TYPICAL APPLICATION



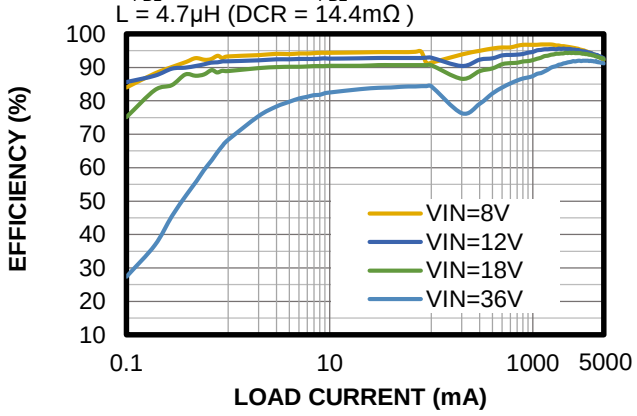
Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 2.2MHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 1µH (DCR = 9.4mΩ)



Efficiency vs. Load Current

AAM mode, V_{OUT} = 5V, f_{SW} = 410kHz,
R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ,
L = 4.7µH (DCR = 14.4mΩ)



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ORDERING INFORMATION

Part Number* (2)	Output Voltage	Package	Top Marking	MSL Rating**
MPQ4348GLE-33-AEC1***	Fixed 3.3V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4348GLE-5-AEC1***	Fixed 5V	QFN-17 (3mmx4mm)	*See Below*	1
MPQ4348JGLE-33-AEC1***	Fixed 3.3V	QFN-19 (3mmx4mm)	*See Below*	1
MPQ4348JGLE-5-AEC1***	Fixed 5V	QFN-19 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ4348GLE-33-AEC1-Z).

**Moisture Sensitivity Level Rating

*** Wettable Flank

Note:

2) Contact an MPS FAE for more details regarding the fixed-output versions.

TOP MARKING
(MPQ4348GLE-33-AEC1 and MPQ4348GLE-5-AEC1)

MPYW
4348
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
4348: Part number
LLL: Lot number
E: Wettable flank

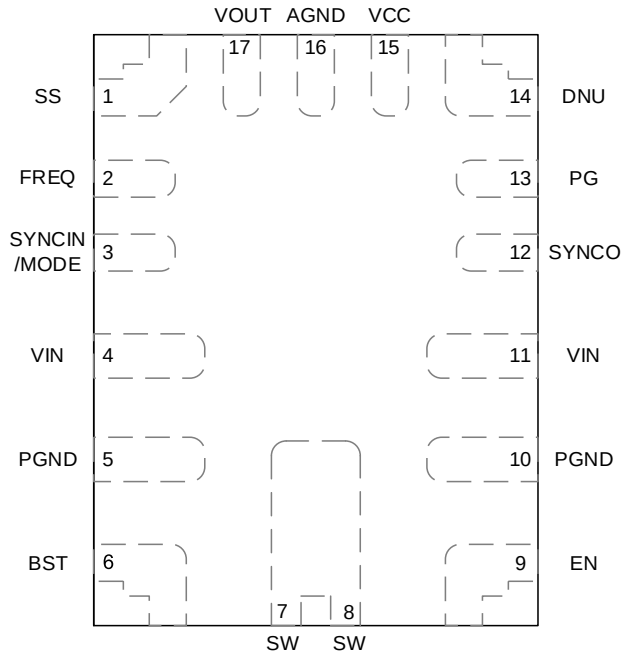
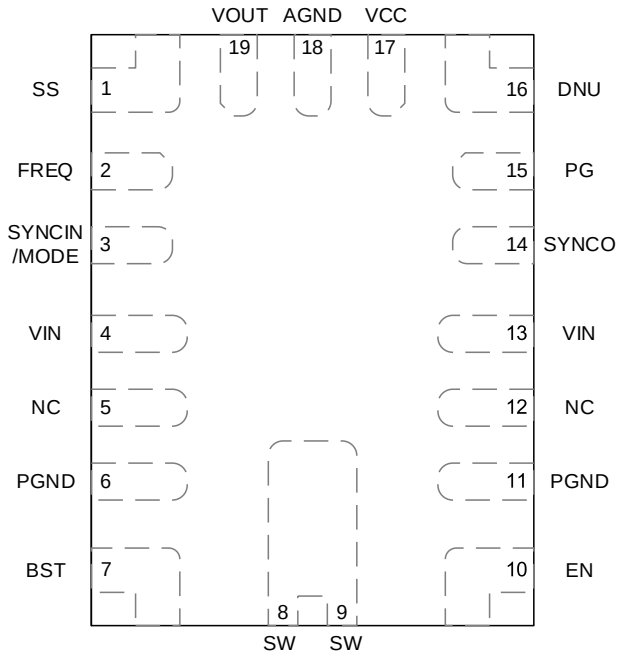
TOP MARKING
(MPQ4348JGLE-33-AEC1 and MPQ4348JGLE-5-AEC1)

MPYW
4348
JLLL
E

MP: MPS prefix
Y: Year code
W: Week code
4348J: Part number
LLL: Lot number
E: Wettable flank

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PACKAGE REFERENCE

TOP VIEW	TOP VIEW
	
QFN-17 (3mmx4mm)	QFN-19 (3mmx4mm)

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PIN FUNCTIONS

Pin # (QFN-19)	Pin # (QFN-17)	Name	Description
1	1	SS	**Soft-start input.** Place a capacitor between the SS and AGND pins to set the soft-start time (t_{SS}). The MPQ4348/4348J sources 10μA from the SS pin to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) increases, the feedback (FB) reference voltage (V_{REF}) increases to limit inrush current during start-up. Do not float this pin.
2	2	FREQ	**Switching frequency setting.** Connect a resistor between the FREQ and AGND pins to set the switching frequency (f_{SW}).
3	3	SYNCIN/ MODE	**Synchronous input and mode selection.** Applying a clock signal to the SYNCIN/MODE pin synchronizes the internal f_{SW} to the external clock. Use an external clock or pull SYNCIN/MODE high to have the device operate in forced continuous conduction mode (FCCM). Pull SYNCIN/MODE low to have the device operate in advanced asynchronous modulation (AAM) mode and pulse-skip mode (PSM) at light loads. Do not float SYNCIN/MODE.
4, 13	4, 11	VIN	**Input supply.** The VIN pin supplies power to all of the internal control circuitry and the power MOSFET connected to SW. Connect a decoupling capacitor to ground, placed close to VIN as possible to reduce switching spikes at the input.
5, 12	-	NC	**Not connected.** Float the NC pin.
6, 11	5, 10	PGND	**Power ground.**
7	6	BST	**Bootstrap.** The bootstrap (BST) pin is the positive power supply for the high-side MOSFET driver connected to SW. Connect a bypass capacitor between the BST and SW pins. See the Bootstrap (BST) Charging section on page 37 for more details.
8, 9	7, 8	SW	**Switch output.** The SW pin is the internal power MOSFET's output.
10	9	EN	**Enable.** Pull the EN above 1V to turn the converter on; pull EN below 0.85V to turn it off. Do not float EN.
14	12	SYNCO	**Synchronous output.** The SYNCO pin outputs a clock signal in phase with the internal oscillator signal or the clock signal applied at the SYNCIN/MODE pin. SYNCO can be floated.
15	13	PG	**Power good output.** The power good (PG) pin is an open-drain output. A pull-up resistor connected to the power source is required if PG is used. If the output voltage (V_{OUT}) is within 94% to 106% of the nominal voltage, then PG is pulled high. If V_{OUT} exceeds 107% or drops below 93% of the nominal voltage, then PG is pulled low. Float PG if not used.
16	14	DNU	**Do not use.** Connect the DNU pin directly to VCC.
17	15	VCC	**Bias supply.** The VCC pin supplies power (5V) to the internal control circuitry and gate drivers. Connect a decoupling capacitor to ground, placed as close to VCC as possible. See the Selecting the VCC Capacitor (C_{VCC}) section on page 39 for more details.
18	16	AGND	**Analog ground.**
19	17	VOUT	**Output regulation point.** Connect VOUT directly to V_{OUT}.

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ABSOLUTE MAXIMUM RATINGS (3)

VIN, EN……-0.3V to +42V
SW……- 0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST…… V_{SW} +5.5V
All other pins……-0.3V to +6V
Continuous power dissipation (T_A = 25°C)
QFN-17 (3mmx4mm) (4) (8) ……4.28W
QFN-19 (3mmx4mm) (4) (8) ……4.13W
Junction temperature……150°C
Lead temperature……260°C
Storage temperature……-65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 2 (5)
Charged device model (CDM).....Class C2b (6)

Recommended Operating Conditions

Input voltage (V_{IN})……3.3V to 36V
Operating junction temp (T_J).....-40°C to +150°C

Thermal Resistance

QFN-17 (3mmx4mm)	θ_{JA}	θ_{JC}	
JESD51-7	44.7	5.2	°C/W (7)
EVQ4348-L-00A	29.2		°C/W (8)

	Ψ_{JT}	
JESD51-7	1.2	°C/W (7)
EVQ4348-L-00A	6.1	°C/W (8)

QFN-19 (3mmx4mm)	θ_{JA}	θ_{JC}	
JESD51-7	43.6	5.4	°C/W (7)
EVQ4348J-L-00A	30.3		°C/W (8)

	Ψ_{JT}	
JESD51-7	0.9	°C/W (7)
EVQ4348J-L-00A	5.17	°C/W (8)

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Per AEC-Q100-002.
6) Per AEC-Q100-011.
7) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. θ_{JC} is the thermal resistance from the junction-to-case bottom. Ψ_{JT} is the characterization parameter from junction-to-case top.
8) Measured on an MPS standard EVB: 8.3cmx8.3cm, 4-layer PCB, 2oz copper thickness. Ψ_{JT} is the characterization parameter from junction-to-case top.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
Minimum operating input voltage (V_{IN})	V_{IN_MIN}				3.3	V
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN_UVLO_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN_UVLO_FALLING}$		2.6	2.8	3	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			200		mV
Quiescent current (9)	I_Q	V_{OUT} = 1.05 x V_{SET}, no load, sleep mode, T_J = -40°C to +85°C	1.9	3	3.6	µA
		V_{OUT} = 1.05 x V_{SET}, no load, sleep mode, T_J = -40°C to +125°C	1.5		15	µA
Sleep mode quiescent current (switching) (9)	I_{SLEEP}	SYNCIN/MODE is pulled to GND, AAM mode, switching, no load, T_J = -40°C to +85°C	2.4	3.5	4.5	µA
		SYNCIN/MODE is pulled to GND, AAM mode, switching, no load, T_J = -40 to +125°C	2		16	µA
Active current (no switching)	I_{ACTIVE}	SYNCIN/MODE is pulled to VCC, FCCM, no switching		1200		µA
Shutdown current	I_{SD}	V_{EN} = 0V,T_J = 25°C		1	3	µA
		V_{EN} = 0V			11	µA
V_{IN} over-voltage protection (OVP) threshold	$V_{IN_OVP_RISING}$		36	38	40	V
V_{IN} OVP hysteresis	$V_{IN_OVP_HYS}$			10		V
Enable (EN)						
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN_FALLING}$		0.65	0.85	1.05	V
EN hysteresis	V_{EN_HYS}			150		mV
MOSFETs and Switching Frequency (f_{SW})						
Switching frequency	f_{SW}	R_{FREQ} = 86.6kΩ	370	410	450	kHz
		R_{FREQ} = 33kΩ	950	1050	1150	kHz
		R_{FREQ} = 15kΩ	1980	2200	2420	kHz
Minimum on time	t_{ON_MIN}			20	35	ns
Minimum off time	t_{OFF_MIN}			120	140	ns
Switch leakage current	I_{SW_LKG}			0.01	5	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)_HS}$	V_{BST} - V_{SW} = 5V		60	110	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)_LS}$	V_{CC} = 5V		35	60	mΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Bootstrap (BST)						
BST to SW refresh rising threshold	$V_{BST-SW-RISING}$			2.5	2.9	V
BST to SW refresh falling threshold	$V_{BST-SW-FALLING}$			2.3	2.7	V
BST to SW refresh hysteresis	V_{BST-SW_HYS}			0.2		V
Soft Start (SS) and VCC						
VCC voltage	V_{CC}	I_{VCC} = 0A	4.7	5	5.3	V
VCC regulation		I_{VCC} = 0mA and 30mA			1	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	50	100		mA
		V_{CC} = 0V		70		mA
Soft-start current	I_{SS}	V_{SS} = 0V		10		µA
Output and Regulation						
Output voltage (V_{OUT}) accuracy (3.3V fixed output version)	$V_{OUT_3.3V}$	T_J = 25°C	3260	3300	3340	mV
		T_J = -40°C to +150°C	3230	3300	3370	mV
V_{OUT} accuracy (5V fixed output version)	V_{OUT_5V}	T_J = 25°C	4940	5000	5060	mV
		T_J = -40°C to +150°C	4900	5000	5100	mV
VOUT current	I_{VOUT}	V_{OUT} = V_{OUT_REG}		300		nA
V_{OUT} discharge	$I_{DISCHARGE}$	V_{EN} = 0V, V_{OUT} = 0.3V, V_{IN} = 3.3V to 36V	1.9			mA
Power Good (PG)						
PG rising threshold	V_{PG_RISING}	V_{OUT} rising	91	94	97	% of V_{OUT}
		V_{OUT} falling	103	106	109	
PG falling threshold	$V_{PG_FALLING}$	V_{OUT} falling	90	93	96	% of V_{OUT}
		V_{OUT} rising	104	107	110	
PG threshold hysteresis	V_{PG_HYS}			1		% of V_{OUT}
PG low voltage	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising deglitch time	t_{PG_RISING}			50		µs
PG falling deglitch time	$t_{PG_FALLING}$			50		µs
SYNCIN and SYNCO						
SYNCIN/MODE rising threshold	V_{SYNCIN_RISING}		1.8			V
SYNCIN/MODE falling threshold	$V_{SYNCIN_FALLING}$				0.4	V
SYNCIN/MODE timeout	t_{MODE}	SYNCIN/MODE is pulled low, AAM mode		41		µs
SYNCIN/MODE clock range	f_{SYNCIN}	Percent of freerunning frequency	90		115	% of f_{SW}
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protections						
High-side (HS) current limit	I_{LIMIT_HS}	30% duty cycle	6.3	7.7	9.7	A
Low-side (LS) valley current limit (9)	I_{LIMIT_LS}		4.1	5.9	7.6	A
Zero-current detection (ZCD) current	I_{ZCD}	AAM mode	-0.05	0.1	+0.25	A
LS-FET reverse current limit	$I_{LIMIT_REVERSE}$	FCCM		4		A
Thermal shutdown (9)	T_{SD}		150	170		°C
Thermal shutdown hysteresis (9)	T_{SD_HYS}			20		°C

Note:

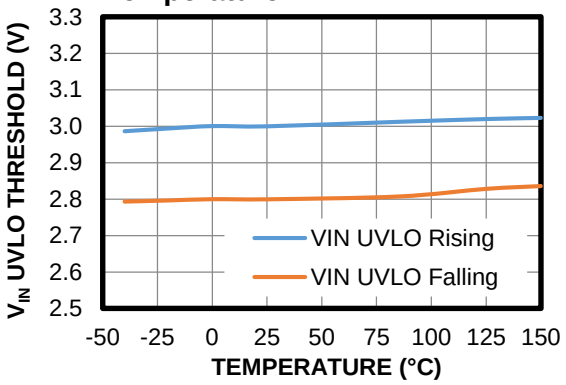
9) Guaranteed by design and characterization. Not tested in production.

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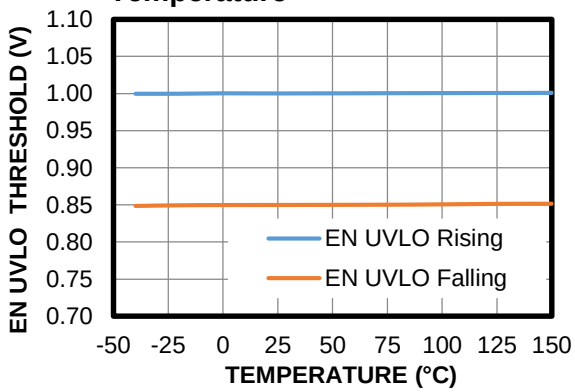
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

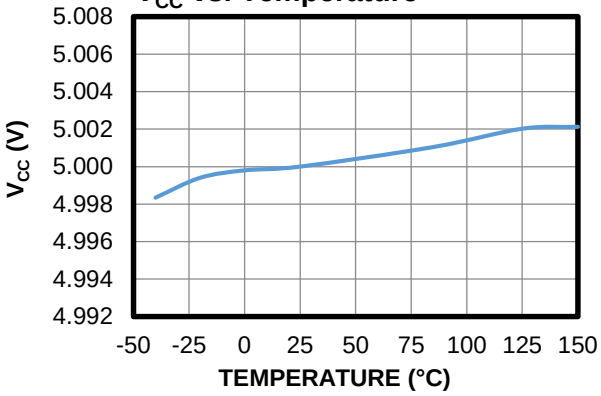
V_{IN} UVLO Threshold vs. Temperature



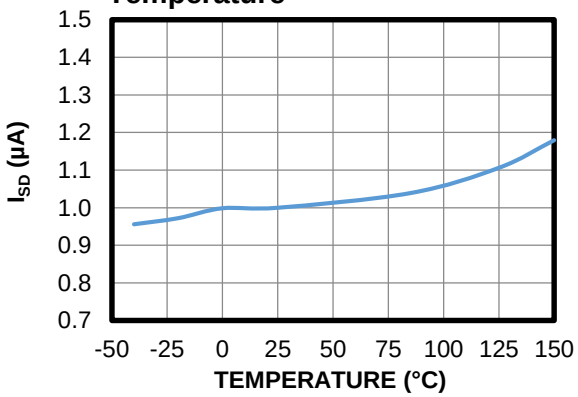
EN UVLO Threshold vs. Temperature



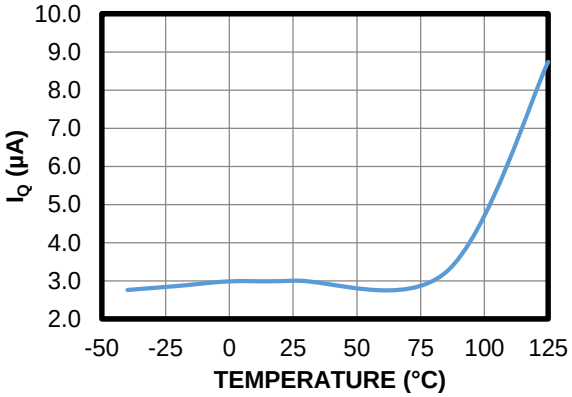
V_{CC} vs. Temperature



Shutdown Current vs. Temperature

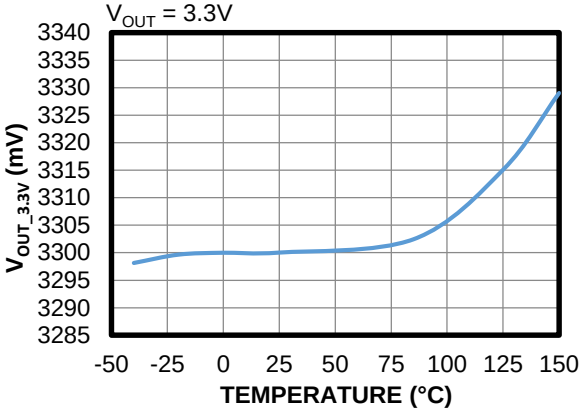


Quiescent Current vs. Temperature



Output Voltage Accuracy vs. Temperature

V_{OUT} = 3.3V

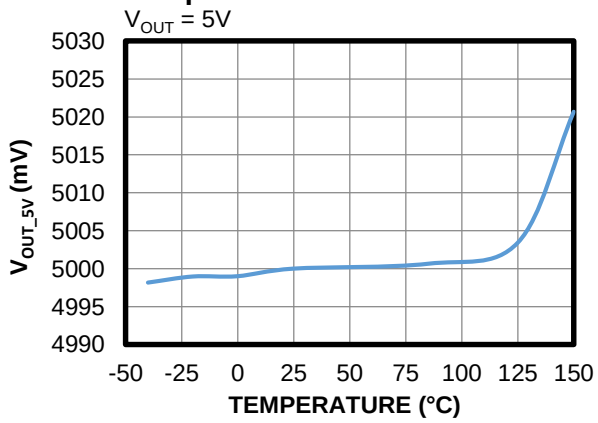


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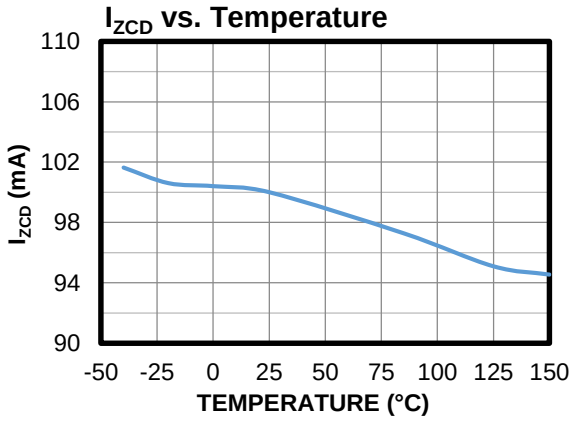
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

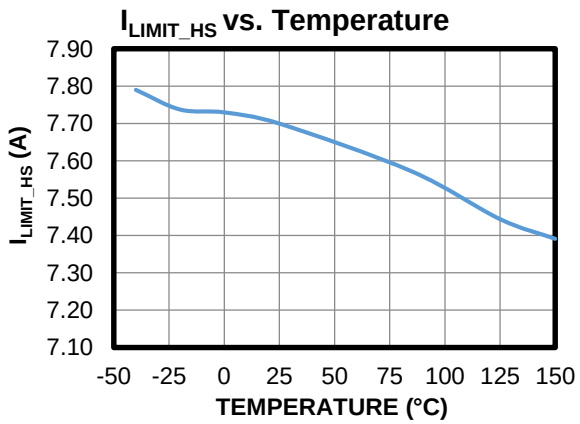
Output Voltage Accuracy vs. Temperature



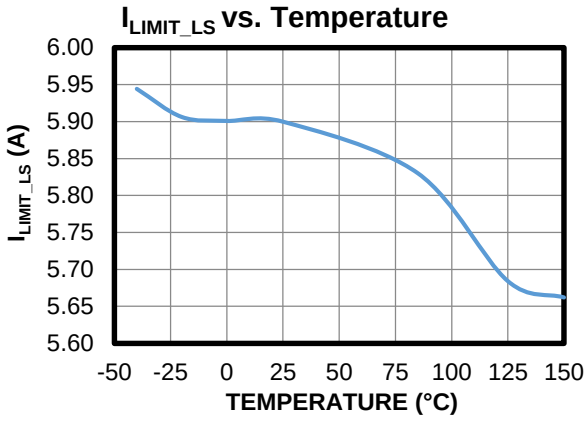
I_{ZCD} vs. Temperature



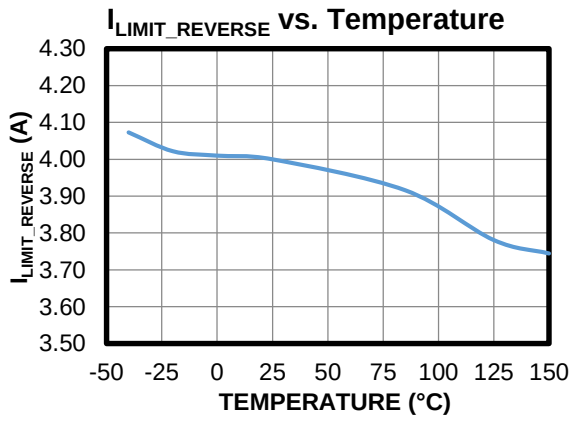
I_{LIMIT_HS} vs. Temperature



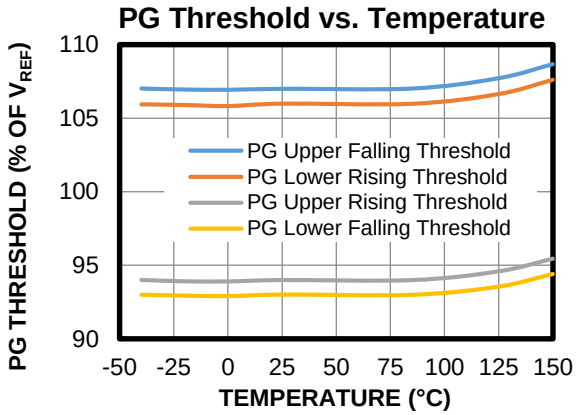
I_{LIMIT_LS} vs. Temperature



$I_{LIMIT_REVERSE}$ vs. Temperature



PG Threshold vs. Temperature

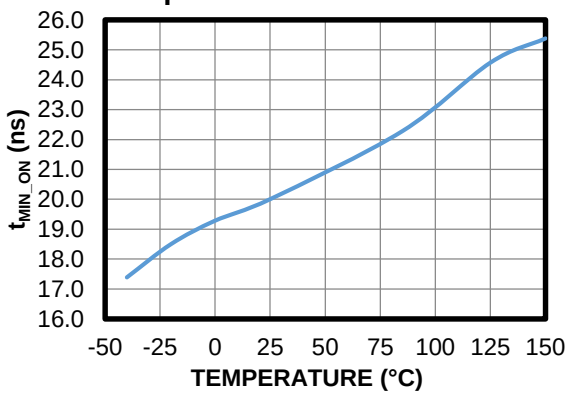


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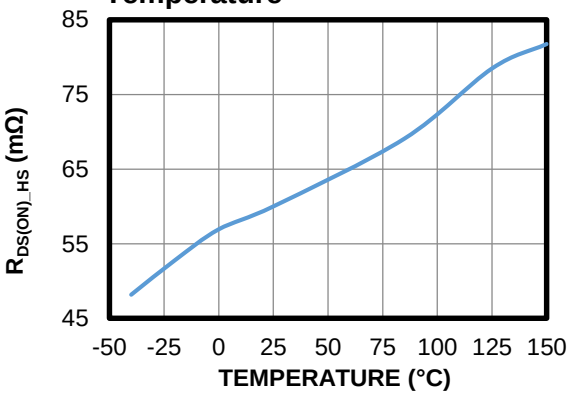
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +150°C, unless otherwise noted.

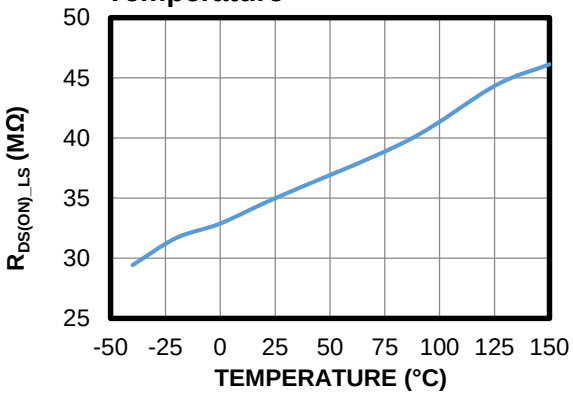
Minimum On Time vs. Temperature



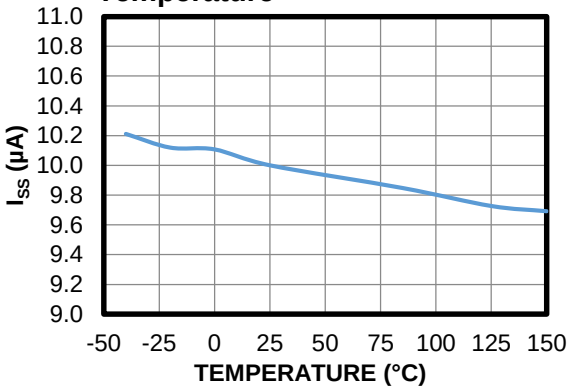
HS-FET On Resistance vs. Temperature



LS-FET On Resistance vs. Temperature

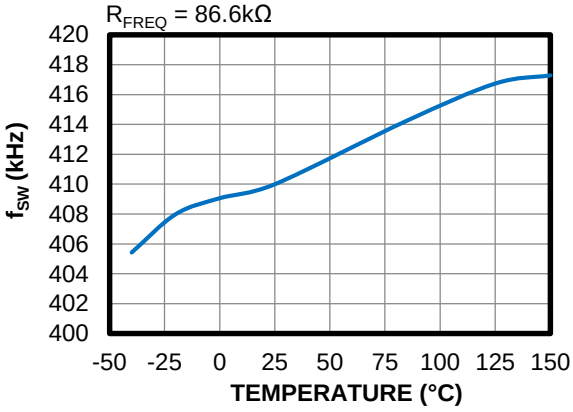


Soft-Start Current vs. Temperature



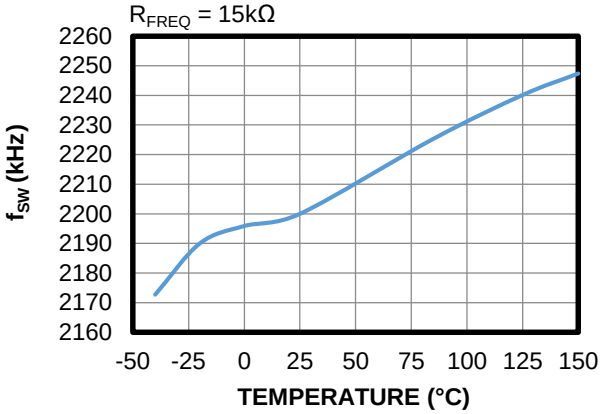
Switching Frequency vs. Temperature

R_{FREQ} = 86.6kΩ



Switching Frequency vs. Temperature

R_{FREQ} = 15kΩ



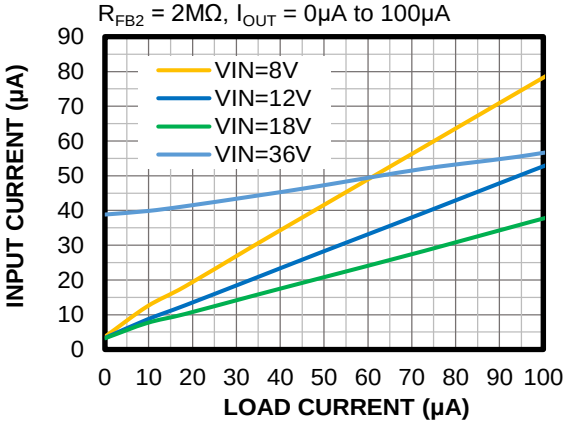
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

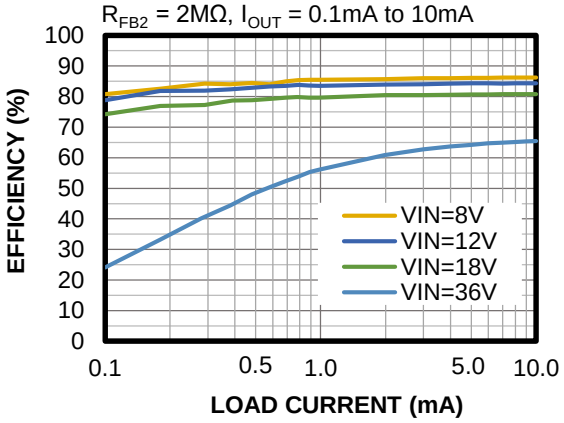
Input Current vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0µA to 100µA



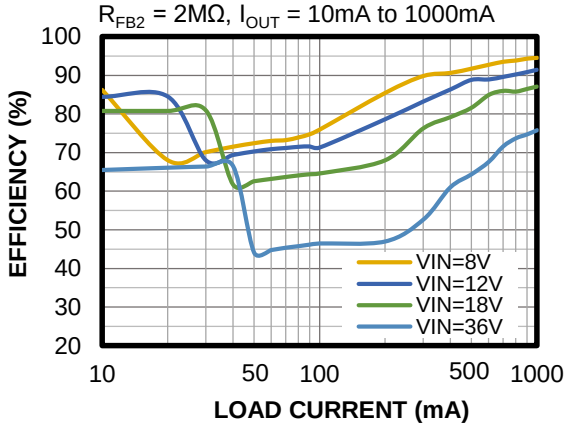
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



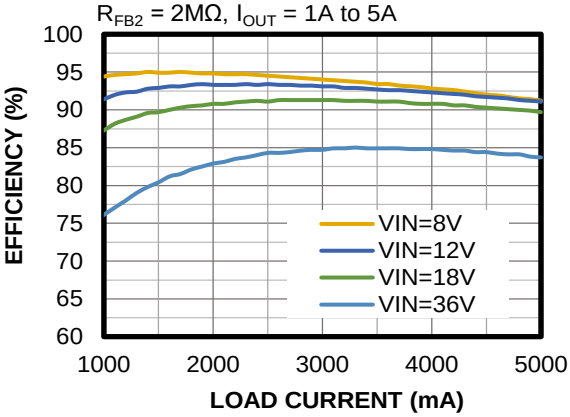
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



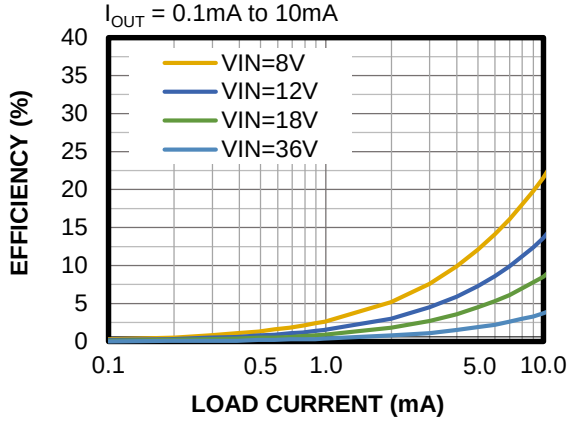
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



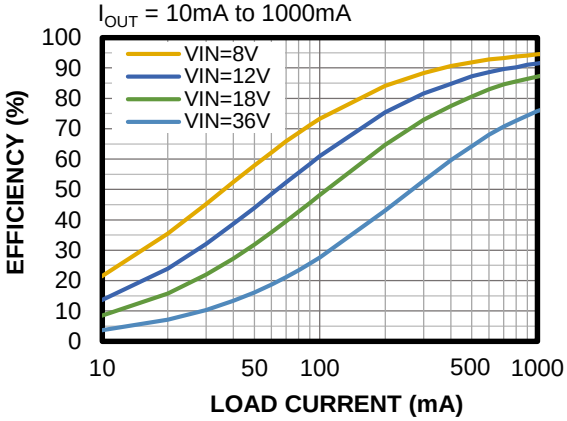
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



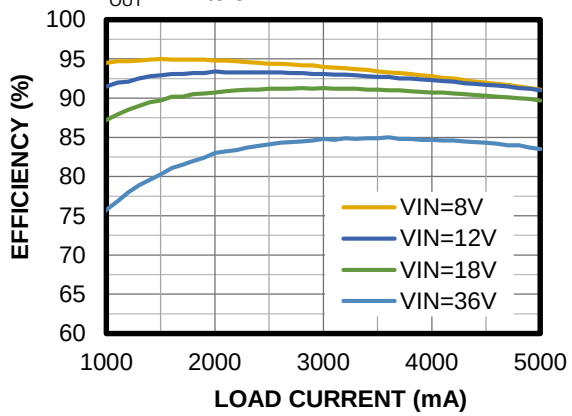
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, T_A = L25°C, unless otherwise noted.

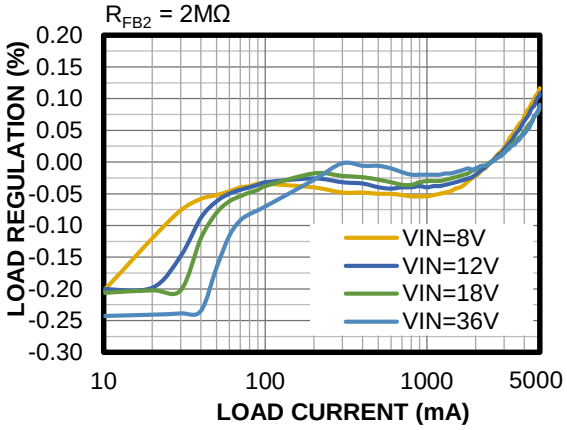
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



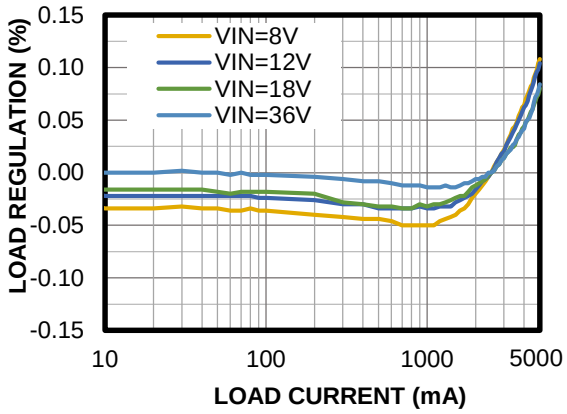
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



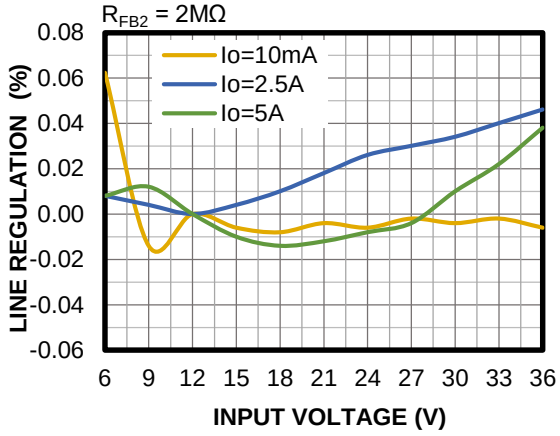
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



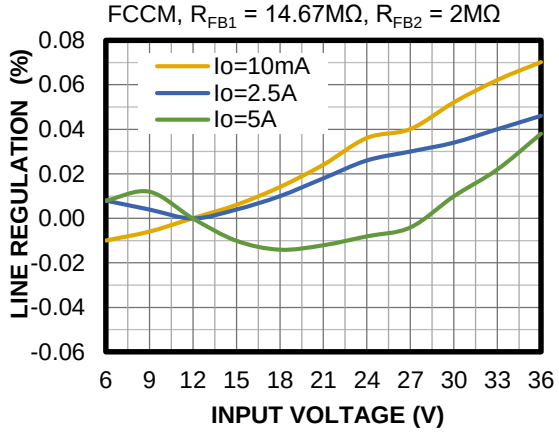
Line Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



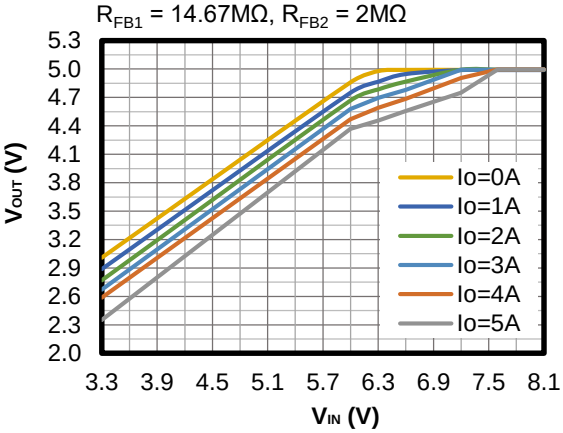
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



Low Dropout

R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



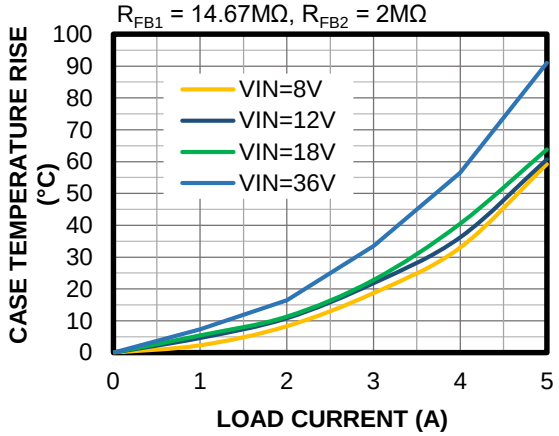
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

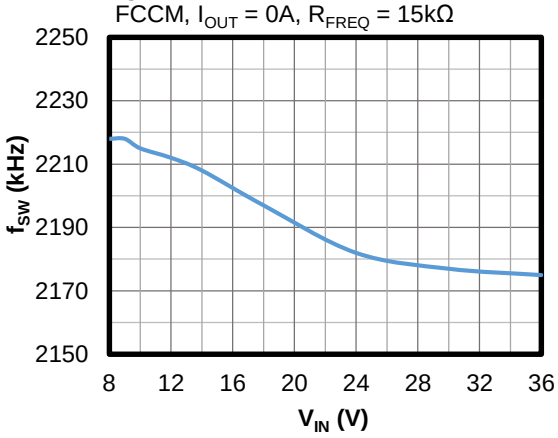
Case Temperature Rise

R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



f_{SW} vs. V_{IN}

FCCM, I_{OUT} = 0A, R_{FREQ} = 15kΩ



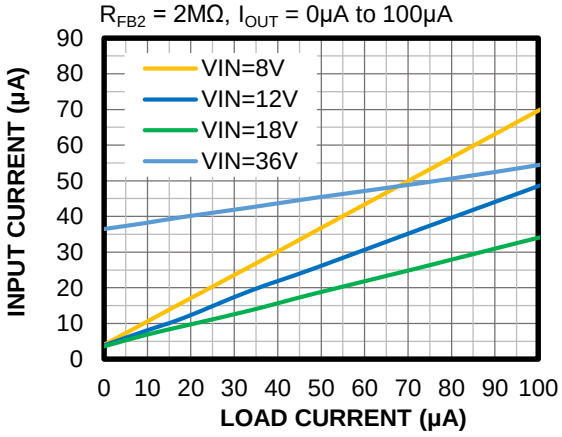
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.

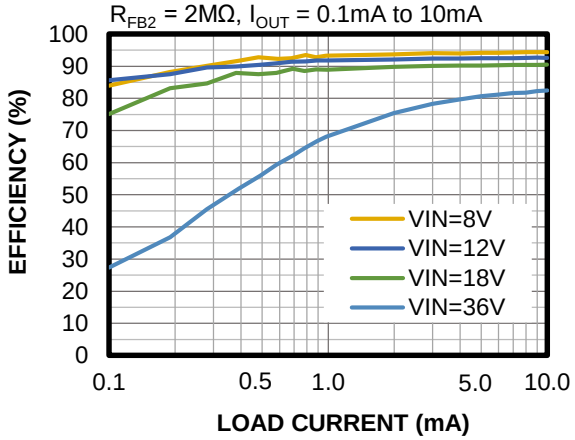
Input Current vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0µA to 100µA



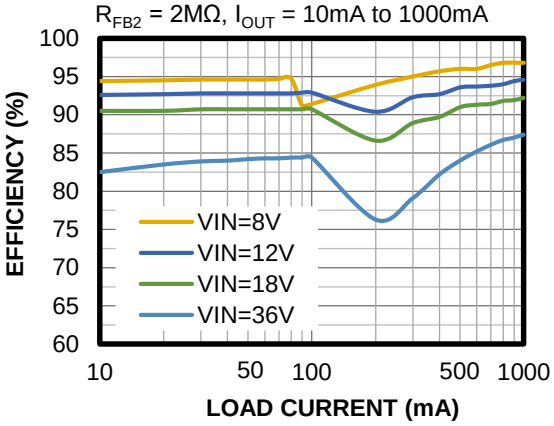
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



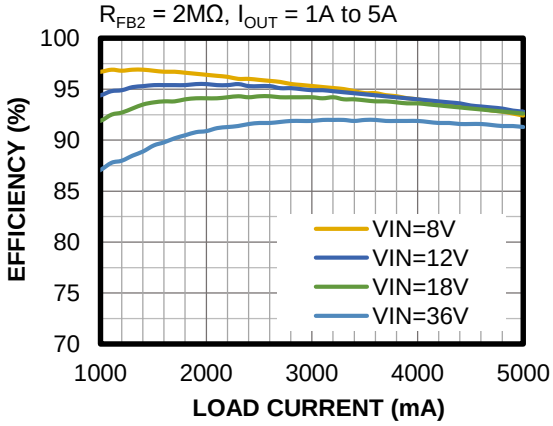
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



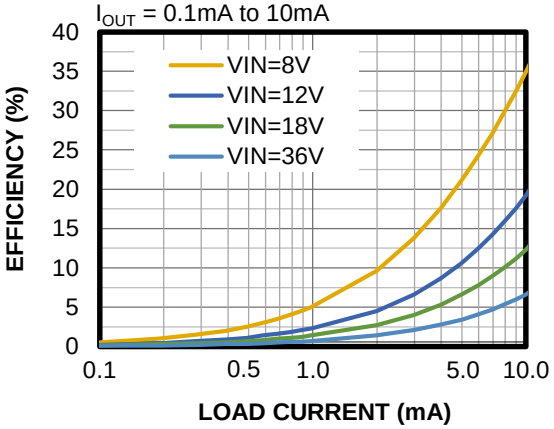
Efficiency vs. Load Current

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



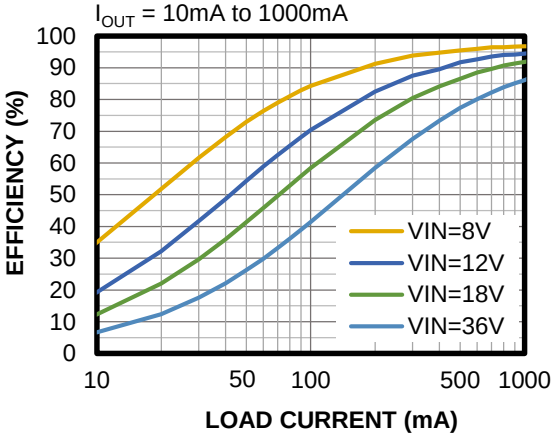
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



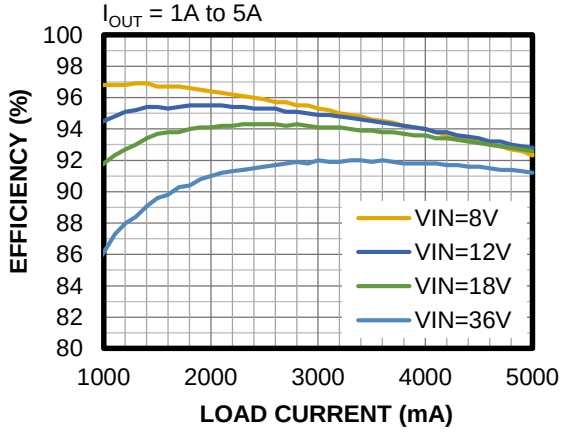
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.

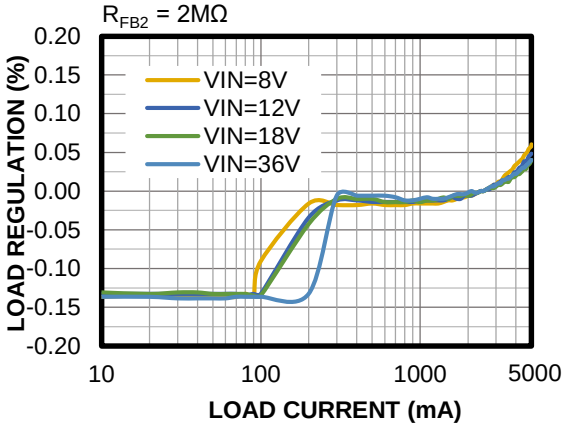
Efficiency vs. Load Current

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



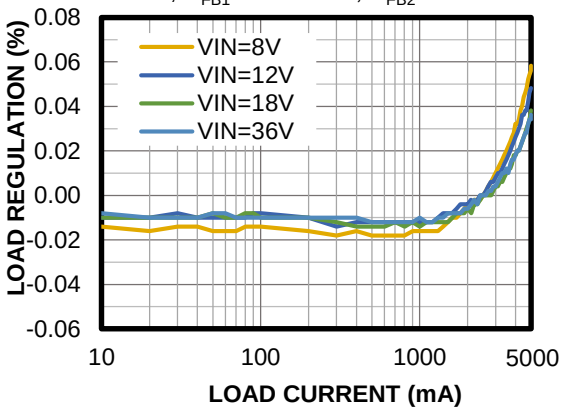
Load Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



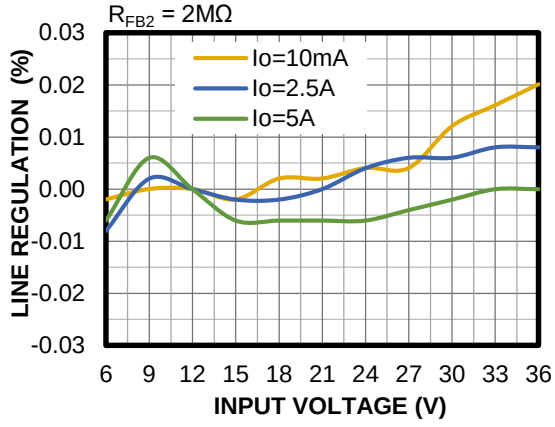
Load Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



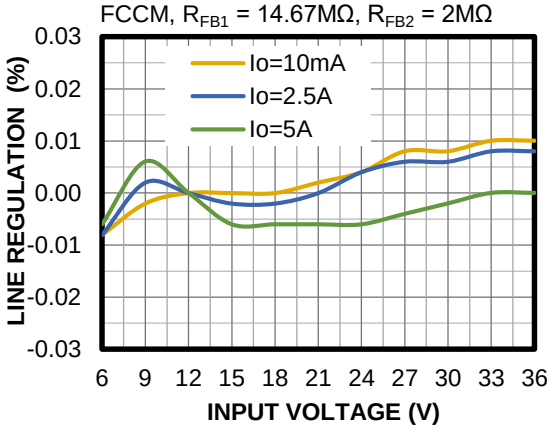
Line Regulation

AAM mode, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



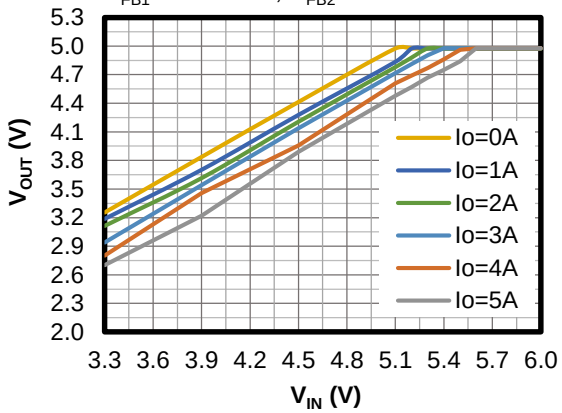
Line Regulation

FCCM, R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



Low Dropout

R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



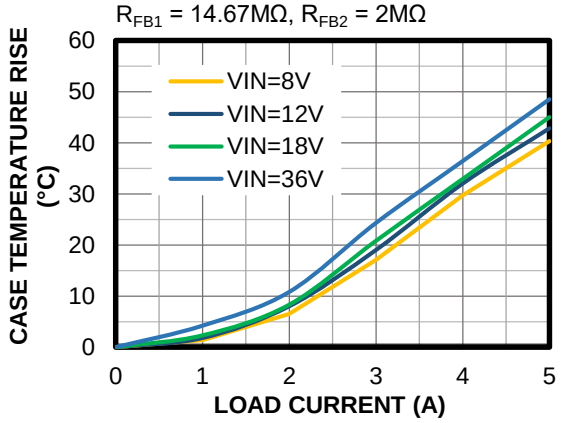
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.

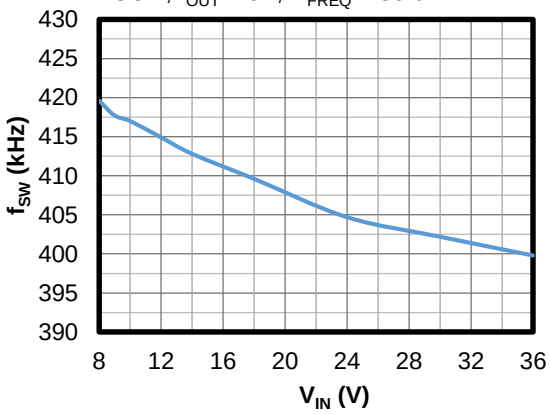
Case Temperature Rise

R_{FB1} = 14.67MΩ, R_{FB2} = 2MΩ



f_{SW} vs. V_{IN}

FCCM, I_{OUT} = 0A, R_{FREQ} = 86.6kΩ



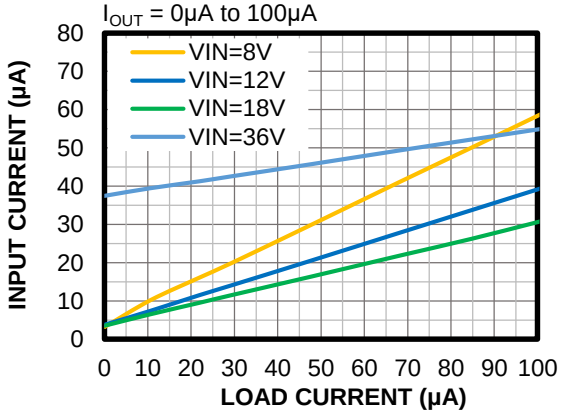
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

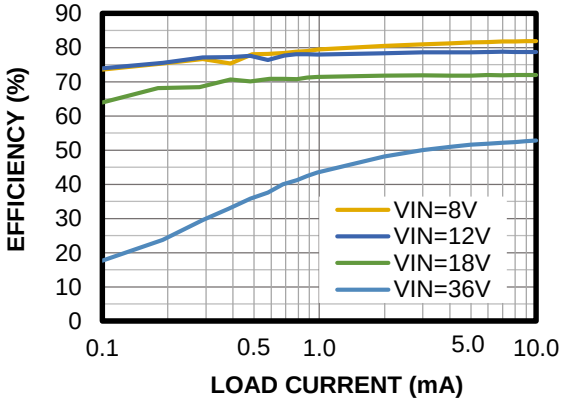
Input Current vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0µA to 100µA



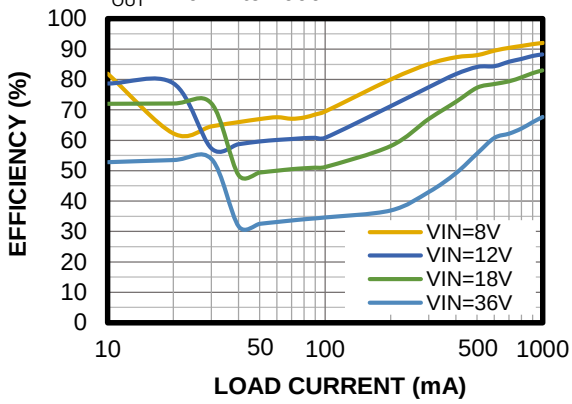
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



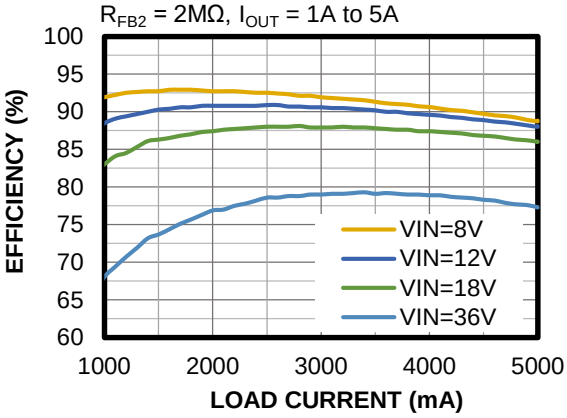
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ I_{OUT} = 10mA to 1000mA



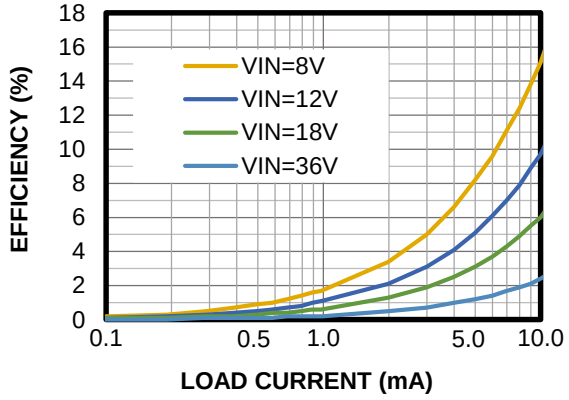
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



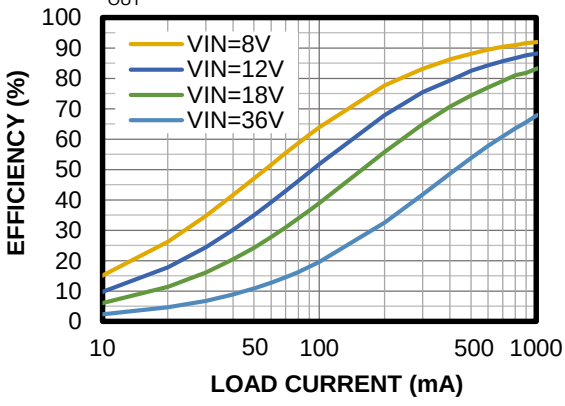
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



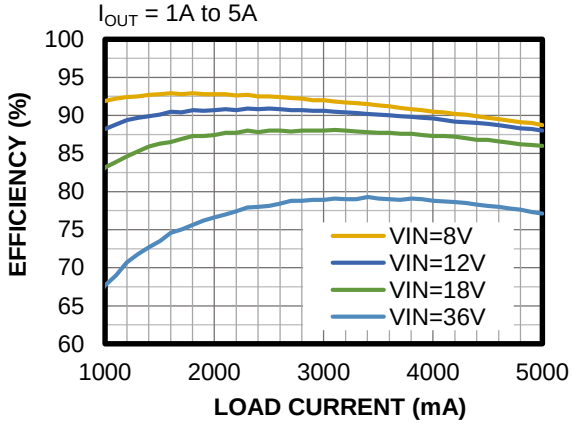
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (DCR = 9.4mΩ), f_{SW} = 2.2MHz, T_A = 25°C, unless otherwise noted.

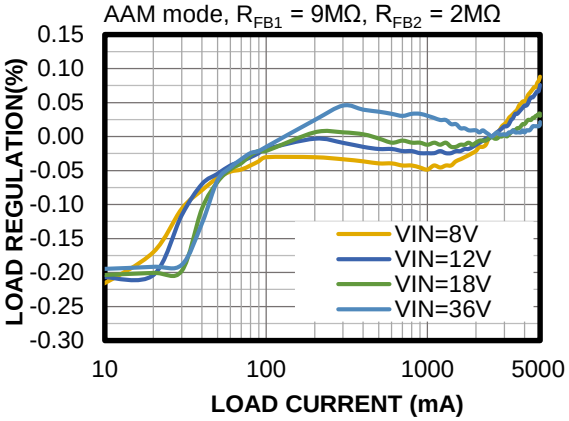
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



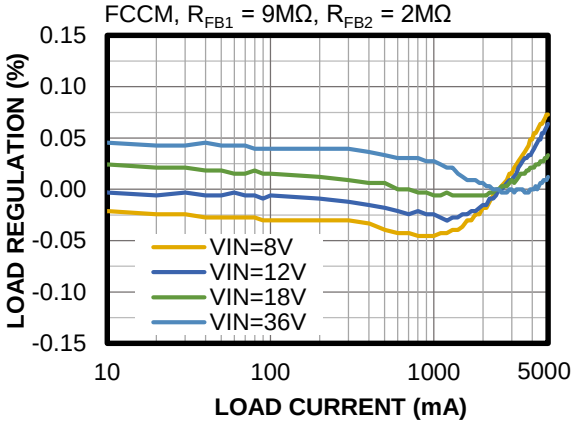
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



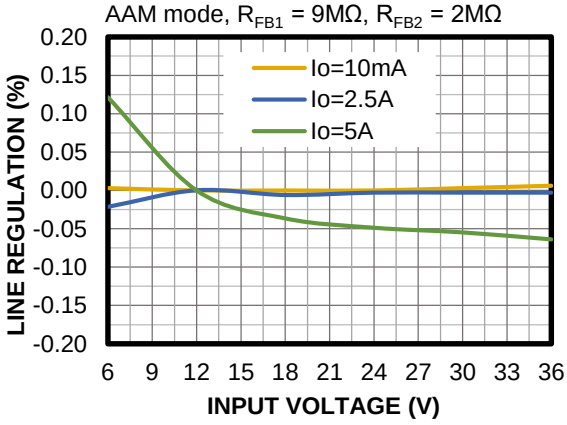
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



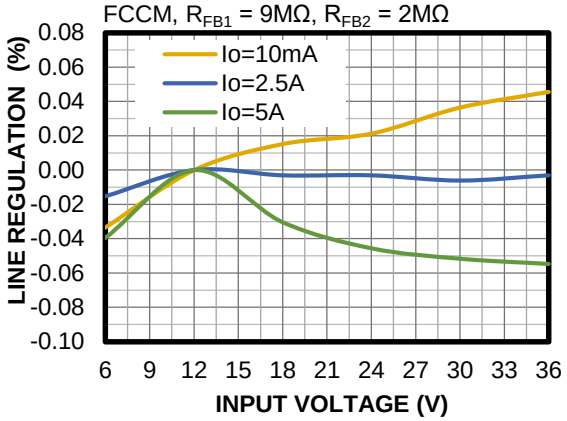
Line Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



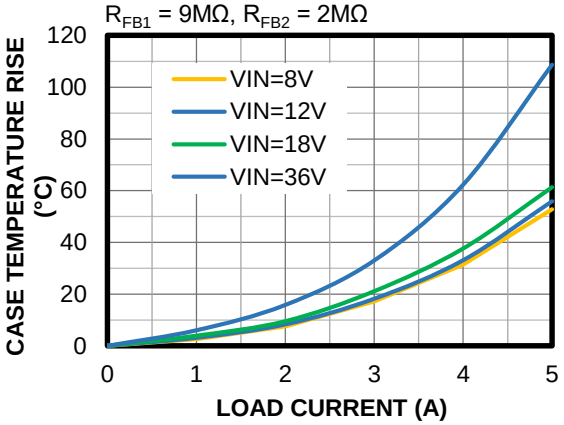
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



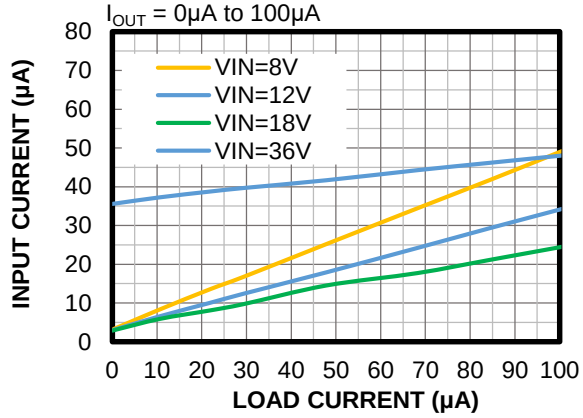
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.

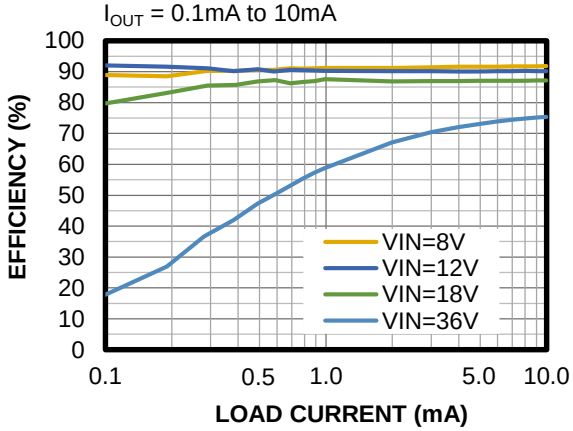
Input Current vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0µA to 100µA



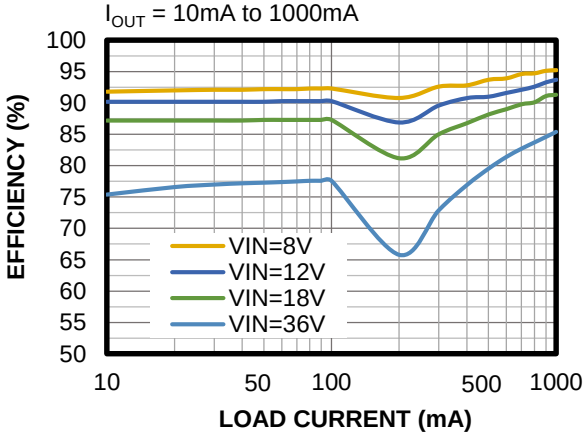
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ I_{OUT} = 0.1mA to 10mA



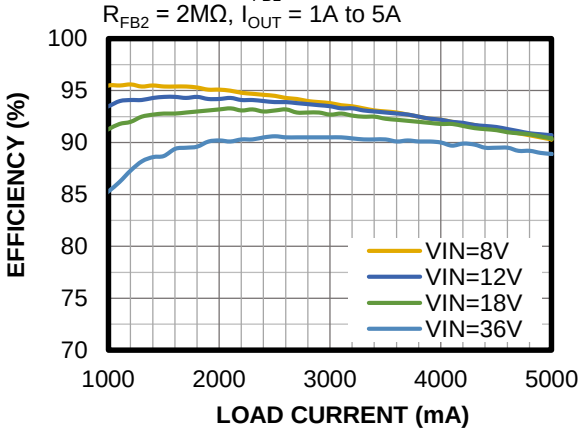
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ I_{OUT} = 10mA to 1000mA



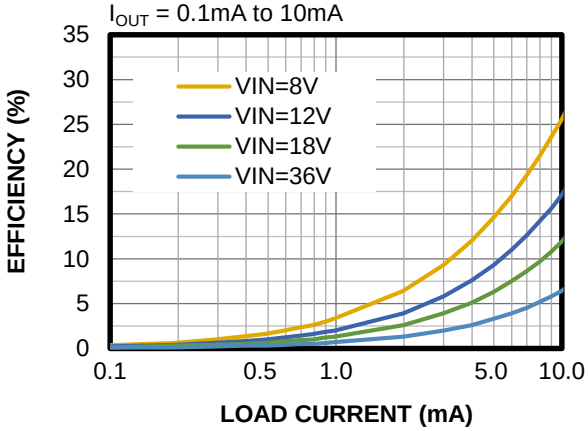
Efficiency vs. Load Current

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 1A to 5A



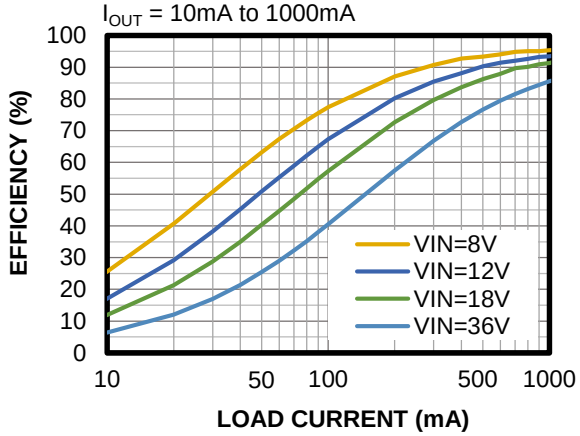
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 0.1mA to 10mA



Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, I_{OUT} = 10mA to 1000mA



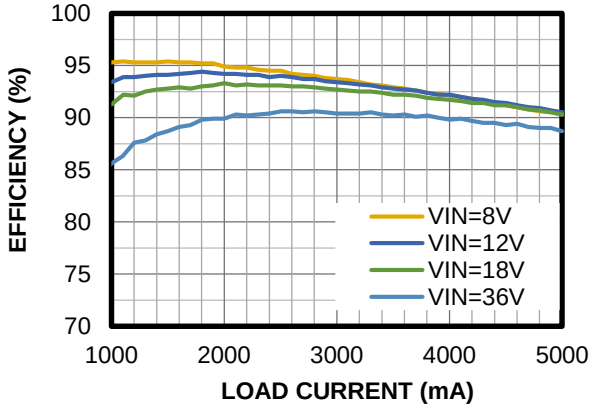
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (DCR = 14.4mΩ), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.

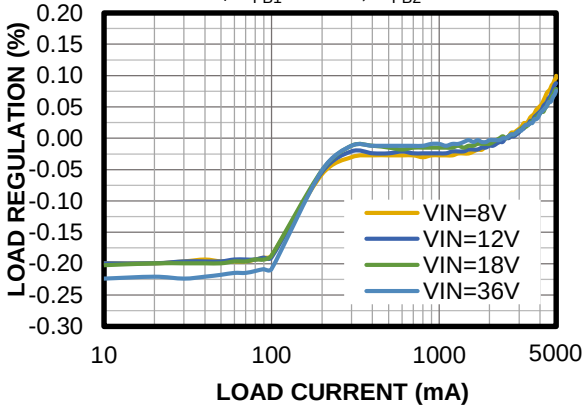
Efficiency vs. Load Current

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ, 1A-5A



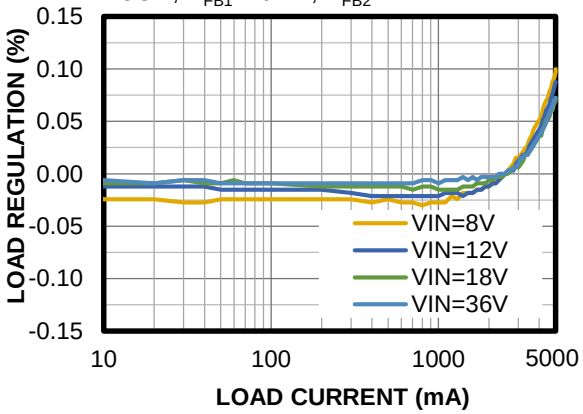
Load Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



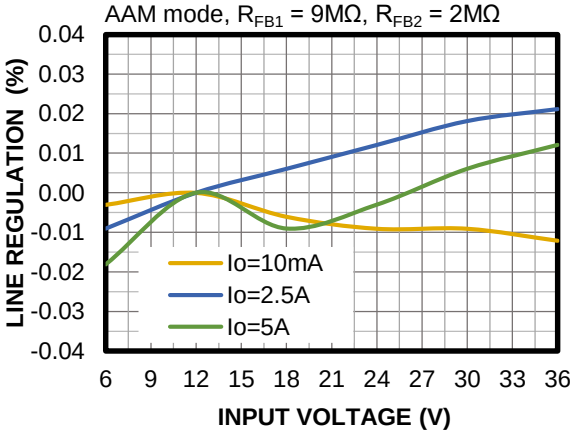
Load Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



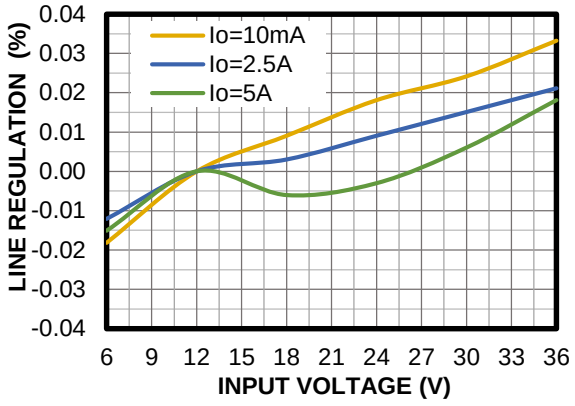
Line Regulation

AAM mode, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



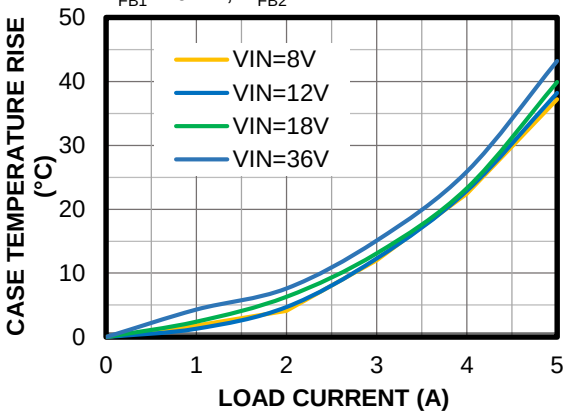
Line Regulation

FCCM, R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



Case Temperature Rise

R_{FB1} = 9MΩ, R_{FB2} = 2MΩ



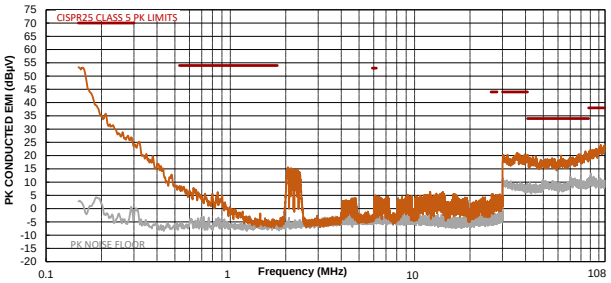
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L= 1µH (10), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (11)

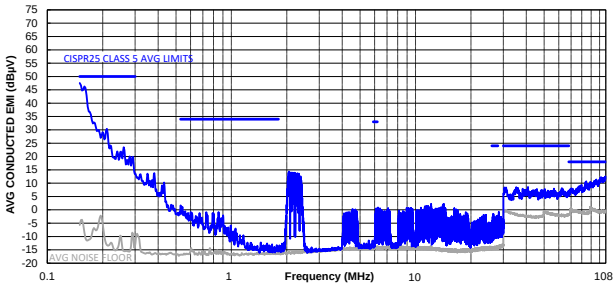
CISPR25 Class 5 Peak Conducted Emissions

150kHz to108MHz



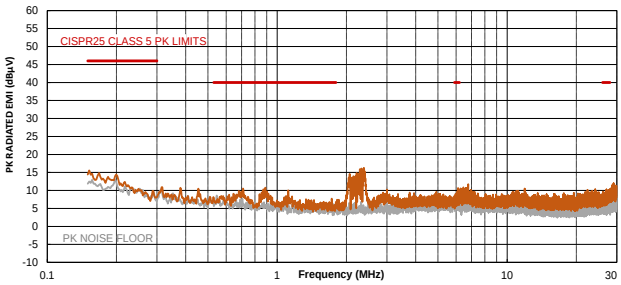
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



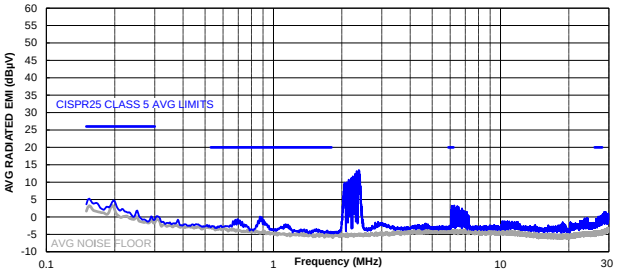
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



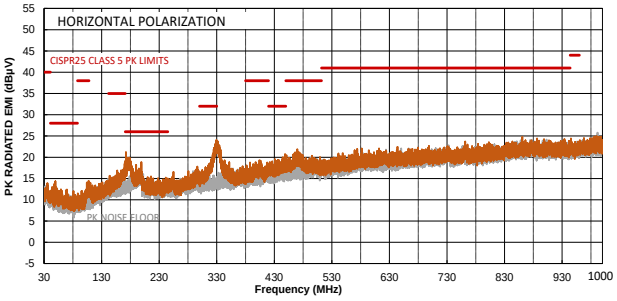
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



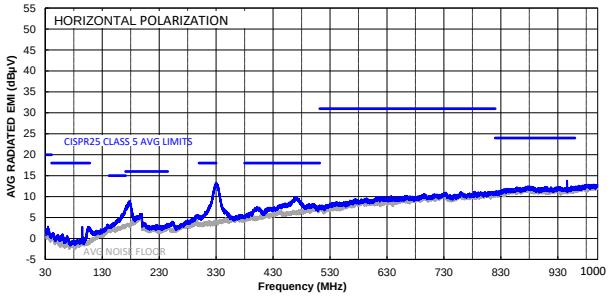
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



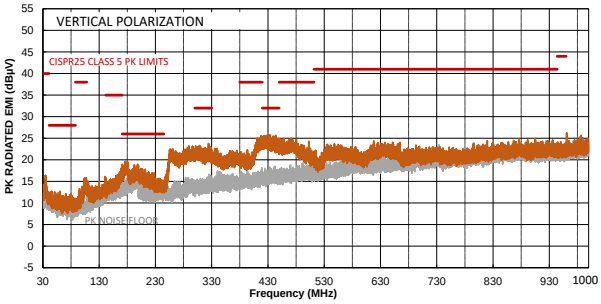
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L= 1µH (10), f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted. (11)

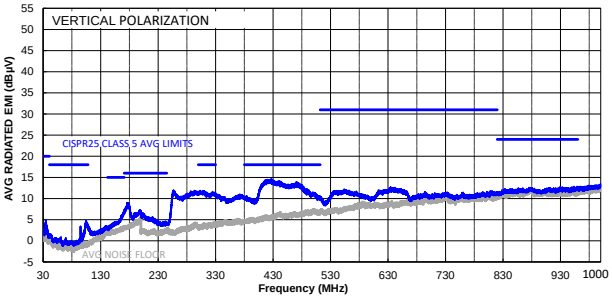
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

10) Inductor part number: XAL5030-102MEB/C; DCR = 9.4mΩ.

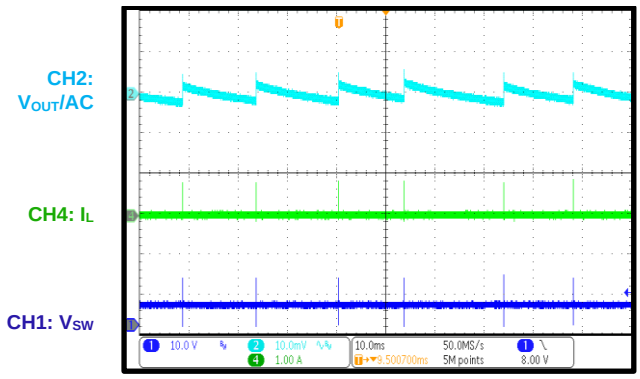
11) The EMC test results are based on the typical application circuit with EMI filters (see Figure 12).

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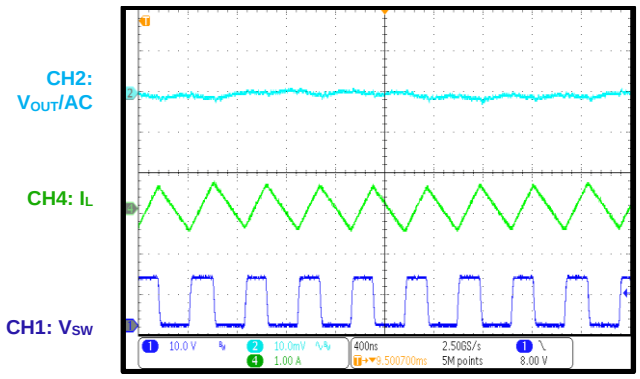
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

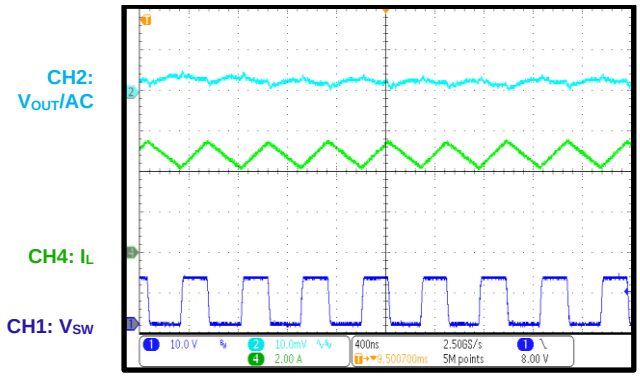
Steady State
I_{OUT} = 0A, AAM mode



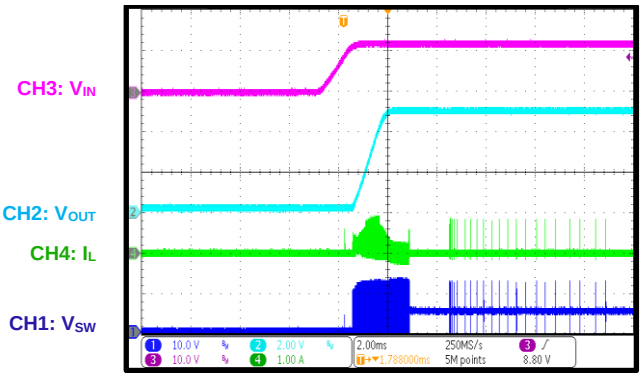
Steady State
I_{OUT} = 0A, FCCM



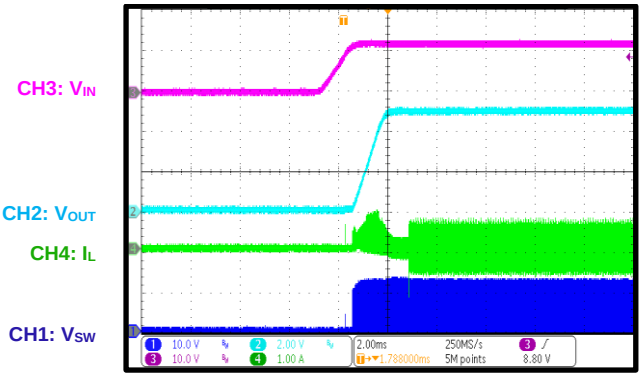
Steady State
I_{OUT} = 5A



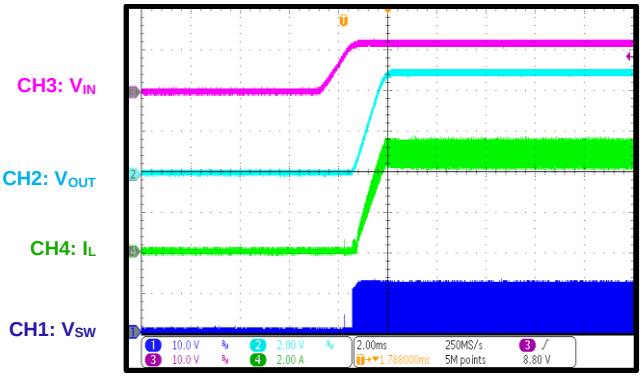
Start-Up through VIN
I_{OUT} = 0A, AAM mode



Start-Up through VIN
I_{OUT} = 0A, FCCM



Start-Up through VIN
I_{OUT} = 5A

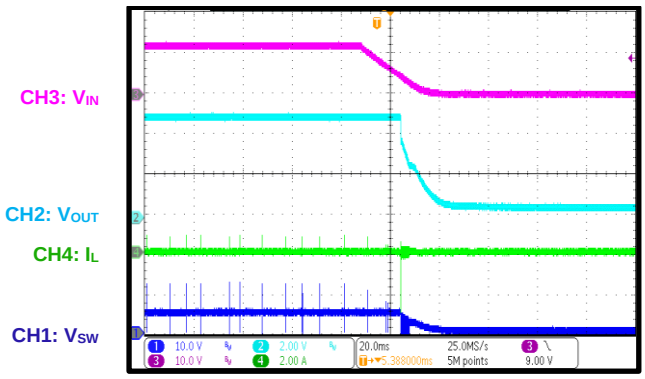


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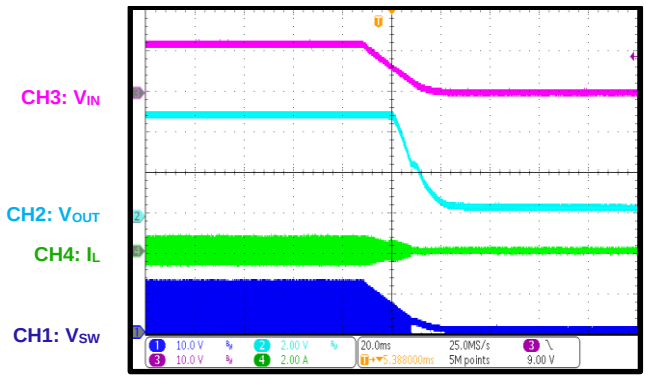
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

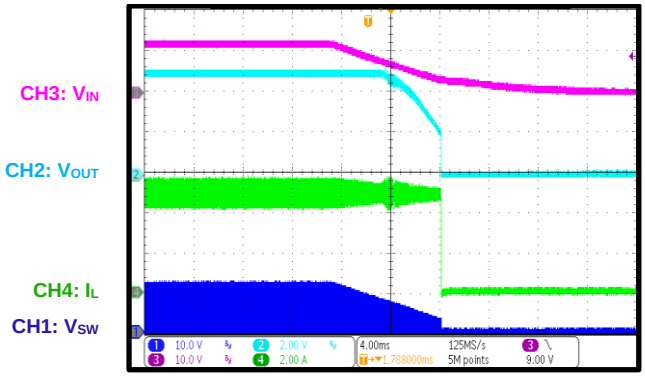
Shutdown through VIN
I_{OUT} = 0A, AAM mode



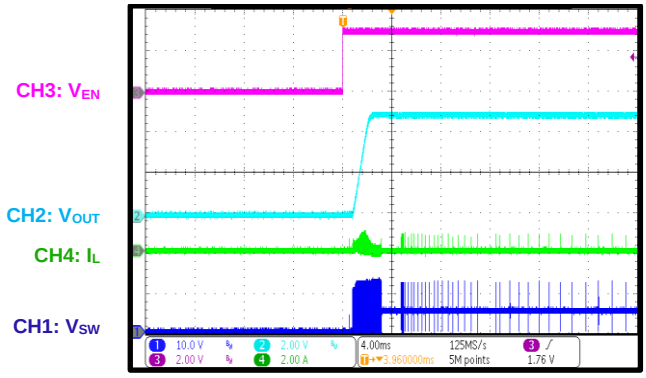
Shutdown through VIN
I_{OUT} = 0A, FCCM



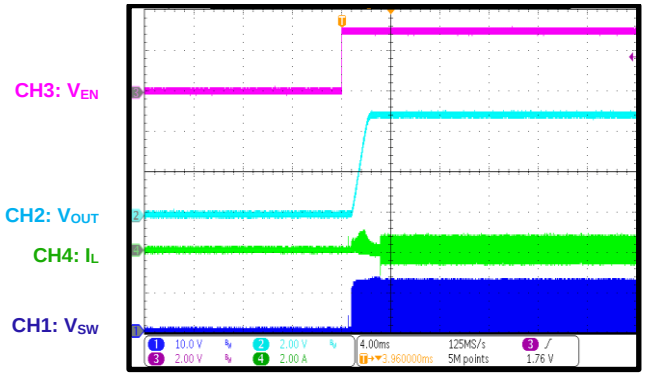
Shutdown through VIN
I_{OUT} = 5A



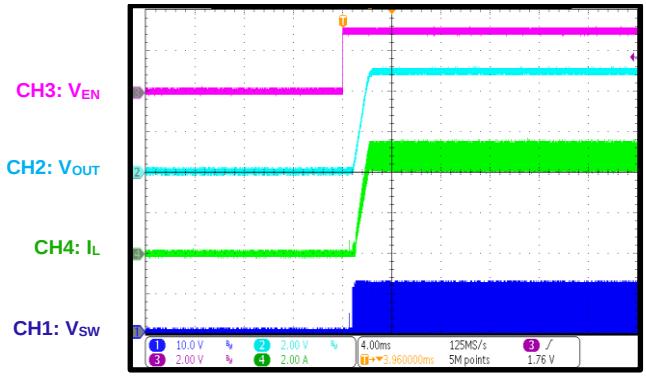
Start-Up through EN
I_{OUT} = 0A, AAM mode



Start-Up through EN
I_{OUT} = 0A, FCCM



Start-Up through EN
I_{OUT} = 5A

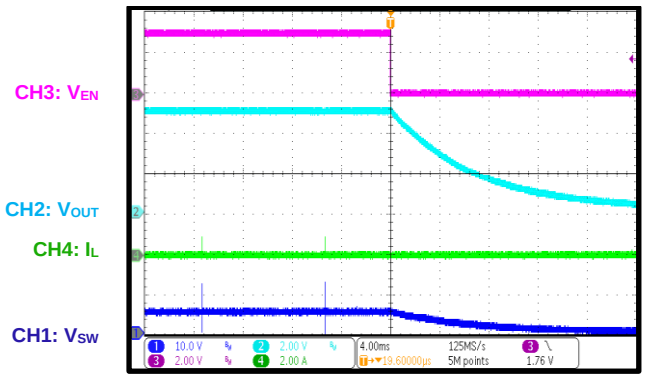


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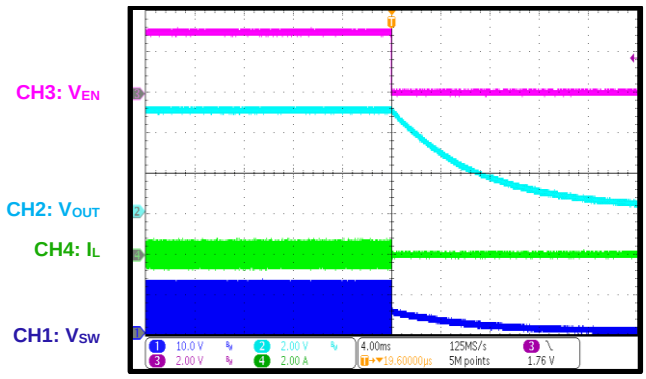
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

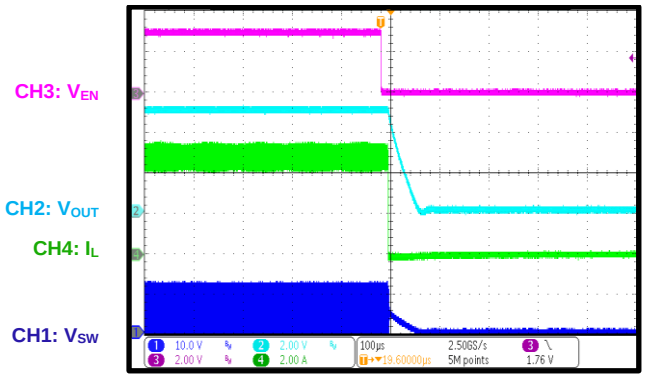
Shutdown through EN
I_{OUT} = 0A, AAM mode



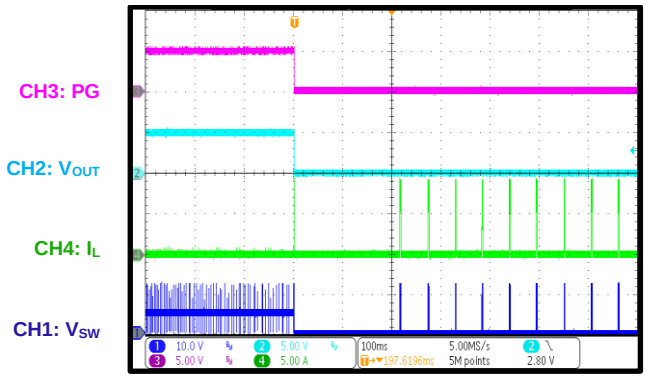
Shutdown through EN
I_{OUT} = 0A, FCCM



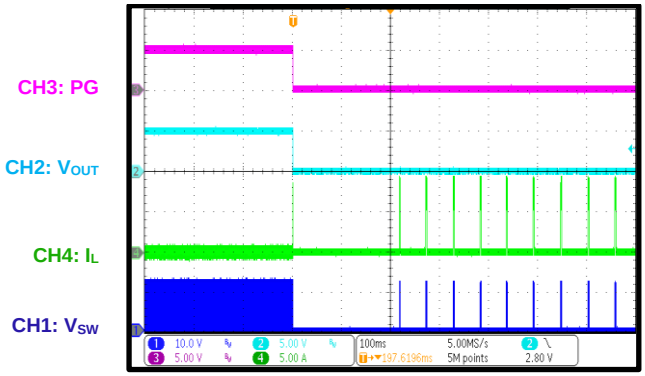
Shutdown through EN
I_{OUT} = 5A



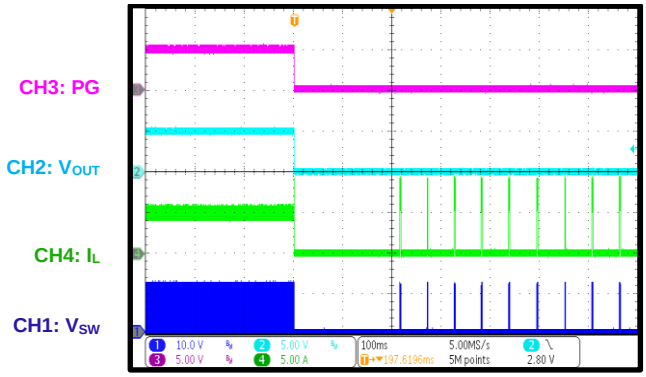
SCP Entry
I_{OUT} = 0A, AAM mode



SCP Entry
I_{OUT} = 0A, FCCM



SCP Entry
I_{OUT} = 5A



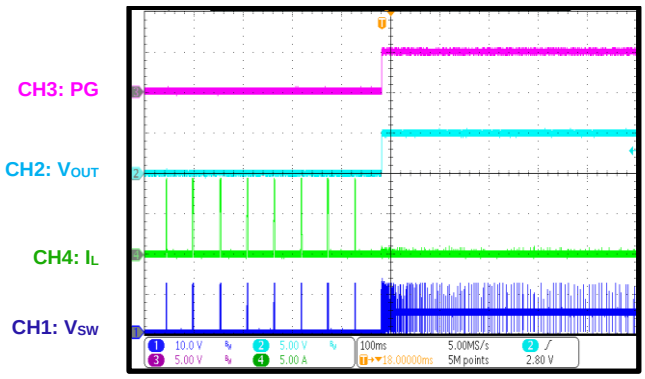
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

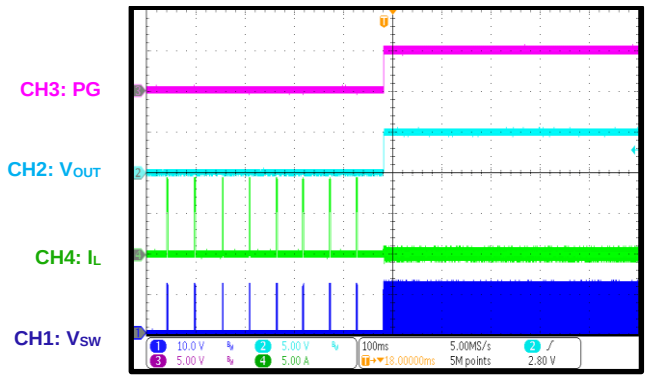
SCP Recovery

I_{OUT} = 0A, AAM mode



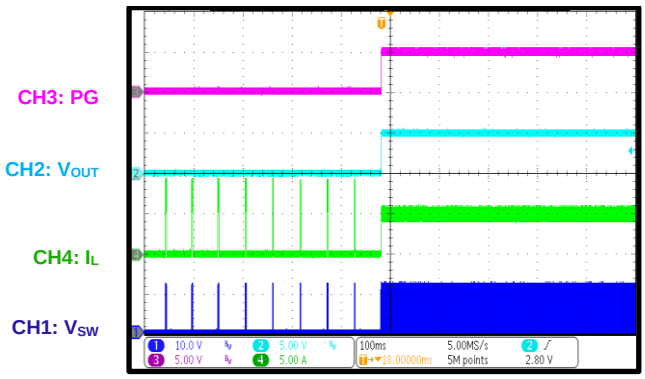
SCP Recovery

I_{OUT} = 0A, FCCM

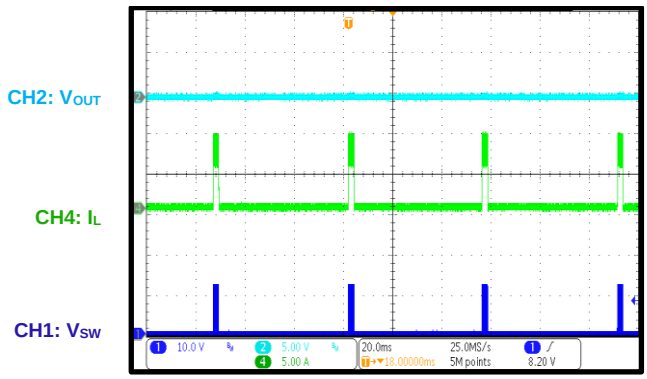


SCP Recovery

I_{OUT} = 5A

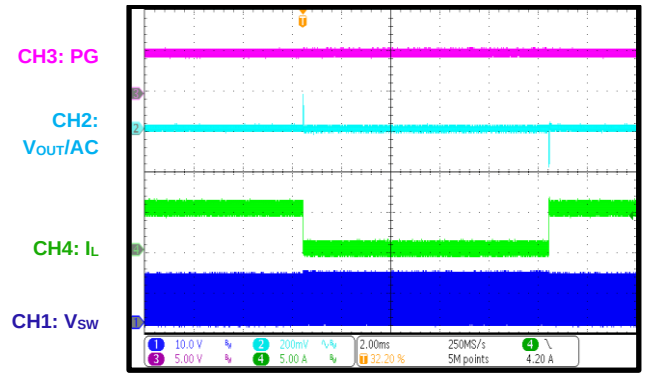


SCP Steady State



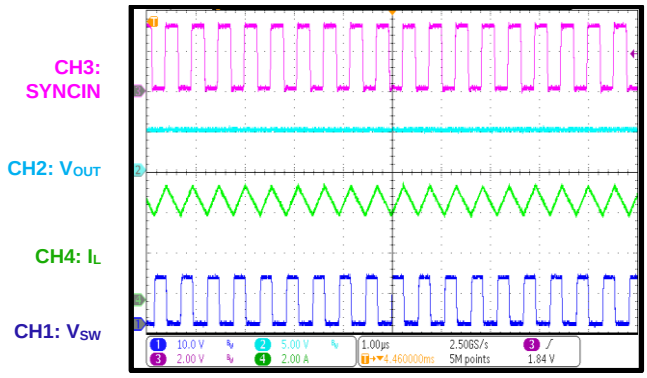
Load Transient

I_{OUT} = 0A to 5A, 1.6A/µs slew rate



SYNCIN Operation

I_{OUT} = 5A, f_{SW} = 2.2MHz, f_{SYNCIN} = 1.9MHz



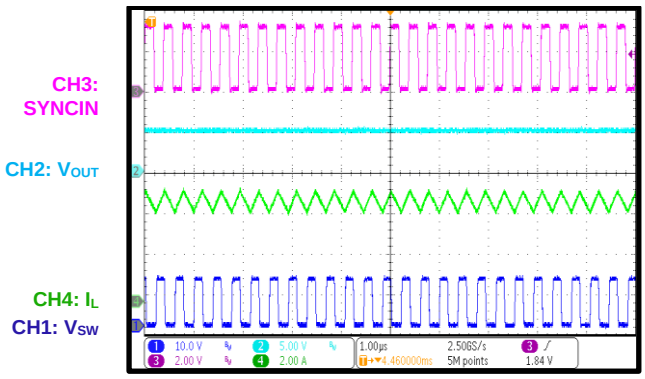
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

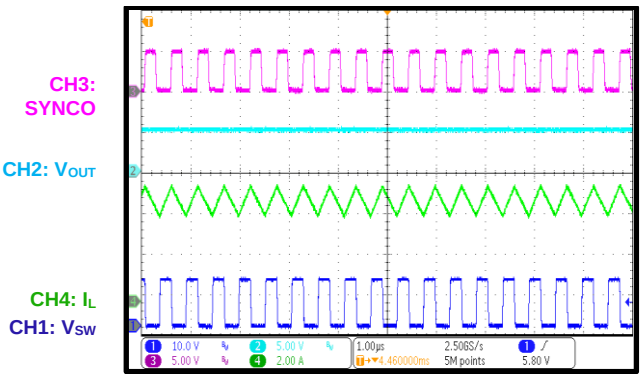
SYNCIN Operation

I_{OUT} = 5A, f_{SW} = 2.2MHz, f_{SYNCIN} = 2.6MHz



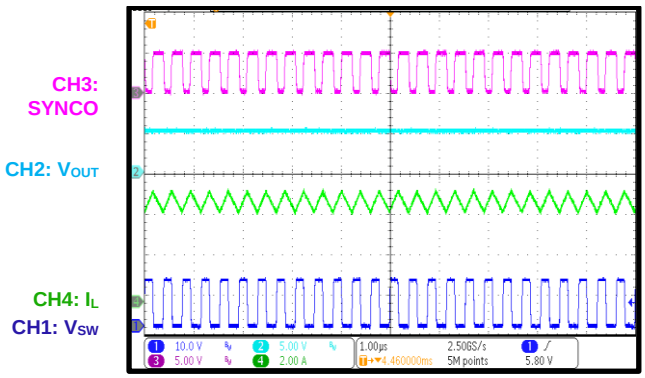
SYNCO Operation

I_{OUT} = 5A, f_{SW} = 2.2MHz, f_{SYNCIN} = 1.9MHz



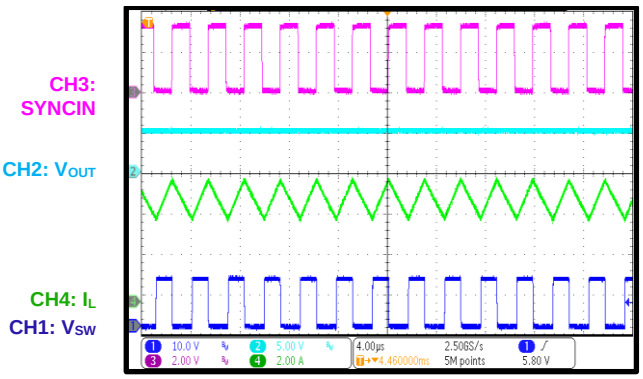
SYNCO Operation

I_{OUT} = 5A, f_{SW} = 2.2MHz, f_{SYNCIN} = 2.6MHz



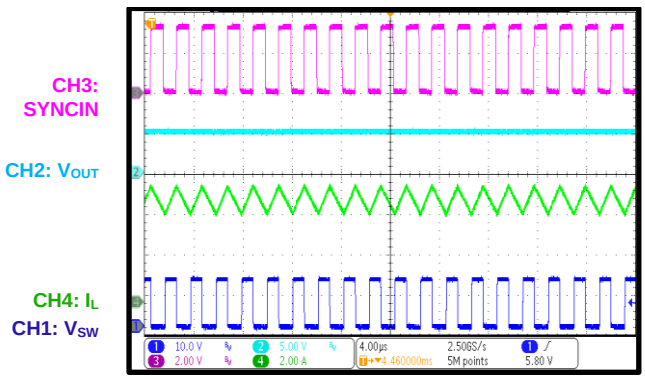
SYNCIN Operation

I_{OUT} = 5A, f_{SW} = 410kHz, L = 4.7µH,
f_{SYNCIN} = 350kHz



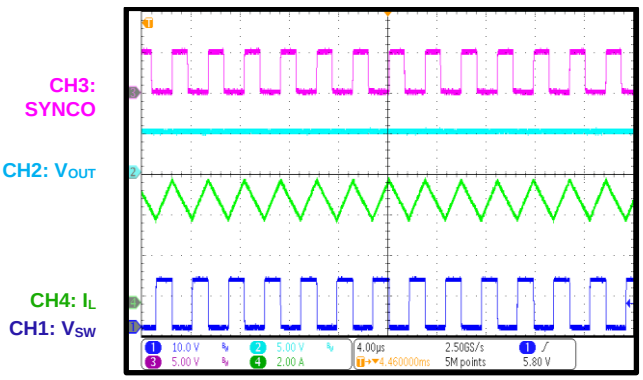
SYNCIN Operation

I_{OUT} = 5A, f_{SW} = 410kHz, L = 4.7µH
f_{SYNCIN} = 480kHz



SYNCO Operation

I_{OUT} = 5A, f_{SW} = 410kHz, L = 4.7µH
f_{SYNCIN} = 350kHz



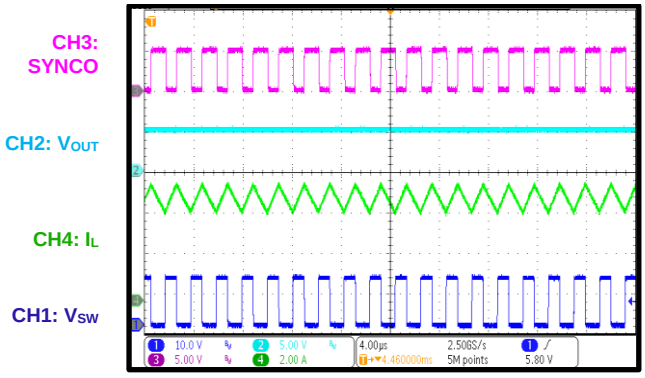
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

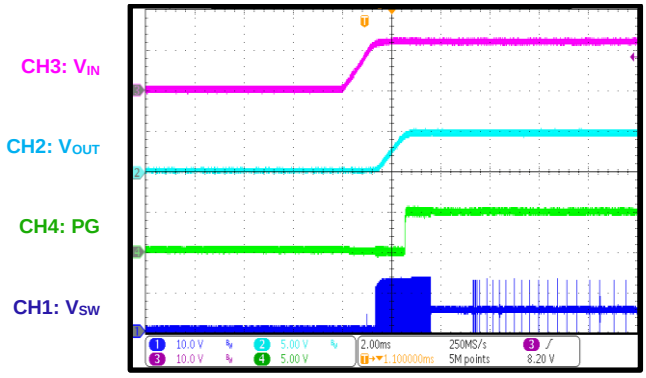
SYNCO Operation

I_{OUT} = 5A, f_{SW} = 410kHz, L = 4.7µH, f_{SYNCIN} = 480kHz



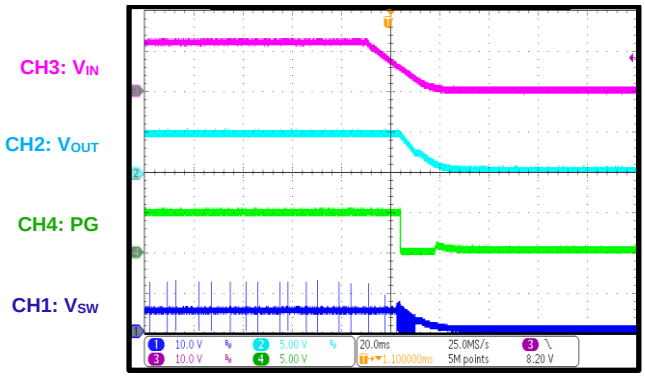
PG Start-Up through VIN

I_{OUT} = 0A, AAM mode



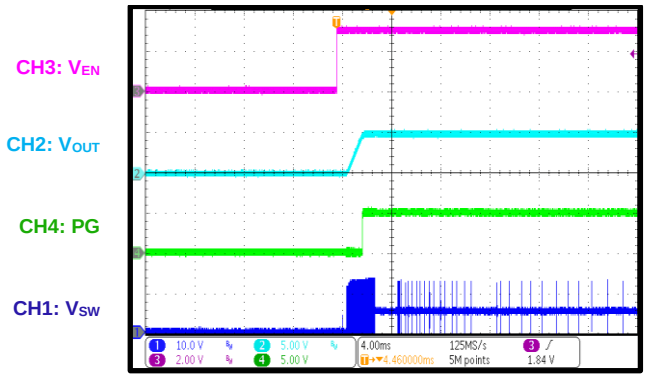
PG Shutdown through VIN

I_{OUT} = 0A, AAM mode



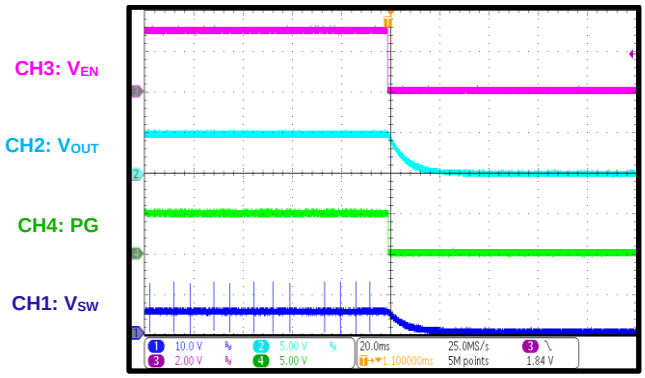
PG Start-Up through EN

I_{OUT} = 0A, AAM mode



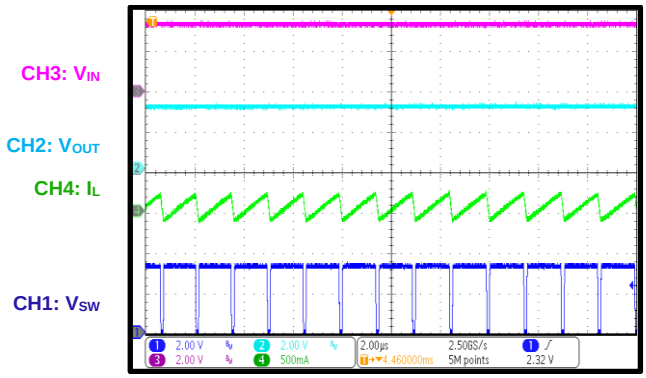
PG Shutdown through EN

I_{OUT} = 0A, AAM mode



Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 5V, I_{OUT} = 0A



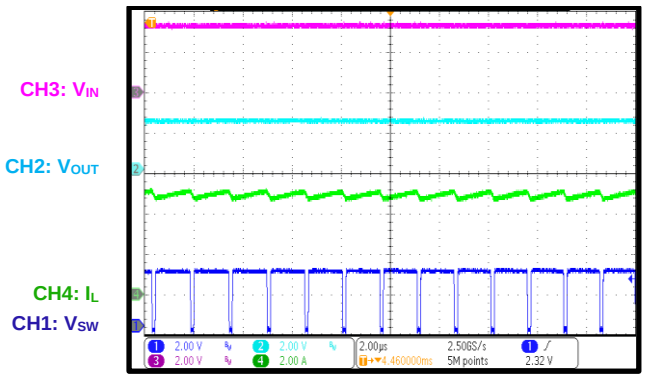
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 1µH, f_{SW} = 2.2MHz, AAM mode, T_A = 25°C, unless otherwise noted.

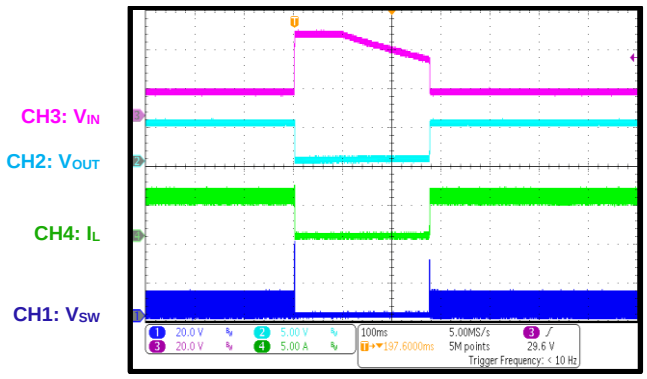
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 5A



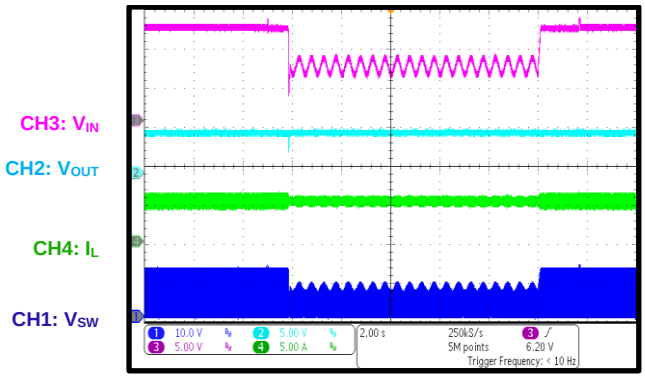
Load Dump

V_{IN} = 12V to 42V, I_{OUT} = 5A



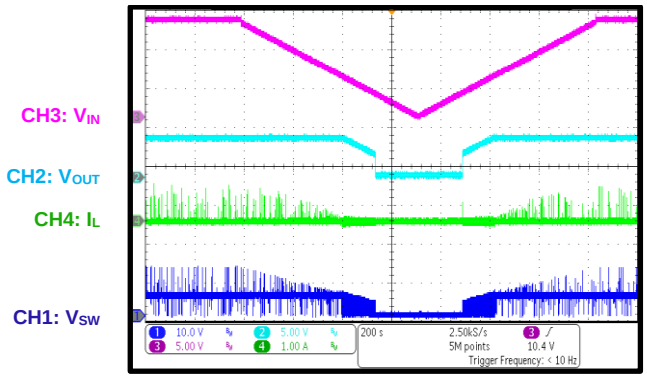
Cold Crank

I_{OUT} = 5A



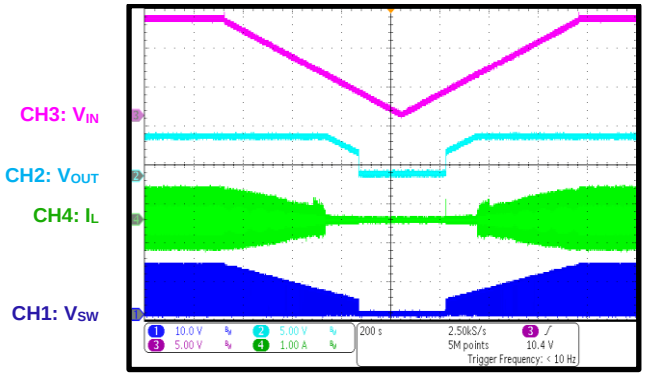
V_{IN} Ramping Up and Down

I_{OUT} = 0A, AAM mode



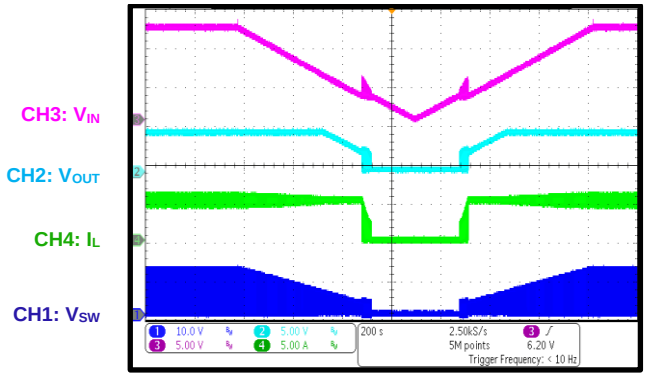
V_{IN} Ramping Up and Down

I_{OUT} = 0A, FCCM



V_{IN} Ramping Up and Down

I_{OUT} = 5A



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FUNCTIONAL BLOCK DIAGRAM

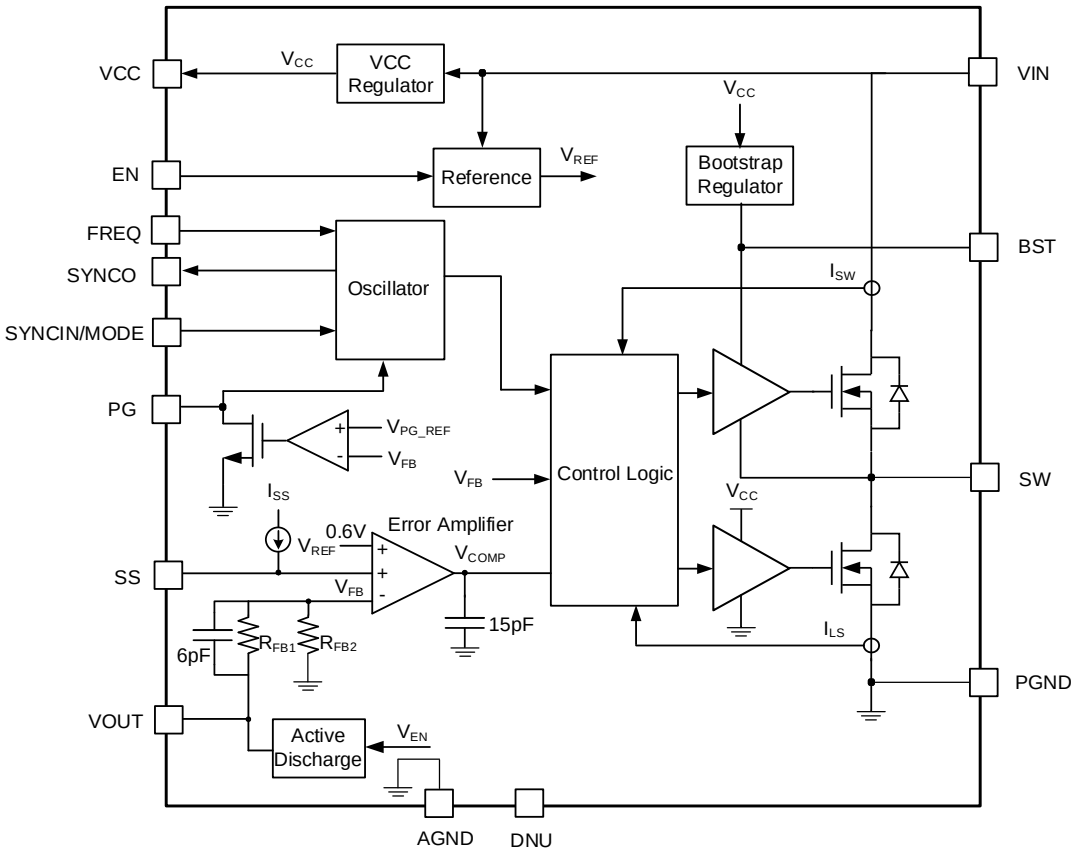


Figure 1: Functional Block Diagram

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OPERATION

The MPQ4348/4348J is a synchronous, step-down switching converter with integrated, internal high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET). It provides up to 5A of highly efficient output current (I_{OUT}) with fixed frequency zero-delay pulse-width modulation (PWM) control.

The MPQ4348/4348J features a wide input voltage (V_{IN}) range, configurable 350kHz to 2.5MHz switching frequency (f_{SW}), external soft start (SS), and precision current limit (I_{LIMIT}). Its very low operational quiescent current (I_Q) makes the MPQ4348/4348J well-suited for battery-powered applications.

Zero-Delay Pulse-Width Modulation (PWM) Control

Automotive applications typically require fixed-frequency operation to reduce EMI, but traditional fixed-frequency control topologies have major limitations. Voltage mode is difficult to compensate for in automotive environments, while peak current mode control cannot always keep up with stringent, modern system-on-chip (SoC) transient requirements without excessive output capacitance. With these requirements in mind, the MPQ4348/4348J introduces fixed-frequency, zero-delay pulse-width modulation (PWM) control.

Zero-delay PWM control combines current information with hysteretic-style output voltage (V_{OUT}) control in a clocked system. This provides a near optimal transient response while maintaining a high phase margin across a wide variety of operating conditions and external component values. In addition, zero-delay PWM control maintains superior EMI performance. The improved transient response reduces the output capacitor (C_{OUT}) requirements and lowers system cost. Trailing-edge modulation facilitates a narrow minimum on time (t_{ON_MIN}) for high conversion ratio applications.

At the beginning of the PWM cycle, the HS-FET turns off, and the LS-FET turns on and remains on until the control signal reaches the comparator voltage (V_{COMP}). The HS-FET remains off for at least 120ns at the beginning of the cycle.

Light-Load Operation

At moderate to high output currents, the MPQ4348/4348J operates at a fixed frequency. Under light-load conditions, MPQ4348/4348J can operate in two different modes by setting the SYNCIN/MODE pin's state.

If the SYNCIN/MODE pin is pulled above 1.8V or an external clock is used, then the MPQ4348/4348J operates in forced continuous conduction mode (FCCM). In FCCM, the device operates with a fixed frequency from no load to full loads. The part has a reverse current limit (-4A) that prevents the negative current from dropping too low and potentially damaging the components. Once the negative inductor current (I_L) reaches the reverse current limit, the LS-FET turns off and the HS-FET turns on. The advantage of FCCM is the constant frequency and lower output ripple at light loads.

If the SYNCIN/MODE pin is pulled below 0.4V then the MPQ4348/4348J operates in advanced asynchronous modulation (AAM) mode. The device cannot enter AAM mode until SS completes. AAM mode optimizes efficiency under light-load and no-load conditions.

In AAM mode, the LS-FET emulates a diode, and the HS-FET has a fixed one-shot on time to charge the inductor and regulate the output. As the load decreases, the interval between one-shots increases. If this interval exceeds 8µs, the part enters sleep mode, which turns off some of the internal circuitry and extends the on time to achieve an ultra-low I_Q.

As the load increases, the interval decreases to be shorter than 6µs, and the part exits sleep mode and enters AAM mode again. In AAM mode, the part employs a zero-current detection (ZCD) circuit to turn off the LS-FET and prevent negative I_L flow under light-load conditions. If the SYNCIIN/MODE pin is pulled high, the device exits AAM mode. If a fault occurs, such as an over-voltage (OV) or over-temperature (OT) fault, the internal circuitry is not disabled in sleep mode.

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Frequency Spread Spectrum (FSS)

The MPQ4348/4348J uses a 12kHz modulation frequency with a 128-step triangular profile to spread the internal f_{SW} across a 20% (±10%) window. The absolute frequency step size varies proportionally with f_{SW} to maintain the ±10% frequency spread spectrum (FSS) (see Figure 2).

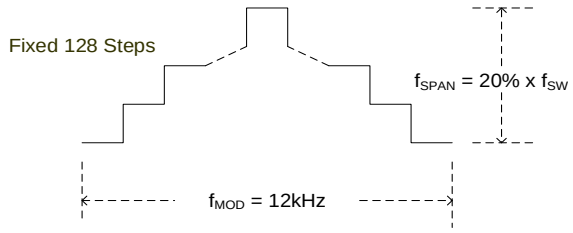


Figure 2: Frequency Spread Spectrum (FSS)

Sidebands are created by modulating f_{SW} with the triangle modulation waveform. The emission power of the fundamental f_{SW} and its harmonics is distributed into smaller pieces. This significantly reduces EMI noise.

Low-Dropout (LDO) Mode

When V_{IN} drops to about 7V, the MPQ4348/4348J folds back the frequency. When V_{IN} is almost equal to V_{OUT}, the device enters low-dropout (LDO) mode. This allows for a shorter off time to achieve a higher duty cycle.

The effective duty cycle during the device's dropout period is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the LS-FET diode, and the PCB resistance.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the device starts up. The reference block starts first, generating a stable reference voltage (V_{REF}) and currents, then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50usec to blank the start-up glitches. When the SS block is enabled, it first holds its SS output low to ensure that the remaining circuitry are ready. Then the SS block ramps up slowly.

Three events can shut down the chip: V_{EN} going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked first to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

SYNCIN and SYNCO

f_{SW} can be synchronized to the rising edge of a clock signal applied to the SYNCIN/MODE pin. The recommended SYNCIN frequency range is between 90% and 115% of f_{SW}, which is set by an external frequency resistor.

The SYNCO pin can output a clock signal in phase with the internal oscillator signal (inverter to switching clock), or the external SYNCIN frequency.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermal runaway. When the silicon die temperature exceeds its upper threshold (170°C), the power MOSFETs shut down. Once the temperature drops below its lower threshold (150°C), the thermal shutdown condition is removed, and the chip initiates a SS to resume normal operation.

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APPLICATION INFORMATION

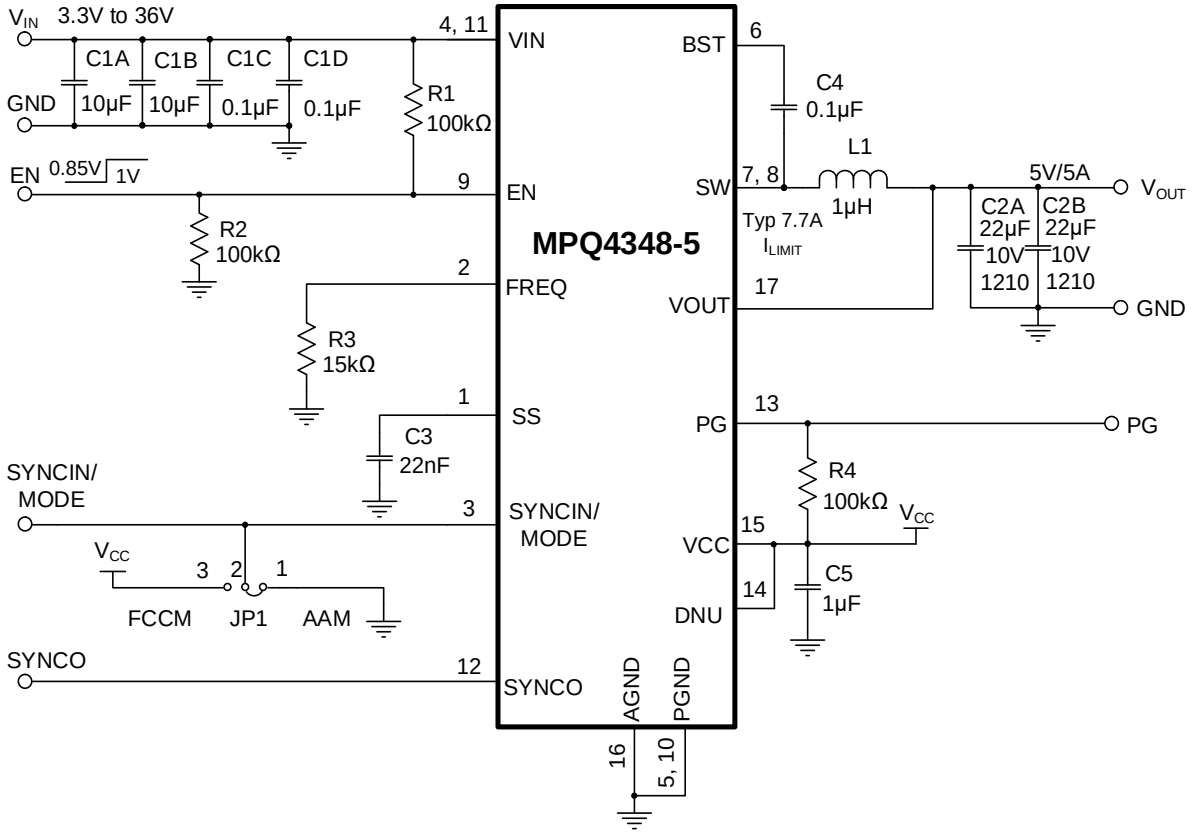


Figure 3: Typical Application Circuit for the MPQ4348GLE-5 (V_{OUT} = 5V, f_{SW} = 2.2MHz)

Table 1: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
1	SS	C3	See the Selecting the Soft-Start Capacitor (C_{SS}) section on page 36
2	FREQ	R3	See the Switching Frequency (f_{SW}) Setting section on page 36
3	SYNCIN/MODE		See the SYNCIN and Mode Selection section on page 36
4, 11	VIN	C1A, C1B, C1C, C1D	See the Selecting the Input Capacitor (C_{IN}) section on page 37
5, 10	PGND		See the Connection to GND section on page 40
6	BST	C4	See the Bootstrap (BST) Charging section on page 37
7,8	SW	L1, C2A, C2B	See the Selecting the Output Capacitor (C_{OUT}) section on page 37 and the Selecting the Inductor section on page 38
9	EN	R1, R2	See the Enable (EN) and V_{IN} Under-Voltage Lockout (UVLO) Protection section on page 38
12	SYNCO		See the SYNCO section on page 39
13	PG	R4	See the Power Good (PG) section on page 39
14	DNU		See the DNU section on page 39
15	VCC	C5	See the Selecting the VCC Capacitor (V_{CC}) section on page 39
16	AGND		See the Connection to GND section on page 40
17	VOUT		See the Output Voltage (V_{OUT}) Setting section on page 39

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Selecting the Soft-Start Capacitor (C_{SS})

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

During SS, an internal current source charges the external soft-start capacitor (C_{SS}). If the soft-start voltage (V_{SS}) drops below the internal V_{REF}, V_{SS} overrides V_{REF}, and the error amplifier (EA) uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} regains control.

C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 16.6 \times t_{SS}(ms) \quad (1)$$

The SS pin can be used for tracking and sequencing.

Switching Frequency (f_{SW}) Setting

f_{SW} can be configured by an external resistor connected from the FREQ pin to ground, placed as close to the device as possible.

The resistance that sets f_{SW} (R_{FREQ}/R3) can be selected using the f_{SW} vs. R_{FREQ} curves. Figure 4 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 1000kHz and 2500kHz.

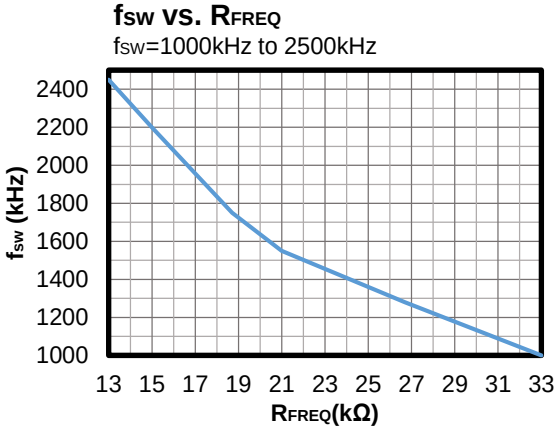


Figure 4: f_{SW} vs. R_{FREQ} (f_{SW} = 1000kHz to 2500kHz)

Figure 5 shows the f_{SW} vs. R_{FREQ} curve when f_{SW} is between 350kHz and 1000kHz.

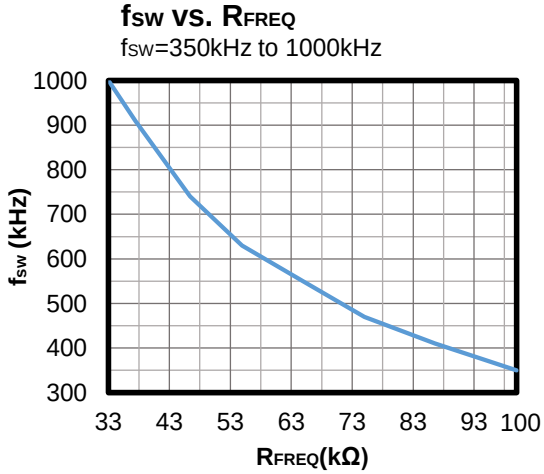


Figure 5: f_{SW} vs. R_{FREQ} (f_{SW} = 350kHz to 1000kHz)

Table 2 shows some common f_{SW} for different R_{FREQ} values.

Table 2: Common f_{SW} for Different R_{FREQ}

R_{FREQ} (kΩ)	f_{SW} (kHz)
100	350
86.6	410
75	470
64.9	550
54.9	630
46.4	740
37.4	910
33	1050
26.7	1280
21	1550
18.7	1750
15	2200
13	2450

SYNCIN and Mode Selection

When the SYNCIN/MODE pin is used as the SYNC input pin (SYNCIN), f_{SW} can be synchronized to the rising edge of a clock signal applied to the SYNCIN/MODE pin. The recommended SYNCIN frequency range is between 90% and 115% of f_{SW}.

When SYNCIN/MODE is used for mode selection (MODE), pulling this pin high forces the device to operate in FCCM. Pulling MODE low forces the device to operate in AAM mode (see Table 3).

Table 3: Mode Selection

SYNCIN/MODE Input	Operation Mode
<0.4V	AAM mode
>1.8V	FCCM
External clock in	FCCM

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Selecting the Input Capacitor (C_{IN})

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC V_{IN}. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current for C_{IN} (I_{CIN}) can be estimated with Equation (2):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, which can be calculated with Equation (3):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The V_{IN} ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

V_{IN} Over-Voltage Protection (OVP)

The MPQ4348/48J has a built-in V_{IN} over-voltage protection (OVP) circuit. V_{IN} OVP is active at 25V. If V_{IN} exceeds the OVP protection threshold (typically 38V), the LS-FET turns on until I_L is fully discharged, and then turns off. Once V_{IN} drops below the OVP falling threshold (typically 28V) and the hiccup restart delay time expires, the device initiates a SS to resume normal operation.

Bootstrap (BST) Charging

It is recommended that the bootstrap (BST) capacitor (C_{BST}/C4) be between 0.1µF to 0.22µF**.**

It is not recommended to place a resistor (R_{BST}) in series with C_{BST}, unless there is a strict EMI requirement. R_{BST} helps enhance EMI performance and reduce voltage stress at high input voltages. It also increases power consumption and reduces efficiency. When R_{BST} is necessary, it should be below 10Ω.

C_{BST} is charged and regulated to about 5V by the dedicated internal BST regulator. When the voltage between the BST and SW pins is below its regulation voltage, an N-channel MOSFET pass transistor connected from VCC to BST turns on to charge C_{BST}. The external circuit should provide enough voltage headroom to facilitate charging.

When the HS-FET is on, the BST voltage (V_{BST}) exceeds V_{CC}, and C_{BST} cannot be charged.

At higher duty cycles, the time available for BST charging is shorter, so C_{BST} may not be charged sufficiently. If the external circuit has an insufficient voltage and not enough time to charge C_{BST}, use additional external circuitry to ensure that V_{BST} remains within the normal operation range.

Selecting the Output Capacitor (C_{OUT})

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the V_{OUT} ripple (ΔV_{OUT}) low. ΔV_{OUT} can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (5)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of C_{OUT}.

For ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can

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be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (7)$$

The characteristics of C_{OUT} also affect the stability of the regulation system. The part can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can be calculated with Equation (8):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current (I_{LP}) can be calculated with Equation (9):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

Peak and Valley Current Limits

Both the HS-FET and LS-FET have cycle-by-cycle current-limit protection. If I_L reaches the high-side (HS) peak current limit (typically 7.7A) or the internal clock's rising edge while the current is rising and the HS-FET is on, the HS-FET is forced off immediately to prevent the current from rising further. If the LS-FET is on, the valley current limit circuit blocks the PWM comparator from turning on the HS-FET until I_L drops below the low-side (LS) valley current limit (typically 5.9A). This current limit scheme prevents current runaway if an overload fault or short circuit occurs.

Short-Circuit Protection (SCP)

If the output is shorted to ground, V_{OUT} drops below 70% of its nominal output, and the LS-FET current exceeds the valley current limit (5.9A). Then the device turns on the LS-FET until the I_L is fully discharged. The device also begins slowly discharging C_{SS}. Once C_{SS} is fully discharged, the device initiates an SS to resume normal operation. This hiccup process is repeated until the fault is removed.

Output Over-Voltage Protection (OVP) and Discharge

There is an internal V_{OUT} OVP circuit. While the device is operating in discontinuous conduction mode (DCM) and V_{OUT} exceeds 106% of the target voltage, an output discharge path from VOUT to GND is activated to V_{OUT}. The output discharge path remains active until the part returns to regulation and resumes switching.

If V_{OUT} exceeds 106% of the target voltage in FCCM, the output discharge path turns on. If the negative current limit is triggered 265 times, the part enters hiccup mode and stops switching. Once V_{OUT} drops to or below 105%, the device initiates a new SS. The V_{OUT} discharge path remains on until V_{OUT} reaches its regulated value, and the device starts switching.

Enable (EN) and V_{IN} Under-Voltage Lockout (UVLO) Protection

EN is a digital control pin that turns the converter on and off.

Enabled by External Logic High/Low Signal

When the EN voltage (V_{EN}) reaches about 0.7V, the VCC supply turns on. Once V_{IN} exceeds 2.7V, VCC provides an accurate V_{REF} for the EN threshold. Pull EN above its rising threshold voltage (1V) to turn the converter on. Pull EN below 0.85V to turn it off.

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Configurable V_{IN} Under-Voltage Lockout (UVLO) Protection

When V_{IN} is sufficiently high, the chip can be enabled and disabled via the EN pin. An internal pull-down resistor in this circuit can generate a configurable V_{IN} under-voltage lockout (UVLO) threshold and hysteresis.

The device requires a higher voltage (≥3.3V) for V_{IN} to directly start up. The part has an internal, fixed UVLO threshold. The rising threshold is 3V, while the falling threshold is about 2.8V. For applications that require a higher UVLO point, an external resistor divider placed between VIN and EN can raise the equivalent UVLO threshold (see Figure 6).

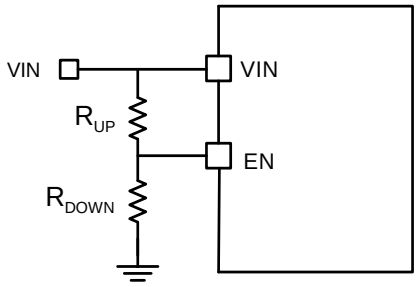


Figure 6: Adjustable UVLO Using the EN Divider

The UVLO rising threshold ($V_{IN_UVLO_RISING}$) can be calculated with Equation (10):

$$V_{IN_UVLO_RISING} = (1+\frac{R_{UP}}{R_{DOWN}}) \times V_{EN_RISING} \quad (10)$$

Where V_{EN_RISING} is 1V.

The UVLO falling threshold ($V_{IN_UVLO_FALLING}$) can be calculated with Equation (11):

$$V_{IN_UVLO_FALLING} = (1+\frac{R_{UP}}{R_{DOWN}}) \times V_{EN_FALLING} \quad (11)$$

Where $V_{EN_FALLING}$ is 0.85V.

SYNCO

The SYNCO pin outputs a clock signal in phase with the internal oscillator signal or the external SYNCIN clock.

Power Good (PG)

The device includes an open-drain power good (PG) output that indicates whether the regulator's output is within its nominal output range. If V_{OUT} is within 94% to 106% of its nominal voltage, PG is pulled high. If V_{OUT} exceeds 107% or is below 93% of its nominal voltage, PG is pulled low. Float PG if not used. Choose the PG resistor (R_{PG}/R4) to be about 100kΩ.

DNU

Connect this pin directly to VCC.

Selecting the VCC Capacitor (C_{VCC})

Most of the internal circuitry is powered by the internal, 5V VCC regulator. This regulator uses V_{IN} as its input, and operates across the entire V_{IN} range. If V_{IN} exceeds 5V, V_{CC} is in full regulation. If V_{IN} drops below 5V, the output V_{CC} degrades.

The VCC capacitor (C_{VCC}) should have a capacitance at least 10 times greater than the boost capacitor, and at least 1µF nominally. A C_{VCC} greater than 68µF nominal is not recommended.

Output Voltage (V_{OUT}) Setting

The feedback (FB) resistor divider is integrated internally (see Figure 7). Connect the VOUT pin directly to the output.

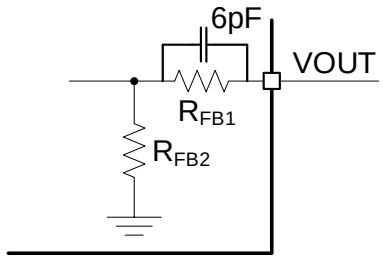


Figure 7: Feedback Divider Network (Fixed Output Version)

The selectable fixed-output options are as follows: 1V, 1.1V, 1.8V, 2.5V, 3V, 3.3V, 3.8V, and 5V.

Table 4 shows the relationship between V_{OUT} and the internal R_{FBx}.

Table 4: V_{OUT} vs. R_{FBx}

V_{OUT} (V)	R_{FB1} (MΩ)	R_{FB2} (MΩ)
1	1.33	2
1.1	1.67	2
1.8	4	2
2.5	6.33	2
3	8	2
3.3	9	2
3.8	10.67	2
5	14.67	2

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Connection to GND

See the PCB Layout Guidelines below for more details.

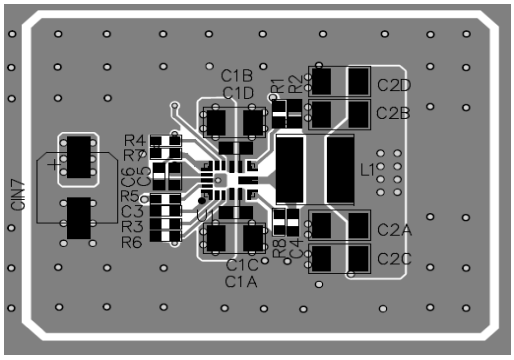
PCB Layout Guidelines (12)

Efficient PCB layout (especially input capacitor placement) is critical for stable operation. A 4-layer layout is strongly recommended for improved thermal performance. For the best results, refer to Figure 8 and follow the guidelines below:

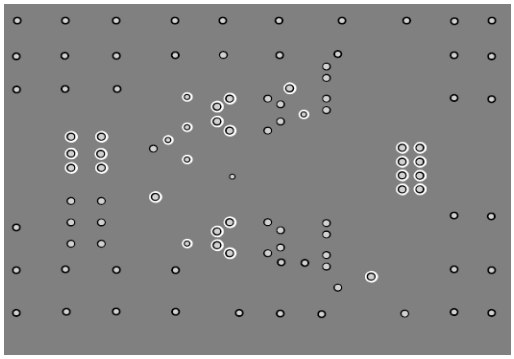
1. Place the symmetric input capacitors as close to VIN and PGND as possible.
2. Use a large ground plane to connect directly to PGND.
3. If the bottom layer is a ground plane, add multiple vias near PGND.
4. Route the high-current paths at GND and VIN using short, direct, and wide traces.
5. Place the ceramic input capacitors, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to reduce high-frequency noise.
6. Keep the connection between C_{IN} and VIN as short and wide as possible.
7. Place C_{VCC} as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

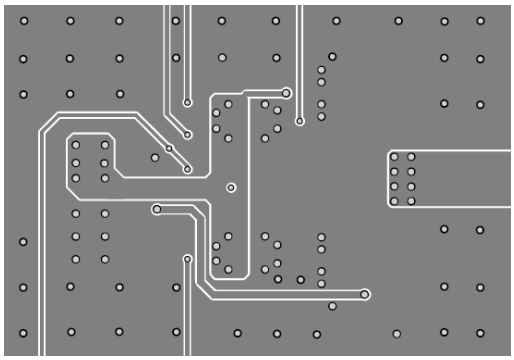
12) The recommended PCB layout is based on Figure 9 on page 41.



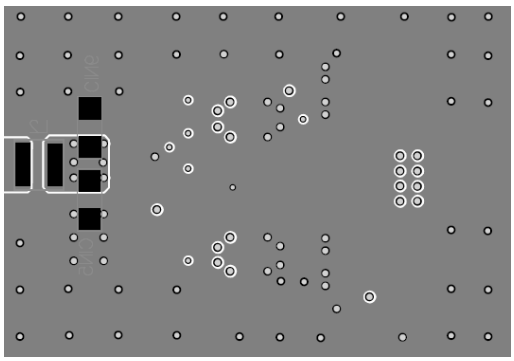
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 8: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

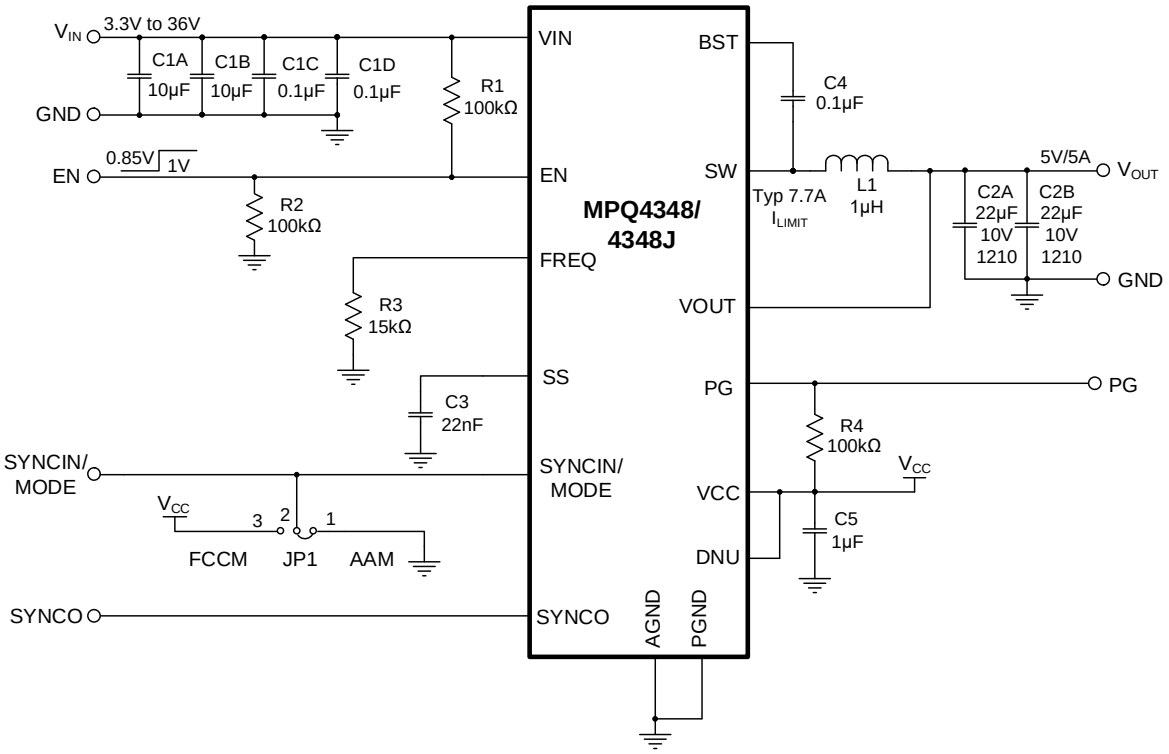


Figure 9: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz)

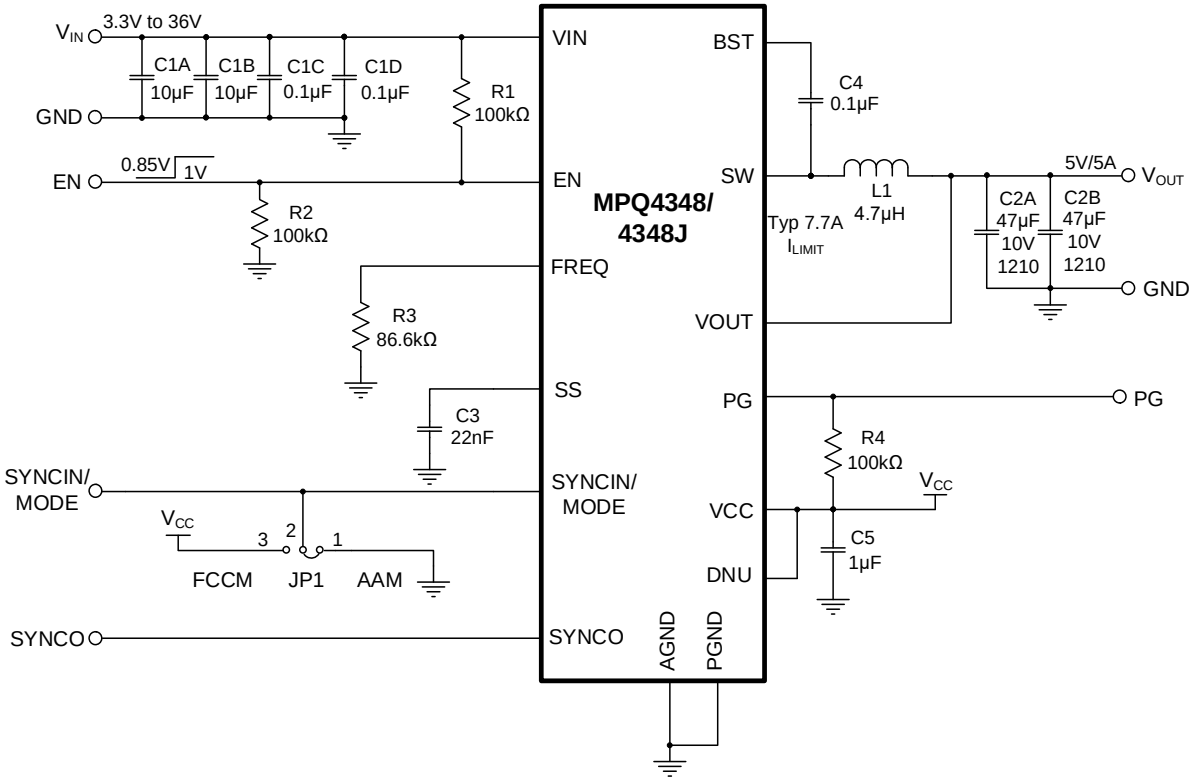


Figure 10: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz)

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TYPICAL APPLICATION CIRCUITS *(continued)*

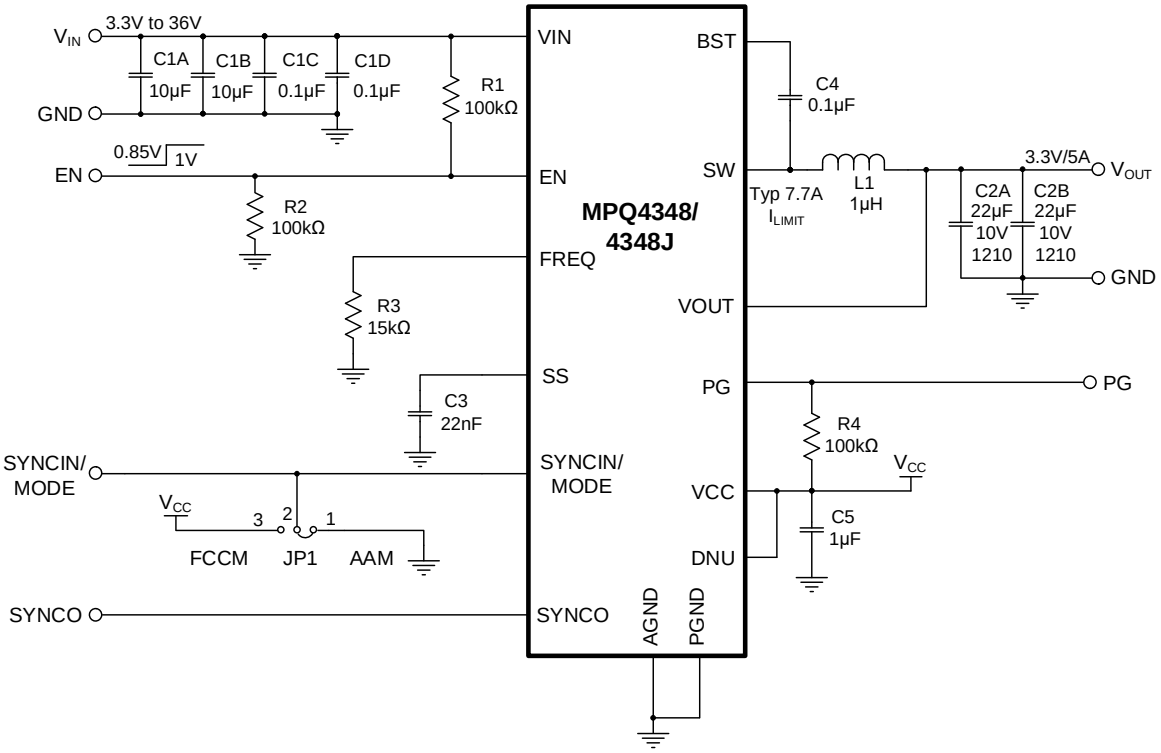


Figure 11: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 2.2MHz)

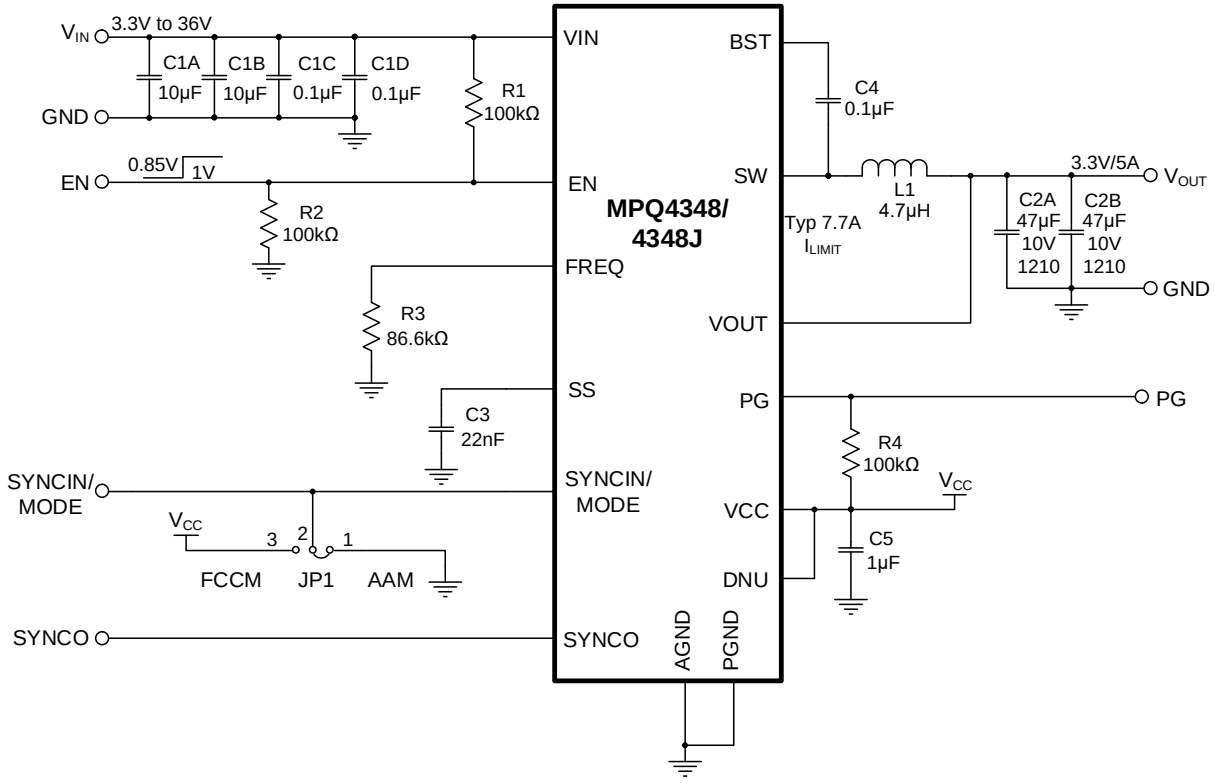


Figure 12: Typical Application Circuit (V_{OUT} = 3.3V, f_{SW} = 410kHz)

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TYPICAL APPLICATION CIRCUITS *(continued)*

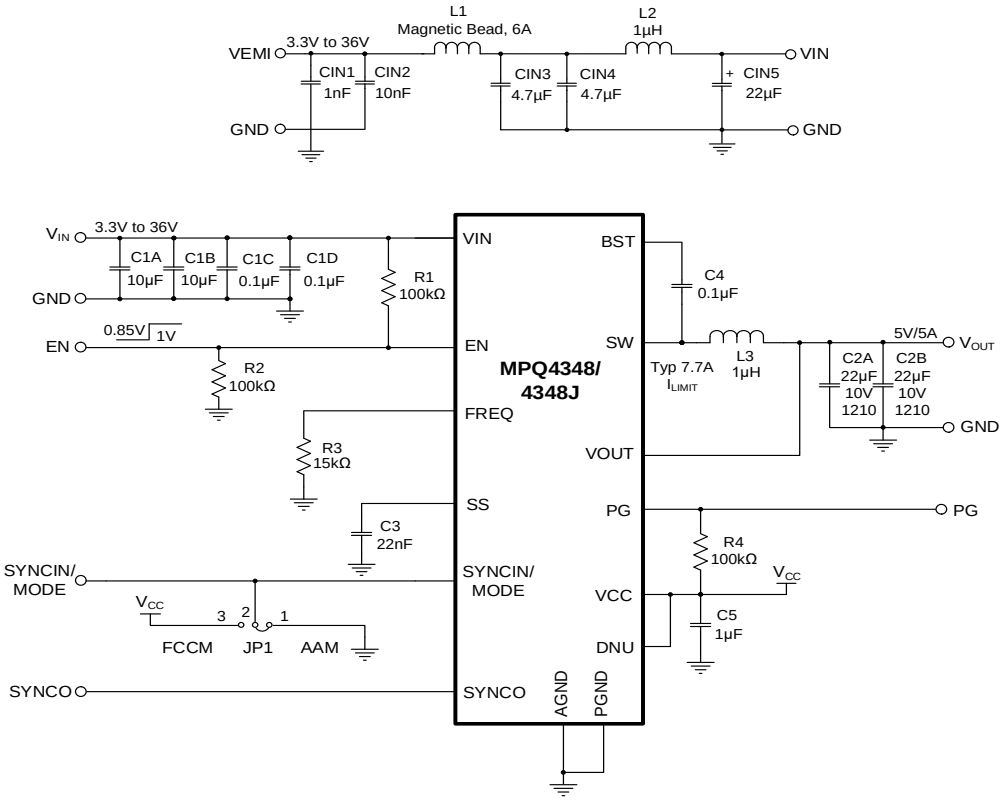


Figure 12: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 2.2MHz with EMI Filter)

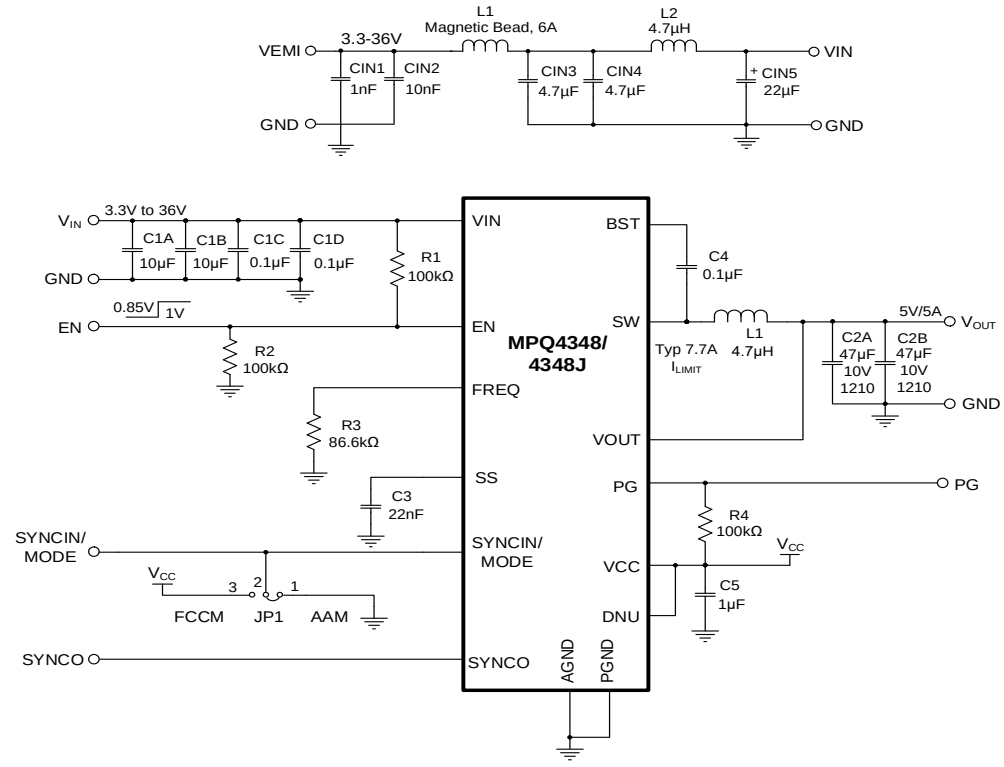
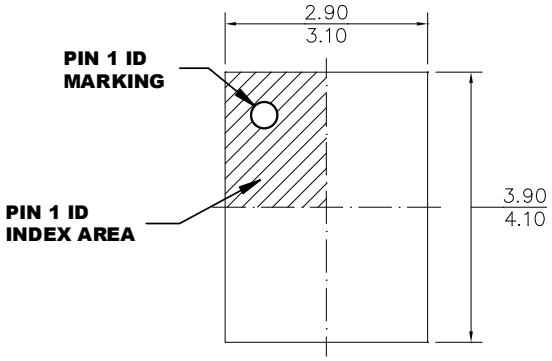


Figure 14: Typical Application Circuit (V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filter)

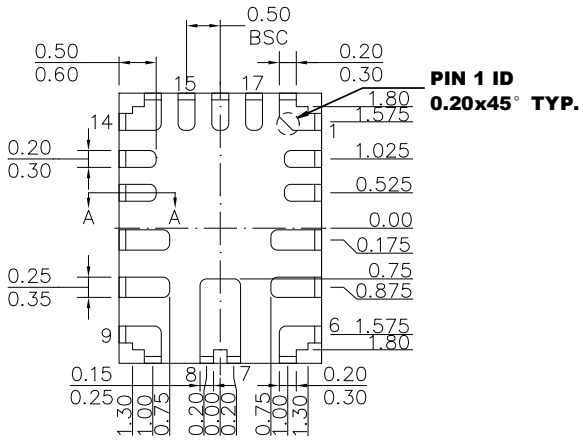
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PACKAGE INFORMATION

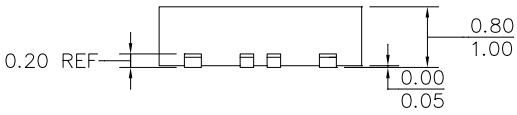
QFN-17 (3mmx4mm)
Wettable Flank



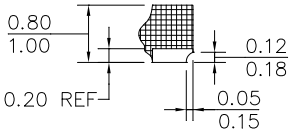
TOP VIEW



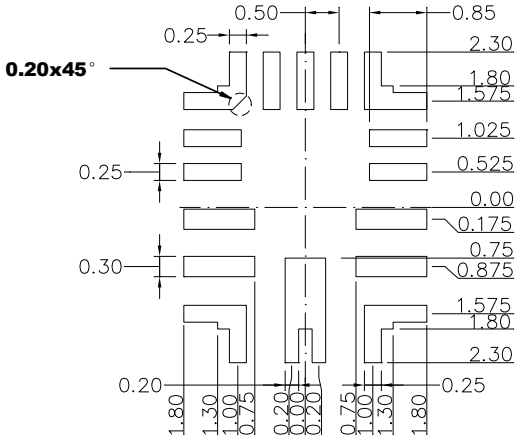
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

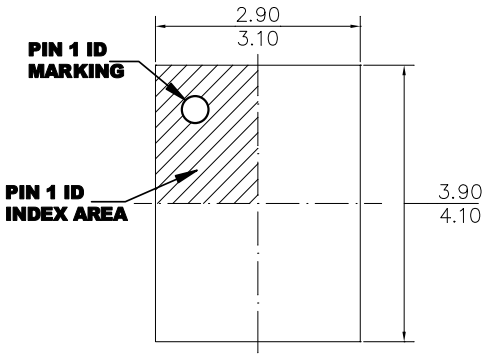
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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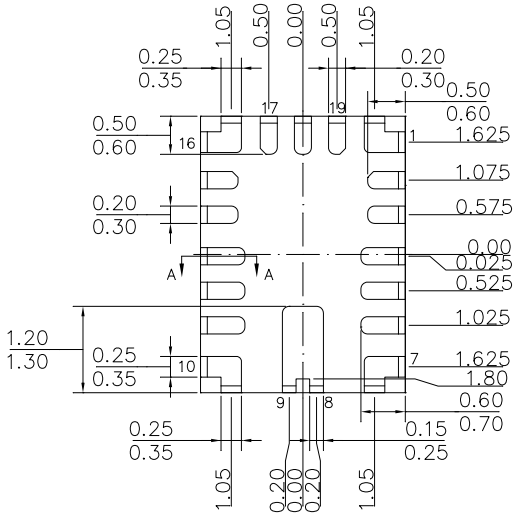
PACKAGE INFORMATION *(continued)*

QFN-19 (3mmx4mm)

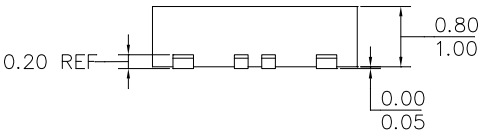
Wettable Flank



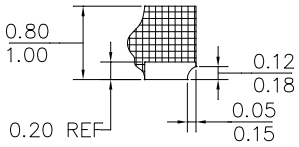
TOP VIEW



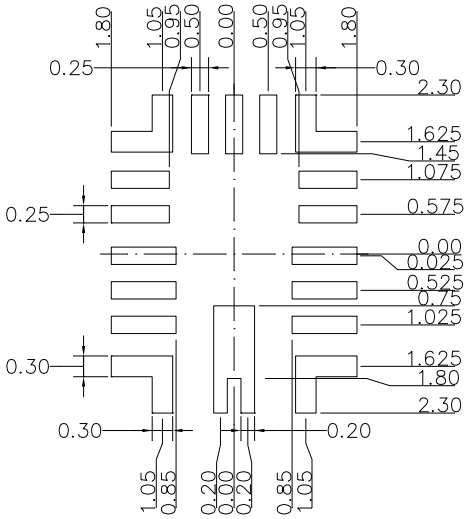
BOTTOM VIEW



SIDE VIEW



SECTION A-A



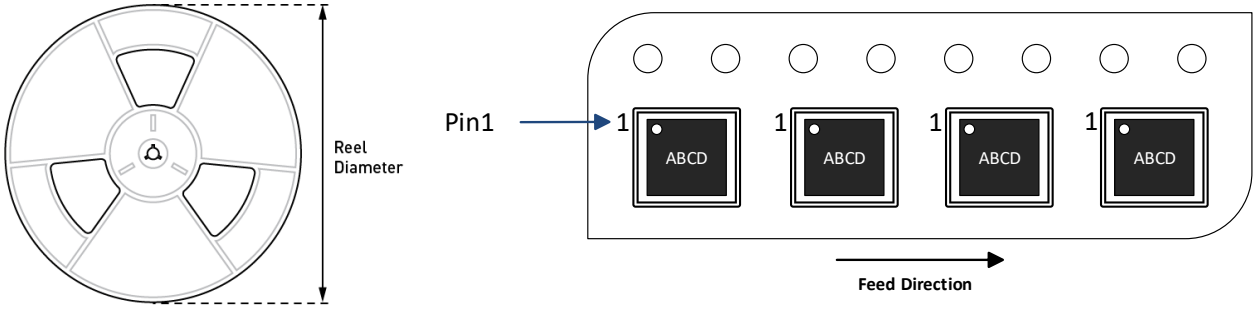
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CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/ Tube (13)	Quantity/Tray (13)	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4348GLE-33-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4348GLE-5-AEC1-Z	QFN-17 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4348JGLE-33-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4348JGLE-5-AEC1-Z	QFN-19 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

Note:

13) N/A indicates “not available” in tubes. For 500-piece tape & reel prototype quantities, contact the factory. The order code for a 500-piece partial reel is “-P”. Tape & reel dimensions are the same as a full reel.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/20/2022	Initial Release	-

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