MPQ3432

21A, High-Efficiency, Fully Integrated, Synchronous Boost Converter with Configurable Current Limit, AEC-Q100 Qualified

DESCRIPTION

The MPQ3432 is 600kHz, fixed-frequency, highly integrated boost converter with a wide input range. The MPQ3432 starts up from an input voltage (V_{IN}) as low as 2.7V, and supports up to 20W of load power from a single-cell battery with integrated low $R_{DS(ON)}$ power MOSFETs.

The MPQ3432 adopts constant-off-time (COT) control to provide fast transient response. The MODE pin allows the user to select pulse-skip mode (PSM), forced continuous conduction mode (FCCM), or ultrasonic mode (USM) under light-load conditions. The configurable current limit provides accurate overload protection. The low-side MOSFET (LS-FET) limits the cycle-by-cycle inductor peak current, and the high-side MOSFET (HS-FET) eliminates the need for an external Schottky diode.

Full protection features include configurable input under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MPQ3432 is available in a QFN-13 (3mmx4mm) package.

FEATURES

- Guaranteed Industrial/Automotive Temperatures
- 2.7V to 13V Start-Up Voltage (V_{ST})
- 0.8V to 13V Operation Input Voltage (V_{IN})
- Up to 16V Output Voltage (V_{OUT})
- Supports 20W Average Power Load and 40W Peak Power Load from 3.3V
- Configurable Switch Peak Current Limit
- Integrated 6mΩ and 9.5mΩ Power MOSFETs
- 95% Efficiency for 3.6V V_{IN} to 9V/3A
- Selectable Pulse-Skip Mode (PSM), >23kHz Ultrasonic Mode (USM), and Forced Continuous Conduction Mode (FCCM) under Light-Load Conditions
- Automatic Pass-Through Function in PSM when $V_{IN} > V_{OUT-SET}$
- 600kHz Fixed Switching Frequency (f_{SW})
- Adaptive Constant-Off-Time (COT) Control for Fast Transient Response
- External Soft Start and Compensation Pins
- Configurable Under-Voltage Lockout (UVLO) and Hysteresis
- 175°C Over-Temperature Protection (OTP)
- Available in a QFN-13 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

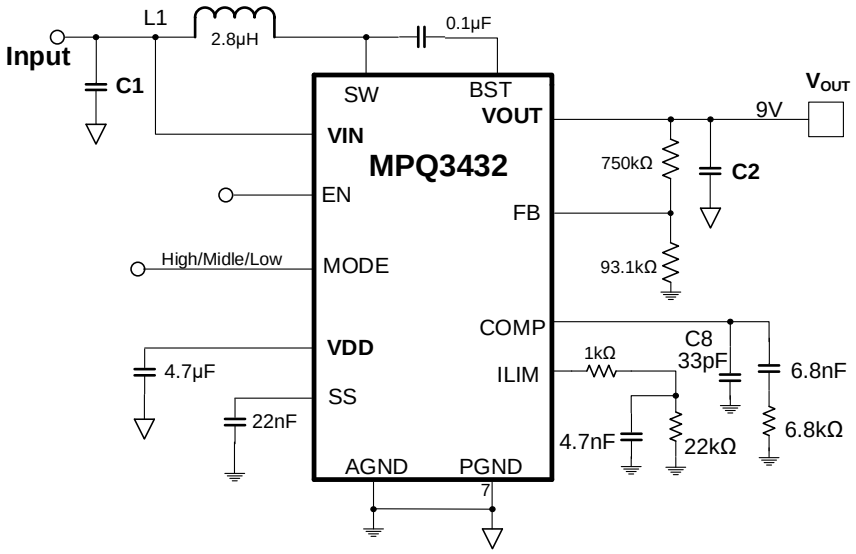
APPLICATIONS

- Automotive Boost
- Super Capacitors
- Backup Batteries

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3432GLE-AEC1	QFN-13 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ3432GLE-AEC1-Z).

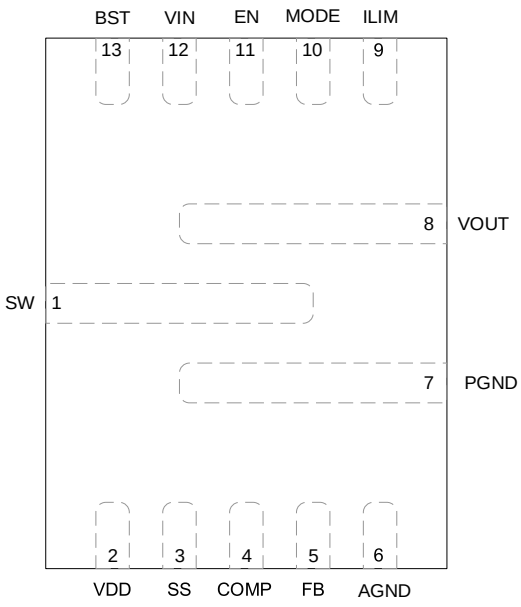
TOP MARKING

MPYW
3432
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
3432: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



QFN-13 (3mmx4mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Converter switch.** The SW pin is connected to the drain of the internal low-side MOSFET (LS-FET) and the source of the internal synchronous high-side MOSFET (HS-FET). Connect the power inductor to the SW pin.
2	VDD	**Internal bias supply.** Decouple the VDD pin with a 4.7μF ceramic capacitor, placed as close to VDD as possible. When V_{IN} exceeds 3.4V, VDD is powered by VIN. Otherwise, VDD is powered by the higher voltage between V_{IN} and V_{OUT}. If the biased voltage connected to VDD exceeds 3.4V, the regulator connected from VIN to VOUT is disabled. The VDD regulator starts working when V_{IN} exceeds 0.9V and EN is high. Supply VIN with a power source exceeding 2.7V during VIN start-up to provide VDD with sufficient power voltage.
3	SS	**Soft start configuration.** Place a capacitor from the SS pin to AGND to set the V_{OUT} rising slew rate.
4	COMP	**Internal error amplifier output.** Connect a capacitor and resistor in series from the COMP pin to AGND for loop compensation.
5	FB	**Feedback input.** Connect a resistor divider from the VOUT pin to the FB pin.
6	AGND	**Analog ground.**
7	PGND	**Power ground.**
8	VOUT	**Output.** The VOUT pin is connected to the drain of the HS-FET. VOUT powers VDD when V_{OUT} exceeds V_{IN}, and V_{IN} is below 3.4V.
9	ILIM	**Switching peak current limit setting.** Place a resistor from the ILIM pin to AGND to set the switching peak current limit.
10	MODE	**MODE selection.** If MODE is floating, the MPQ3432 operates in ultrasonic mode (USM). If MODE is high, the MPQ3432 operates in forced continuous conduction mode (FCCM). If MODE is low, the MPQ3432 operates in pulse-skip mode (PSM).
11	EN	**Chip enable control.** When the EN pin is not in use, connect EN to the VIN pin for automatic start-up. EN can configure the V_{IN} under-voltage lockout (UVLO) threshold. Do not float this pin.
12	VIN	**Input supply.** The VIN pin must be bypassed locally. Supply VIN with power source exceeding 2.7V during VIN start-up to provide VDD with sufficient power voltage.
13	BST	**Bootstrap.** A capacitor between the BST and SW pins powers the synchronous HS-FET.

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ABSOLUTE MAXIMUM RATINGS (1)

SW ……..
…-0.3V (-3.5V for <10ns) to +18V (22V for <10ns)
VIN, EN, MODE, VOUT ..... -0.3V to +18V
BST ..... -0.3V to V_{SW} + 4.5V
All other pins..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (2)
.....4W (5)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (3)

Start-up input voltage (V_{ST}) ..... 2.7V to 13V
Operation input voltage (V_{IN})..... 0.8V to 13V
Start-up input voltage with VDD bias (V_{ST2}).....
..... 0.9V to 13V
Maximum external VDD bias voltage 3.6V (4)
Boost output voltage (V_{OUT})..... V_{IN} to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-13 (3mmx4mm)		
EVQ3432-L-00A (5)	31	4 °C/W
JESD51-7 (6)	48	11 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) If the external VDD bias voltage drops below the normal VDD regulated voltage, the external power prevents the current from flowing out of VDD.
5) Measured on EVQ3432-L-00A, 4-layer 63mmx63mm PCB.
6) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage	V_{ST}	No VDD bias	2.7		13	V
		V_{DD} = 3V	0.9		13	V
Operating input voltage	V_{IN}		0.8		13	V
Operating VDD voltage [8]	V_{DD}	V_{IN} = 2.7V, 0mA to 10mA	2.3	2.55		V
		V_{IN} = 12V, 0mA to 15mA		3.4		V
VDD UVLO rising [8]	VDD_{UVLO-R}	V_{DD} rising	2.2	2.4	2.6	V
VDD UVLO falling	VDD_{UVLO-F}	V_{DD} falling	2	2.2	2.4	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	µA
Quiescent current	I_Q	V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on VIN			25	µA
		V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on VOUT		450	550	µA
Enable (EN) Control						
EN turn-on threshold voltage	V_{EN-ON}	V_{EN} rising (switching)		1.23		V
EN high threshold voltage	V_{EN-H}	V_{EN} rising (micro power)			1	V
EN low threshold voltage	V_{EN-L}	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1V < EN < V_{EN-ON}	3.5	5	6.5	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN on to switching		65		µs
Frequency						
Switching frequency	f_{SW}		500	600	700	kHz
LS-FET minimum on time [9]	t_{MIN-ON}			80		ns
LS-FET maximum on time	t_{MAX-ON}			7.1		µs
Loop Control						
FB reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.1V			50	nA
Error amp. voltage gain [10]	A_{V-EA}			300		V/V
Error amp. transconductance	G_{EA}			410		µA/V
Error amp. max output current		V_{FB} = 0.8V, V_{COMP} = 1V		60		µA
		V_{FB} = 1.2V, V_{COMP} = 1V		-60		µA
COMP to current gain	G_{CS}			20		A/V
COMP PSM threshold [9]	V_{PSM}	V_{MODE} = 0V		0.5		V
COMP high clamp		V_{FB} = 0.8V		2.6		V
Soft-start charge current	I_{SS}		6	7.5	9	µA
MODE Selection						
PSM mode tri-state region	$V_{MODE-TRI}$				0.7	V
USM mode tri-state region [11]			0.9		1.2	
FCCM mode E tri-state region			1.6		V_{DD}	
USM frequency	f_{USM}		23	33		kHz
HS-FET zero-current detection (ZCD) (PSM)		V_{FB} = 1V, L = 1.5µH, V_{OUT} = 9V		50		mA
HS-FET ZCD (USM, FCCM) [9] [12]		V_{FB} = 1.1V			-2	A

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power MOSFET						
Low-side MOSFET (LS-FET) on resistance	R_{ON-L}			6		mΩ
High-side synchronous switch on resistance	R_{ON-H}			9.5		mΩ
LS-FET leakage current		V_{SW} = 16V, T_J = 25°C			0.15	μA
High-side MOSFET (HS-FET) leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.15	μA
BST Power						
BST voltage				3.3		V
Current Limit						
Switching current limit	$I_{PK-LIMT}$	R_{LIM} = 36kΩ	7	9	11	A
Protection						
Output OVP threshold				16.5		V
Output OVP hysteresis				0.2		V
Thermal Protection						
Thermal shutdown (9)	T_{SD}			175		°C
Thermal shutdown hysteresis (9)	T_{SD-HYS}			25		°C

Notes:

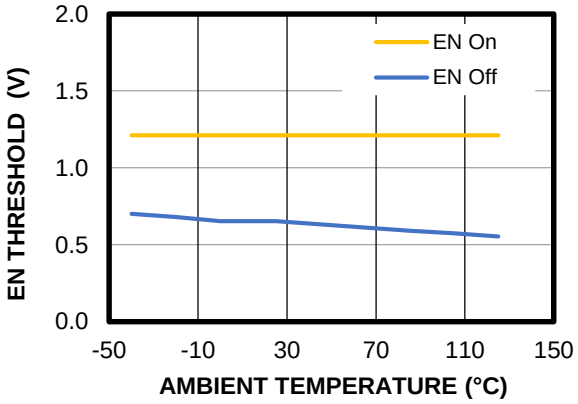
7) Guaranteed by over-temperature correlation. Not tested in production.
8) The VDD regulation voltage is from 2.7V. V_{IN} exceeds the V_{DD} UVLO rising threshold, which guarantees that the IC starts up with a 2.7V V_{IN}.
9) Guaranteed by sample characterization. Not tested in production.
10) Guaranteed by design. Not tested in production.
11) Add an external voltage within this range, or float the MODE pin for USM.
12) The HS-FET ZCD is below -2A in USM and FCCM.

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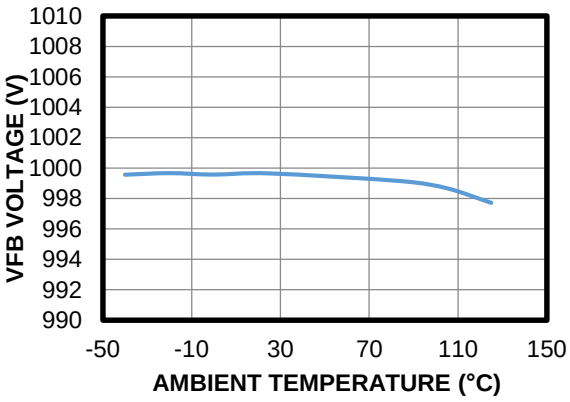
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

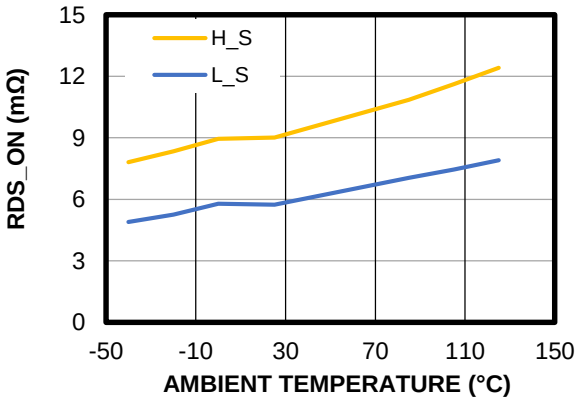
EN Threshold vs. Ambient Temperature



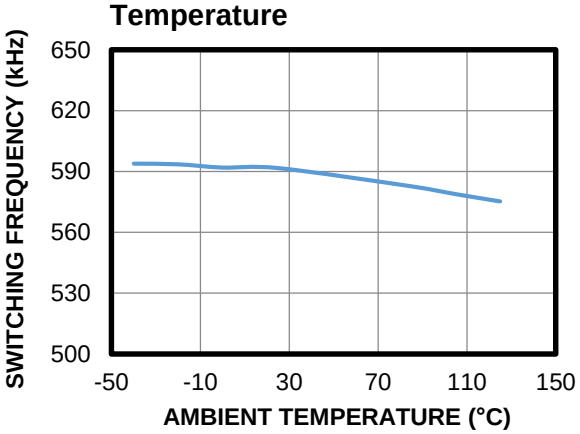
VFB vs. Ambien Temperature



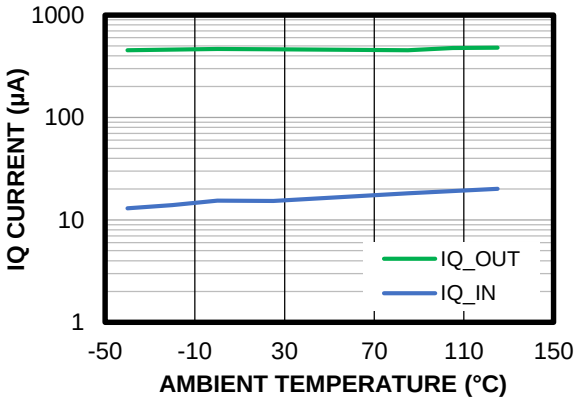
R_{DS_ON} vs. Ambient Temperature



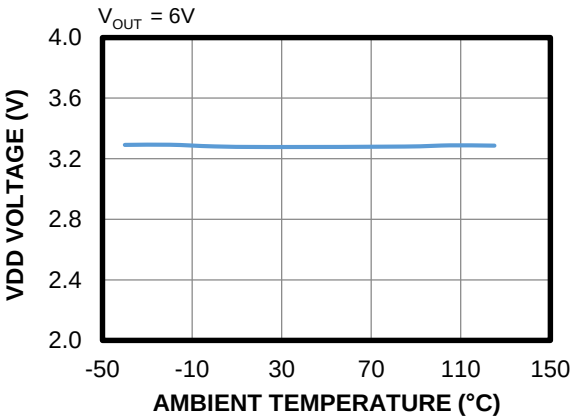
Switching vs. Ambient Temperature



IQ Current vs. Ambient Temperature



VDD vs. Ambient Tempreture



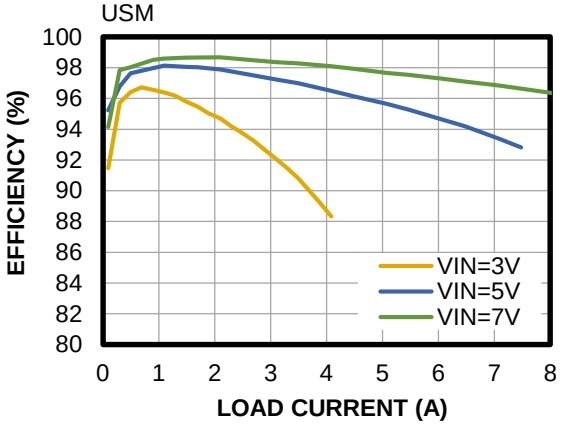
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

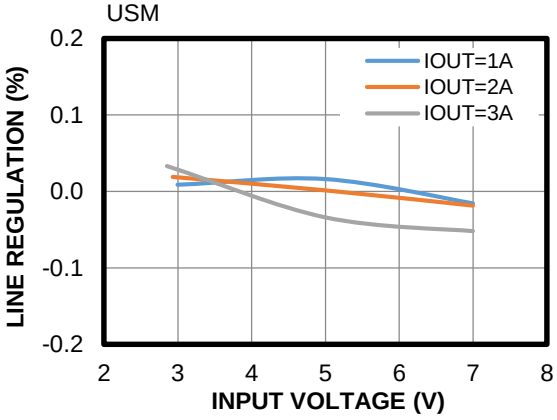
Efficiency vs. Load Current

USM



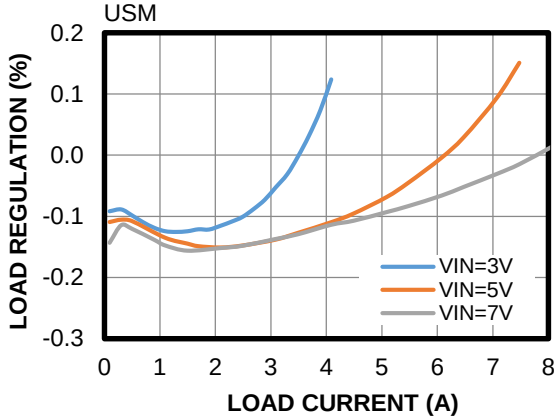
Line Regulation

USM



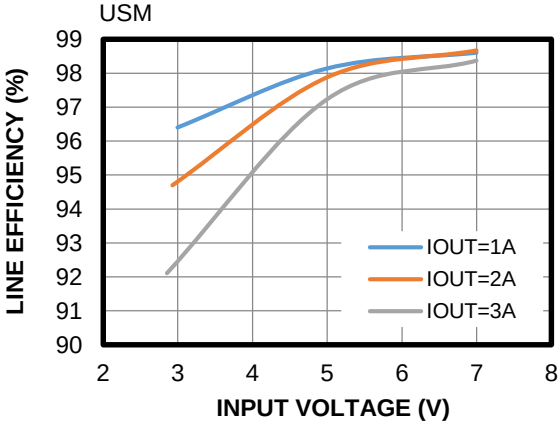
Load Regulation

USM



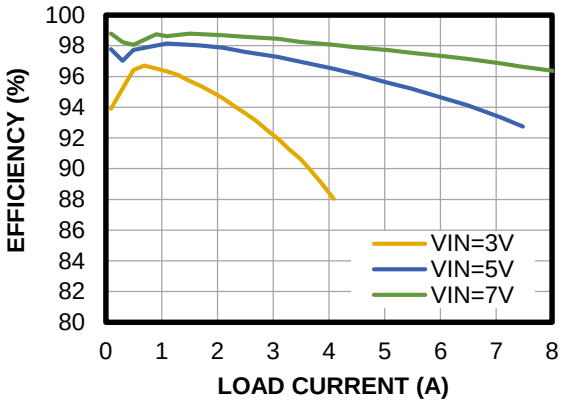
Line Regulation

USM



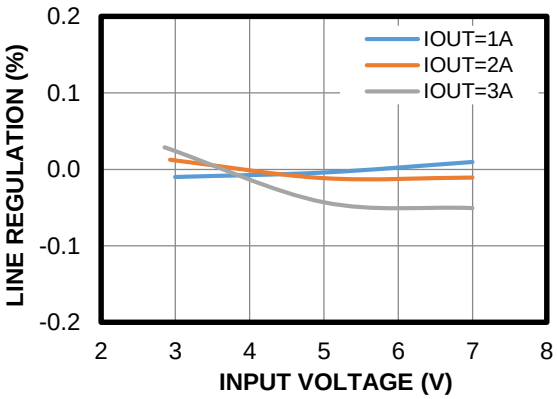
Efficiency vs. Load Current

PSM



Line Regulation

PSM

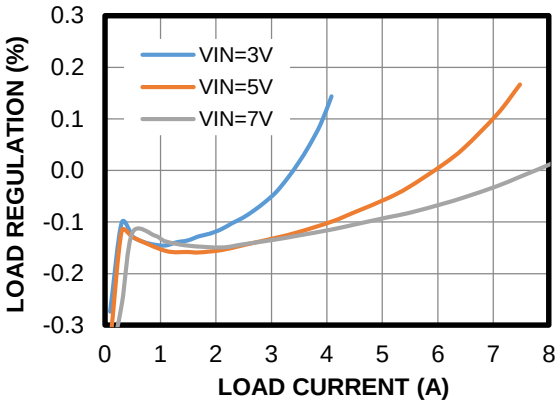


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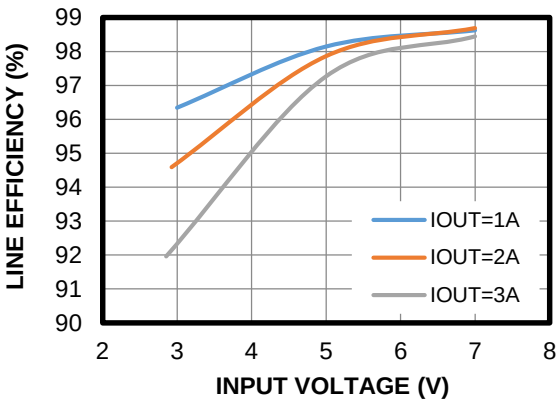
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

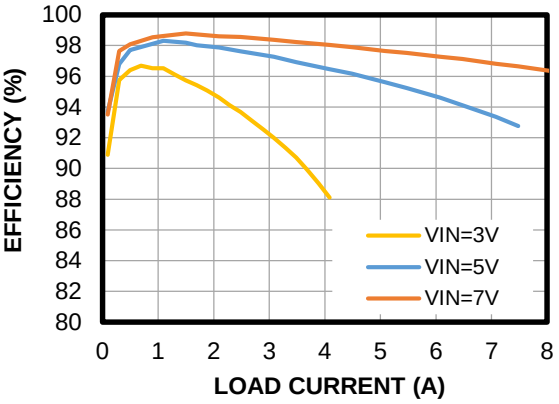
Load Regulation
PSM



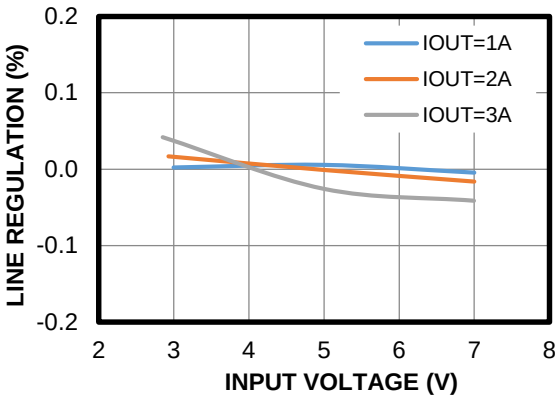
Line Efficiency
PSM



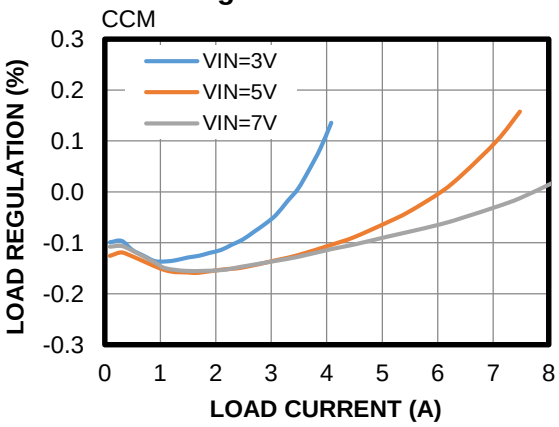
Efficiency vs. Load Current
CCM



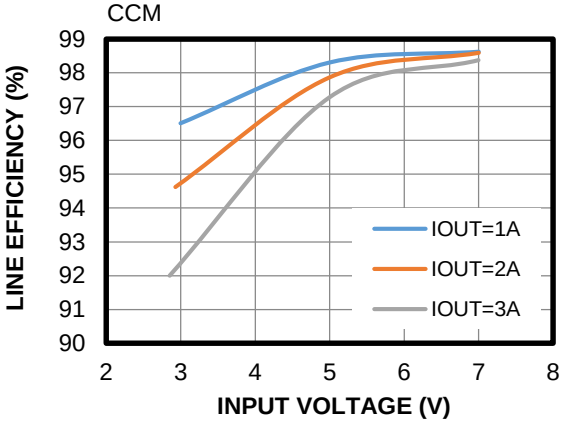
Line Regulation
CCM



Load Regulation
CCM



Line Efficiency
CCM



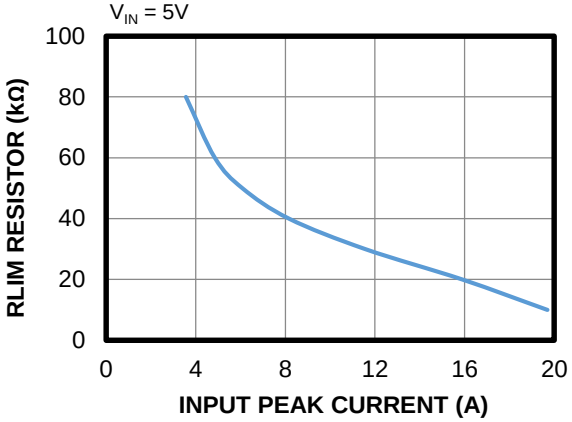
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

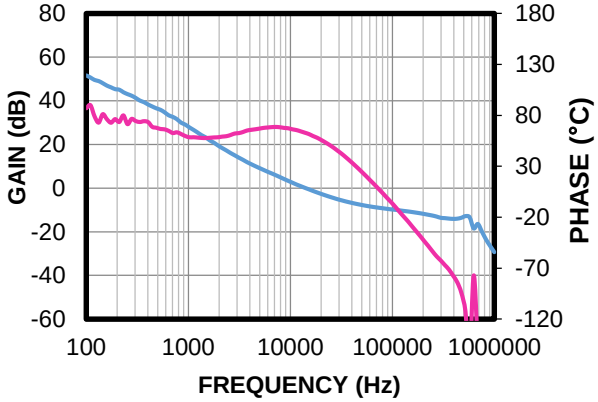
RLIM vs. Input Peak Current

V_{IN} = 5V



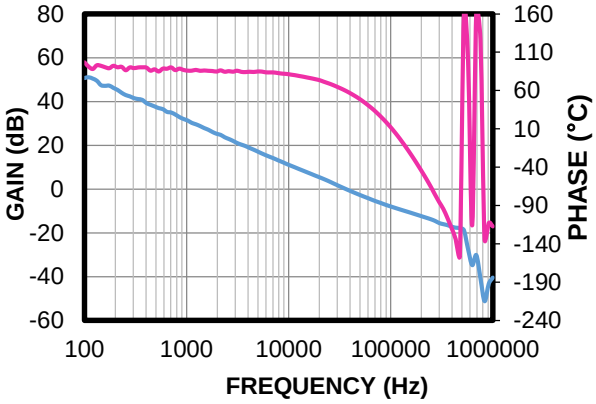
Bode Plot

V_{IN} = 3V, I_{OUT} = 1A



Bode Plot

V_{IN} = 7V, I_{OUT} = 2A

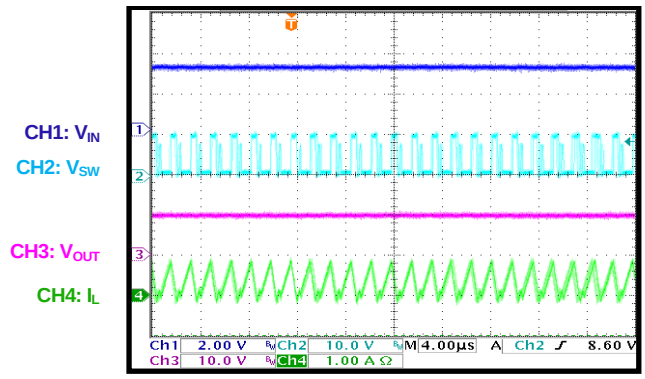


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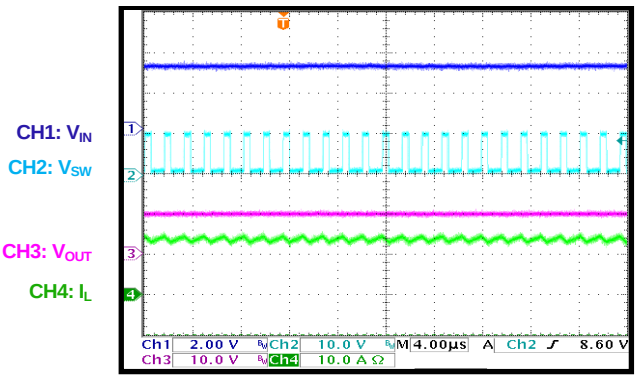
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

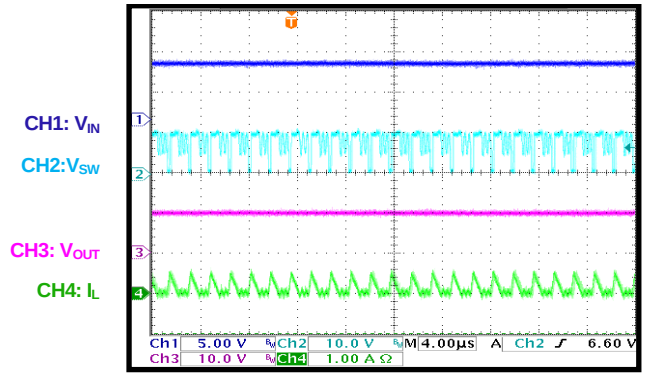
Steady State
V_{IN} = 3V, I_{OUT} = 0.1A, USM



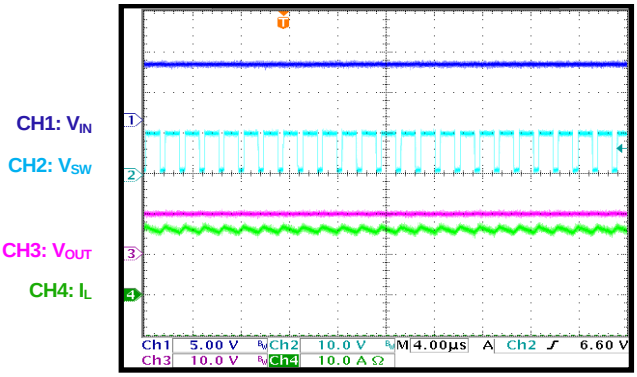
Steady State
V_{IN} = 3V, I_{OUT} = 4A, USM



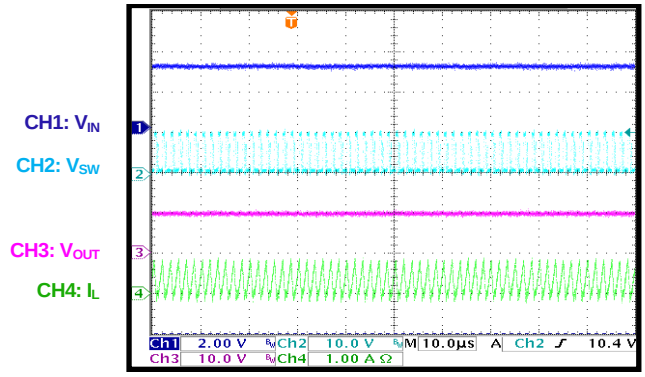
Steady State
V_{IN} = 7V, I_{OUT} = 0.1A, USM



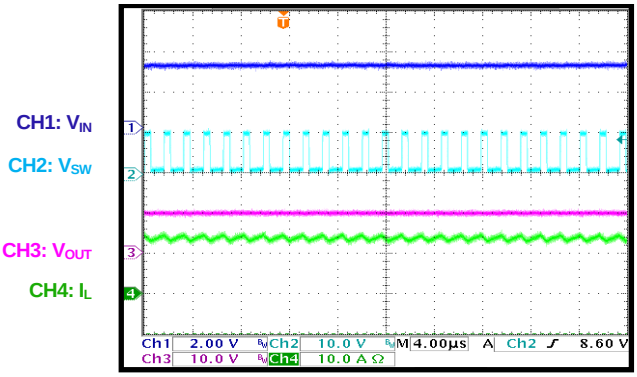
Steady State
V_{IN} = 7V, I_{OUT} = 11A, USM



Steady State
V_{IN} = 3V, I_{OUT} = 0.1A, PSM



Steady State
V_{IN} = 3V, I_{OUT} = 4A, PSM

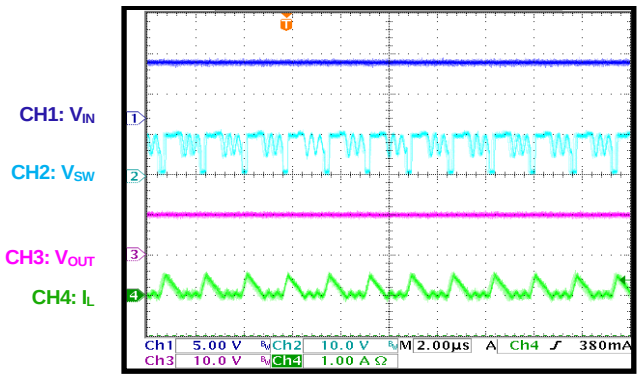


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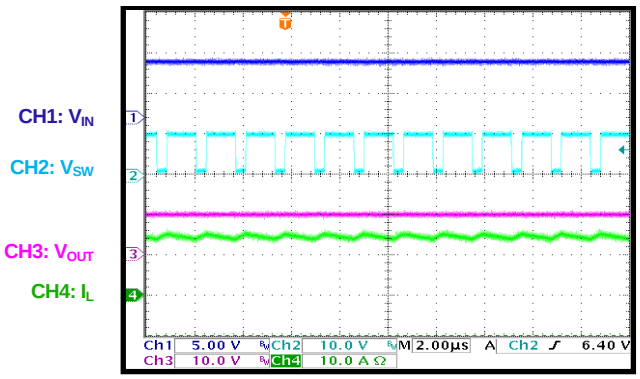
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

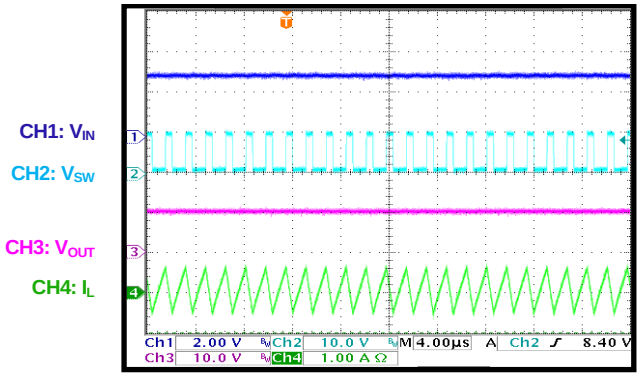
Steady State
V_{IN} = 7V, I_{OUT} = 0.1A, PSM



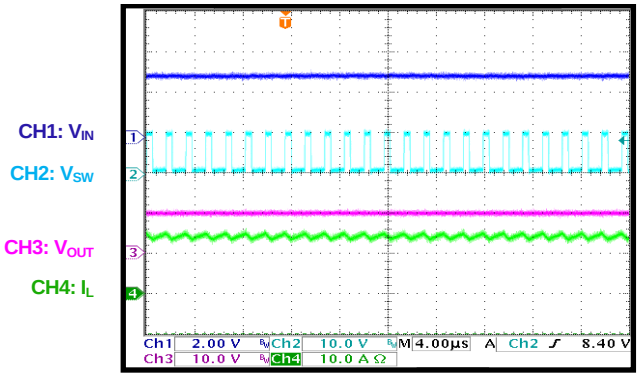
Steady State
V_{IN} = 7V, I_{OUT} = 10A, PSM



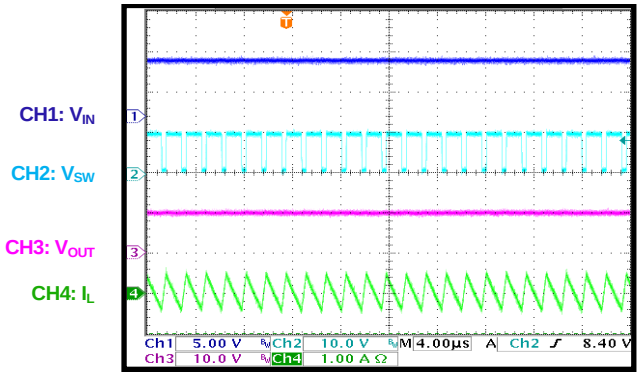
Steady State
V_{IN} = 3V, I_{OUT} = 0A, CCM



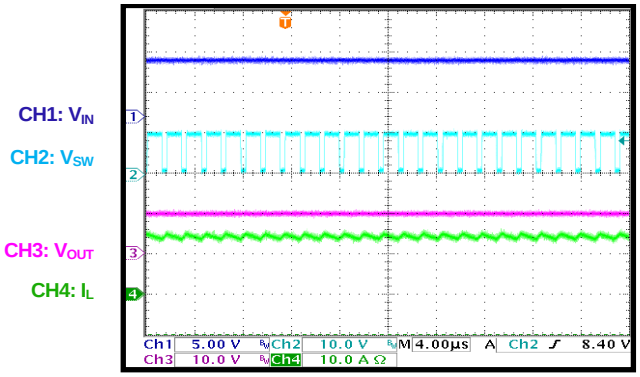
Steady State
V_{IN} = 3V, I_{OUT} = 4A, CCM



Steady State
V_{IN} = 7V, I_{OUT} = 0A, CCM



Steady State
V_{IN} = 7V, I_{OUT} = 10A, CCM



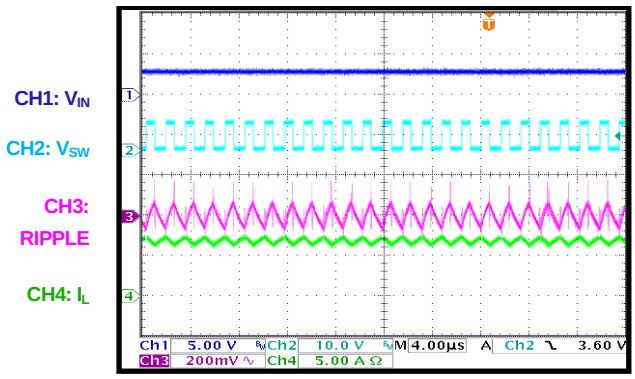
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

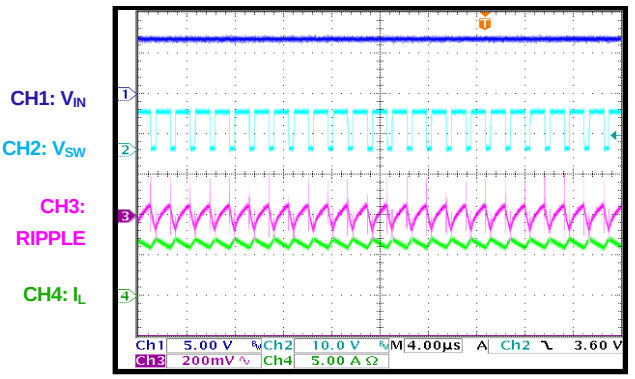
Output Voltage Ripple

V_{IN} = 3V, I_{OUT} = 3A



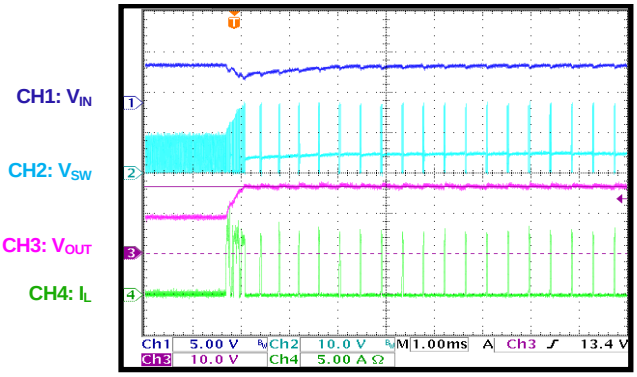
Output Voltage Ripple

V_{IN} = 7V, I_{OUT} = 5A



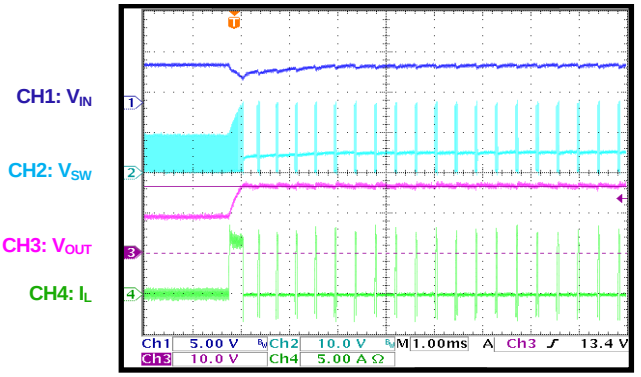
Output OVP

V_{IN} = 5V, USM



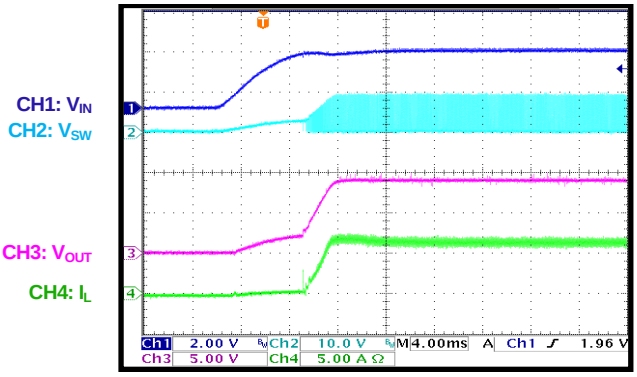
Output OVP

V_{IN} = 5V, CCM



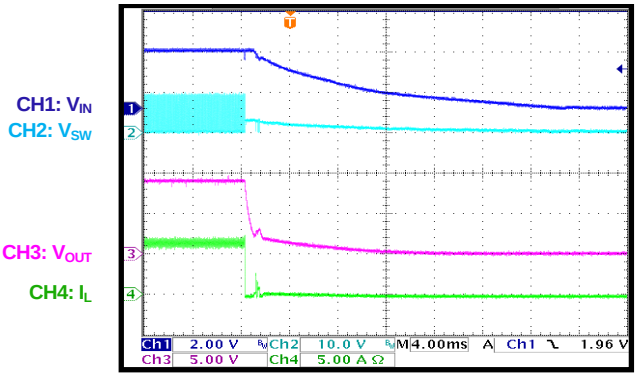
Start-Up through VIN

V_{IN} = 3V, I_{OUT} = 2A



Shutdown through VIN

V_{IN} = 3V, I_{OUT} = 2A



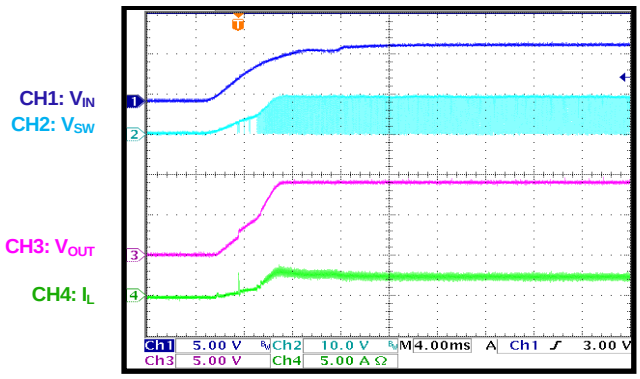
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

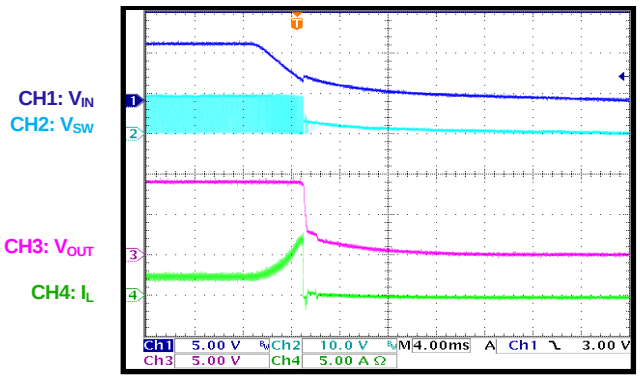
Start-Up through VIN

V_{IN} = 7V, I_{OUT} = 2A



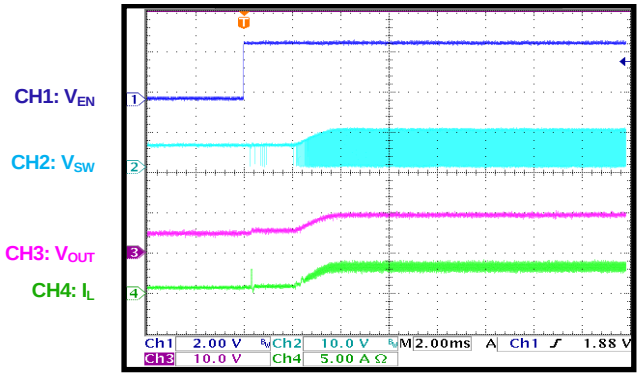
Shutdown through VIN

V_{IN} = 7V, I_{OUT} = 2A



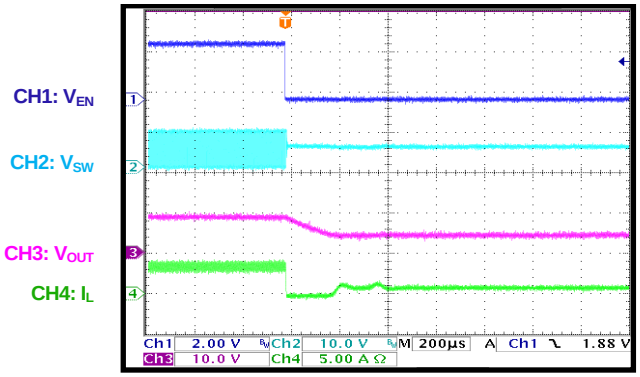
Enable On

V_{IN} = 5V, I_{OUT} = 2A



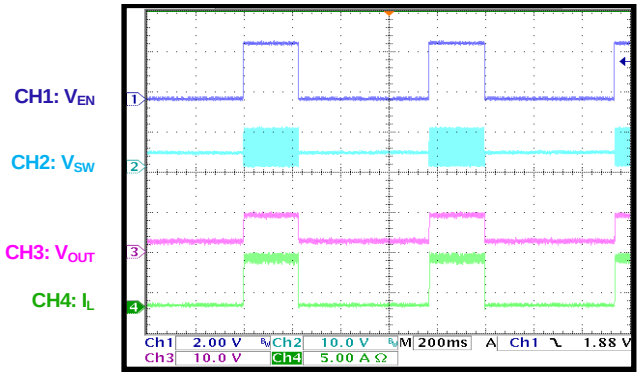
Enable Off

V_{IN} = 5V, I_{OUT} = 2A



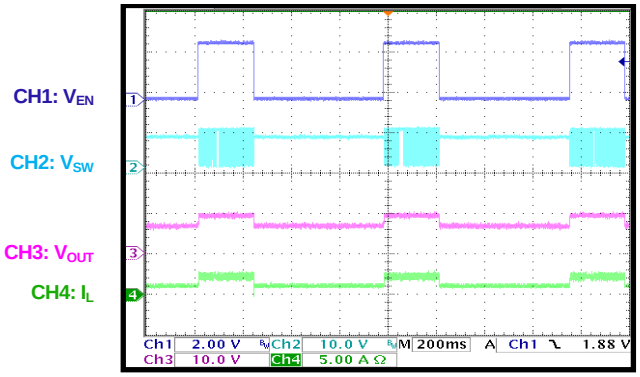
Enable On/Off

V_{IN} = 3V, I_{OUT} = 2A



Enable On/Off

V_{IN} = 7V, I_{OUT} = 2A



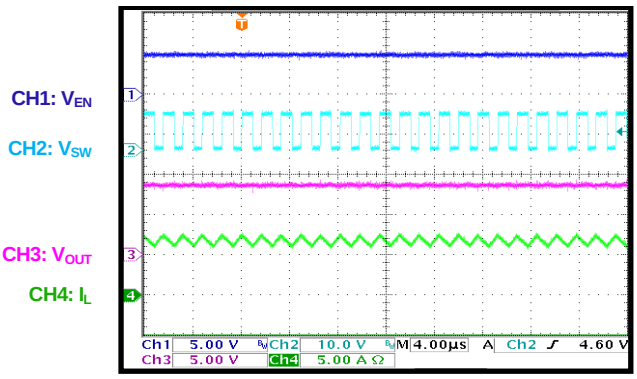
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 9V, L = 2.8µH, I_{OUT} = 3.5A, USM, T_A = 25°C, unless otherwise noted.

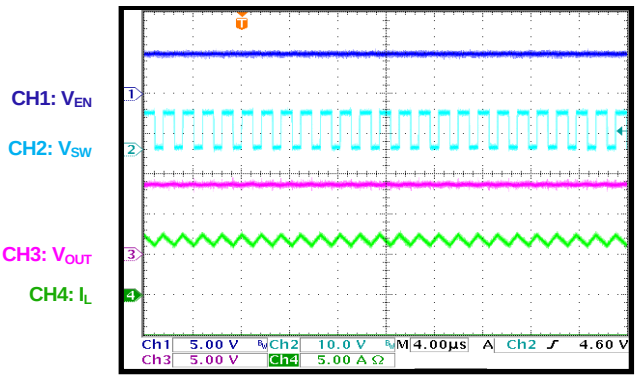
Current Limit

V_{IN} = 5V, R_{LIM} = 44kΩ, USM



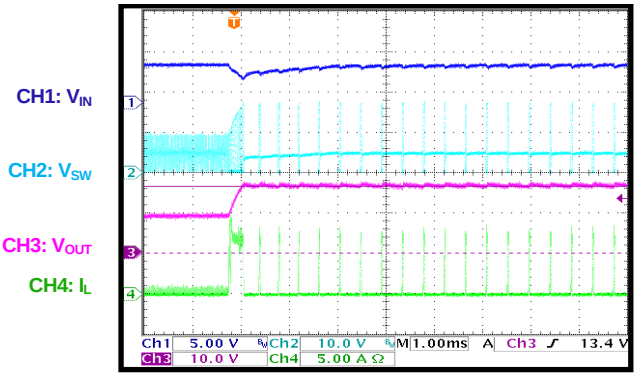
Current Limit

V_{IN} = 5V, R_{LIM} = 44kΩ, PSM



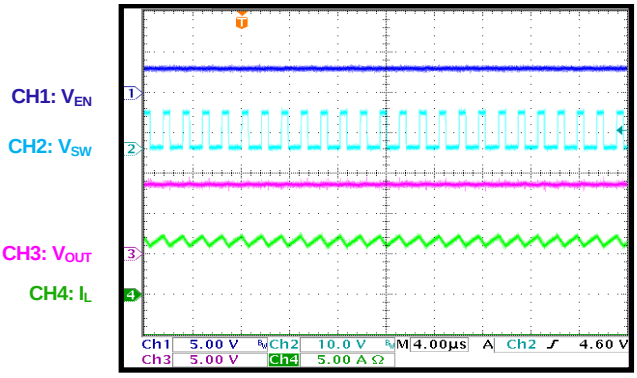
Output OVP

V_{IN} = 5V, PSM



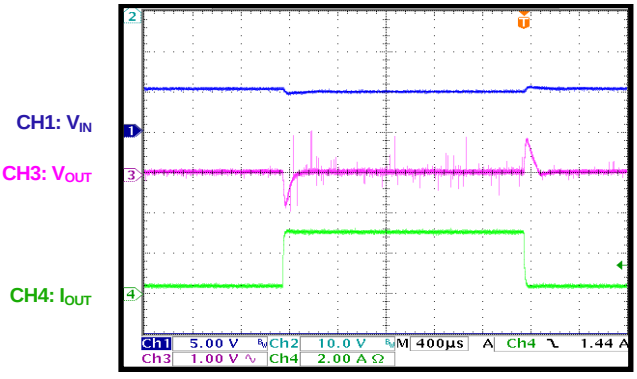
Current Limit

V_{IN} = 5V, R_{LIM} = 44kΩ, CCM



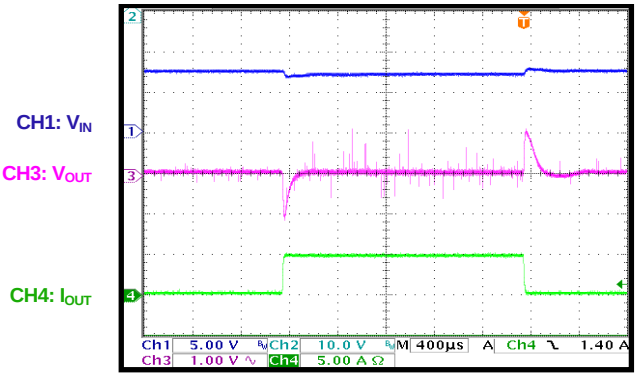
Load Transient Response

V_{IN} = 5V, I_{OUT} = 0A to 3A, CCM



Load Transient Response

V_{IN} = 7V, I_{OUT} = 0A to 5A, CCM



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FUNCTIONAL BLOCK DIAGRAM

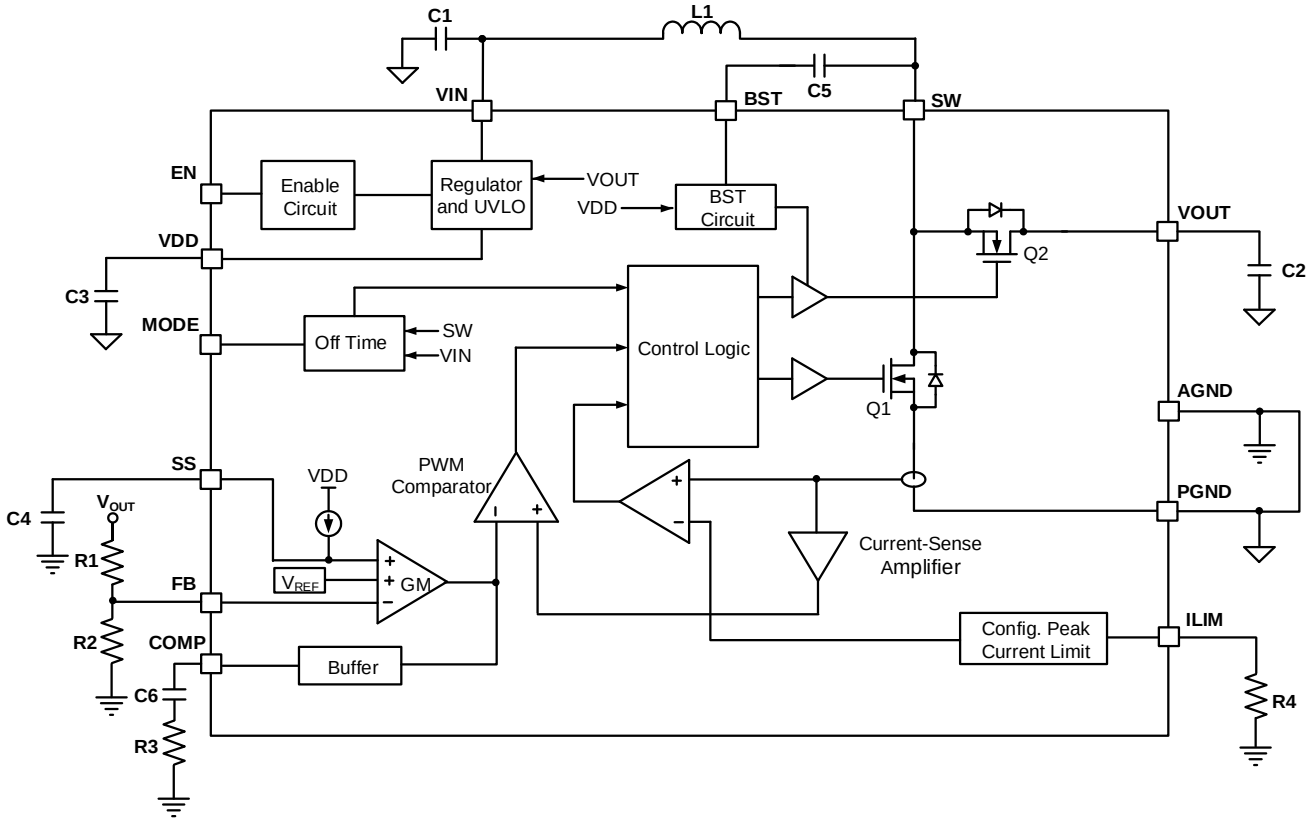


Figure 1: Functional Block Diagram

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OPERATION

The MPQ3432 is a 600kHz, fixed-frequency, high-efficiency boost converter with a wide input range. Its fully integrated low $R_{DS(ON)}$ MOSFETs provide small size and high efficiency for high-power step-up applications. Constant-off-time (COT) control provides fast transient response, while the MODE pin provides flexible light-load performance design.

Boost Operation

The MPQ3432 uses COT control to regulate the output voltage (V_{OUT}). At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET) (Q1) turns on and forces the inductor current (I_L) to rise.

The device senses the current through the LS-FET. If the current signal exceeds the output of the transconductance error amplifier (COMP) voltage (V_{COMP}), then the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. I_L then flows to the output capacitor through the high-side MOSFET (HS-FET) and decreases. V_{COMP} is an amplifier output that compares the feedback voltage (V_{FB}) to the internal reference voltage (V_{REF}).

After a fixed off time, the LS-FET turns on again and the cycle repeats. During each cycle, the LS-FET off time is determined by the V_{IN} / V_{OUT} ratio, and the on time is controlled by V_{COMP}. The peak inductor current is controlled by COMP, and COMP is controlled by V_{OUT}. Therefore, V_{OUT} regulates I_L.

Operation Mode

The MPQ3432 works with a 600kHz quasi-constant frequency with pulse-width modulation (PWM) control under heavy-load conditions. When the load current decreases, the MPQ3432 works in forced continuous conduction mode (FCCM), PSM, or ultrasonic mode (USM) based on the MODE pin setting. Select the mode before operating the device.

Forced Continuous Conduction Mode (FCCM)

If the MODE pin is high (>1.6V), the MPQ3432 works in a fixed-frequency PWM mode under any load condition. The off time is determined by the internal circuit to achieve the 600kHz frequency based on the V_{IN} / V_{OUT} ratio.

When the load decreases, the average input current drops, and the inductor current from VOUT to VIN may become negative during the off time (while the LS-FET is off and the HS-FET is on). This forces I_L to work in FCCM with a fixed frequency, and produces a lower output voltage ripple than in PSM.

Pulse-Skip Mode (PSM)

The device works in PSM under light-load conditions if the MODE voltage (V_{MODE}) is below 0.7V. Once I_L drops to 0A, the HS-FET turns off to stop current flowing from VOUT to VIN, and I_L is forced to work in discontinuous conduction mode (DCM). At the same time, the internal off time becomes longer when the MPQ3432 enters DCM. The off time is inversely proportional to the HS-FET on period in each cycle. In DCM, the MPQ3432 reduces the switching frequency (f_{SW}) and reduces power loss.

If V_{COMP} drops to the 0.5V PSM threshold, the MPQ3432 stops switching to further reduce switching power loss. Switching resumes once V_{COMP} exceeds 0.5V. The switching pulse skips based on V_{COMP} under light-load conditions. PSM has much higher efficiency than FCCM under light-load conditions, but the output voltage ripple may be higher. In addition, the frequency may drop and produce audible noise in PSM.

Note that the frequency is low in DCM. If the LS-FET has a prolonged off time, it does not turn on. If the load increases and V_{COMP} rises, the off time shortens, and the MPQ3432 returns to the regular 600kHz fixed frequency. Then the loop can respond to higher load currents.

The Automatic Pass-Through Function in PSM

If V_{IN} rises to be almost equal to $V_{OUT-SET}$ in PSM, V_{OUT} is charged above $V_{OUT-SET}$ due to the LS-FET minimum on time. In this mode, V_{COMP} drops to the PSM threshold, and the MPQ3432 works with group switching pulses. If V_{IN} continues rising and V_{COMP} remains low for a set time under this condition, the MPQ3432 enters automatic pass-through mode. In this mode, the high-side MOSFET (HS-FET) is always on, while the LS-FET is always off.

Pass-through mode avoids the HS-FET body-diode conduction current when V_{IN} exceeds

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$V_{OUT-SET}$. In pass-through mode, if V_{OUT} drops and V_{COMP} exceeds the PSM threshold, the MPQ3432 exits automatic pass-through mode and recovers to normal switching mode.

If V_{IN} is almost equal to $V_{OUT-SET}$, the MPQ3432 may switch between boost mode and automatic pass-through mode. However, switching between these modes can create a high output voltage ripple. To avoid this scenario, it is recommended to use the feedback resistor to make $V_{OUT-SET}$ much lower than V_{IN} when pass-through mode is required.

Ultrasonic Mode (USM)

To prevent audible noise when f_{SW} is below 20kHz in PSM, the MPQ3432 implements USM by floating the MODE pin or setting MODE to the USM range (between 0.9V and 1.2V). In USM, I_L works in DCM. Meanwhile, when the load drops to a moderate level the frequency stretches as it would in PSM. However, switching does not stop when V_{COMP} drops to the 0.5V PSM threshold. The LS-FET on time is controlled by COMP, even if V_{COMP} is below the PSM threshold. VCOMP controls the LS-FET unless V_{COMP} triggers the minimum on time.

If the load continues to decrease, the MPQ3432 continues reducing f_{SW}. Once the LS-FET is off for 30µs, the device forces the LS-FET back on. This limits the frequency to avoid audible noise under light-load or no-load conditions.

USM may convert more energy to the output than the required load due to the minimum 23kHz frequency, which can cause V_{OUT} to rise above the normal voltage setting. When V_{OUT} rises and V_{COMP} drops, the inductor's peak current may also drop.

If V_{COMP} drops below one internally clamped level, the HS-FET zero-current detection (ZCD) threshold is gradually regulated to a negative level, so that the energy in the inductor can flow back to VIN in each cycle. This keeps V_{OUT} at the set voltage with a frequency exceeding 23kHz. The MPQ3432 works with a 600kHz frequency if V_{COMP} rises again.

If the frequency exceeds 33kHz, USM has the same efficiency as PSM. If the frequency is clamped at the standard 33kHz, USM has a greater power loss than PSM, though it does not create audible noise like the group pulses in PSM.

Minimum On Time and Minimum Off Time

The MPQ3432 blanks the LS-FET on state with 80ns in each cycle to enhance noise immunity. This 80ns minimum on time prevents applications from having an exceedingly high V_{IN} / V_{OUT} ratio. The MPQ3432 also blanks the LS-FET off state with a minimum off time in each cycle. During the minimum off time, the LS-FET cannot turn on, and the minimum off time is short enough to convert the 0.8V input to a 16V output.

LS-FET and HS-FET Maximum On Time

If the inductor current (I_L) cannot trigger V_{COMP} with an on time of 7.5µs, the MPQ3432 shuts down the LS-FET. After the LS-FET shuts down, I_L goes through the HS-FET and charges VOUT during the off time. This refreshes V_{OUT} with a minimum frequency of about 133kHz under heavy-load transient conditions.

During CCM, the HS-FET on time is limited below 8µs. This limits the maximum LS-FET off time when V_{OUT} is close to V_{IN} in USM. If V_{IN} approaches V_{OUT} in USM or heavy-load PSM, the HS-FET may turn off after 8µs HS-FET maximum on time because I_L cannot ramp down within this 8µs limit. After the HS-FET turns off, the LS-FET turns on immediately with one pulse controlled by V_{COMP}, and the HS-FET turns on again. This makes the LS-FET work within a quasi-constant minimum duty cycle.

If V_{IN} is sufficiently high, V_{OUT} exceeds the voltage set for this duty cycle ratio. The MPQ3432 works with normal PSM logic under PSM and light-load conditions. The device stops working when V_{OUT} exceeds the set voltage; it resumes switching when V_{OUT} drops below the set voltage.

VDD Power

The MPQ3432's internal circuit is powered by VDD. A minimum 4.7µF ceramic capacitor must be placed on VDD. When V_{IN} is below 3.4V, VDD is powered from the higher value between V_{IN} or V_{OUT}. This allows the MPQ3432 to maintain a low $R_{DS(ON)}$ and high efficiency, even with a low V_{IN}. When V_{IN} exceeds 3.4V, VDD is always powered by the VIN pin. This reduces VOUT to VDD regulator loss because V_{OUT} is always above V_{IN}.

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If VDD is powered by an external supply and the voltage exceeds 3.4V, the regulators from VIN and VOUT are disabled. Under this condition, the MPQ3432 starts once the external VDD power supply exceeds the V_{DD} under-voltage lockout threshold (VDD_{UVLO}), even if V_{IN} is as low as 0.9V. When VDD is powered by the external power supply, the MPQ3432 continues working if V_{IN} and V_{OUT} are dropping but exceed 0.8V. The external VDD power source should be limited within 3.6V.

There is a reverse-blocking circuit to limit the current flowing between VIN and VOUT. If the external VDD power supply exceeds the VDD regulation voltage, the current is supplied from the external power, and there is no path for the current from the VDD pin to the VIN pin, or from the VDD pin to the VOUT pin. VDD is charged when V_{IN} exceeds 0.9V and EN is above the micro-power threshold. If EN is low, VDD is disconnected from VIN and VOUT.

Supply VIN with a power source exceeding 2.7V during V_{IN} start-up to provide VDD with sufficient voltage power.

Start-Up

When the MPQ3432 input is powered, it starts charging VDD from VIN. Once EN is high and V_{DD} rises above its UVLO threshold, the device starts switching with closed-loop control. If VDD is powered by an additional supply, the MPQ3432 starts switching once V_{DD} exceeds its under-voltage lockout (UVLO) threshold.

After the device is enabled, the MPQ3432 starts up with a soft start (SS). The SS signal is controlled by charging the SS pin from 0V and comparing that value with the internal reference voltage (V_{REF}). The lower of the two values is fed to the error amplifier to control V_{OUT}. After the SS signal rises above V_{REF}, soft start is completed, and the internal reference takes charge of feedback loop regulation.

If there is a biased voltage on VOUT during PSM, the MPQ3432 stops switching until the SS signal rises above V_{FB}, which is proportional to the V_{OUT} biased voltage. If the IC is in USM or FCCM, the device works with a frequency between 33kHz and 600kHz. Both USM and FCCM have a negative inductor current, so the energy may transfer from VOUT to VIN if the V_{OUT} bias is high.

Synchronous Rectifier and BST Function

The MPQ3432 integrates both an LS-FET (Q1) and HS-FET (Q2) to reduce the number of external components. During switching, the rectifier switch (Q2) is powered from the BST pin's voltage (typically 3.4V above the SW voltage). This 3.4V bootstrap voltage is charged from VDD when the LS-FET turns on.

Current Limit

The MPQ3432 provides both a fixed cycle-by-cycle switching peak current limit and a configurable average input current limit function.

Switching Peak Current Limit

The MPQ3432 provides a configurable switching peak current limit. The switching peak current is set by a resistor on the ILIM pin. The ILIM current (I_{LIM}) can be calculated with Equation (1):

$$I_{LIM} = \frac{320}{R_{ILIM}\text{-}4} \quad (1)$$

Where R_{ILIM} is the resister on ILIM (in kΩ). When R_{ILIM} is sufficiently small, or ILIM is shorted to GND, the switching current has a maximum value. When R_{ILIM} is sufficiently high, or ILIM is floating, the switching current has a minimum value (see the Typical Characteristics Curve on page 11).

In each cycle, the internal current-sense circuit monitors the LS-FET current signal. Once the sensed current reaches the set current limit, the LS-FET turns off. The LS-FET current signal is blanked for about 80ns internally to enhance noise immunity.

Enable (EN) Control and Configurable Under-Voltage Lockout (UVLO)

The EN pin enables and disables the MPQ3432. When applying a voltage to EN above its high threshold (about 1V), the MPQ3432 starts up some of the internal circuits in micro-power mode. If the EN voltage exceeds the turn-on threshold (1.23V), the MPQ3432 enables all functions and starts boost operation. Boost switching is disabled when the EN voltage falls below 1.23V. To completely shut down the MPQ3432, EN must have a low-level voltage below 0.4V. After shutdown, the MPQ3432 sinks a current from the input power (generally below 2μA). EN is compatible with voltages up to 13V.

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For automatic start-up, connect EN directly to VIN.

The MPQ3432 features a configurable UVLO hysteresis. When powering up in micro-power mode, EN sinks a 5μA current from an upper resistor (R_{TOP}) (see Figure 2).

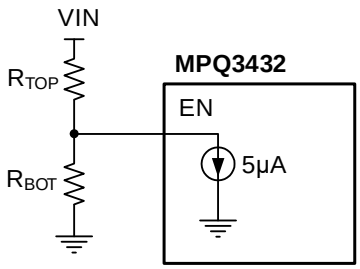


Figure 2: V_{IN} UVLO Configuration

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold can be estimated with Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN-ON}, the 5μA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold. The hysteresis can be calculated with Equation (3):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (3)$$

Over-Voltage Protection (OVP)

If the device detects that V_{OUT} is exceeding its 16.5V threshold, the MPQ3432 stops switching immediately until the voltage drops to 16.3V. This prevents an over-voltage (OV) condition on the output and internal power MOSFETs.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds 175°C, the IC shuts downs. Normal operation resumes when the die temperature drops by 25°C.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (V_{OUT}). Choose R1 to be between 300kΩ and 800kΩ. Calculate R2 with Equation (4):

$$R2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R1 \quad (4)$$

Where V_{REF} is 1V, R1 is the top feedback resistor, and R2 is the bottom feedback resistor.

Selecting the Input Capacitor

The input capacitor (C1) maintains the DC input voltage. Low-ESR ceramic capacitors are recommended. The input voltage ripple can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{V_{IN}}{8 f_{SW}^2 \times L \times C1} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (5)$$

Where f_{SW} is the switching frequency, and L is the inductor value.

Selecting the Output Capacitor

The boost converter has a discontinuous output current, and requires an output capacitor (C2) to supply AC current to the load. For the best performance, low-ESR ceramic capacitors are recommended. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times R_L \times C2} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (6)$$

Where R_L is the value of the load resistor.

Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

An inductor is required to transfer the energy between the input source and the output capacitors. A larger-value inductor results in a lower ripple current and lower peak inductor current, which reduces stress on the power MOSFET. However, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance value can be calculated with Equation (7):

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta I_L} \quad (7)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 20% to 50% of the maximum inductor peak current. Typically, a 1.5µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Selecting the Soft-Start (SS) Capacitor

The soft-start capacitor (C_{SS}) can be estimated with Equation (8):

$$C_{SS} = \frac{t_{RISE} \times I_{SS}}{V_{REF}} \quad (8)$$

Where t_{RISE} is the required output voltage rising time, and I_{SS} is the SS charging current (7.5µA). It is recommended to set C_{SS} to 22nF for about 3ms of the rising time.

Input Current Limit Setting

The ILIM resistor (R5) sets the input current limit. One 1kΩ resistor in series connected to the ILIM pin prevents noise injection. Calculate R5 with Equation (9):

$$R5 = \frac{980}{3.45 \times \left[I_{IN_LIM} - (1.2 - V_{IN} \times 0.12) \right]} - 1 \quad (9)$$

For example, if the required current limit is 13A, and V_{IN} is 3.3V, then R5 is calculated to be 22.29kΩ. Choose R5 to be 22kΩ for a 13A input current limit. Place a decoupling capacitor between 4.7nF and 10nF in parallel with R5.

If the input current limit function is not used, connect ILIM to AGND.

Selecting the VDD Capacitor

The MPQ3432 integrates the VDD power at about 3.4V, which powers the internal MOSFET gate driver and internal control circuit. One ceramic bypass capacitor (4.7µF or greater) is required for the internal regulator. Do not connect the external load to the VDD power.

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Selecting the Bootstrap (BST) Capacitor

The MPQ3432 uses one bootstrap (BST) circuit to power the output N-channel MOSFET. One external BST capacitor is required for the charge pump power. It is recommended to place a 0.1µF ceramic capacitor between the BST and SW pins

Configurable Under-Voltage Lockout (UVLO)

The MPQ3432 features a configurable under-voltage lockout (UVLO) hysteresis. When powering up, EN sinks a 5µA current from an upper resistor (R_{TOP}) (see Figure 3). V_{IN} must increase to overcome the current sink.

Estimate the V_{IN} start-up threshold with Equation (10):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (10)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once the EN voltage reaches V_{EN-ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold, which can be calculated with Equation (11):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (11)$$

For automatic start-up, connect EN with a 30kΩ R_{TOP} resistor to operate with a 150mV hysteresis.

MODE Selection

The MPQ3432 can work in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting. Pull the MODE pin directly to VDD for FCCM, float MODE for USM, and pull the MODE voltage to GND for PSM.

Compensation

The output of the transconductance error amplifier (COMP) compensates for the regulation control system. The system uses two poles and one zero to stabilize the control loop.

Pole f_{P1} is set by the output capacitor (C2) and the load resistance. Pole f_{P2} starts from the origin. The zero f_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). f_{P1} and f_{Z1} can be estimated with Equation (12) and Equation (13), respectively:

$$f_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (12)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (13)$$

Where R_{LOAD} is the load resistance.

There is a right half-plane zero that exists in FCCM, where the inductor current does not drop to zero in each cycle. The frequency of the right half-plane zero (f_{RHPZ}) can be calculated with Equation (14):

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (14)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, which results in a smaller phase margin and gain margin. The worst-case condition occurs when the device is at the minimum input voltage and maximum output power.

Design Example

Table 1 shows a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN}	3V to 8.4V
I_{IN_LIM}	10A
V_{OUT}	9V
I_{OUT}	2.5A

See Figure 4 and Figure 5 on page 25 for detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 8. For more device applications, refer to the related evaluation board datasheet.

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PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. Use a 4-layer PCB for high-power applications. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the output capacitor (C2A to C2C) as close to VOUT and PGND as possible.
2. Place a 0.1µF capacitor (C2D) close to the IC to reduce parasitic inductance.
3. Keep the connection between VOUT, PGND, and the output capacitor (C2) short and wide with copper.
4. Place the copper, IC, and C2 on the same layer.
5. Place the FB dividers (R1 and R2) as close to FB pin as possible.
6. Route the FB trace away from noise sources, such as the SW node.
7. Place the current limit setting net (R4, R5, and C7) close to ILIM.
8. Connect the ILIM ground to AGND.
9. Connect the compensation components and SS capacitor to AGND with a short loop.
10. Connect the VDD capacitor to PGND with a short loop.
11. Keep the input loop (C1, L1, SW, and PGND) as small as possible.
12. Place enough GND vias close to the MPQ3432 to improve thermal dissipation.
13. Use separate AGND and PGND layouts connected between the AGND and PGND pins under the package.

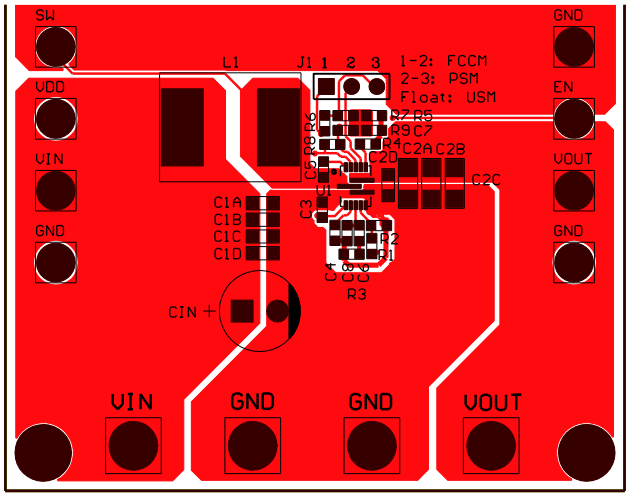


Figure 3: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUITS

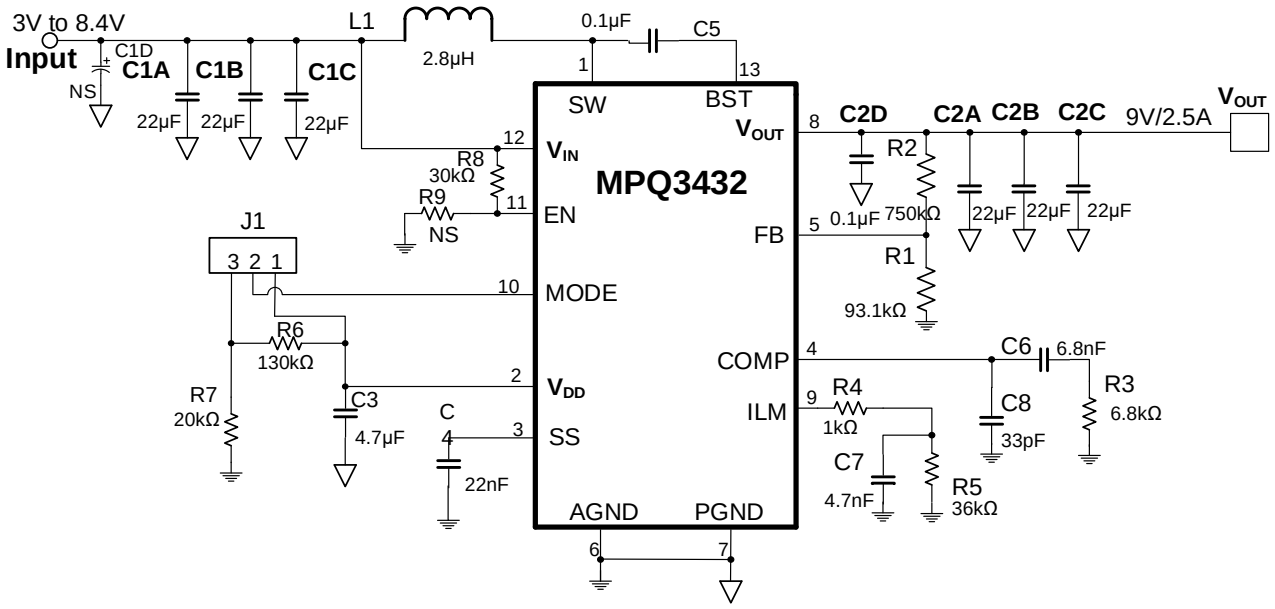


Figure 4: Typical Application Circuit

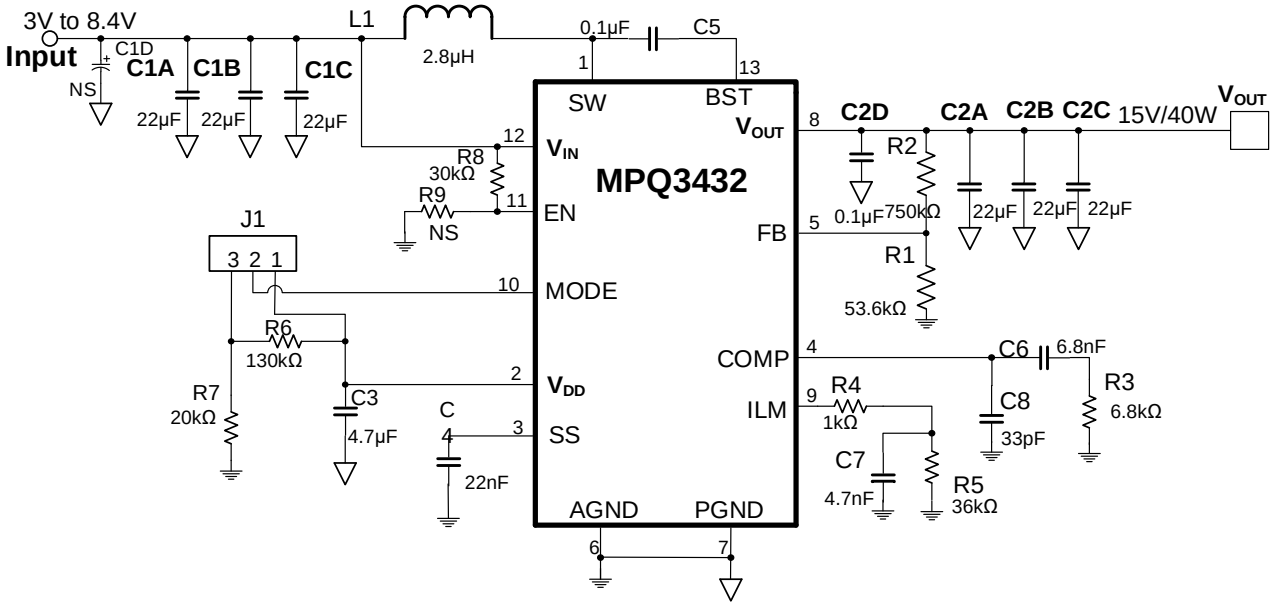
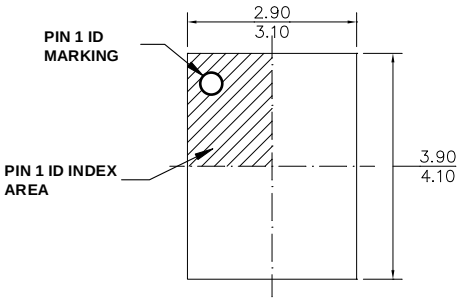


Figure 5: Typical Application Circuit (V_{OUT} = 15V)

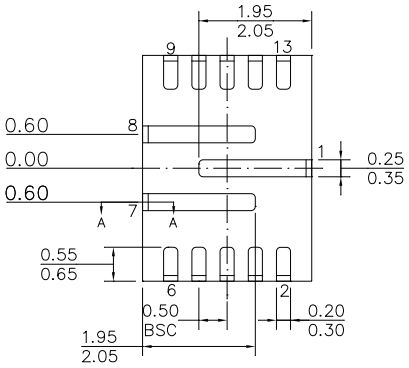
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PACKAGE INFORMATION

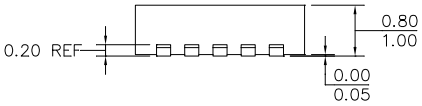
QFN-13 (3mmx4mm)



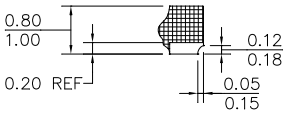
TOP VIEW



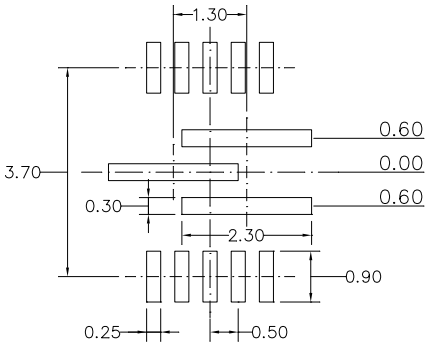
BOTTOM VIEW



SIDE VIEW



SECTION A-A



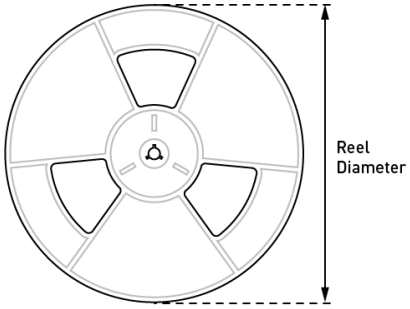
RECOMMENDED LAND PATTERN

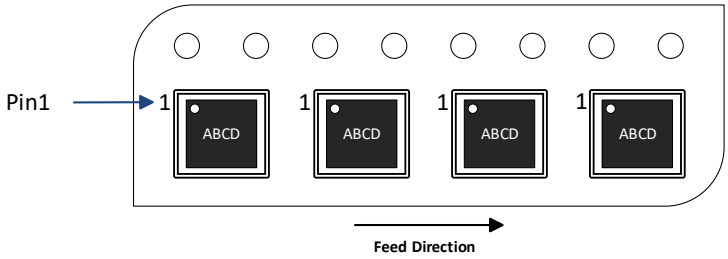
NOTE:

1) LAND PATTERNS OF PIN1,7 AND 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3432GLE-AEC1-Z	QFN-13 (3mmx4mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/8/2022	Initial Release	-

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