MPQ3431C

21A, High-Efficiency, Fully Integrated, Synchronous Boost Converter with Configurable Peak Switching Current Limit, AEC-Q100 Qualified

DESCRIPTION

The MPQ3431C is a 450kHz, fixed-frequency, highly integrated boost converter with a wide input voltage (V_{IN}) range. The MPQ3431C starts from a V_{IN} as low as 2.7V, and supports up to 20W of load power from a single-cell battery with integrated, low on resistance ($R_{DS(ON)}$) power MOSFETs.

The MPQ3431C adopts constant-off-time (COT) control topology, which provides fast transient response. The MODE pin allows the user to select pulse-skip mode (PSM), forced continuous conduction mode (FCCM), or ultrasonic mode (USM) under light-load conditions. The configurable current limit provides accurate overload protection. The low-side MOSFET (LS-FET) limits the cycle-by-cycle inductor peak current, and the high-side MOSFET (HS-FET) eliminates the requirement for an external Schottky diode.

Full protection features include configurable input under-voltage lockout (UVLO) and over-temperature protection (OTP).

The MPQ3431C is available in a QFN-13 (3mmx4mm) package.

FEATURES

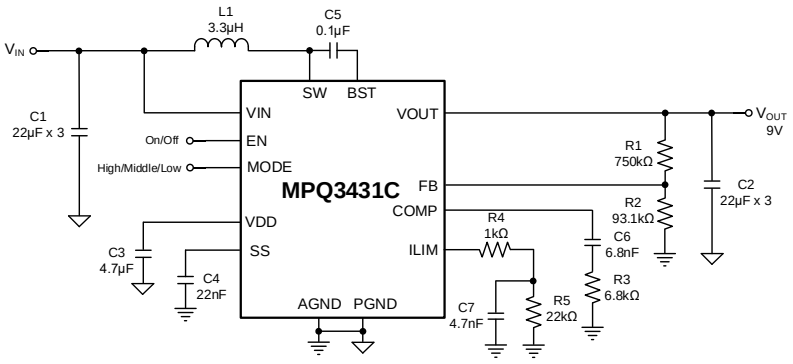
- Guaranteed Industrial/Automotive Temp
- 2.7V to 13V Start-Up Voltage
- 0.8V to 13V Operating Voltage
- Up to 16V Output Voltage (V_{OUT})
- Supports 20W Average Power Load and 40W Peak Power Load from 3.3V
- Configurable Peak Switching Current Limit
- Integrated 6mΩ and 9.5mΩ Power MOSFETs
- 95% Efficiency for 3.6V V_{IN} to 9V/3A
- Selectable PSM, >23kHz USM, and FCCM under Light-Load Conditions
- 450kHz Fixed Switching Frequency (f_{SW})
- Adaptive COT for Fast Transient Response
- External Soft Start and Compensation Pins
- Configurable UVLO and Hysteresis
- 175°C Over-Temperature Protection (OTP)
- Available in a QFN-13 (3mmx4mm) Package
- Available in AEC-Q100 Grade 1

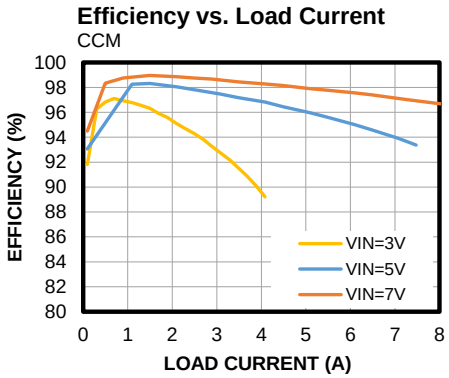
APPLICATIONS

- Automotive Boost
- Super Capacitors
- Backup Batteries

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ3431CGLE-AEC1	QFN-13 (3mmx4mm)	*See Below*	1

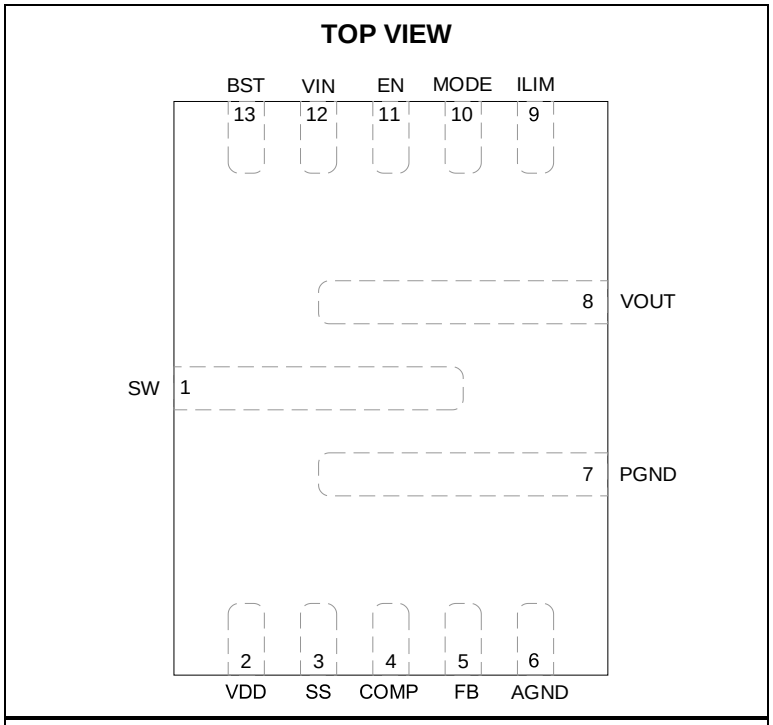
* For Tape & Reel, add suffix -Z (e.g. MPQ3431CGLE-AEC1-Z).

TOP MARKING

MPYW
3431
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
3431C: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-13 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	SW	**Converter switch.** The SW pin is connected to the internal low-side MOSFET (LS-FET) drain and the internal, synchronous, high-side MOSFET (HS-FET) source. Connect the power inductor to SW.
2	VDD	**Internal bias supply.** Decouple the VDD pin using a 4.7µF ceramic capacitor, placed as close to VDD as possible. When V_{IN} exceeds 3.4V, VDD is powered by V_{IN}. Otherwise, VDD is powered by V_{IN} or V_{OUT}, whichever voltage is higher. If the bias voltage connected to VDD exceeds 3.4V, the regulator from VIN and VOUT is disabled. If EN is high, then the VDD regulator starts working when V_{IN} exceeds about 0.9V. Supply VIN with a power source above 2.7V during start-up through VIN to provide sufficient VDD power voltage.
3	SS	**Soft-start (SS) configuration.** Place a capacitor from SS to AGND to set the VOUT rising slew rate.
4	COMP	**Internal error amplifier (EA) output.** Connect a capacitor and resistor in series from COMP to AGND for loop compensation.
5	FB	**Feedback input.** Connect a resistor divider from VOUT to FB.
6	AGND	**Analog ground.**
7	PGND	**Power ground.**
8	VOUT	**Output.** The VOUT pin is connected to the HS-FET drain. If V_{OUT} is above V_{IN} and V_{IN} is below 3.4V, then VOUT powers VDD.
9	ILIM	**Peak switching current limit setting.** Place a resistor from ILIM to AGND to set the peak switching current limit.
10	MODE	**MODE selection.** If the MODE pin is floating, then the MPQ3431C works in ultrasonic mode (USM). If MODE is high, then the MPQ3431C works in forced continuous conduction mode (FCCM). If MODE is low, then the MPQ3431C works in pulse-skip mode (PSM).
11	EN	**Chip enable control.** When not in use, connect the EN pin to VIN for automatic start-up. EN can configure the V_{IN} UVLO. Do not leave EN floating.
12	VIN	**Input supply.** VIN must be bypassed locally. Supply VIN with a power source above 2.7V during start-up through VIN to provide sufficient VDD power voltage.
13	BST	**Bootstrap.** Place a capacitor between BST and SW to power the synchronous HS-FET.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

SW .....-0.3V (-3.5V for <10ns)
……..to +18V (22V for <10ns)
VIN, EN, MODE, VOUT ..... -0.3V to +18V
BST ..... -0.3V to V_{SW} + 4.5V
All other pins..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (2)
.....4W (5)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM).....±2kV
Charged device model (CDM).....±750V

Recommended Operating Conditions (3)

Start-up input voltage (V_{ST}) ..... 2.7V to 13V
Operating input voltage (V_{IN})..... 0.8V to 13V
Start-up input voltage with VDD bias (V_{ST2}).....
..... 0.9V to 13V
Maximum external VDD bias voltage 3.6V (4)
Boost output voltage (V_{OUT})..... V_{IN} to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-13 (3mmx4mm)		
EVQ3431C-L-00A (5)	31	4 °C/W
JESD51-7 (6)	48	11 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) When the external VDD bias voltage drops below the normal VDD regulated voltage, the external power prevents the current from flowing out of VDD.
5) Measured on the EVQ3431C-L-00A, a 4-layer PCB (63mmx63mm).
6) Measured on the JESD51-7, a 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Start-up input voltage	V_{ST}	No VDD bias	2.7		13	V
		V_{DD} = 3V	0.9		13	V
Operating input voltage	V_{IN}		0.8		13	V
Operating VDD voltage [8]	V_{DD}	V_{IN} = 2.7V, 0mA to 10mA	2.3	2.55		V
		V_{IN} = 12V, 0mA to 15mA		3.4		V
V_{DD} under-voltage lockout (UVLO) rising threshold [8]	V_{DD_UVLO-R}	V_{DD} rising	2.2	2.4	2.6	V
V_{DD} UVLO falling threshold	V_{DD_UVLO-F}	V_{DD} falling	2	2.2	2.4	V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on VIN			2	µA
Quiescent current	I_Q	V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on VIN			25	µA
		V_{FB} = 1.1V, V_{IN} = 3V, V_{OUT} = 9V, no switching, measured on VOUT		450	550	µA
Enable (EN) Control						
EN turn-on threshold voltage	V_{EN-ON}	V_{EN} rising (switching)		1.23		V
EN high threshold voltage	V_{EN-H}	V_{EN} rising (micro-power)			1	V
EN low threshold voltage	V_{EN-L}	V_{EN} falling (micro-power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1.0V < EN < V_{EN-ON}	3.5	5	6.5	µA
EN input current	I_{EN}	V_{EN} = 0V, 1.5V		0		µA
EN turn-on delay		EN on to switching		65		µs
Frequency						
Switching frequency	f_{SW}		380	450	520	kHz
Low-side MOSFET (LS-FET) minimum on time [9]	t_{MIN-ON}			80		ns
LS-FET maximum on time	t_{MAX-ON}			7.1		µs
Loop Control						
Feedback (FB) reference voltage	V_{REF}	T_J = 25°C	0.99	1	1.01	V
		T_J = -40°C to +125°C	0.985	1	1.015	V
FB input current	I_{FB}	V_{FB} = 1.1V			50	nA
Error amplifier (EA) voltage gain [10]	A_{V-EA}			300		V/V
EA transconductance	G_{EA}			410		µA/V
EA maximum output current		V_{FB} = 0.8V, V_{COMP} = 1V		60		µA
		V_{FB} = 1.2V, V_{COMP} = 1V		-60		µA
COMP to current gain	G_{CS}			20		A/V
COMP pulse-skip mode (PSM) threshold [9]	V_{PSM}	V_{MODE} = 0V		0.5		V
COMP high clamp		V_{FB} = 0.8V		2.6		V
Soft-start (SS) charge current	I_{SS}		6	7.5	9	µA
MODE Selection						
PSM MODE tri-state region	$V_{MODE-TRI}$				0.7	V
Ultrasonic mode (USM) MODE tri-state region [11]			0.9		1.2	V
Forced continuous conduction mode (FCCM) MODE tri-state region			1.6		V_{DD}	V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USM frequency	f_{USM}		23	33		kHz
High-side MOSFET (HS-FET) zero-current detection (ZCD) (PSM)		V_{FB} = 1V, L = 1.5µH, V_{OUT} = 9V		50		mA
HS-FET ZCD (USM, FCCM) (9) (12)		V_{FB} = 1.1V			-2	A
Power MOSFET						
LS-FET on resistance	$R_{DS(ON)-L}$			6		mΩ
HS-FET synchronous on resistance	$R_{DS(ON)-H}$			9.5		mΩ
LS-FET leakage current		V_{SW} = 16V, T_J = 25°C			0.15	µA
HS-FET leakage current		V_{OUT} = 16V, V_{SW} = 0V, T_J = 25°C			0.15	µA
Bootstrap (BST) Power						
BST voltage				3.3		V
Current Limit						
Switching current limit	$I_{PK-LIMT}$	R_{LIM} = 36kΩ	7	9	11	A
Protection						
Output over-voltage protection (OVP) threshold				16.5		V
Output OVP hysteresis				0.2		V
Thermal Protection						
Thermal shutdown (9)	T_{SD}			175		°C
Thermal shutdown hysteresis (9)	T_{SD-HYS}			25		°C

Notes:

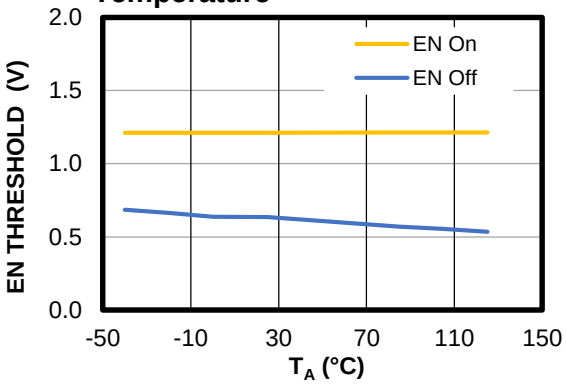
7) Guaranteed by over-temperature correlation. Not tested in production.
8) VDD regulation voltage from 2.7V. V_{IN} is above the V_{DD} UVLO rising threshold in each unit, which guarantees that the IC starts up with 2.7V V_{IN}.
9) Guaranteed by sample characterization. Not tested in production.
10) Guaranteed by design. Not tested in production.
11) For USM, add an external voltage within this range or float MODE.
12) The HS-FET ZCD is below -2A in USM and FCCM.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

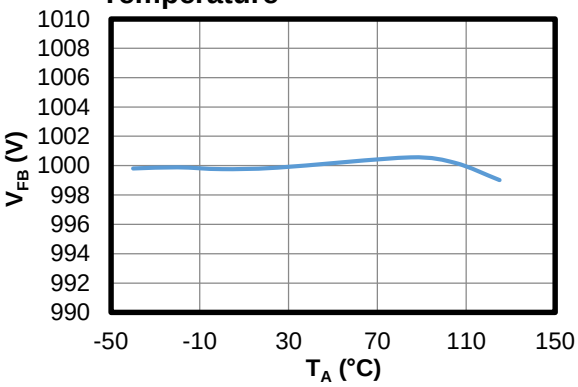
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 9V, R_{LIM} = 36kΩ, L = 2.8μH, T_J = -40°C to +125°C, unless otherwise noted.

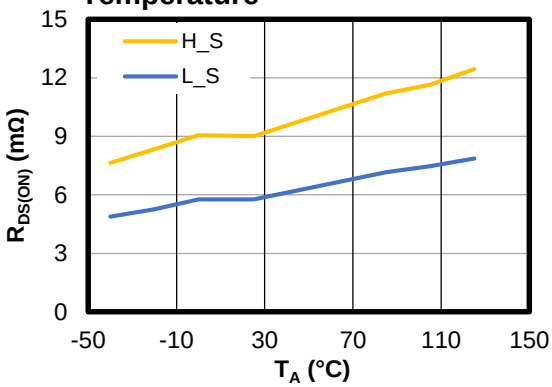
EN Threshold vs. Ambient Temperature



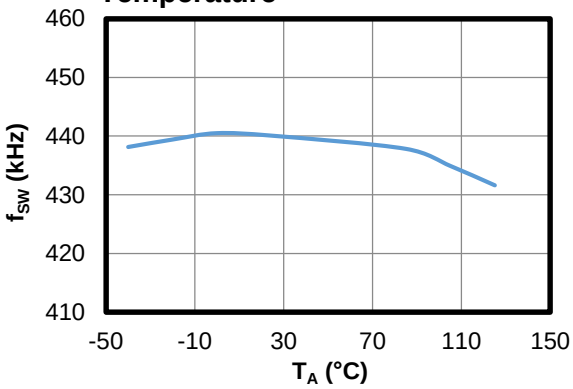
FB Voltage vs. Ambient Temperature



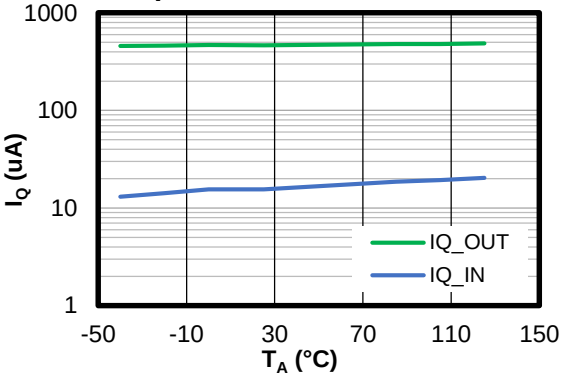
On Resistance vs. Ambient Temperature



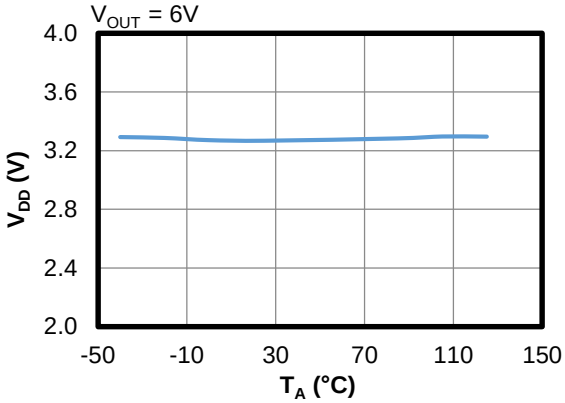
Switching Frequency vs. Ambient Temperature



Quiescent Current vs. Ambient Temperature



VDD Voltage vs. Ambient Temperature



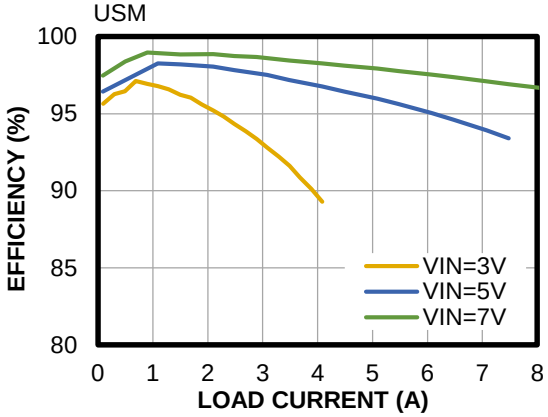
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 9V, R_{LIM} = 36kΩ, L = 2.8μH, T_A = 25°C, unless otherwise noted.

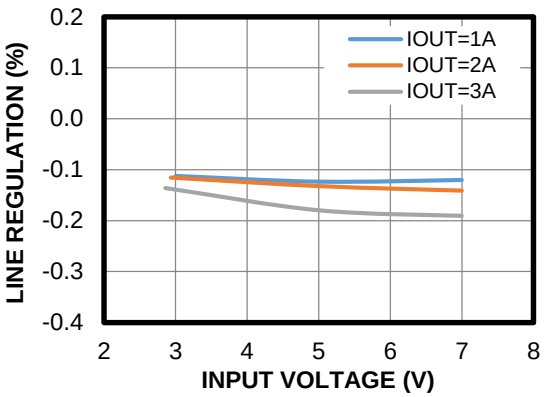
Efficiency vs. Load Current

USM



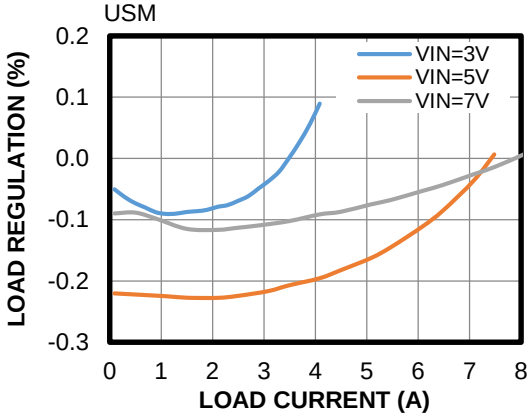
Line Regulation

USM



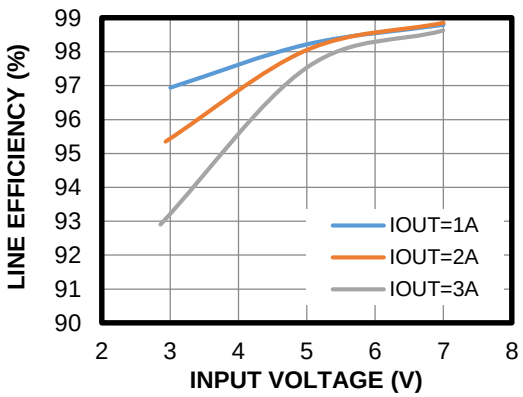
Load Regulation

USM



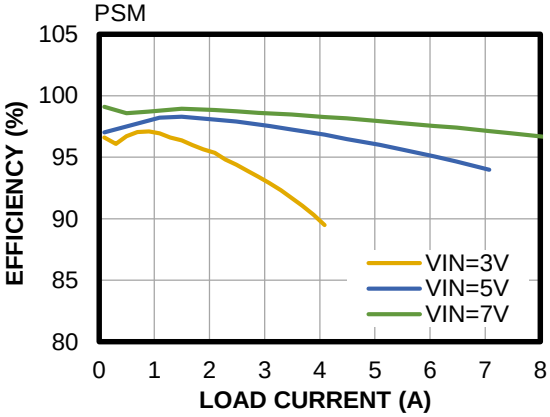
Line Regulation

USM



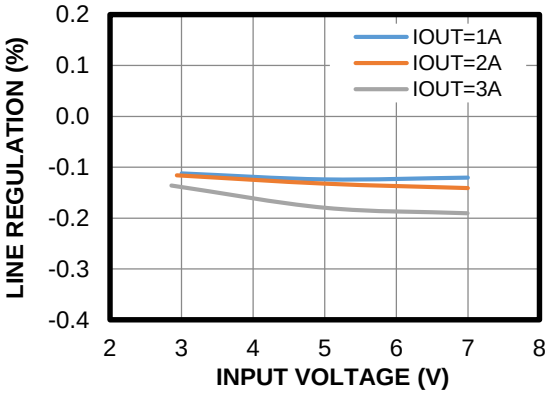
Efficiency vs. Load Current

PSM



Line Regulation

PSM

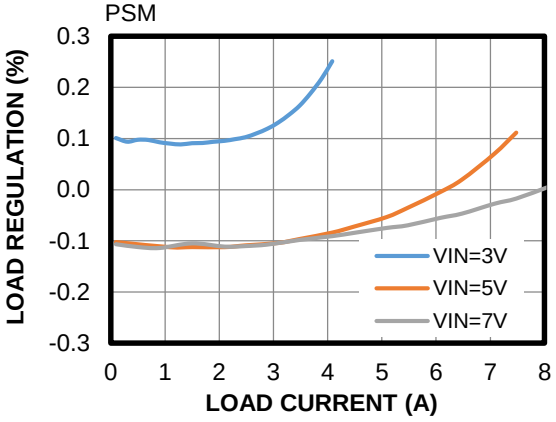


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

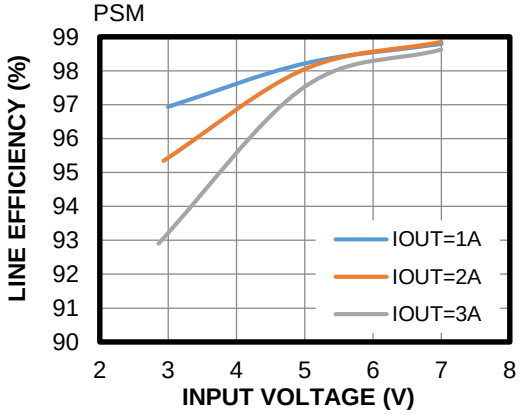
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 9V, R_{LIM} = 36kΩ, L = 2.8µH, T_A = 25°C, unless otherwise noted.

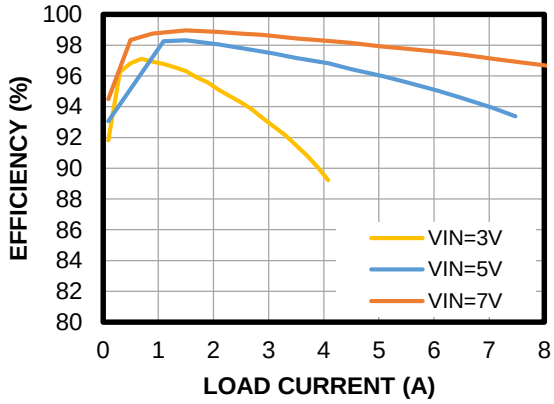
Load Regulation
PSM



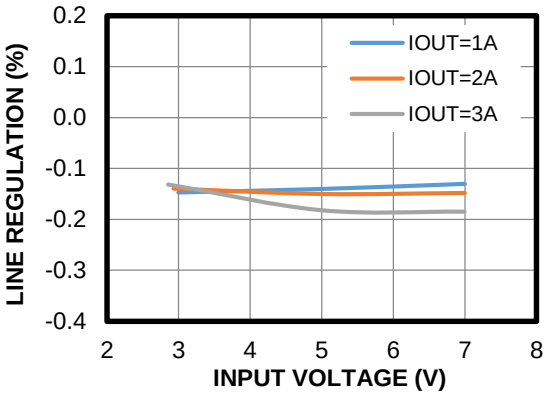
Line Efficiency
PSM



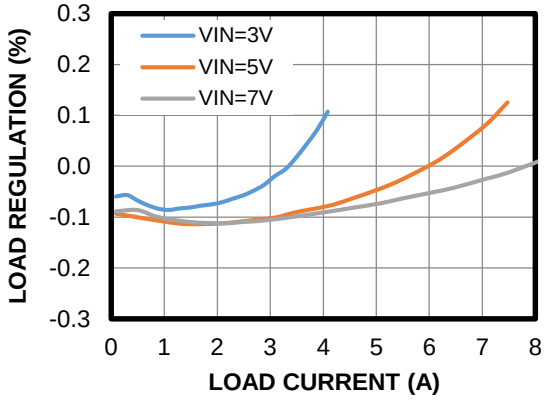
Efficiency vs. Load Current
CCM



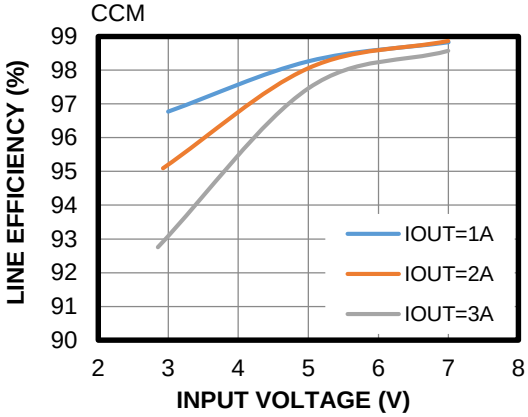
Line Regulation
CCM



Load Regulation
CCM



Line Efficiency
CCM



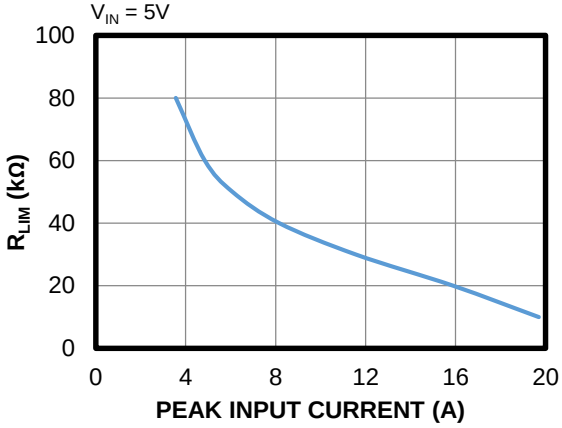
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 9V, R_{LIM} = 36kΩ, L = 2.8μH, T_A = 25°C, unless otherwise noted.

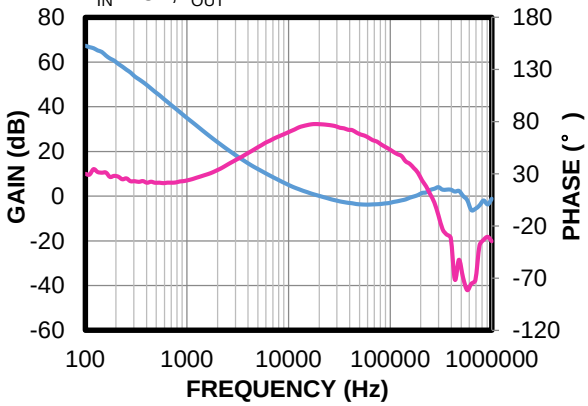
R_{LIM} vs. Peak Input Current

V_{IN} = 5V



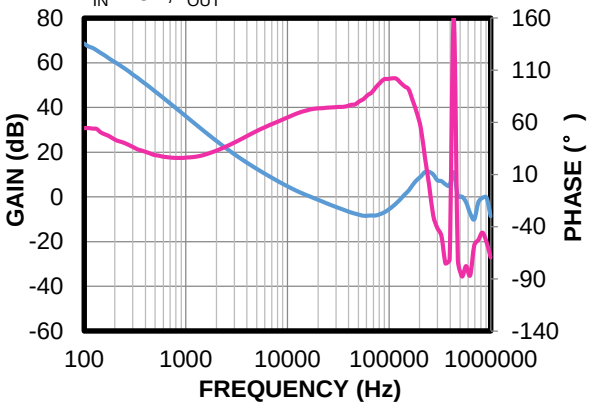
Bode Plot

V_{IN} = 3V, I_{OUT} = 1A



Bode Plot

V_{IN} = 5V, I_{OUT} = 2A

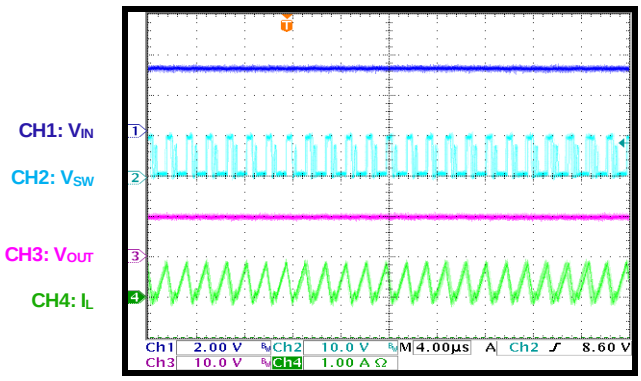


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

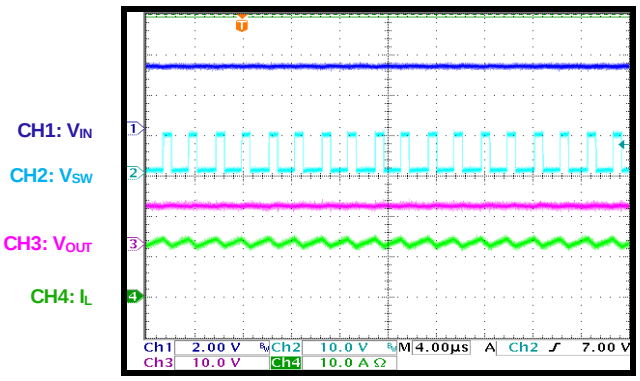
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

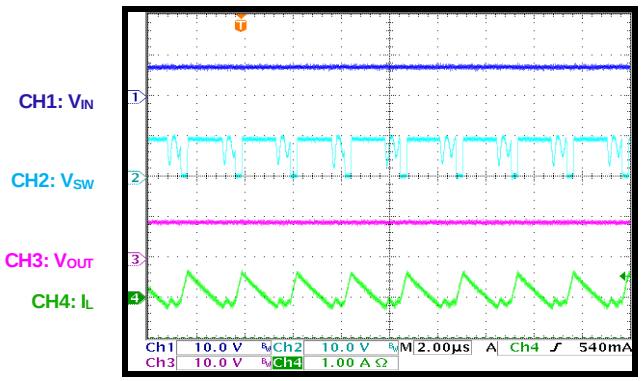
Steady State
V_{IN} = 3V, I_{OUT} = 0.1A, USM



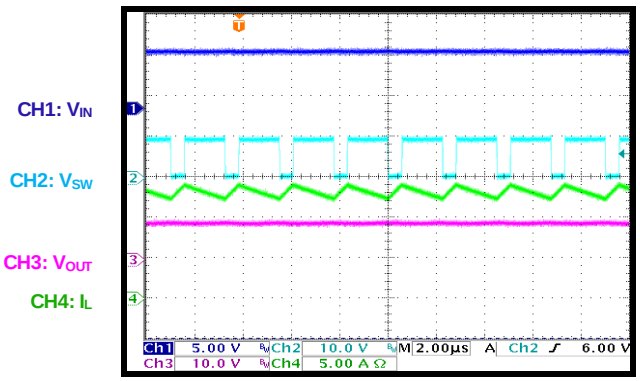
Steady State
V_{IN} = 3V, I_{OUT} = 4A, USM



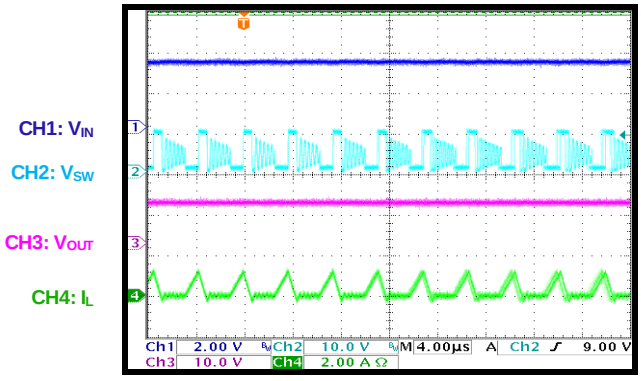
Steady State
V_{IN} = 7V, I_{OUT} = 0.2A, USM



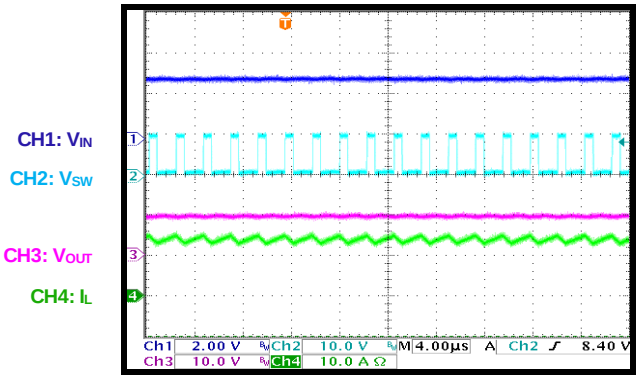
Steady State
V_{IN} = 7V, I_{OUT} = 10A, USM



Steady State
V_{IN} = 3V, I_{OUT} = 0.1A, PSM



Steady State
V_{IN} = 3V, I_{OUT} = 4A, PSM

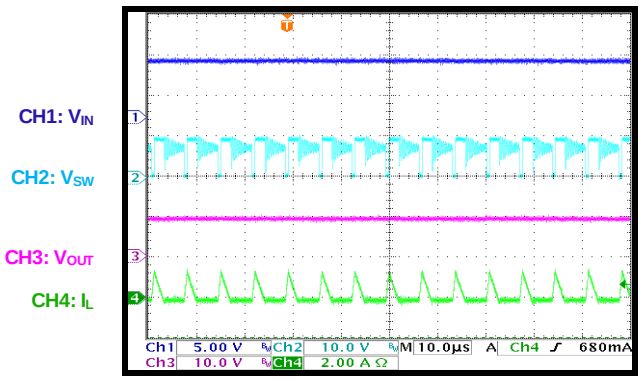


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

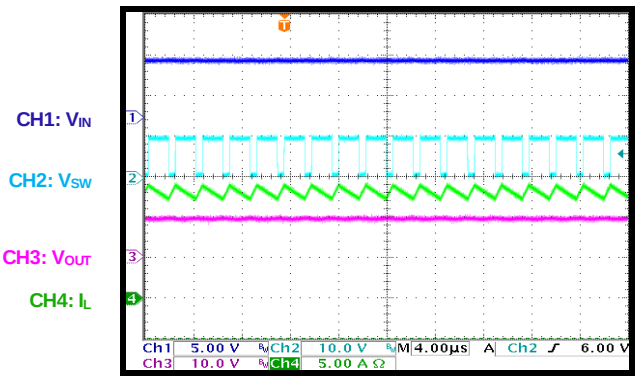
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

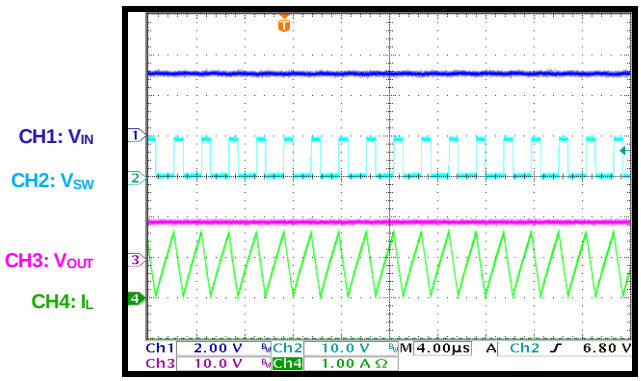
Steady State
V_{IN} = 7V, I_{OUT} = 0.2A, PSM



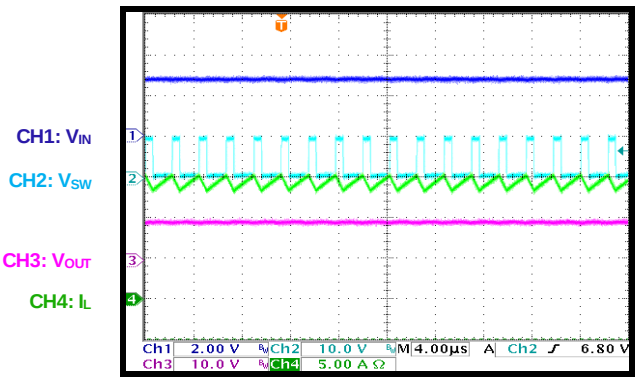
Steady State
V_{IN} = 7V, I_{OUT} = 10A, PSM



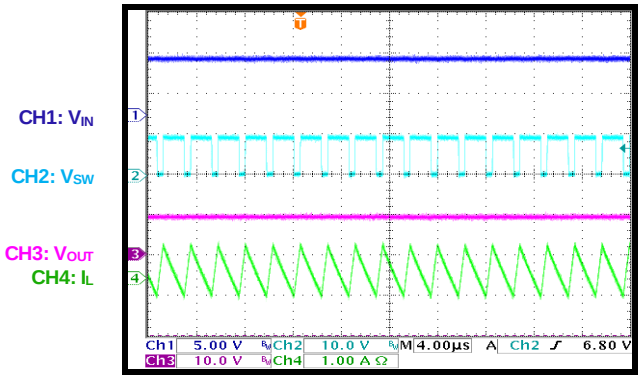
Steady State
V_{IN} = 3V, I_{OUT} = 0.1A, CCM



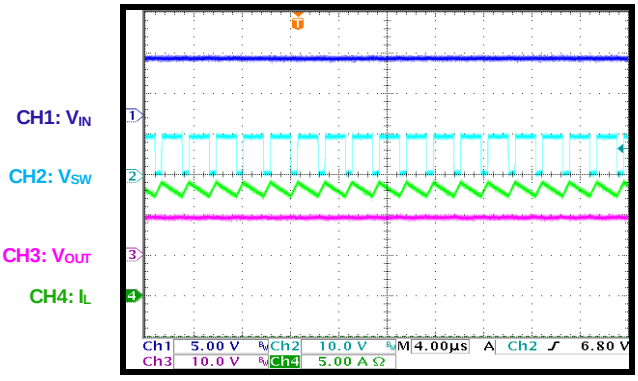
Steady State
V_{IN} = 3V, I_{OUT} = 4A, CCM



Steady State
V_{IN} = 7V, I_{OUT} = 0.2A, CCM



Steady State
V_{IN} = 7V, I_{OUT} = 10A, CCM

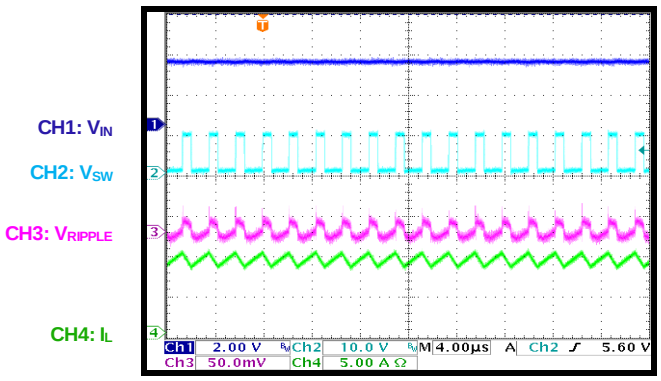


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

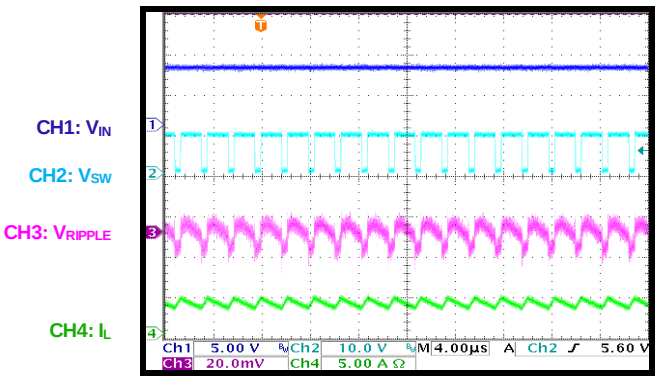
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

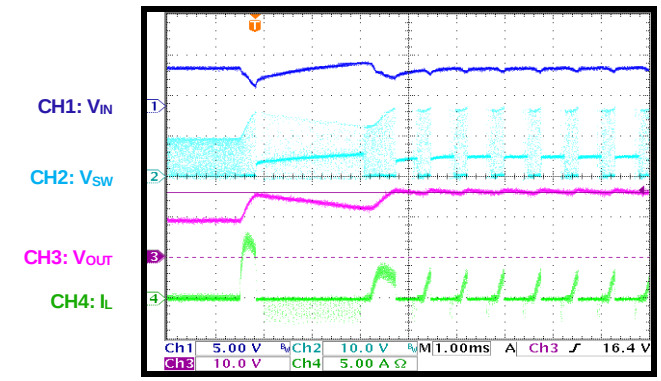
Ripple
V_{IN} = 3V, I_{OUT} = 3A



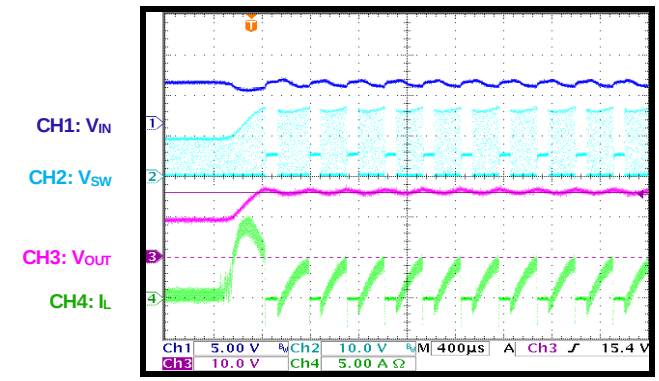
Ripple
V_{IN} = 7V, I_{OUT} = 3A



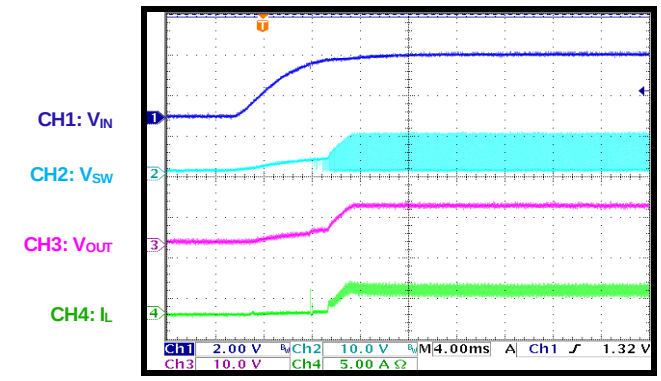
Output Over-Voltage Protection
V_{IN} = 5V, USM



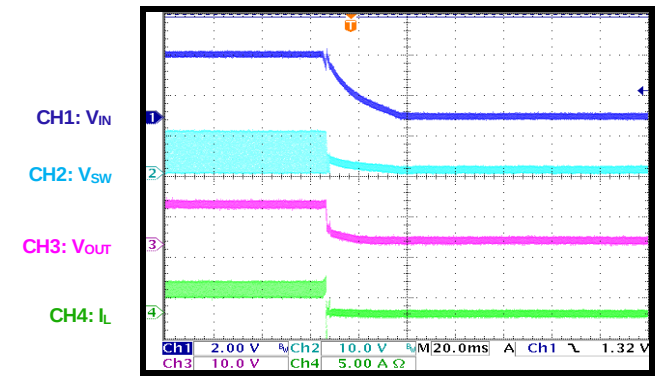
Output Over-Voltage Protection
V_{IN} = 5V, CCM



Start-Up through VIN
V_{IN} = 3V, I_{OUT} = 1A



Shutdown through VIN
V_{IN} = 3V, I_{OUT} = 1A



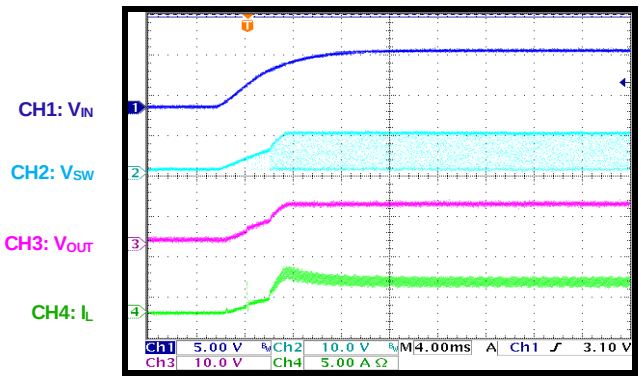
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

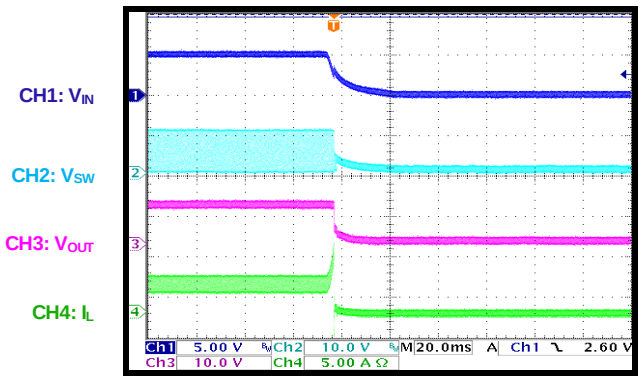
Start-Up through VIN

V_{IN} = 7V, I_{OUT} = 3A



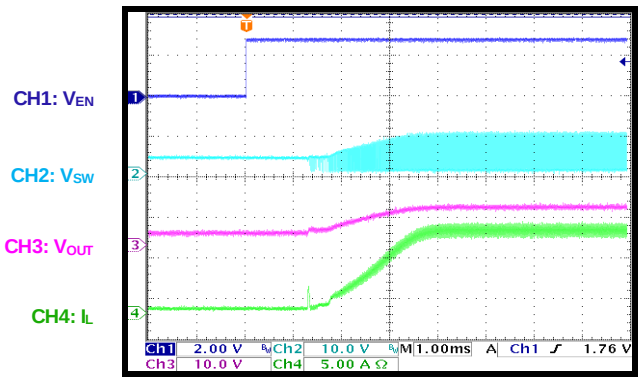
Shutdown through VIN

V_{IN} = 7V, I_{OUT} = 3A



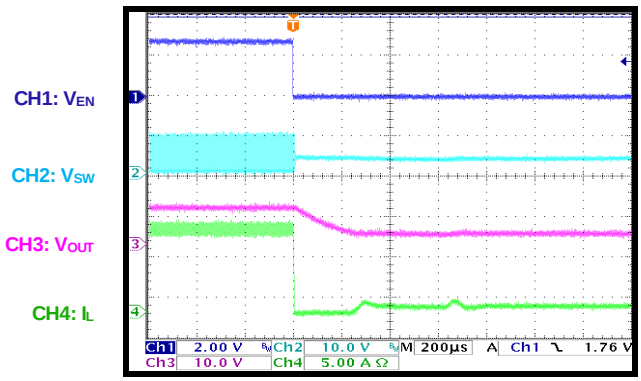
Start-Up through EN

V_{IN} = 3V, I_{OUT} = 3A



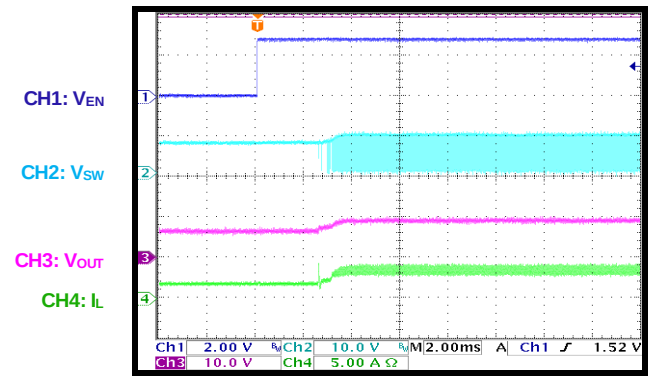
Shutdown through EN

V_{IN} = 3V, I_{OUT} = 3A



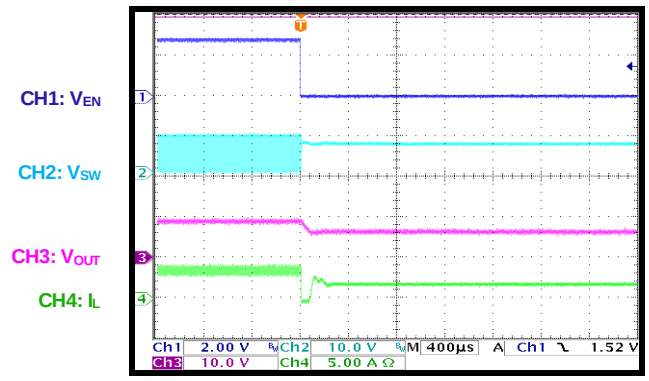
Start-Up through EN

V_{IN} = 7V, I_{OUT} = 3A



Shutdown through EN

V_{IN} = 7V, I_{OUT} = 3A



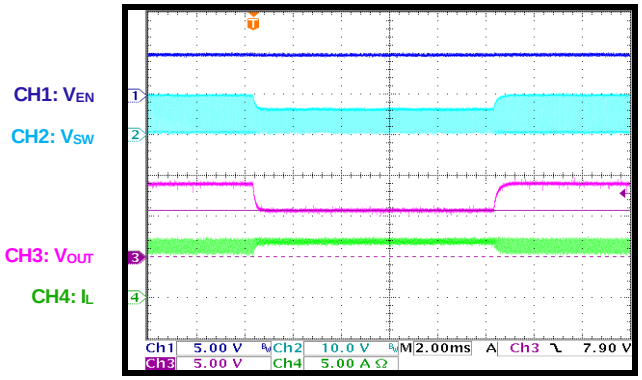
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3V, V_{OUT} = 9V, L = 2.8µH, T_A = 25°C, unless otherwise noted.

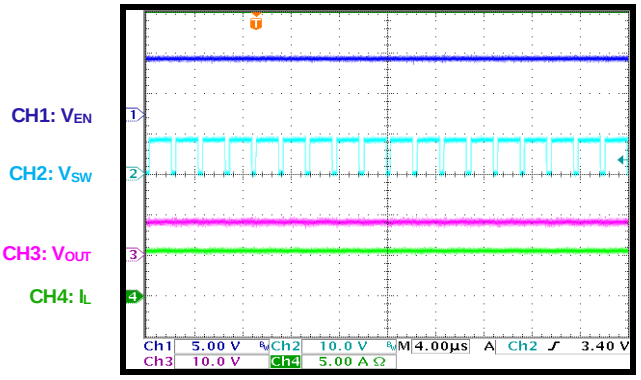
Current Limit

V_{IN} = 5V, R_{LIM} = 44kΩ,
I_{OUT} = 3.5A to 6A to 3.5A



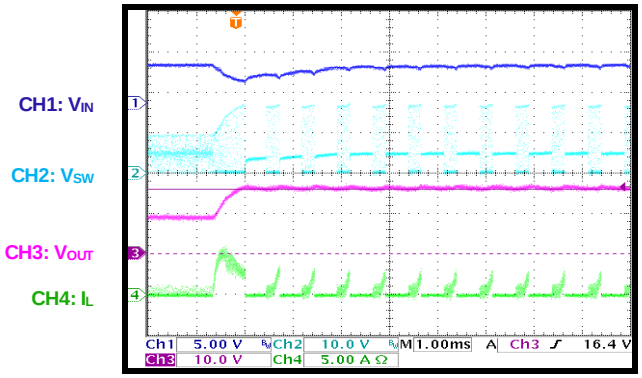
Current Limit

V_{IN} = 7V, R_{LIM} = 44kΩ, I_{OUT} = 5.8A



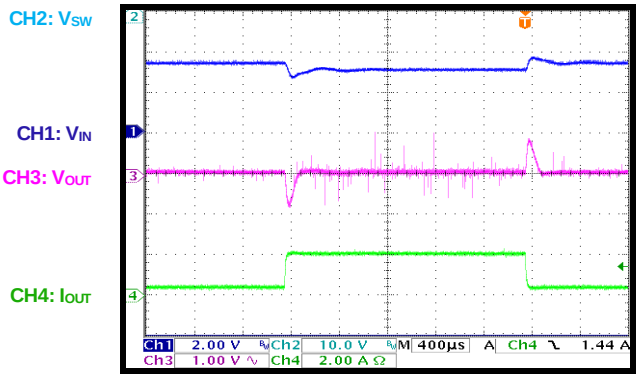
Output Over-Voltage Protection

V_{IN} = 5V, PSM



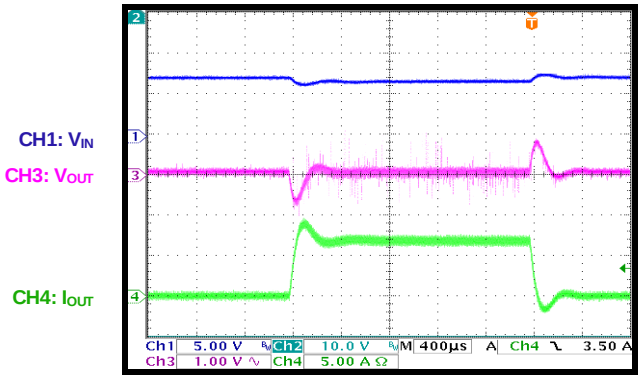
Load Transient

V_{IN} = 3V, I_{OUT} = 0.3A to 2A, USM



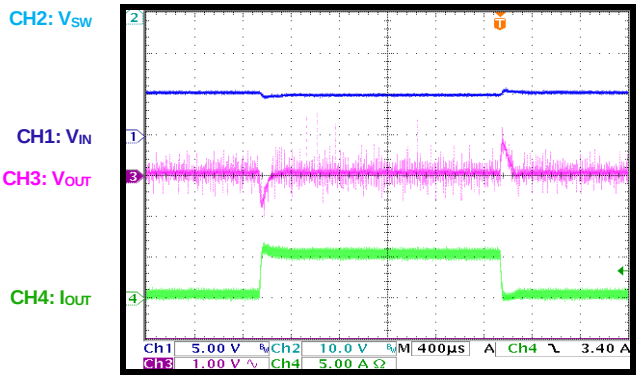
Load Transient

V_{IN} = 7V, I_{OUT} = 0A to 7A, CCM



Load Transient

V_{IN} = 5V, I_{OUT} = 0.3A to 5A, PSM



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

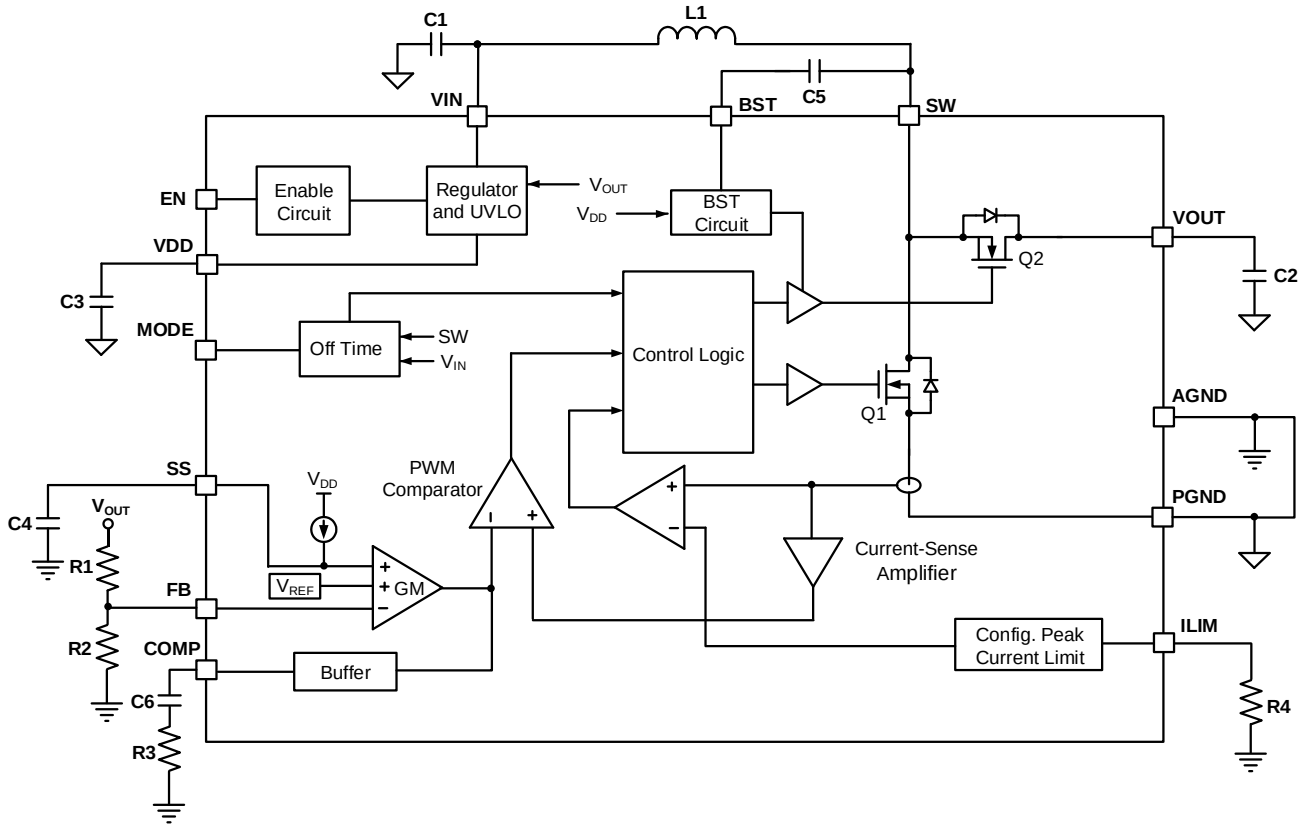


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

OPERATION

The MPQ3431C is a 450kHz, fixed-frequency, high-efficiency boost converter with a wide input voltage (V_{IN}) range. Its fully integrated, low on resistance ($R_{DS(ON)}$) MOSFETs provide small size and high efficiency for high-power step-up applications. Constant-off-time (COT) control provides fast transient response, while the MODE pin provides flexible light-load performance design.

Boost Operation

The MPQ3431C uses COT control to regulate the output voltage (V_{OUT}). At the beginning of each cycle, the low-side N-channel MOSFET (LS-FET) (Q1) turns on and forces the inductor current (I_L) to rise.

The device senses the current through the LS-FET. If the current signal exceeds the output of the transconductance error amplifier (COMP) voltage (V_{COMP}), then the pulse-width modulation (PWM) comparator flips and turns the LS-FET off. I_L then flows to the output capacitor through the high-side MOSFET (HS-FET) and decreases. V_{COMP} is an amplifier output that compares the feedback voltage (V_{FB}) to the internal reference voltage (V_{REF}).

After a fixed off time, the LS-FET turns on again and the cycle repeats. During each cycle, the LS-FET off time is determined by V_{IN} / V_{OUT} ratio, and the on time is controlled by V_{COMP}. The peak inductor current is controlled by COMP, and COMP is controlled by V_{OUT}. Therefore, V_{OUT} regulates I_L.

Operation Mode

Under heavy-load conditions, the MPQ3431C works with a 450kHz, quasi-constant frequency with PWM control. When the load current decreases, the MPQ3431C works in forced continuous conduction mode (FCCM), pulse-skip mode (PSM), or ultrasonic mode (USM) based on the MODE setting. Select the mode before enabling the device.

Forced Continuous Conduction Mode (FCCM)

If MODE is high (>1.6V), then the MPQ3431C works in fixed-frequency pulse-width modulation (PWM) mode for all load conditions. In PWM mode, the off time is determined by the internal circuit to achieve the 470kHz frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current (I_{IN}) drops, and I_L from V_{OUT} to V_{IN} may become negative during the LS-FET off time (while the HS-FET is on). This forces I_L to work in FCCM with a fixed frequency, and produces a lower V_{OUT} ripple than in PSM.

Pulse-Skip Mode (PSM)

If the MODE voltage (V_{MODE}) is below 0.7V, the device works in PSM under light-load conditions. Once I_L drops to 0A, the HS-FET turns off to stop current flowing from V_{OUT} to V_{IN}, forcing I_L to work in discontinuous conduction mode (DCM). At the same time, the internal off time becomes longer when the MPQ3431C enters DCM. The off time is inversely proportional to the HS-FET on period in each cycle. In deep DCM conditions, the MPQ3431C slows down the switching frequency (f_{SW}) and saves power loss.

If V_{COMP} drops to the 0.5V PSM threshold, then the MPQ3431C stops switching to further decrease the switching power loss. Once V_{COMP} exceeds 0.5V, the device resumes switching. Under light-load conditions, the switching pulse skips based on V_{COMP}. PSM has much higher efficiency than FCCM under light-load conditions, but the V_{OUT} ripple may be higher and the frequency may go down, which can produce audible noise.

The frequency is low in DCM, and if the LS-FET has a prolonged off time, then it does not turn on. If the load increases and COMP runs higher, then the off time shortens and the MPQ3431C returns to the regular 600kHz fixed frequency. As a result, the loop can respond to high load currents.

Ultrasonic Mode (USM)

To prevent audible noise when there is a f_{SW} below 20kHz in PSM, the MPQ3431C implements USM by floating MODE or setting MODE to the 0.9V to 1.2V USM range. In USM, I_L works in DCM and the frequency stretches, similar to when the load decreases to a moderate level in PSM. However, switching does not stop when COMP drops to the 0.5V PSM threshold. The LS-FET on time is

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

controlled by COMP, even if V_{COMP} is below the PSM threshold, unless V_{COMP} triggers the minimum on time.

If the load continues to decrease, the MPQ3431C continues decreasing f_{SW}. Once the LS-FET is off for 30µs, the device forces the LS-FET to turn on. This limits the frequency to avoid audible noise under light-load or no-load conditions.

USM may convert more energy to the output than the required load due to the minimum 23kHz frequency, which causes V_{OUT} to exceed the normal voltage setting. When V_{OUT} rises and V_{COMP} drops, the peak inductor current may also drop.

If V_{COMP} drops below an internally clamped level, then the HS-FET zero-current detection (ZCD) threshold is gradually regulated to a negative level, allowing the energy in the inductor to flow back to VIN in each cycle. This keeps the output at the set voltage with a frequency above 23kHz. The MPQ3431C also works with a 450kHz frequency if V_{COMP} rises again.

If the frequency is above 33kHz, then USM has the same efficiency as PSM. USM has more power loss than PSM if the frequency is clamped at the standard 33kHz, but USM does not introduce audible noise, which is caused by the group pulse in PSM.

Minimum On and Off Time

The MPQ3431C blanks the LS-FET on state with 80ns in each cycle to enhance noise immunity. This 80ns minimum on time restricts applications with a high V_{IN} / V_{OUT} ratio. The MPQ3431C also blanks the LS-FET off state with a minimum off time in each cycle. During the minimum off time, the LS-FET cannot turn on, and the minimum off time is short enough to convert the 0.8V input to a 16V output.

LS-FET and HS-FET Maximum On Time

If I_L cannot trigger V_{COMP} with an on time of 7.5µs, the MPQ3431C shuts down the LS-FET. After the LS-FET shuts down, I_L goes through the HS-FET and charges V_{OUT} during the off time. This refreshes V_{OUT} with a minimum frequency of about 133kHz under heavy-load transient conditions.

During CCM, the HS-FET on time is limited below 8µs. This limits the maximum LS-FET off time when V_{OUT} is close to V_{IN} in USM. If V_{IN} approaches V_{OUT} in USM or heavy-load PSM, then the HS-FET may be turned off by the 8µs HS-FET maximum on time because I_L cannot ramp down within this 8µs limit. After the HS-FET turns off, the LS-FET turns on immediately with a pulse control by V_{COMP}, and the HS-FET turns on again. This makes the LS-FET work in a quasi-constant, minimum duty cycle.

If V_{IN} is high enough, V_{OUT} should exceed the voltage set for this duty cycle ratio. The IC works with normal PSM logic under PSM and light-load conditions. The IC stops working when V_{OUT} exceeds the set voltage, and resumes switching when V_{OUT} drops below the set voltage.

VDD Power

The MPQ3431C's internal circuit is powered by VDD. A minimum 4.7µF ceramic capacitor is required on VDD. If V_{IN} is below 3.4V, VDD is powered by V_{IN} or V_{OUT}, whichever is higher. This allows the MPQ3431C to maintain a low $R_{DS(ON)}$ and high efficiency, even with a low V_{IN}. When V_{IN} exceeds 3.4V, VDD is always powered by V_{IN}. This decreases the VOUT-to-VDD regulator loss because V_{OUT} always exceeds V_{IN}.

If VDD is powered by an external supply and the voltage exceeds 3.4V, the regulators from VIN and VOUT are disabled. In this condition, the MPQ3431C starts once the external VDD power supply exceeds the V_{DD} under-voltage lockout (UVLO) threshold (V_{DD_UVLO}), even if V_{IN} is as low as 0.9V. When VDD is powered by the external power supply, the MPQ3431C continues working if V_{IN} and V_{OUT} are dropping but remain above 0.8V. The external VDD power source should be limited to below 3.6V.

There is a reverse-blocking circuit to limit the current flowing between VIN and VOUT. If the external VDD power exceeds the VDD regulation voltage, the current is supplied from the external power, and there is no path for the current from VDD to VIN, or from VDD to VOUT.

VDD is charged when V_{IN} exceeds 0.9V and EN is above the micro-power threshold. If EN is low, then VDD is disconnected from VIN and VOUT.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

Supply VIN with a power source exceeding 2.7V during start-up through VIN to provide VDD with sufficient voltage power.

Start-Up

When the MPQ3431C input is powered, it starts charging VDD from VIN. Once EN is high and V_{DD} exceeds its UVLO threshold, the device starts switching with closed-loop control. If VDD is powered by an additional supply, then the MPQ3431C starts switching once V_{DD} exceeds its UVLO threshold.

After the IC is enabled, the MPQ3431C starts up with a soft start (SS). The SS signal (V_{SS}) is controlled by charging SS from 0V and comparing that value to the internal V_{REF}. The lower of the two values is fed to the error amplifier (EA) to control V_{OUT}. After V_{SS} exceeds V_{REF}, SS is complete, and V_{REF} takes charge of feedback loop regulation.

If there is a biased voltage on VOUT during PSM, then the MPQ3431C stops switching until V_{SS} exceeds V_{FB}, which is proportional to the V_{OUT} bias. If the IC is in USM or FCCM, then the device works with a frequency of about 33kHz to 450kHz. Both USM and FCCM have a negative I_L, so the energy may transfer from VOUT to VIN if the V_{OUT} bias is high.

Synchronous Rectifier and Bootstrap (BST) Function

The MPQ3431C integrates both an LS-FET (Q1) and HS-FET (Q2) to reduce the number of external components. During switching, the rectifier switch (Q2) is powered from BST (typically 3.4V above the SW voltage). This 3.4V bootstrap voltage (V_{BST}) is charged from VDD when the LS-FET turns on.

Current Limit

The MPQ3431C provides both a fixed cycle-by-cycle peak switching current limit and configurable average current limit function.

Peak Switching Current Limit

The MPQ3431C provides a configurable peak switching current limit function. The peak switching current (I_{LIM}) is set by a resistor on ILIM, which can be calculated using Equation (1):

$$I_{LIM}=\frac{320}{R_{ILIM}-4} \quad (1)$$

Where R_{ILIM} is the resistor on ILIM (in kΩ).

If R_{ILIM} is small enough or ILIM is shorted to GND, the switching current has a maximum value. If R_{ILIM} is big enough or ILIM is floated, the switching current has a minimum value (see the Typical Performance Characteristics section on page 7). During each cycle, the internal current-sensing circuit monitors the LS-FET current signal. If the sensed current reaches the setting current limit, the LS-FET turns off. The LS-FET current signal is blanked for about 80ns internally to enhance noise immunity.

Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin enables and disables the MPQ3431C. If the EN voltage (V_{EN}) exceeds the EN high threshold (about 1V), the MPQ3431C starts up some of the internal circuits in micro-power mode. If V_{EN} exceeds the turn-on threshold (1.23V), then the MPQ3431C enables all functions and starts boost operation. Boost switching is disabled when V_{EN} falls below its turn-on threshold (1.23V). To completely shut down the MPQ3431C, V_{EN} must be below 0.4V. After shutdown, the MPQ3431C sinks a current from the input power (generally below 2μA). EN is compatible with voltages up to 13V. For automatic start-up, connect EN directly to VIN.

The MPQ3431C features a configurable UVLO hysteresis. When starting up in micro-power mode, EN sinks a 5μA current from an upper resistor (R_{TOP}) (see Figure 2).

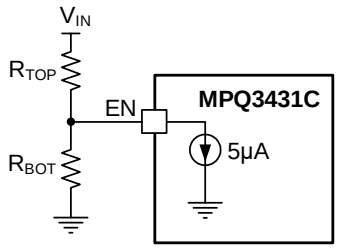


Figure 2: V_{IN} UVLO Configuration

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold (V_{IN-ON}) can be calculated using Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the V_{EN} turn-on threshold (typically 1.23V), R_{TOP} is the upper resistor, and R_{BOT} is the lower resistor.

Once V_{EN} reaches V_{EN-ON}, the 5µA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold ($V_{IN-UVLO-HYS}$), which can be calculated using Equation (3):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (3)$$

Over-Voltage Protection (OVP)

If V_{OUT} exceeds its 16.5V threshold, then the MPQ3431C stops switching immediately until V_{OUT} drops to 16.3V. This prevents an over-voltage (OV) condition on the output and internal power MOSFETs.

Thermal Protection

Thermal shutdown prevents the IC from operating at exceedingly high temperatures. If the die temperature exceeds 175°C, the IC shuts downs. Once the die temperature drops by 25°C, the device resumes normal operation.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT}. Select R1 to be between 300kΩ and 800kΩ. R2 can be calculated using Equation (4):

$$R_{BOT} = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_{TOP} \quad (4)$$

Where V_{REF} is 1V.

Selecting the Input Capacitor

The input capacitor (C1) maintains the DC V_{IN}. Low-ESR ceramic capacitors are recommended. The V_{IN} ripple (ΔV_{IN}) can be estimated using Equation (5):

$$\Delta V_{IN} = \frac{V_{IN}}{8 f_{SW}^2 \times L \times C1} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (5)$$

Where f_{SW} is the switching frequency, and L is the inductance.

Selecting the Output Capacitor

The boost converter has a discontinuous output current, and requires an output capacitor (C2) to supply AC current to the load. For the best performance, low-ESR ceramic capacitors are recommended. The V_{OUT} ripple (ΔV_{OUT}) can be estimated using Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times R_L \times C2} \times (1 - \frac{V_{IN}}{V_{OUT}}) \quad (6)$$

Where R_L is the load resistance.

Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients.

Selecting the Inductor

An inductor is required to transfer the energy between the input source and the output capacitors. A larger-value inductor results in a lower ripple current and peak inductor current, reducing stress on the power MOSFETs; however, it also has a larger physical size, higher series resistance, and lower saturation current.

For most designs, the inductance (L) can be calculated using Equation (7):

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta I_L} \quad (7)$$

Where ΔI_L is the inductor ripple current.

Select the inductor ripple current to be approximately 20% to 50% of the maximum peak inductor current. Typically, a 1.5µH inductor is recommended. Ensure that the inductor does not saturate under the worst-case condition. The inductor should have a low series resistance (DCR) to reduce the resistive power loss.

Soft-Start (SS) Capacitor Selection

With the required V_{OUT} rising time (t_{RISE}), the SS capacitance (C_{SS}) can be calculated using Equation (8):

$$C_{SS} = \frac{t_{RISE} \times I_{SS}}{V_{REF}} \quad (8)$$

Where I_{SS} is the SS charging current (7.5µA).

It is typically recommended to set C_{SS} to 22nF for about 3ms of the rising time.

Setting the Input Current Limit

The ILIM resistor (R5) sets the input current limit (I_{IN_LIM}). An 1kΩ resistor (R5) connected in series with ILIM prevents noise injection. R5 can be calculated using Equation (9):

$$R5 = \frac{980}{3.45 \times \left[I_{IN_LIM} - (1.2 - V_{IN} \times 0.12) \right]} - 1 \quad (9)$$

For example, if the required current limit is 13A, and V_{IN} is 3.3V, then R5 is calculated to be 22.29kΩ. Therefore, a 22kΩ value should be selected for a 13A I_{IN_LIM}. Place a decoupling capacitor (4.7nF to 10nF) in parallel with R5.

If the input current limit function is not used, connect ILIM to AGND.

VDD Capacitor Selection

The MPQ3431C integrates the VDD power at about 3.4V to power the internal MOSFET gate driver and internal control circuit. A ceramic bypass capacitor with at least 4.7µF is required for the internal regulator. Do not connect the external load to the VDD power.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

BST Capacitor

The MPQ3431C uses a BST circuit to power the output N-channel MOSFET. An external BST capacitor (C_{BST}) is required for the charge pump power. A 0.1µF ceramic capacitor between BST and SW is recommended.

Configurable UVLO

The MPQ3431C features a configurable UVLO hysteresis. When powering up, EN sinks a 5µA current from R_{TOP} (see the Electrical Characteristics on page 5). V_{IN} must increase to overcome the current sink.

V_{IN-ON} can be estimated using Equation (10):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 5\mu A \times R_{TOP} \quad (10)$$

Where V_{EN-ON} is the EN voltage turn-on threshold (typically 1.23V).

Once V_{EN} reaches V_{EN-ON}, the 5µA sink current turns off to create a reverse hysteresis for $V_{IN-UVLO-HYS}$, which can be calculated using Equation (11):

$$V_{IN-UVLO-HYS} = 5\mu A \times R_{TOP} \quad (11)$$

For automatic start-up, connect EN with a 30kΩ R_{TOP} resistor to operate with a 150mV hysteresis.

MODE Selection

The MPQ3431C can work in FCCM, PSM, or USM based on the MODE setting. Pull MODE directly to VDD for FCCM, float MODE for USM, and pull MODE to GND for PSM.

Compensation

The COMP pin compensates for the regulation control system. The system uses two poles and one zero to stabilize the control loop.

Pole f_{P1} is set by the output capacitor (C_{OUT}) and the load resistance (R_{LOAD}). Pole f_{P2} starts from the origin. The zero f_{Z1} is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). f_{P1} can be calculated using Equation (12):

$$f_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (12)$$

f_{Z1} can be calculated using Equation (13):

$$f_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (13)$$

A right half-plane zero exists in FCCM, in which I_L does not drop to zero during each cycle. The frequency of the right half-plane zero (f_{RHPZ}) can be calculated with Equation (14):

$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (14)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, resulting in a smaller phase margin and gain margin. The worst-case condition is when the device is at the minimum V_{IN} and maximum output power.

Design Example

Table 1 shows a design example following the application guidelines for the specifications below.

Table 1: Design Example

V_{IN}	I_{IN_LIM}	V_{OUT}	I_{OUT}
3V to 8.4V	10A	9V	2.5A

For detailed application schematics, see Figure 4 and Figure 5 on page 24. For the typical performance and circuit waveforms, see the Typical Performance Characteristics section on page 7. For more device applications, refer to the related evaluation board datasheet.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. Poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. A 4-layer layout is recommended for high-power applications. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the output capacitors (C2A, C2B, and C2C) as close to VOUT and PGND as possible.
2. Place a 0.1µF capacitor (C2D) close to the IC to reduce parasitic inductance.
3. Keep VOUT and PGND's connections to the output capacitor short and wide, using copper areas.
4. Place the copper, IC, and C_{OUT} on the same layer.
5. Place the FB dividers (R1 and R2) as close to FB as possible.
6. Route the FB trace away from noise sources, such as the SW node.
7. Place the current limit setting net (R4, R5, and C7) close to ILIM.
8. Connect the ILIM ground to AGND.
9. Connect the compensation components and C_{SS} to AGND with a short loop.
10. Connect the VDD capacitor to PGND with a short loop.
11. Keep the input loop (C1, L1, SW, and PGND) as small as possible.
12. Place enough GND vias close to the device for good thermal dissipation.
13. Use separate layouts connected between AGND and PGND under the package.

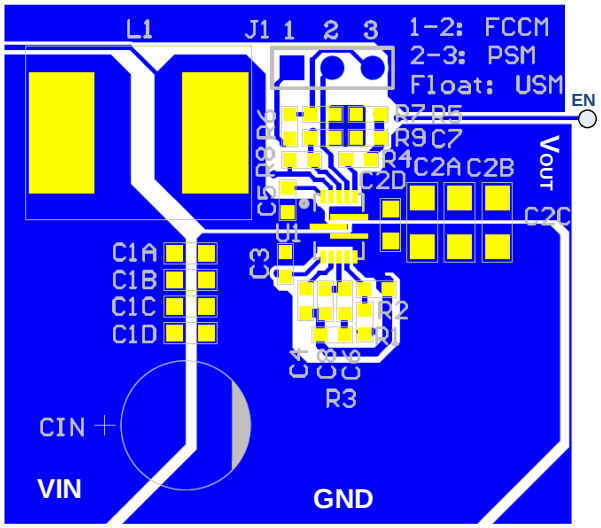


Figure 3: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

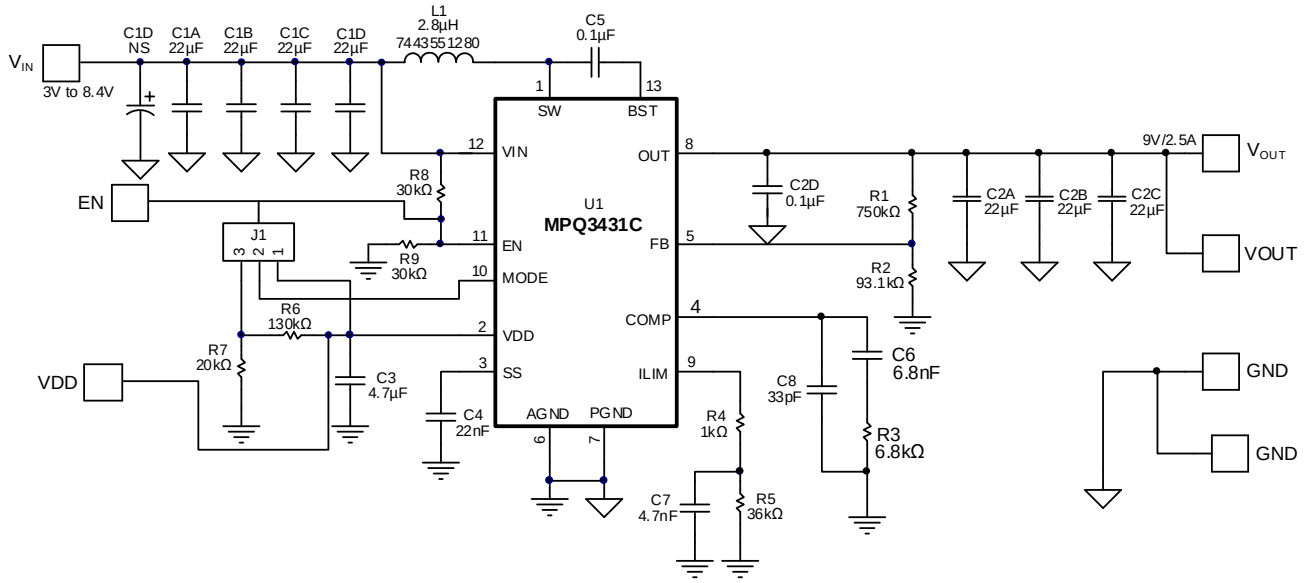


Figure 4: Typical Application Circuit (V_{OUT} = 9V)

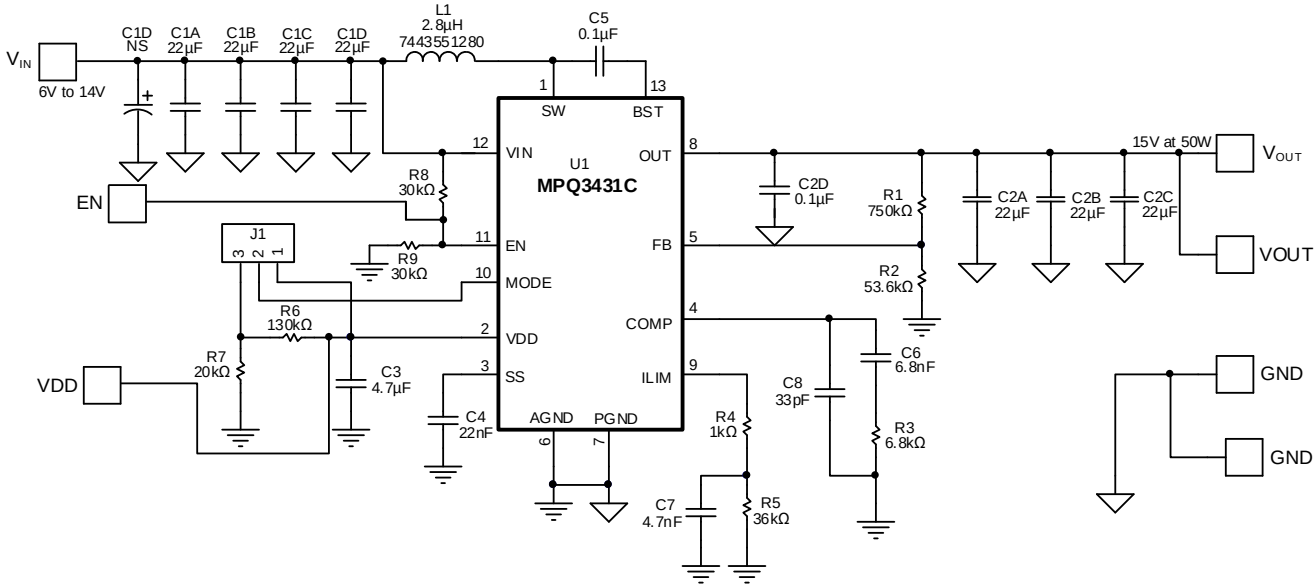
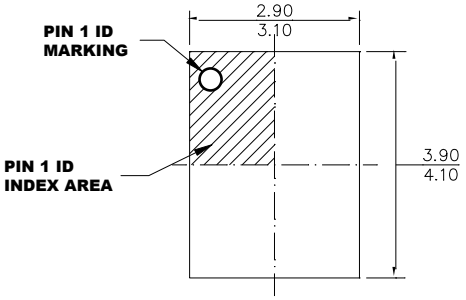


Figure 5: Typical Application Circuit (V_{OUT} = 15V)

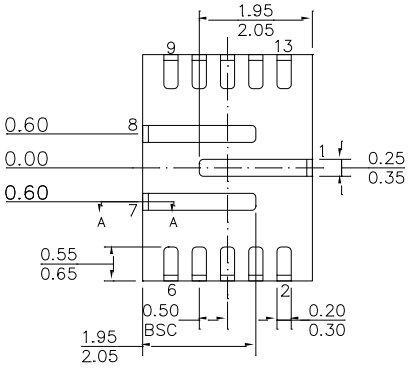
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

PACKAGE INFORMATION

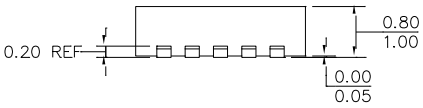
QFN-13 (3mmx4mm)



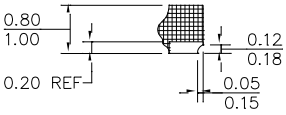
TOP VIEW



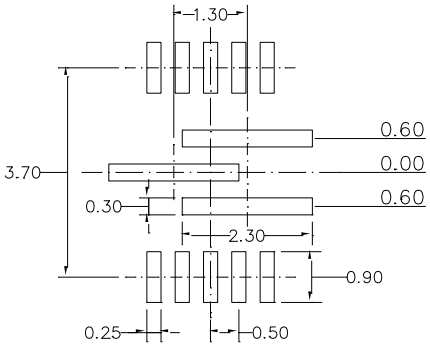
BOTTOM VIEW



SIDE VIEW



SECTION A-A



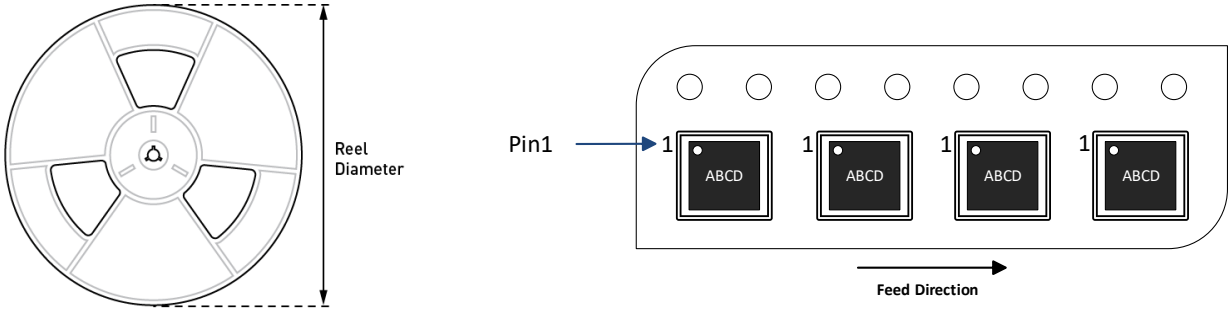
RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,7 AND 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ3431CGLE-AEC1-Z	QFN-13 (3mmx4mm)	5000	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2022 MPS. All Rights Reserved.